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Signetics

Linear Data Manual Volume 2: Industrial

Signetics

Linear Products

1987 Linear Data Manual Volume 2: Industrial

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Preface

Linear Products

The Linear Division, one of four Signetics product divisions, is a major supplier of a broad line of linear integrated circuits ranging from high performance application specific designs to many of the more popular industry standard devices.

A fifth Signetics division, the Military Division, provides military-grade integrated circuits, including Linear. Please consult the Signetics Military data book for information on such devices.

Employing Signetics' high quality processing and screening standards, the Linear Division is dedicated to providing high-quality linear products to our customers worldwide.

The three 1987 Linear Data and Applications Manuals provide extensive technical data and application information for a broad range of products serving the needs of a wide variety of markets.

Volume 1 — Communications:
Contains data and application information concerning our radio and audio circuits, compandors, phase-locked loops, compact disc circuits, and ICs for RF communication, telephony and modem applications.

Volume 2 — Industrial:
Contains data and application information concerning our data conversion products (analog-to-digital and digital-to-analog), sample-and-hold circuits, comparators, driver/receiver ICs, amplifiers, position measurement devices, power conversion and control ICs and music/speech synthesizers.

Volume 3 — Video:
Contains data and application information concerning our video products. This includes tuning, video IF and audio IF circuits, sync processors/generators, color decoders and encoders, video processing ICs, vertical deflection circuits, Videotex and Teletext ICs and power supply controllers for video applications.

Each volume contains extensive product-specific application information. In addition there are selector guides and product-specific symbols and definitions to facilitate the selection and understanding of Linear products. A functional Table of Contents for each of the three volumes and a complete product and application note listing is also included.

Although every effort has been made to ensure the accuracy of information in these manuals, Signetics assumes no liability for inadvertent errors.

Your suggestions for improvement in future editions are welcome.

Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Volume 2
Industrial

Linear Products

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Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
AMD	AM6012DC	AM6012F	0 to +70	Ceramic
	DAC-08AQ	DAC-08AF	-55 to +125	Ceramic
	DAC-08CN	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08EN	DAC-08EN	0 to +70	Plastic
	DAC-08EQ	DAC-08EF	0 to +70	Ceramic
	DAC-08HN	DAC-08HN	0 to +70	Plastic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	-55 to +125	Ceramic
	LF198H	LF198H	-55 to +125	Metal Can
	LF198H	SE5537H	-55 to +125	Metal Can
	LF398H	LF398H	0 to +70	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398L	LF398D	0 to +70	SO
	LF398L	NE5537D	0 to +70	SO
	LF398N	LF398N	0 to +70	Plastic
	LF398N	NE5537N	0 to +70	Plastic
Datel	AM-453-2	NE5534/AF	0 to +70	Ceramic
	AM-453-2C	NE5534/AF	0 to +70	Ceramic
	AM-453-2M	SE5534/AF	-55 to +125	Ceramic
	DAC-UP10BC	NE5020N	0 to +70	Plastic
	DAC-UP8BC	NE5018N	0 to +70	Plastic
	DAC-UP8BM	SE5019F	-55 to +125	Ceramic
	DAC-UP8BQ	SE5018F	-55 to 125	Ceramic
Exar	XR-5532/A N	NE5532/AF	0 to +70	Ceramic
	XR-5532/A P	NE5532/AN	0 to +70	Plastic
	XR-L567CN	NE567F	0 to +70	Ceramic
	XR-L567CP	NE567N	0 to +70	Plastic
	XR-5534/A CN	NE5534/AF	0 to +70	Ceramic
	XR-5534/A CP	NE5534/AN	0 to +70	Plastic
	XR-5534/A M	SE5534/AF	-55 to +125	Ceramic
	XR-558CN	NE558F	0 to +70	Ceramic
	XR-558CP	NE558N	0 to +70	Plastic
	XR-558M	SE558F	-55 to +125	Ceramic
	XR-1524N	SG3524F	0 to +70	Ceramic
	XR-1524P	SG3524N	0 to +70	Plastic
	XR-2524P	SG3524N	0 to +70	Plastic
	XR-3524N	SG3524F	0 to +70	Ceramic
	XR-3524P	SG3524N	0 to +70	Plastic
Fairchild	μA080/DA	DAC-08F	0 to +70	Ceramic
	μA0801CDC	MC1408F	0 to +70	Ceramic
	μA0801CPC	MC1408N	0 to +70	Plastic
	μA0801EDC	DAC-08EF	0 to +70	Ceramic
	μA0801EPC	DAC-08AF	0 to +70	Ceramic
	μA1458TC	MC1458N	0 to +70	Plastic
	μA1488DC	MC1488F	0 to +70	Ceramic
	μA1488PC	MC1488N	0 to +70	Plastic
	μA1489/A PC	MC1489/AF	0 to +70	Ceramic
	μA1489/A PC	MC1489/AN	0 to +70	Plastic
	μA198HM	NE5537H	0 to +70	Metal Can
	μA198RM	NE5537N	0 to +70	Plastic
	μA2901DC	LM2901F	-40 to +85	Ceramic
	μA2901PC	LM2901N	-40 to +85	Plastic
	μA311RC	LM311F	0 to +70	Ceramic
	μA324DC	LM324F	0 to +70	Ceramic
	μA324PC	LM324N	0 to +70	Plastic
	μA3302DC	MC3302F	-40 to +85	Ceramic
	μA3302PC	MC3302N	-40 to +85	Plastic
	μA339/ADC	LM339/AF	0 to +70	Ceramic
	μA339/APC	LM339/AN	0 to +70	Plastic
	μA3403DC	MC3403F	0 to +70	Ceramic
	μA3403PC	MC3403N	0 to +70	Plastic
	μA398HC	SE5537H	-55 to +125	Metal Can
	μA398RC	SE5537N	-55 to +125	Plastic
	μA555TC	NE555N	0 to +70	Plastic
	μA556PC	NE556-1N, NE556N	0 to +70	Plastic
	μA723DC	μA723CF	0 to +70	Ceramic
	μA723DM	μA723F	-55 to +125	Ceramic
	μA723HC	μA723CH	0 to +70	Metal Can
	μA723PC	μA723CN	0 to +70	Plastic
	μA733DC	μA733F	0 to +70	Ceramic
	μA733DM	μA733F	-55 to +125	Ceramic
	μA733PC	μA733N	0 to +70	Plastic
	μA741NM	μA741N	-55 to +125	Plastic
	μA741RC	μA741CF	0 to +70	Ceramic
	μA741TC	μA741CN	0 to +70	Plastic
	μA747DC	μA747CF	0 to +70	Ceramic
	μA747PC	μA747CN	0 to +70	Plastic
	μA9667DC	ULN2003F	0 to +70	Ceramic
	μA9667PC	ULN2003N	0 to +70	Plastic
	μA9668DC	ULN2004F	0 to +70	Ceramic
	μA9668PC	ULN2004N	0 to +70	Plastic
Harris	HA-2539	NE5539	0 to +70	Plastic
	HA-2420-2/8B	SE5060F	-55 to +125	Ceramic
	HA-2425N	NE5060N	0 to +70	Plastic
	HA-2425B	NE5060F	0 to +70	Ceramic
	HA1-5102-2	SE5532/AF	-55 to +125	Ceramic
	HA1-5135-2	SE5534/AF	-55 to +125	Ceramic
	HA1-5135-5	NE5534/AF	0 to +70	Ceramic
	HA3-5102-5	NE5532/AN	0 to +70	Plastic
	HA1-5202-5	NE5532/AF	0 to +70	Ceramic
	HA-5320B	NE5060F	0 to +70	Ceramic
Intersil	ADC0803LCD	ADC0803-1 LCF	-40 to +85	Ceramic
	ADC0804	ADC0804-1 CN	0 to +70	Plastic
	ADC0805	ADC0805-1 LCN	-40 to +85	Plastic
Motorola	DAC-08CD	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08ED	DAC-08EN	0 to +70	Plastic
	DAC-08EF	DAC-08EF	0 to +70	Ceramic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	-55 to +125	Ceramic

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Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
	LM2901N	LM2901N	−40 to +85	Plastic
	LM311J-8	LM311F	0 to +70	Ceramic
	LM311N	LM311N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM339/A J	LM339/AF	0 to +70	Ceramic
	LM339/A N	LM339/AN	0 to +70	Plastic
	LM358N	LM358N	0 to +70	Plastic
	LM393A/J	LM393/AF	0 to +70	Ceramic
	LM393A/N	LM393/AN	0 to +70	Plastic
	MC1408L	MC1408F	0 to +70	Ceramic
	MC1408P	MC1408N	0 to +70	Plastic
	MC1488L	MC1488F	0 to +70	Ceramic
	MC1488P	MC1488N	0 to +70	Plastic
	MC1489/A L	MC1489/AF	0 to +70	Ceramic
	MC1489/A P	MC1489/AN	0 to +70	Plastic
	MC1496L	MC1496F	0 to +70	Ceramic
	MC1496P	MC1496N	0 to +70	Plastic
	MC3302L	MC3302F	−40 to +85	Ceramic
	MC3302P	MC3302N	−40 to +85	Plastic
	MC3361D	MC3361D	0 to +70	SO
	MC3361P	MC3361N	0 to +70	Plastic
	MC3403L	MC3403F	0 to +70	Ceramic
	MC3403P	MC3403N	0 to +70	Plastic
	MC3410CL	MC3410CF	0 to +70	Ceramic
	MC3410L	MC3410F	0 to +70	Ceramic
		NE5410F	0 to +70	Ceramic
	MC3510L	SE5410F	0 to +70	Ceramic
	NE592F	NE592F-8	0 to +70	Ceramic
	NE592F	NE592F-14	0 to +70	Ceramic
	NE592N	NE592N	0 to +70	Plastic
	NE565N	NE565N	0 to +70	Plastic
	SE592F	SE592F-8	−55 to +125	Ceramic
	SE592F	SE592F-14	−55 to +125	Ceramic
	SE592H	SE592H	−55 to +125	Metal Can
National	ADC0803F	ADC0803-1 LCF	−40 to +85	Ceramic
	ADC0803N	ADC0803-1 LCN	−40 to +85	Plastic
	ADC0805	ADC0805-1 LCN	−40 to +85	Plastic
	ADC0820BCN	ADC0820BNEN	0 to +70	Plastic
	ADC0820CCN	ADC0820CNEN	0 to +70	Plastic
	ADC0820BCD	ADC0820BSAN	−40 to +85	Plastic
	ADC0820CCD	ADC0820CSAN	−40 to +85	Plastic
	ADC0820BD	ADC0820BSEF	−55 to +125	Ceramic
	ADC0820CD	ADC0820CSEF	−55 to +125	Ceramic
	DAC0800LCJ	DAC-08EF	0 to +70	Ceramic
	DAC0800LJ	DAC-08F	−55 to +125	Ceramic
	DAC0800LCN	DAC-08EN	0 to +70	Plastic
	DAC0801LCJ	DAC-08CF	0 to +70	Ceramic
	DAC0801LCN	DAC-08CN	0 to +70	Plastic
	DAC0802LJ	DAC-08AF	−55 to +125	Ceramic
	DAC0802LCJ	DAC-08HF	0 to +70	Ceramic
	DAC0802LCN	DAC-08HN	0 to +70	Plastic
	DAC0806LCJ	MC1408-6F	0 to +70	Ceramic
	DAC0806LCN	MC1408-6N	0 to +70	Plastic
	DAC0807LCJ	MC1408-7F	0 to +70	Ceramic
	DAC0807LCN	MC1408-7N	0 to +70	Plastic
	DAC0808LCJ	MC1408F	0 to +70	Ceramic

Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
	DAC0808LCN	MC1408N	0 to +70	Plastic
	DAC0808LD	MC1408F	0 to +70	Ceramic
	LF198H	SE5537H	−55 to +125	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398N	NE5537N	0 to +70	Plastic
	LM13600AN	NE5517N	0 to +70	Plastic
	LM13600N	NE5517N	0 to +70	Plastic
	LM1458N	MC1458N	0 to +70	Plastic
	LM161H	SE529H	−55 to +125	Metal Can
	LM161J	SE529F	−55 to +125	Ceramic
	LM2524J	SG3524F	0 to +70	Ceramic
	LM2524N	SG3524N	0 to +70	Plastic
	LM2901N	LM2901N	−40 to +85	Plastic
	LM2903N	LM2903N	−40 to +85	Plastic
	LM3089	CA3089N	−55 to +125	Plastic
	LM319J	LM319F	0 to +70	Ceramic
	LM319N	LM319N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM324AD	LM324AD	0 to +70	Plastic
	LM324AN	LM324AN	0 to +70	Plastic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM3524J	SG3524F	0 to +70	Ceramic
	LM3524N	SG3524N	0 to +70	Plastic
	LM358H	LM358H	0 to +70	Metal Can
	LM358N	LM358N	0 to +70	Plastic
	LM361H	NE529H	0 to +70	Metal Can
	LM361J	NE529D	0 to +70	SO
	LM361N	NE529N	0 to +70	Plastic
	LM393/AN	LM393/AN	0 to +70	Plastic
	LM555J	NE555F	0 to +70	Ceramic
	LM555N	NE555N	0 to +70	Plastic
	LM556J	SE556-1F	−55 to +125	Ceramic
	LM556N	SE556-1N	−55 to +125	Plastic
	LM556CJ	NE556-1F	0 to +70	Ceramic
	LM556CN	NE556-1N	0 to +70	Plastic
	LM565CN	NE565N	0 to +70	Plastic
	LM566N	SE566N	−55 to +125	Plastic
	LM566CN	NE566N	0 to +70	Plastic
	LM567CN	NE567N	0 to +70	Plastic
	LM733CN	μA733CN	0 to +70	Plastic
	LM741CJ	μA741CF	0 to +70	Ceramic
	LM741CN	μA741CN	0 to +70	Plastic
	LM741J	μA741F	−55 to +125	Ceramic
	LM741N	μA741N	−55 to +125	Plastic
	LM747CJ	μA747CF	0 to +70	Ceramic
	LM747CN	μA747CN	0 to +70	Plastic
	LM747J	μ747F	−55 to +125	Ceramic
	LM747N	μA747N	−55 to +125	Plastic
	UC3842D	UC3842D	0 to +70	Plastic
	UC3842J	UC3842FE	0 to +70	Ceramic
	UC3842N	UC3842N	0 to +70	Plastic
	UC2842D	UC2842D	0 to +70	Plastic
	UC2842J	UC2842FE	0 to +70	Ceramic
	UC2842N	UC2842N	0 to +70	Plastic
	UC1842J	UC1842FE	−55 to +125	Ceramic
	UC1842N	UC1842N	−55 to +125	Plastic

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Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
NEC	μPC1571C	NE571N	0 to +70	Plastic
PMI	CMP-05GP	NE5105N	0 to +70	Plastic
	CMP-05CZ	SE5105F	-55 to +125	Ceramic
	CMP-05BZ	SE5105F	-55 to +125	Ceramic
	CMP-05GZ	SA5105N	-40 to +85	Plastic
	CMP-05FZ	SA5105N	-40 to +85	Plastic
	DAC1408A-6P	MC1408-6N	0 to +70	Plastic
	DAC1408A-6Q	MC1408-6F	0 to +70	Ceramic
	DAC1408A-7N	MC1408-7N	0 to +70	Plastic
	DAC1408A-7Q	MC1408-7F	0 to +70	Ceramic
	DAC1408A-8N	MC1408-8N	0 to +70	Plastic
	DAC1408A-8Q	MC1408-8F	0 to +70	Ceramic
	DAC1508A-8Q	MC1408-8F	-55 to +125	Ceramic
	DAC312FR	AM6012F	0 to +70	Ceramic
	OP27BZ	SE5534AFE	-55 to +125	Ceramic
	OP27CZ	SE5534FE	-55 to +125	Ceramic
	PM747Y	μA747N	-55 to +125	Plastic
	SMP-10AY	SE5060F	-55 to +125	Ceramic
	SMP-10EY	NE5060N	0 to +70	Plastic
	SMP-11AY	SE5060F	-55 to +125	Ceramic
	SMP-11EY	NE5060N	0 to +70	Plastic
Raytheon	RC4805DE	NE5105N	0 to +70	Plastic
	RC4805EDE	NE5105AN	0 to +70	Plastic
	RM4805DE	SE5105F	-55 to +125	Ceramic
	RM4805ADE	SE5105AF	-55 to +125	Ceramic
	RC5532/A DE	NE5532/AF	0 to +70	Ceramic
	RC5532/A NB	NE5532/AN	0 to +70	Plastic
	RC5534/A DE	NE5534/AF	0 to +70	Ceramic
	RC5534/A NB	NE5534/AN	0 to +70	Plastic
	RM5532/A DE	SE5532/AF	-55 to +125	Ceramic
	RM5534/A DE	SE5534/AF	-55 to +125	Ceramic
Silicon General	SG3524J	SG3524F	0 to +70	Ceramic
	SG3526N	SG3526N	0 to +70	Plastic
Sprague	UDN6118A	SA594N	-40 to +85	Plastic
	UDN6118R	SA594F	-40 to +85	Ceramic
	ULN8142M	UC3842N	0 to +70	Plastic
	ULN8160A	NE5560N	0 to +70	Plastic
	ULN8160R	NE5560F	0 to +70	Ceramic
	ULN8161M	NE5561N	0 to +70	Plastic
	ULN8168M	NE5568N	0 to +70	Plastic
	ULN8564A	NE564N	0 to +70	Plastic
	ULN8564R	NE564F	0 to +70	Ceramic
	ULS8564R	SE564F	-55 to +125	Ceramic
TI	ADC0803N	ADC0803-1 LCN	-40 to +85	Plastic
	ADC0804CN	ADC0804-1 CN	0 to +70	Plastic
	ADC0805N	ADC0805-1 LCN	-40 to +85	Plastic
	LM111J	LM111F	-55 to +125	Ceramic
	LM311D	LM311D	0 to +70	Plastic
	LM311J	LM311F	0 to +70	Ceramic
	LM311JG	LM311FE	0 to +70	Ceramic
	LM324D	LM324N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM358P	LM358N	0 to +70	Plastic
	LM393/A P	LM393/AN	0 to +70	Plastic
	MC1458P	MC1458N	0 to +70	Plastic
	NE5532/A JG	NE5532/AF	0 to +70	Ceramic
	NE5532/A P	NE5532/AN	0 to +70	Plastic
	NE5534/A JG	NE5534/AF	0 to +70	Ceramic
	NE5534/A P	NE5534/AN	0 to +70	Plastic
	NE555JG	NE555N	0 to +70	Plastic
	NE555P	NE555N	0 to +70	Plastic
	NE556D	NE556N	0 to +70	Plastic
	NE556J	NE556-1F	0 to +70	Ceramic
	NE556N	NE556-1N	0 to +70	Plastic
	NE592	NE592N14	0 to +70	Plastic
	NE592A	NE592F14	0 to +70	Ceramic
	NE592J	NE592F	0 to +70	Ceramic
	NE592N	NE592N-14	0 to +70	Plastic
	SA556D	SA556N	-40 to +85	Plastic
	SE5534/A JG	SE5534/AF	-55 to +125	Ceramic
	SE555JG	SE555N	-55 to +125	Plastic
	SE556J	SE556-1F	-55 to +125	Ceramic
	SE556N	SE556-1N	-55 to +125	Plastic
	SE592	SE592N14	-55 to +125	Plastic
	SE592J	SE592F-14	-55 to +125	Ceramic
	SE592N	SE592N-14	-55 to +125	Plastic
	SN55107AJ	NE521F	0 to +70	Plastic
	SN55108AJ	SE522F	-55 to +125	Ceramic
	SN75107AJ	NE521F	0 to +70	Plastic
	SN75107AN	NE521N	0 to +70	Plastic
	SN75108AJ	NE522F	0 to +70	Ceramic
	SN75108AN	NE522N	0 to +70	Plastic
	SN75188J	MC1488F	0 to +70	Ceramic
	SN75188N	MC1488N	0 to +70	Plastic
	SN75189AJ	MC1489AF	0 to +70	Ceramic
	SN75189AN	MC1489AN	0 to +70	Plastic
	SN75189J	MC1489F	0 to +70	Ceramic
	SN75189N	MC1489A	0 to +70	Plastic
	TL592A	NE592F14	0 to +70	Ceramic
	TL592P	NE592NB	0 to +70	Plastic
	μA723CJ	μA723CF	0 to +70	Ceramic
	μA723CN	μA723CN	0 to +70	Plastic
	μA723MJ	μA723F	-55 to +125	Ceramic
	μA723MU	μA723D	-55 to +125	SO
Unitrode	UC3524J	SG3524F	0 to +70	Ceramic
	UC3524N	SG3524N	0 to +70	Plastic

*THERE MAY BE PARAMETRIC DIFFERENCES BETWEEN SIGNETICS' PARTS AND THOSE OF THE COMPETITION.

SO Availability List

Linear Products

PART NUMBER	SMD PACKAGE	DESCRIPTION
ADC0820D	SOL-20	8-Bit CMOS A/D
*DAC08ED	SO-16	8-Bit D/A Converter
*LF398D	SO-14	Sample-and-Hold Amp
LM1870D	SOL-20	Stereo Demodulator
LM2901D	SO-14	Quad Volt Comparator
LM2903D	SO-8	Dual Volt Comparator
LM311D	SO-8	Voltage Comparator
LM319D	SO-14	High-Speed Dual Comparator
LM324AD	SO-14	Quad Op Amp
LM324D	SO-14	Quad Op Amp
LM339D	SO-14	Quad Volt Comparator
LM358AD	SO-8	Dual Op Amp
LM358D	SO-8	Dual Op Amp
LM393D	SO-8	Dual Comparator
*MC1408-8D	SO-16	8-Bit D/A Converter
MC1458D	SO-8	Dual Op Amp
MC1488D	SO-14	Quad Line Driver
MC1489D	SO-14	Quad Line Receiver
MC1489AD	SO-14	Quad Line Receiver
MC3302D	SO-14	Quad Volt Comparator
MC3361D	SOL-16	Low Power FM IF
MC3403D	SO-14	Quad Low Power Op Amp
NE4558D	SO-8	Dual Op Amp
*NE5018D	SOL-24	8-Bit D/A Converter
*NE5019D	SOL-24	8-Bit D/A Converter
*NE5036D	SO-14	6-Bit A/D Converter
NE5037D	SO-16	6-Bit A/D Converter
NE5044D	SO-16	Prog 7-Channel Encoder
NE5045D	SO-16	7-Channel Decoder
NE5090D	SOL-16	Address Relay Driver
NE5105/AD	SO-8	High-Speed Comparator
NE5170A	PLCC-28	Octal Line Driver
NE5180A	PLCC-28	Octal Line Receiver
NE5204D	SO-8	High-Frequency Amp
NE5205D	SO-8	High-Frequency Amp
NE521D	SO-14	High-Speed Dual Comparator
NE5212D8	SO-8	Transimedance Amplifier
NE522D	SO-14	High-Speed Dual Comparator
NE5230D	SO-8	Low Voltage Op Amp
NE527D	SO-14	High-Speed Comparator
NE529D	SO-14	High-Speed Comparator
NE532D	SO-8	Dual Op Amp
*NE544D	SOL-16	Servo Amp
*NE5512D	SO-8	Dual Hi-Perf Op Amp
*NE5514D	SOL-16	Quad Hi-Perf Op Amp
NE5517D	SO-16	Dual Hi-Perf Amp
NE5520D	SOL-16	LVDT Signal Cond Ckt
*NE5532D	SOL-16	Dual Low-Noise Op Amp
*NE5533D	SOL-16	Low-Noise Op Amp
NE5534AD	SO-8	Low-Noise Op Amp
NE5534D	SO-8	Low-Noise Op Amp
NE5537D	SO-14	Sample-and-Hold Amp
NE5539D	SO-14	Hi-Freq Amp Wideband
NE555D	SO-8	Single Timer
NE556D	SO-14	Dual Timer
NE5560D	SO-16	SMPS Control Ckt
NE5561D	SO-8	SMPS Control Ckt
NE5562D	SOL-20	SMPS Control Ckt
NE5568D	SO-8	SMPS Control Ckt
NE558D	SOL-16	Quad Timer
NE5592D	SO-14	Dual Video Amp
NE564D	SO-16	Hi-Frequency PLL
*NE565D	SO-14	Phase Locked Loop
NE566D	SO-8	Function Generator
NE567D	SO-8	Tone Decoder PLL
NE568D	SOL-20	PLL
NE571D	SOL-16	Compandor
NE572D	SOL-16	Prog Compandor
*NE587D	SOL-20	7 Seq LED Driver (Anode)
*NE589D	SOL-20	7 Seq LED Driver (Cath)
NE5900D	SOL-16	Call Progress Decoder
NE592D14	SO-14	Video Amp
NE592D8	SO-8	Video Amp
NE592HD14	SO-14	Hi-Gain Video Amp
NE592HD8	SO-8	Hi-Gain Video Amp
*NE594D	SOL-20	Vac Fluor Disp Driver
NE602D	SO-8	Double Bal Mixer/Oscillator
NE604D	SO-16	Low Power FM IF System
NE605	SOL-20	FM IF System
NE612D	SO-8	Double Balanced Mixer/Oscillator
NE614D	SO-16	Low Power FM IF System
*PCD3311TD	SO-16	DTMF/Melody Generator

SO Availability List

PART NUMBER	SMD PACKAGE	DESCRIPTION
PCD3312TD	SO-8	DTMF/Melody Generator With ICC
PCD3315TD	SOL-28	Repertory Pulse Dial
PCD3360TD	SO-16	Progress Tone Ringer
PCF2100TD	SOL-28	LCD Duplex Driver (40)
PCF2111TD	VSO-40	LCD Duplex Driver (64)
PCF2112TD	VSO-40	LCD Duplex Driver (32)
PCF8570TD	SO-8	Static RAM (256 × 8)
PCF8571TD	SO-8	1K Serial RAM
PCF8573TD	SO-16	Clock/Timer
PCF8574TD	SO-16	Remote I/O Expander
PCF8576TD	VSO-56	MUX/Static Driver
PCF8577TD	VSO-40	32-/64-Segment LCD Driver
SA5105/AD	SO-8	High-Speed Comparator
SA5230D	SO-8	Low Voltage Op Amp
SA5212D8	SO-8	Transimpedance Amp
SA532D	SO-8	Dual Op Amp
SA534D	SO-14	Dual Op Amp
SA555D	SO-8	Single Timer
SA571D	SOL-16	Compandor
SA572D	SOL-16	Compandor
*SA594D	SOL-20	Vac Fluor Disp Driver
SA602D	SO-8	Double Bal Mixer/ Oscillator
SA604D	SO-16	Lower Power FM IF System

PART NUMBER	SMD PACKAGE	DESCRIPTION
SAA3004TD	SOL-20	R/C Transmitter
SG3524D	SO-16	SMPS Control Circuit
TDA1001BTD	SO-16	Noise Suppressor
TDA1005ATD	SO-16	Stereo Decoder
TDA3047TD	SO-16	IR Preamp
TDA3048TD	SO-16	IR Preamp
TDA5040TD	SO-8	Brushless DC Motor Driver
TDA7010TD	SO-16	FM Radio Circuit
TDA7050TD	SO-8	Mono/Stereo Amp
TDD1742TD	SOL-28	Frequency Synthesizer
ULN2003D	SO-16	Transistor Array
ULN2004D	SO-16	Transistor Array
μA723CD	SO-14	Voltage Regulator
μA741CD	SO-8	Single Op Amp
μA747CD	SO-14	Dual Op Amp

NOTE:
*Non-standard pinout.

UNDER DEVELOPMENT

PART NUMBER	SMD PACKAGE	DESCRIPTION
26LS31D	SO-16	RS-422 Line Driver
26LS32D	SO-16	RS-422 Line Receiver
26LS33D	SO-16	RS-422 Line Receiver
26LS29D	SO-16	RS-423 Line Driver
26LS30D	SO-16	RS-423 Line Receiver

NOTE:
For information regarding additional SO products released since the publication of this document, contact your local Signetics Sales Office.

Ordering Information for Prefixes ADC, AM, CA, DAC, ICM, LF, LM, MC, NE, OP, SA, SE, SG, μA, UC, ULN

Linear Products

Signetics' Linear integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order
$250 per line item per order

Military Product:

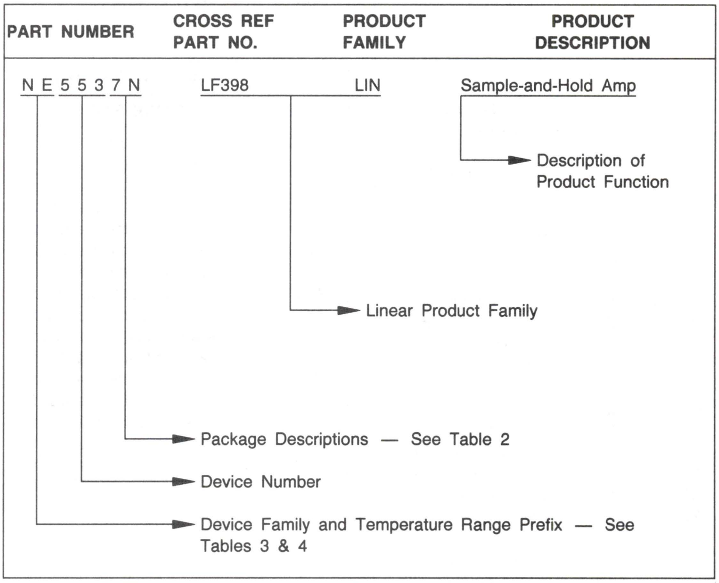
$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that an SE prefix (−55°C to +125°C) indicates only the operating temperature range of a device and *not* its military qualification status. The military qualification status of any Linear product can be determined by either looking in the Military Data Manual and/or contacting your local sales office.

Table 1. Part Number Description


PART NUMBER
CROSS REF PART NO.
PRODUCT FAMILY
PRODUCT DESCRIPTION
N E 5 5 3 7 N
LF398
LIN
Sample-and-Hold Amp
Description of Product Function
Linear Product Family
Package Descriptions — See Table 2
Device Number
Device Family and Temperature Range Prefix — See Tables 3 & 4

Ordering Information

Table 2. Package Descriptions

OLD	NEW	PACKAGE DESCRIPTION
A, AA	N	14-lead plastic DIP
A	N-14	14-lead plastic DIP (selected analog products only)
B, BA	N	16-lead plastic DIP
	D	Microminiature package (SO)
F	F	14-, 16-, 18-, 22-, and 24-lead ceramic DIP (Cerdip)
I, IK	I	14-, 16-, 18-, 22-, 28-, and 4-lead ceramic DIP
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA, NX	N	24-lead plastic DIP
Q, R	Q	10-, 14-, 16-, and 24-lead ceramic flat
T, TA	H	8-lead TO-99
U	U	SIP plastic power
V	N	8-lead plastic DIP
XA	N	18-lead plastic DIP
XC	N	20-lead plastic DIP
XC	N	22-lead plastic DIP
XL, XF	N	28-lead plastic DIP
	A	PLCC
	EC	TO-46 header
	FE	8-lead ceramic DIP

Table 3. Signetics Prefix and Device Temperature

PREFIX	DEVICE TEMPERATURE RANGE
NE	0 to +70°C
SE	−55°C to +125°C
SA	−40°C to +85°C

Table 4. Industry Standard Prefix

PREFIX	DEVICE FAMILY
ADC	Linear Industry Standard
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
ICM	Linear Industry Standard
LF	Linear Industry Standard
LM	Linear Industry Standard
MC	Linear Industry Standard
NE	Linear Industry Standard
OP	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
UC	Linear Industry Standard
ULN	Linear Industry Standard

Ordering Information for Prefixes HE, OM, MA, ME, PC, PN, SA, TB, TC, TD, TE

Signetics' integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors.

Minimum Factory Order:
Commercial Product:

$ 1000 per order

$ 250 per line item per order

Table 1 provides part number information concerning Signetics/Philips integrated circuits.

Table 2 provides package suffixes and descriptions for all presently existing types. Letters following the device number not used in Table 2 are considered to be part of the device number.

Table 3 provides explanations on the various prefixes employed in the part number descriptions. As noted in Table 3, Signetics/Philips device operating temperature is defined by the appropriate prefix.

OPERATING TEMPERATURE:

The third letter of the prefix, in a three-letter prefix, is the temperature designator.

The letters A to F give information about the operating temperature:

A: Temperature range not specified. See data sheet.
e.g. TDA2541N
B: 0 to +70°C
e.g. PCB8573PN
C: -55°C to +125°C
e.g. PCC2111PN
D: -25°C to +70°C
e.g. PCD8571PN
E: -25°C to +85°C
e.g. PCE2111PN
F: -40°C to +85°C
e.g. PCF2111PN

Table 1. Part Number Description

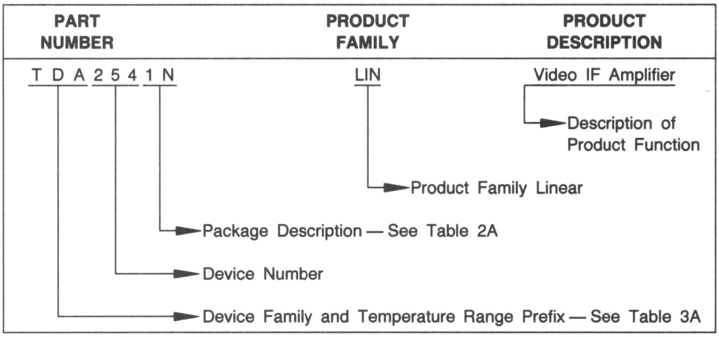

PART NUMBER
PRODUCT FAMILY
PRODUCT DESCRIPTION
T D A 2 5 4 1 N
LIN
Video IF Amplifier
Description of Product Function
Product Family Linear
Package Description — See Table 2A
Device Number
Device Family and Temperature Range Prefix — See Table 3A

Table 2. Package Description

SUFFIX	PACKAGE DESCRIPTION
PN	8-, 14-, 16-, 18-, 20-, 24-, 28-, 40-lead plastic DIP
TD	Microminiature Package (SO)
DF	14-, 16-, 18-, 22-, 24-lead ceramic DIP
U	Single in-line plastic (SIP) and SIP power packages

Table 3. Device Prefix

PREFIX	DEVICE FAMILY
HEx	CMOS circuit
OM	Linear circuit
MAx	Microcomputer
MEx	Microcomputer peripheral
PCx	CMOS circuit
PNx	NMOS circuit
SAx	Digital circuit
TBx	Linear circuit
TCx	Linear circuit
TDx	Linear circuit
TEx	Linear circuit

Signetics

Linear Products

Section 2
Quality and Reliability

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Linear Division Quality and Reliability 2-5
Linear Division Product Flow 2-8

"Given the increasingly intense competitive pressures our customers face, they should demand nothing less than zero defects from every IC vendor. We now know that zero defects is an achievable goal. Why should IC customers pay for errors?"

Norman Neumann
President
Signetics Corporation

Quality and Reliability

SIGNETICS' ZERO DEFECTS PROGRAM

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressures. As a result of this quality focus, it is becoming clear that what was once thought to be unattainable — zero defects — is, in fact, achievable.

The IC supplier committed to a standard of zero defects provides a competitive advantage to today's electronics OEM. That advantage can be summed up in four words: *reduced cost of ownership*. As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that the quality-conscious supplier represents a viable cost reduction resource. Consistently high quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures.

REDUCING THE COST OF OWNERSHIP THROUGH TOTAL QUALITY PERFORMANCE

Quality involves more than just IC's that work. It also includes cost-saving advantages that come with error-free service — on-time delivery of the right quantity of the right product at the agreed-upon price. Beyond the product, you want to know you can place an order and feel confident that no administrative problems will arise to tie up your time and personnel.

Today, as a result of Signetics' growing appreciation of the concern with cost of ownership, our quality improvement efforts extend out from the traditional areas of product conformance into every administrative function, including order entry, scheduling, delivery, shipping, and invoicing. Driving this process is a Corporate Quality Improvement Team, comprised of the president and his staff, which oversees the activities of 30 other Quality Improvement Teams throughout the company.

CUSTOMER/VENDOR COOPERATION IS AT THE HEART OF ZERO DEFECTS AND REDUCED COSTS

Working to a zero defects standard requires that emphasis be consistently placed, not on "catching" defects, but on preventing them from ever occurring. This strong preventive focus, which demands that quality be "built-in" rather than "inspected in," includes a much greater attention to ongoing communication on quality-related issues. At Signetics, a focus on this cooperative approach has resulted in better service to all customers and the development of two innovative customer/vendor programs: Ship-to-Stock and Self-Qual.

As a result of their participation in the Ship-to-Stock Program, many of our customers have eliminated costly incoming testing on selected ICs. We will work together with any customer interested to establish a Ship-to-Stock Program, and identify the products to be included in the program and finalize all necessary terms and conditions. From that point, the specified products can go directly from the receiving dock to the assembly line or into inventory. Signetics then provides, free of charge, monthly reports on those products.

In our efforts to continually reduce cost of ownership, we are now using the experience we have gained with Ship-to-Stock to begin developing a Just-in-Time Program. With Just-in-Time, products will be delivered to the receiving dock just as they are needed, permitting continuous-flow manufacturing and eliminating the need for expensive inventories.

Like Ship-to-Stock, our Self-Qual Program employs a cooperative approach based on ongoing information exchange. At Signetics, formal qualification procedures are required for all new or changed materials, processes, products, and facilities. Prior to 1983, we created our qualification programs independently. Our major customers would then test samples to confirm our findings. Now, under the new Self-Qual Program, customers can be directly involved in the prequalification stage. When we feel we have a promising enhancement to offer, customers will be invited to participate in the development of the qualification plan. This eliminates the need to duplicate expensive qualification testing and also adds another dimension to our ongoing efforts to build in quality.

PRODUCT RELIABILITY: QUALITY OVER TIME IS THE GOAL

Our concern with product reliability has developed from communication with many customers. In discussions, these customers have emphasized the high cost of field failures, both in terms of dollars and reputations in the marketplace.

In response to these concerns, we have placed an emphasis on improving product reliability. As a result of this effort, our product reliability has improved more than fourfold in a five-year period (see Figure 1). A key program, SURE (Systematic and Uniform Reliability Evaluation), highlights the significant progress made in this critical area.

SURE was first instituted in 1964 as the core reliability measurement for all Signetics products. In 1980, as a first major step toward improving product reliability, SURE was enhanced by increasing sampling frequency and size and by extending stress tests. As a result of these improvements, most of our major customers now utilize SURE data with no requests for additional reliability testing.

WE WANT TO WORK WITH YOU

At Signetics, we know that our success depends on our ability to support all our customers with the defect-free, higher density, higher performance products needed to compete effectively in today's demanding business environment. To achieve this goal, quality in another arena — that of communications — is vital. Here are some specific ways we can maintain an ongoing dialogue and information exchange between your company and ours on the quality issue:

- Periodical face-to-face exchanges of data and quality improvement ideas between the customer and Signetics can help prevent problems before they occur.
- Test correlation data is very useful. Line pull information and field failure reports also help us improve product performance.
- When a problem occurs, provide us as soon as possible with whatever specific data you have. This will assist us in taking prompt corrective action.

Quality products are, in large measure, the result of quality communication. By working together, by opening up channels through which we can talk openly to each other, we will insure the creation of the innovative, reliable, cost effective products that help insure a competitive edge.

Quality and Reliability

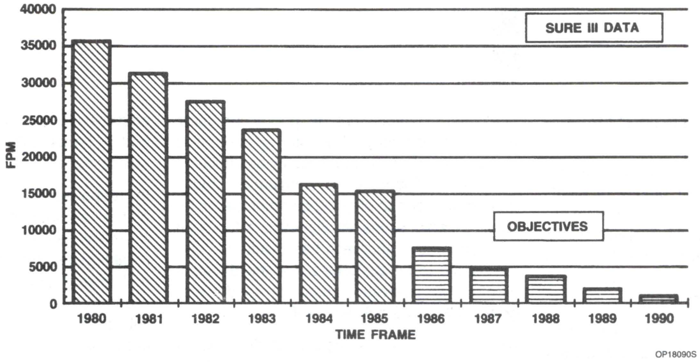


Figure 1

QUALITY AND RELIABILITY ASSURANCE

Signetics' Linear Division Quality and Reliability Assurance Department is involved in all stages of the production of our Linear ICs:

- Product Design and Process Development
- Wafer Fabrication
- Assembly
- Inspection and Test
- Product Reliability Monitoring
- Customer liaison

The result of this continual involvement at all stages of production enables us to provide feedback to refine present and future designs, manufacturing processes, and test methodology to enhance both the quality and reliability of the products delivered to our customers.

LINEAR PRODUCT QUALITY

Signetics has put together a winning process for the manufacturing of Linear Integrated Circuits. The circuits produced by our Linear Division must meet rigid criteria as defined in our design rules and as evaluated through product characterization over the device operating temperature range. Product conformance to specification is measured throughout the manufacturing cycle. Our standard is Zero Defects and our customers' statistics and awards for outstanding product quality demonstrate our advance toward this goal.

Nowhere is this more evident than at our Electrical Outgoing Product Assurance inspection gate. Over the past six years, the measured defect level at the first submission to Product Assurance for Linear products has dropped from over 4000PPM (0.4%) to under 150PPM (0.015%) (see Figure 2). Signetics calls the first submittal to a Product or Quality Assurance gate our Estimated Process Quality or EPQ. It is an internal measure used to drive our Quality Improvement Programs toward our goal of Zero Defects. All product acceptance sampling plans have zero as their acceptance criteria. Only shipments that demonstrate zero defects during these acceptance tests may be shipped to our customers. This is in accordance with our commitment to our Zero Defect policy.

The results from our Quality Improvement Program have allowed Signetics to take the industry leadership position with its Zero Defects Limited Warranty policy. No longer is it necessary to negotiate a mutually acceptable AQL between buyer and Signetics. Signetics will replace any lot in which a customer finds one verified defective part.

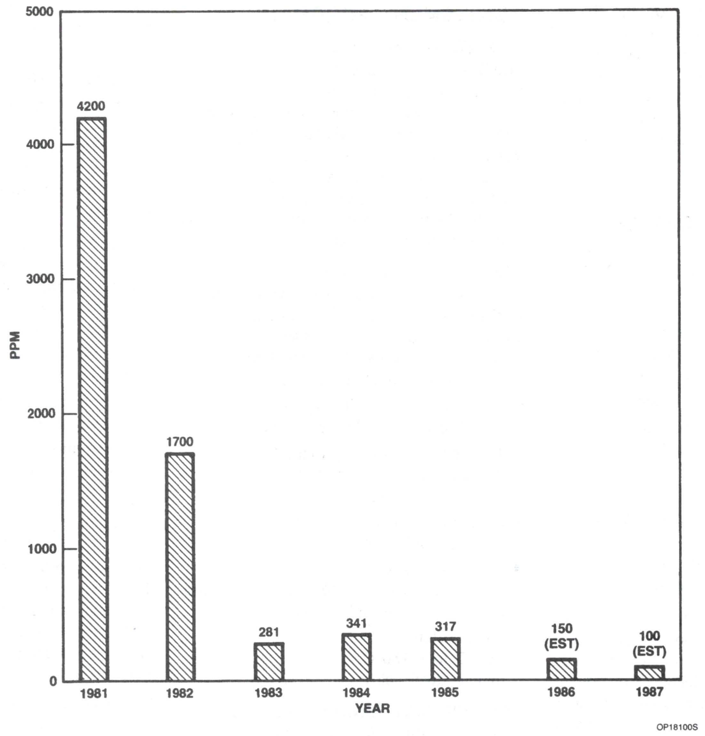


Figure 2. Electrical Estimated Process Quality (EPQ)

QUALITY DATABASE REPORTING SYSTEM — QA05

The capabilities of our manufacturing process are measured and the results are recorded through our corporate-wide QA05 database system. The QA05 system collects the results on all finished lots and feeds this data back to concerned organizations where appropriate corrective actions can be taken. The QA05 reports Estimated Process Quality (EPQ) data which are the sample inspection results for first submittal lots to Quality Assurance inspection for electrical, visual/mechanical, hermeticity, and documentation. Data from this system is available upon request and is distributed routinely to our customers who have formally adopted our Ship-to-Stock program.

SIGNETICS' SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into inventory or to the assembly line from the customer's receiving dock without incoming inspection. This program was developed at the request of several major customers after they had worked with us and had a chance to experience the data exchange and joint corrective action that occurs as part of our quality improvement program.

The key elements of the Ship-to-Stock program are:

- Signetics and customer agree on a list of products to be certified, complete device correlation, and sign a specification.
- The product Estimated Product Quality (EPQ) must be 300ppm or less for the past 3 months.
- Signetics will share Quality (QA05) and Reliability data on a regular basis.
- Signetics will alert Ship-to-Stock customers of any changes in quality or reliability which could adversely impact their product.

Any customer interested in the benefits of the Ship-to-Stock program should contact his local Signetics sales office for a brochure and further details.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 5×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. All circuit designs are computer-checked using the latest CAD software for adherence to design rules. Simulations are performed for functionality and parametric performance over the full operating ranges of voltage and temperature before going to production. These steps allow us to meet device specifications not only the first time, but also every time thereafter.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees.

PRODUCT QUALIFICATION

Linear products are subjected to rigorous qualification procedures for all new products or redesigns to current products. Qualification testing consists of:

- High Temperature Operating Life: $T_J = 150°C$, 1000 hours, static bias
- High Temperature Storage Life: $T_J = 150°C$, 1000 hours, unbiased
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker: 15 psig, 121°C, 192 hours, unbiased
- Thermal Shock: −65°C to +150°C, 300 cycles, 5 minute dwell, liquid to liquid, unbiased

Formal qualification procedures are required for all new or changed products, processes, and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

ONGOING RELIABILITY ASSESSMENT PROGRAMS

The SURE Program

The SURE (Systematic and Uniform Reliability Evaluation) program audits products from each of Signetics Linear Division's process families: Low Voltage, Medium Voltage, High Voltage, and Dual-Layer Metal, under a variety of accelerated stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The Audit Program

Samples are selected from each process family every four weeks and are subjected to each of the following stresses:

- High Temperature Operating Life: $T_J = 150°C$, 1000 hours, static bias
- High Temperature Storage Life: $T_J = 150°C$, 1000 hours, unbiased
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker: 20 psig, 127°C, 72 hours, unbiased
- Thermal Shock: −65°C to +150°C, 300 cycles, 5 minute dwell, liquid-to-liquid, unbiased
- Temperature Cycling: −65°C to +150°C, 1000 cycles, 10 minute dwell, air-to-air, unbiased

The Product Monitor Program

In addition, each Signetics assembly plant performs Pressure Cooker and Thermal Shock SURE Product Monitor stresses on a weekly basis on each molded package by pin count per the same conditions as the SURE Program.

Product Reliability Reports

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms, and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request. Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Reliability Engineering

In addition to the product performance monitors encompassed in the Linear SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

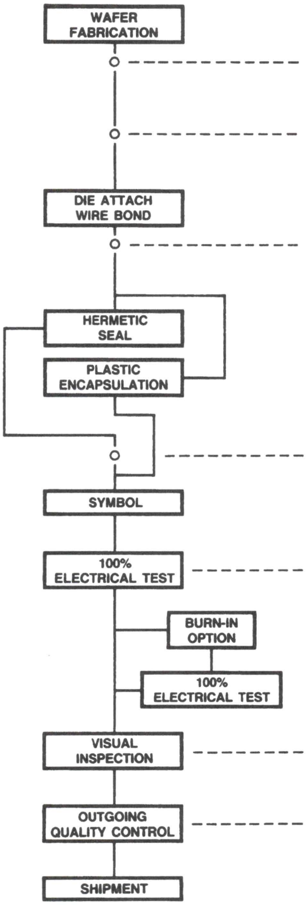
- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in some evaluation programs.

Failure Analysis

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional, and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

LINEAR DIVISION LINEAR PROCESS FLOW



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

DIE ATTACH AND WIRE BONDING

The latest automated equipment is used under statistical process control program.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% and fine gross leak testing.

SYMBOL

Devices are marked with the Signetics logo, device number and period date code of assembly or custom symbol per individual specification requirements.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

BURN-IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum Junction Temperature.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

VISUAL

All products are visually inspected per the requirements specified in Signetics' or customer documents.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees the specified mechanical and electrical AQL's. Every shipment is sealed and identified by QA personnel.

PF00850S

Signetics

Section 3
Small Area Networks

Linear Products

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Introduction to I^2C

THE I^2C CONCEPT

The Inter-IC bus (I^2C) is a 2-wire serial bus designed to provide the facilities of a small area network, not only between the circuits of one system, but also between different systems; e.g., teletext and tuning.

Philips/Signetics manufactures many devices with built-in I^2C interface capability, any of which can be connected in a system by simply "clipping" it to the I^2C bus. Hence, any collection of these devices around the I^2C bus is known as "clips."

The I^2C bus consists of two bidirectional lines: the Serial Data (SDA) line and the Serial Clock (SCL) line. The output stages of devices connected to the bus (these devices could be NMOS, CMOS, I^2C, TTL, ...) must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred at a rate up to 100kbits/sec. The physical bus length is limited to 13 feet and the number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

The inherent synchronization process, built into the I^2C bus structure using the wired-AND technique, not only allows fast devices to communicate with slower ones, but also eliminates the "Carrier Sense Multiple Access/Collision Detect" (CSMA/CD) effect found in some local area networks, such as Ethernet.

Master-slave relationships exist on the I^2C bus; however, there is no central master. Therefore, a device addressed as a slave during one data transfer could possibly be the master for the next data transfer. Devices are also free to transmit or receive data during a transfer.

To summarize, the I^2C bus eliminates interfacing problems. Since any peripheral device can be added or taken away without affecting any other devices connected to the bus, the I^2C bus enables the system designer to build various configurations using the same basic architecture.

Application areas for the I^2C bus include:

Video Equipment
Audio Equipment
Computer Terminals
Home Appliances
Telephony
Automotive
Instrumentation
Industrial Control

I^{2}C Bus Specification

INTRODUCTION

For 8-bit applications, such as those requiring single-chip microcomputers, certain design criteria can be established:

- **A complete system usually consists of at least one microcomputer and other peripheral devices, such as memories and I/O expanders.**
- **The cost of connecting the various devices within the system must be kept to a minimum.**
- **Such a system usually performs a control function and does not require high-speed data transfer.**
- **Overall efficiency depends on the devices chosen and the interconnecting bus structure.**

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be resolved to decide which device will be in control of the bus and when. And if different devices with different clock speeds are connected to the bus, the bus clock source must be defined.

All these criteria are involved in the specification of the I^{2}C bus.

THE I^{2}C BUS CONCEPT

Any manufacturing process (NMOS, CMOS, I^{2}L) can be supported by the I^{2}C bus. Two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Each device is recognized by a unique address – whether it is a microcomputer, LCD driver, memory or keyboard interface – and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, while a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I^{2}C bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually microcomputers, let's consider the case of a data transfer between two microcomputers connected to the I^{2}C bus (Figure 1). This highlights the master-slave and receiver-transmitter relationships to be found on the I^{2}C bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would follow in this way:

1) Suppose microcomputer A wants to send information to microcomputer B
   - microcomputer A (master) addresses microcomputer B (slave)
   - microcomputer A (master transmitter) sends data to microcomputer B (slave receiver)
   - microcomputer A terminates the transfer.
2) If microcomputer A wants to receive information from microcomputer B
   - microcomputer A (master) addresses microcomputer B (slave)
   - microcomputer A (master receiver) receives data from microcomputer B (slave transmitter)
   - microcomputer A terminates the transfer.

Even in this case, the master (microcomputer A) generates the timing and terminates the transfer.

The possibility of more than one microcomputer being connected to the I^{2}C bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event, an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all devices to the I^{2}C bus.

If two or more masters try to put information on to the bus, the first to produce a one when the other produces a zero will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Arbitration and Clock Generation).

Generation of clock signals on the I^{2}C bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow slave

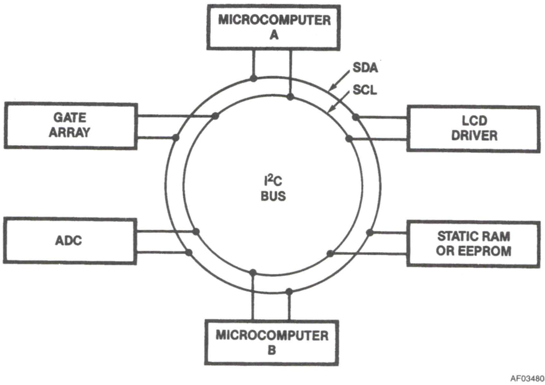


Figure 1. Typical I^{2}C Bus Configuration

Table 1. Definition of I^{2}C Bus Terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

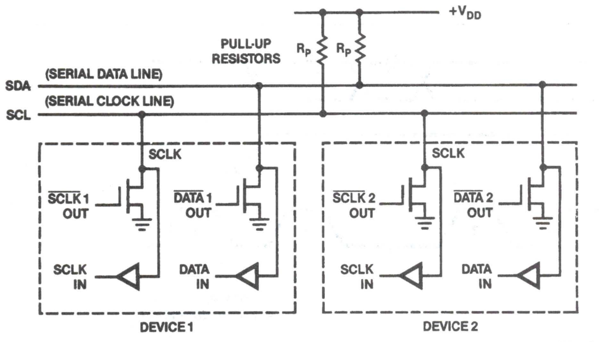

+V$_{DD}$
PULL-UP RESISTORS
R$_P$
R$_P$
SDA
(SERIAL DATA LINE)
SCL
(SERIAL CLOCK LINE)
SCLK
$\overline{\text{SCLK}}$ 1 OUT
$\overline{\text{DATA}}$ 1 OUT
SCLK IN
DATA IN
DEVICE 1
SCLK
$\overline{\text{SCLK}}$ 2 OUT
$\overline{\text{DATA}}$ 2 OUT
SCLK IN
DATA IN
DEVICE 2
LD05610S

Figure 2. Connection of Devices to the I^{2}C Bus

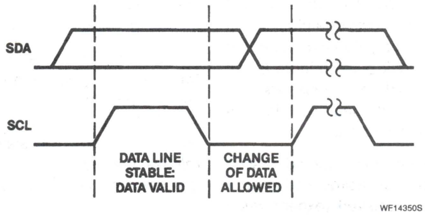

SDA
SCL
DATA LINE STABLE: DATA VALID
CHANGE OF DATA ALLOWED
WF14350S

Figure 3. Bit Transfer on the I^{2}C Bus

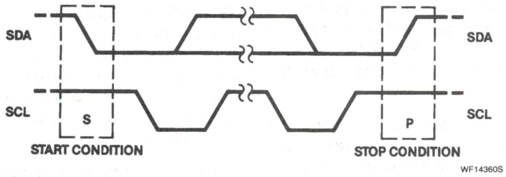

SDA
SCL
S
START CONDITION
SDA
SCL
P
STOP CONDITION
WF14360S

Figure 4. Start and Stop Conditions

device holding down the clock line or by another master when arbitration takes place.

GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 2). When the bus is free, both lines are High. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I^{2}C bus can be transferred at a rate up to 100kbit/s. The number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, I^{2}L) which can be connected to the I^{2}C bus, the levels of the logical 0 (Low) and 1 (High) are not fixed and depend on the appropriate level of V$_{DD}$ (see Electrical Specifications). One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the High period of the clock. The High or Low state of the data line can only change when the clock signal on the SCL line is Low (Figure 3).

Start and Stop Conditions

Within the procedure of the I^{2}C bus, unique situations arise which are defined as start and stop conditions (see Figure 4).

A High-to-Low transition of the SDA line while SCL is High is one such unique case. This situation indicates a start condition.

A Low-to-High transition of the SDA line while SCL is High defines a stop condition.

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again a certain time after the stop condition. This bus free situation will be described later in detail.

Detection of start and stop conditions by devices connected to the bus is easy if they possess the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

TRANSFERRING DATA

Byte Format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit.

I^{2}C Bus Specification

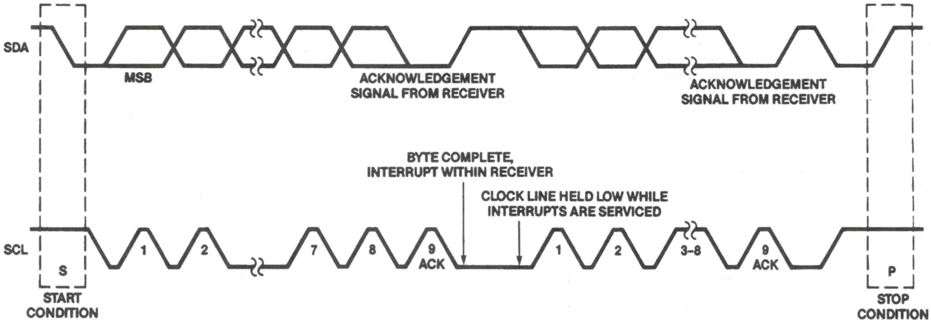

SDA
MSB
ACKNOWLEDGEMENT SIGNAL FROM RECEIVER
ACKNOWLEDGEMENT SIGNAL FROM RECEIVER
BYTE COMPLETE, INTERRUPT WITHIN RECEIVER
CLOCK LINE HELD LOW WHILE INTERRUPTS ARE SERVICED
SCL
S
1
2
7
8
9 ACK
1
2
3-8
9 ACK
P
START CONDITION
STOP CONDITION
WF14370S

Figure 5. Data Transfer on the I^{2}C Bus

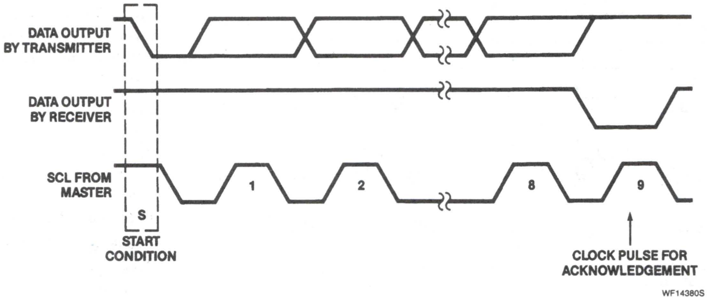

DATA OUTPUT BY TRANSMITTER
DATA OUTPUT BY RECEIVER
SCL FROM MASTER
S
START CONDITION
1
2
8
9
CLOCK PULSE FOR ACKNOWLEDGEMENT
WF14380S

Figure 6. Acknowledge on the I^{2}C Bus

Data is transferred with the most significant bit (MSB) first (Figure 5). If a receiving device cannot receive another complete byte of data until it has performed some other function, for example, to service an internal interrupt, it can hold the clock line SCL Low to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases the clock line SCL.

In some cases, it is permitted to use a different format from the I^{2}C bus format, such as CBUS compatible devices. A message which starts with such an address can be terminated by the generation of a stop condition, even during the transmission of a byte. In this case, no acknowledge is generated.

Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitting device releases the SDA line (High) during the acknowledge clock pulse.

The receiving device has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable Low during the high period of this clock pulse (Figure 6). Of course, setup and hold times must also be taken into account and these will be described in the Timing section.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received (except when the message starts with a CBUS address.

When a slave receiver does not acknowledge on the slave address, for example, because it is unable to receive while it is performing some real-time function, the data line must be left High by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver does acknowledge the slave address, but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave not generating the acknowledge on the first byte following. The slave leaves the data line High and the master generates the STOP condition.

In the case of a master receiver involved in a transfer, it must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate the STOP condition.

ARBITRATION AND CLOCK GENERATION

Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I^{2}C bus. Data is only valid during the clock High period on the SCL line; therefore, a defined clock is needed if the bit-by-bit arbitration procedure is to take place.

Clock synchronization is performed using the wired-AND connection of devices to the SCL LINE. This means that a High-to-Low transi-

I^{2}C Bus Specification

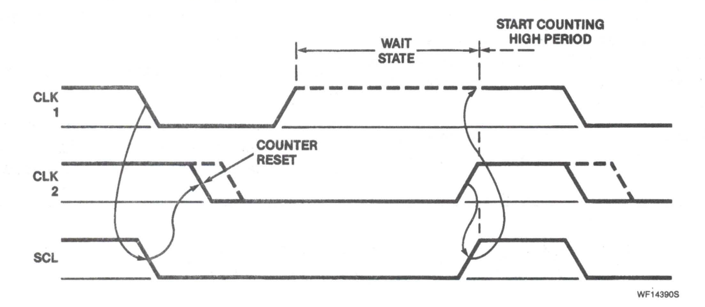


Figure 7. Clock Synchronization During the Arbitration Procedure

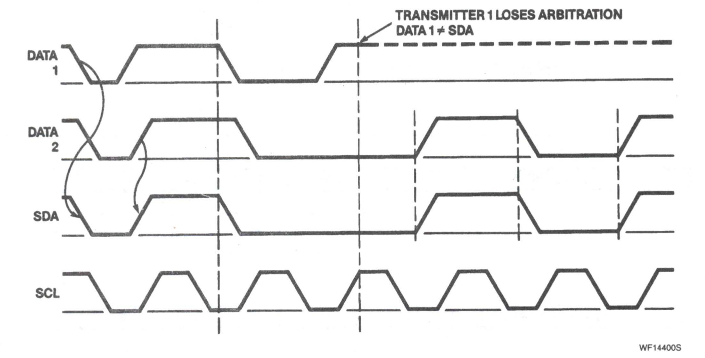


Figure 8. Arbitration Procedure of Two Masters

tion on the SCL line will affect the devices concerned, causing them to start counting off their Low period. Once a device clock has gone Low it will hold the SCL line in that state until the clock High state is reached (Figure 7). However, the Low-to-High change in this device clock may not change the state of the SCL line if another device clock is still within its Low period. Therefore, SCL will be held Low by the device with the longest Low period. Devices with shorter Low periods enter a High wait state during this time.

When all devices concerned have counted off their Low period, the clock line will be released and go High. There will then be no difference between the device clocks and the state of the SCL line and all of them will start counting their High periods. The first device to complete its High period will again pull the SCL line Low.

In this way, a synchronized SCL clock is generated for which the Low period is determined by the device with the longest clock Low period while the High period on SCL is determined by the device with the shortest clock High period.

Arbitration

Arbitration takes place on the SDA line in such a way that the master which transmits a High level, while another master transmits a Low level, will switch off its DATA output stage since the level on the bus does not correspond to its own level.

Arbitration can carry on through many bits. The first stage of arbitration is the comparison of the address bits. If the masters are each trying to address the same device, arbitration continues into a comparison of the data. Because address and data information is used on the I^{2}C bus for the arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master does lose arbitration during the addressing stage, it is possible that the winning master is trying to address it. Therefore, the losing master must switch over immediately to its slave receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course more may be involved, depending on how many masters are connected to the bus. The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a High output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. As control of the I^{2}C bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Use of the Clock Synchronizing Mechanism as a Handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receiving devices to cope with fast data transfers, either on a byte or bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slave devices can then hold the SCL line Low, after reception and acknowledge of a byte, to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcomputer without a hardware I^{2}C interface on-chip can slow down the bus clock by extending each clock Low period. In this way, the speed of any master is adapted to the internal operating rate of this device.

I²C Bus Specification

FORMATS

Data transfers follow the format shown in Figure 9. After the start condition, a slave address is sent. This address is 7 bits long; the eighth bit is a data direction bit (R/$\overline{W}$). A zero indicates a transmission (WRITE); a one indicates a request for data (READ). A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate another start condition, and address another slave without first generating a stop condition. Various combinations of read/write formats are then possible within such a transfer.

At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave.

The stop condition is generated by the master.

During a change of direction within a transfer, the start condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

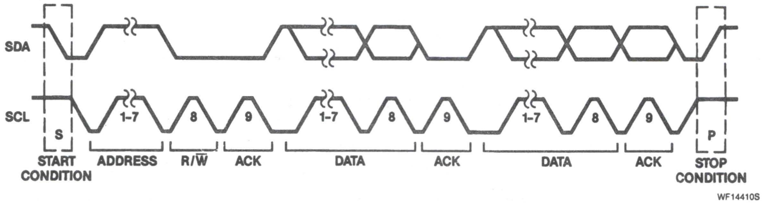
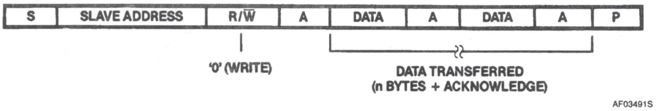

SDA
SCL
S
1-7
8
9
1-7
8
9
1-7
8
9
P
START CONDITION
ADDRESS
R/W̄
ACK
DATA
ACK
DATA
ACK
STOP CONDITION
WF14410S

Figure 9. A Complete Data Transfer

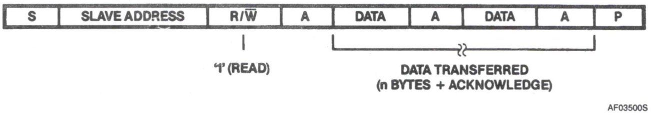
Possible Data Transfer Formats are:

a) Master transmitter transmits to slave receiver. Direction is not changed.

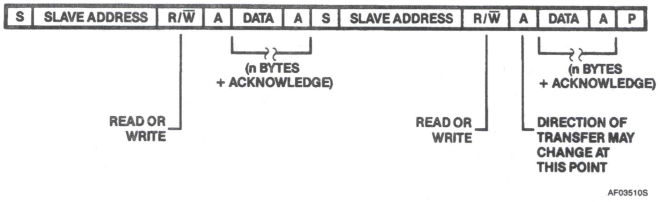
A = ACKNOWLEDGE
S = START
P = STOP


S
SLAVE ADDRESS
R/W̄
A
DATA
A
DATA
A
P
'0' (WRITE)
DATA TRANSFERRED
(n BYTES + ACKNOWLEDGE)
AF03491S

b) Master reads slave immediately after first byte.


S
SLAVE ADDRESS
R/W̄
A
DATA
A
DATA
A
P
'1' (READ)
DATA TRANSFERRED
(n BYTES + ACKNOWLEDGE)
AF03500S

c) Combined formats.


S
SLAVE ADDRESS
R/W̄
A
DATA
A
S
SLAVE ADDRESS
R/W̄
A
DATA
A
P
(n BYTES + ACKNOWLEDGE)
(n BYTES + ACKNOWLEDGE)
READ OR WRITE
READ OR WRITE
DIRECTION OF TRANSFER MAY CHANGE AT THIS POINT
AF03510S

NOTES:
1. Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the start condition is repeated, data can then be transferred.
2. All decisions on auto-increment or decrement of previously accessed memory locations, etc., are taken by the designer of the device.
3. Each byte is followed by an acknowledge as indicated by the A blocks in the sequence.
4. I²C devices have to reset their bus logic on receipt of a start condition so that they all anticipate the sending of a slave address.

ADDRESSING

The first byte after the start condition determines which slave will be selected by the master. Usually, this first byte follows that start procedure. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge, although devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

Definition of Bits in the First Byte

The first seven bits of this byte make up the slave address (Figure 10). The eighth bit (LSB – least significant bit) determines the direction of the message. A zero on the least significant position of the first byte means that the master will write information to a selected slave; a one in this position means that the master will read information from the slave.

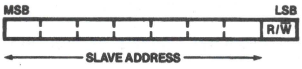


Figure 10. The First Byte After the Start Procedure

When an address is sent, each device in a system compares the first 7 bits after the start condition with its own address. If there is a match, the device will consider itself addressed by the master as a slave receiver or slave transmitter, depending on the R/$\overline{W}$ bit.

The slave address can be made up of a fixed and a programmable part. Since it is expected that identical ICs will be used more than once in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I^{2}C bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of eight identical devices can be connected to the same bus.

The I^{2}C bus committee is available to coordinate allocation of I^{2}C addresses.

The bit combination 1111XXX of the slave address is reserved for future extension purposes.

The address 1111111 is reserved as the extension address. This means that the addressing procedure will be continued in the next byte(s). Devices that do not use the extended addressing do not react at the reception of this byte. The seven other possibilities in group 1111 will also only be used for extension purposes but are not yet allocated.

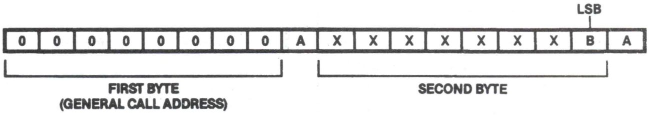


Figure 11. General Call Address Format

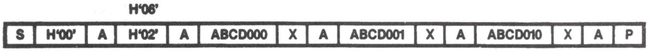


Figure 12. Sequence of a Programming Master

The combination 0000XXX has been defined as a special group. The following addresses have been allocated:

FIRST BYTE			
Slave Address		$R/\overline{W}$	
0000	000	0	General call address
0000	000	1	Start byte
0000	001	X	CBUS address
0000	010	X	Address reserved for different bus format
0000	011	X	To be defined
0000	100	X	
0000	101	X	
0000	110	X	
0000	111	X	

No device is allowed to acknowledge at the reception of the start byte.

The CBUS address has been reserved to enable the intermixing of CBUS and I^{2}C devices in one system. I^{2}C bus devices are not allowed to respond at the reception of this address.

The address reserved for a different bus format is included to enable the mixing of I^{2}C and other protocols. Only I^{2}C devices that are able to work with such formats and protocols are allowed to respond to this address.

General Call Address

The general call address should be used to address every device connected to the I^{2}C bus. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If a device does require data from a general call address, it will acknowledge this address and behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging.

The meaning of the general call address is always specified in the second byte (Figure 11).

There are two cases to consider:

1. When the least significant bit B is a zero.
2. When the least significant bit B is a one.

When B is a zero, the second byte has the following definition:

00000110 (H'06') Reset and write the programmable part of slave address by software and hardware. On receiving this two-byte sequence, all devices (designed to respond to the general call address) will reset and take in the programmable part of their address.

Precautions must be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

00000010 (H'02') Write slave address by software only. All devices which obtain the programmable part of their address by software (and which have been designed to respond to the general call address) will enter a mode in which they can be programmed. The device will not reset.

I^{2}C Bus Specification

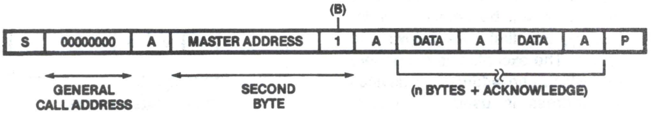
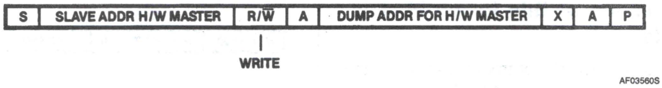
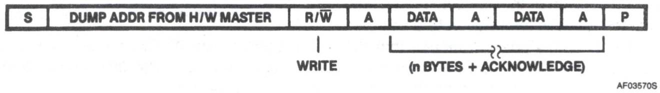


Figure 13. Data Transfer From Hardware Master Transmitter



a. Configuring master sends dump address to hardware master



b. Hardware master dumps data to selected slave device

Figure 14. Data Transfer of Hardware Master Transmitter Capable of Dumping Data Directly to Slave Devices

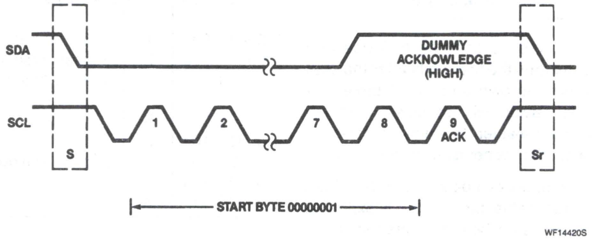


Figure 15. Start Byte Procedure

An example of a data transfer of a programming master is shown in Figure 12 (ABCD represents the fixed part of the address).

00000100 (H'04') Write slave address by hardware only. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two-byte sequence. The device will not reset.

00000000 (H'00') This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore these codes.

When B is a one, the two-byte sequence is a hardware general call. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master does not know in advance to which device the message must be transferred, it can only generate this hardware general call and its own address, thereby identifying itself to the system (Figure 13).

The seven bits remaining in the second byte contain the device address of the hardware master. This address is recognized by an intelligent device, such as a microcomputer, connected to the bus which will then direct the information coming from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems an alternative could be that the hardware master transmitter is brought in the slave receiver mode after the system reset. In this way, a system configuring master can tell the hardware master transmitter (which is now in slave receiver mode) to which address data must be sent (Figure 14). After this programming procedure, the hardware master remains in the master transmitter mode.

Start Byte
Microcomputers can be connected to the I^{2}C bus in two ways. If an on-chip hardware I^{2}C bus interface is present, the microcomputer can be programmed to be interrupted only by requests from the bus. When the device possesses no such interface, it must constantly monitor the bus via software. Obviously, the more times the microcomputer monitors, or polls, the bus, the less time it can spend carrying out its intended function.

Therefore, there is a difference in speed between fast hardware devices and the relatively slow microcomputer which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Figure 15). The start procedure consists of:

a) A start condition, (S)
b) A start byte 00000001
c) An acknowledge clock pulse
d) A repeated start condition, (Sr)

After the start condition (S) has been transmitted by a master requiring bus access, the start byte (00000001) is transmitted. Another microcomputer can therefore sample the SDA line on a low sampling rate until one of the seven zeros in the start byte is detected. After detection of this Low level on the SDA line, the microcomputer is then able to switch to a higher sampling rate in order to find the second start condition (Sr) which is then used for synchronization.

A hardware receiver will reset at the reception of the second start condition (Sr) and will therefore ignore the start byte.

After the start byte, an acknowledge-related clock pulse is generated. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the start byte.

I^2C Bus Specification

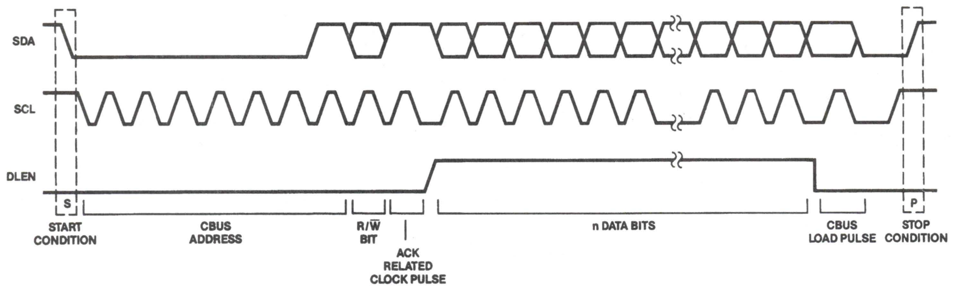


Figure 16. Data Format of Transmissions With CBUS Receiver/Transmitter

CBUS Compatibility

Existing CBUS receivers can be connected to the I^2C bus. In this case, a third line called DLEN has to be connected and the acknowledge bit omitted. Normally, I^2C transmissions are multiples of 8-bit bytes; however, CBUS devices have different formats.

In a mixed bus structure, I^2C devices are not allowed to respond on the CBUS message. For this reason, a special CBUS address (0000001X) has been reserved. No I^2C device will respond to this address. After the transmission of the CBUS address, the DLEN line can be made active and transmission, according to the CBUS format, can be performed (Figure 16).

After the stop condition, all devices are again ready to accept data.

Master transmitters are allowed to generate CBUS formats after having sent the CBUS address. Such a transmission is terminated by a stop condition, recognized by all devices. In the low speed mode, full 8-bit bytes must always be transmitted and the timing of the DLEN signal adapted.

If the CBUS configuration is known and no expansion with CBUS devices is foreseen, the user is allowed to adapt the hold time to the specific requirements of device(s) used.

ELECTRICAL SPECIFICATIONS OF INPUTS AND OUTPUTS OF I^2C DEVICES

The I^2C bus allows communication between devices made in different technologies which might also use different supply voltages.

For devices with fixed input levels, operating on a supply voltage of +5V ± 10%, the following levels have been defined:

V_{ILmax} = 1.5V (maximum input Low voltage)

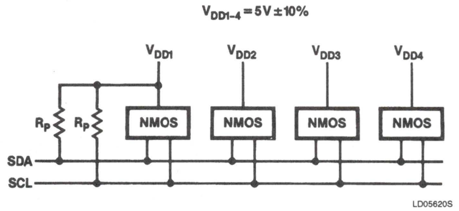


Figure 17. Fixed Input Level Devices Connected to the I^2C Bus

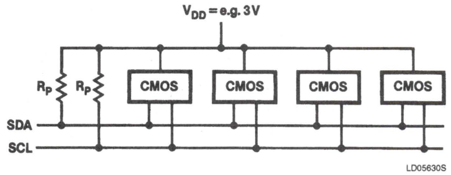


Figure 18. Devices With a Wide Range of Supply Voltages Connected to the I^2C Bus

V_{IHmin} = 3V (minimum input High voltage)

Devices operating on a fixed supply voltage different from +5V (e.g. I^2L), must also have these input levels of 1.5V and 3V for V_{IL} and V_{IH}, respectively.

For devices operating over a wide range of supply voltages (e.g. CMOS), the following levels have been defined:

V_{ILmax} = $0.3V_{DD}$ (maximum input Low voltage)

V_{IHmin} = $0.7V_{DD}$ (minimum input High voltage)

For both groups of devices, the maximum output Low value has been defined:

V_{OLmax} = 0.4V (max. output voltage Low) at 3mA sink current

The maximum low-level input current at V_{OLmax} of both the SDA pin and the SCL pin of an I^2C device is −10μA, including the leakage current of a possible output stage.

The maximum high-level input current at $0.9V_{DD}$ of both the SDA pin and SCL pin of an I^2C device is 10μA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA pin and the SCL pin of an I^2C device is 10pF.

Devices with fixed input levels can each have their own power supply of +5V ± 10%. Pull-up resistors can be connected to any supply (see Figure 17).

However, the devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (see Figure 18).

I^{2}C Bus Specification

When devices with fixed input levels are mixed with devices with V_{DD}-related levels, the latter devices have to be connected to one common supply line of +5V ± 10% along with the pull-up resistors (Figure 19).

Input levels are defined in such a way that:

1. The noise margin on the Low level is 0.1 V_{DD}.
2. The noise margin on the High level is 0.2 V_{DD}.
3. Series resistors (R_S) up to 300Ω can be used for flash-over protection against high voltage spikes on the SDA and SCL line (due to flash-over of a TV picture tube, for example) (Figure 20).

The maximum bus capacitance per wire is 400pF. This includes the capacitance of the wire itself and the capacitance of the pins connected to it.

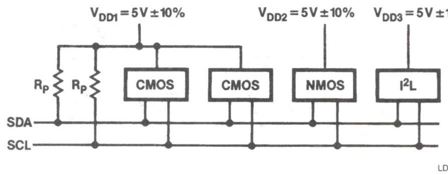


Figure 19. Devices With V_{DD} Related Levels Mixed With Fixed Input Level Devices on the I^{2}C Bus

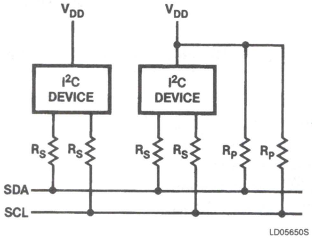


Figure 20. Serial Resistors (R_S) for Protection Against High Voltage

TIMING

The clock on the I^{2}C bus has a minimum Low period of 4.7μs and a minimum High period of 4μs. Masters in this mode can generate a bus clock with a frequency from 0 to 100kHz.

All devices connected to the bus must be able to follow transfers with frequencies up to 100kHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch the Low periods. In the latter case the frequency is reduced.

Figure 21 shows the timing requirements in detail. A description of the abbreviations used is shown in Table 2. All timing references are at V_{ILmax} and V_{ILmin}.

LOW-SPEED MODE

As explained previously, there is a difference in speed on the I^{2}C bus between fast hardware devices and the relatively slow microcomputer which relies on software polling. For this reason a low speed mode is available on the I^{2}C bus to allow these microcomputers to poll the bus less often.

Start and Stop Conditions

In the low-speed mode, data transfer is preceded by the start procedure.

Data Format and Timing

The bus clock in this mode has a Low period of 130μs ± 25μs and a High period of 390μs ± 25μs, resulting in a clock frequency of approx. 2kHz. The duty cycle of the clock has this Low-to-High ratio to allow for more efficient use of microcomputers without an on-chip hardware I^{2}C bus interface. In this mode also, data transfer with acknowledge is obligatory. The maximum number of bytes transferred is not limited (Figure 22).

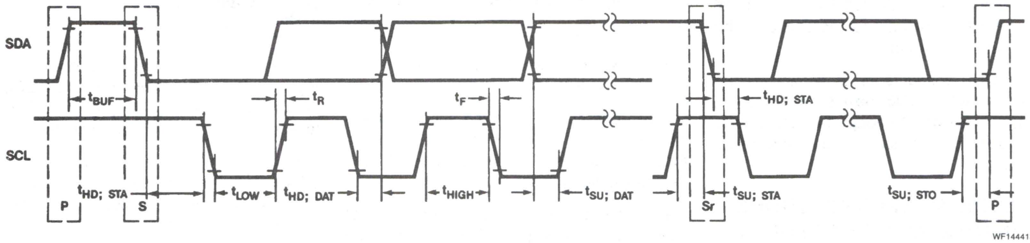


Figure 21. Timing Requirements for the I^{2}C Bus

Table 2. Timing Requirement for the I^2C Bus

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
f_{SCL}	SCL clock frequency	0	100	kHz
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		μs
$t_{HD;\ STA}$	Hold time start condition. After this period the first clock pulse is generated	4		μs
t_{LOW}	The Low period of the clock	4.7		μs
t_{HIGH}	The High period of the clock	4		μs
$t_{SU;\ STA}$	Setup time for start condition (Only relevant for a repeated start condition)	4.7		μs
$t_{HD;\ DAT}$	Hold time DATA for CBUS compatible masters for I^2C devices	 5 0*		 μs μs
$t_{SU;\ DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	μs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;\ STO}$	Setup time for stop condition	4.7		μs

NOTES:

All values referenced to V_{IH} and V_{IL} levels.

* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

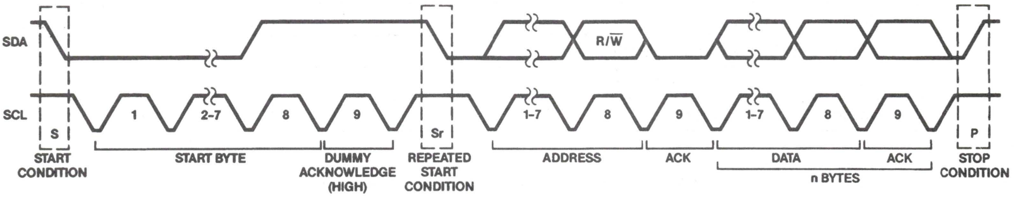

SDA
SCL
R/$\overline{W}$
1
2-7
8
9
S
Sr
1-7
8
9
1-7
8
9
P
START CONDITION
START BYTE
DUMMY ACKNOWLEDGE (HIGH)
REPEATED START CONDITION
ADDRESS
ACK
DATA
ACK
n BYTES
STOP CONDITION
WF14450S

Figure 22. Data Transfer Low-Speed Mode

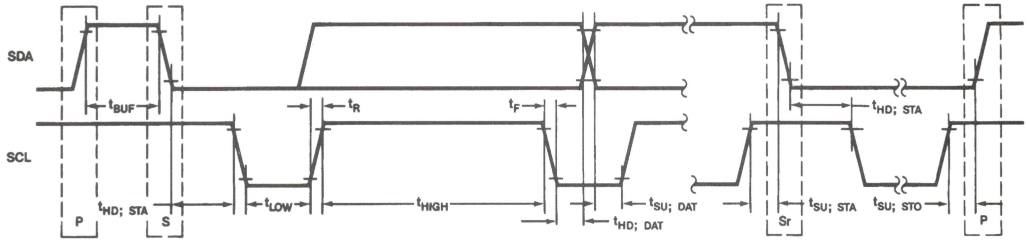

SDA
SCL
t_{BUF}
t_R
t_F
$t_{HD;\ STA}$
P
S
t_{LOW}
t_{HIGH}
$t_{SU;\ DAT}$
$t_{HD;\ DAT}$
Sr
$t_{HD;\ STA}$
$t_{SU;\ STA}$
$t_{SU;\ STO}$
P
WF14461S

Figure 23. Timing Low-Speed Mode

LOW SPEED MODE

CLOCK : $t_{LOW} = 130\mu s \pm 25\mu s$
DUTY CYCLE : $t_{HIGH} = 390\mu s \pm 25\mu s$
: 1:3 Low-to-High (Duty cycle of clock generator)
START BYTE : 0000 0001
MAX. NO. OF BYTES : UNRESTRICTED
PREMATURE TERMINATION OF TRANSFER : NOT ALLOWED
ACKNOWLEDGE CLOCK BIT : ALWAYS PROVIDED
ACKNOWLEDGEMENT OF SLAVES : OBLIGATORY

In this mode, a transfer cannot be terminated during the transmission of a byte.

The bus is considered busy after the first start condition. It is considered free again one minimum clock Low period, 105µs, after the detection of the stop condition. Figure 23 shows the timing requirements in detail, Table 3 explains the abbreviations.

Table 3. Timing Low Speed Mode

SYMBOL	PARAMETER	LIMITS Min	LIMITS Max	UNIT
t_{BUF}	Time the bus must be free before a new transmission can start	105		µs
$t_{HD;\,STA}$	Hold time start condition. After this period the first clock pulse is generated	365		µs
$t_{HD;\,STA}$	Hold time (repeated start condition only)	210		µs
t_{LOW}	The Low period of the clock	105	155	µs
t_{HIGH}	The High period of the clock	365	415	µs
$t_{SU;\,STA}$	Setup time for start condition (Only relevant for a repeated start condition)	105	155	µs
$t_{HD};\ t_{DAT}$	Hold time DATA for CBUS compatible masters for I^2C devices	 5 0*		 µs µs
$t_{SU;\,DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	µs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;\,STO}$	Setup time for stop condition	105	155	µs

NOTES:

All values referenced to V_{IH} and V_{IL} levels.

* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

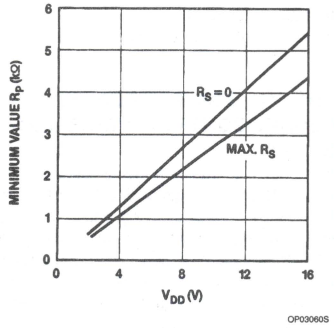
I^2C Bus Specification

APPENDIX A

Maximum and minimum values of the pull-up resistors R_P and series resistors R_S (See Figure 20).

In a I^2C bus system these values depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices (input current + leakage current)
  1) The supply voltage limits the minimum value of the R_P resistor due to the specified 3mA as minimum sink current of the output stages, at 0.4V as maximum low voltage. In Graph 1, V_{DD} against R_{Pmin} is shown.

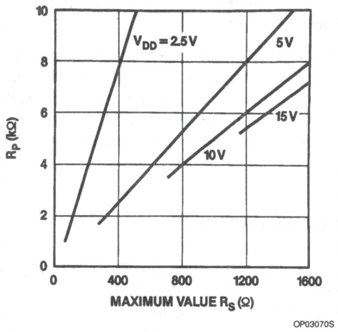


Graph 1

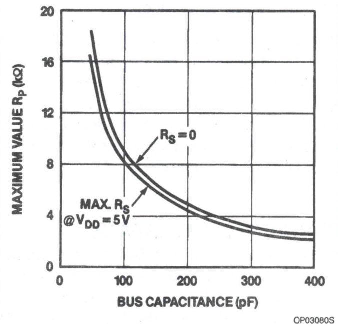
The desired noise margin of 0.1 V_{DD} for the low level limits the maximum value of R_S.

In Graph 2, R_{Smax} against R_P is shown.

2) The bus capacitance is the total capacitance of wire, connections, and pins. This capacitance limits the maximum value of R_P because of the specified rise time of 1µs.



Graph 2

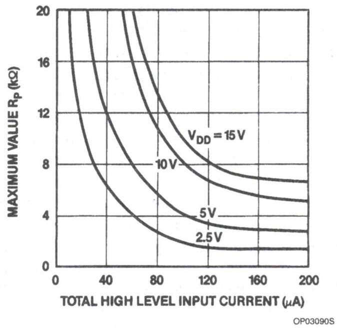


Graph 3

In Graph 3, the bus capacitance – R_{Pmax} relationship is shown.

3) The maximum high-level input current of each input/output connection has a specified value of 10µA max. Due to the desired noise margin of 0.2 V_{DD} for the high level, this input current limits the maximum value of R_P. This limit is dependent on V_{DD}.

In Graph 4 the total high-level input current – R_{Pmax} relationship is shown.



Graph 4

I^2C LICENSE

Purchase of Signetics or Philips I^2C components conveys a license under the Philips I^2C patent rights to use these components in an I^2C system, provided that the system conforms to the I^2C standard specification as defined by Philips.

Signetics

Linear Products

AN168

The Inter-Integrated Circuit (I^{2}C) Serial Bus: Theory and Practical Consideration

Application Note

Author: Carl Fenger

INTRODUCTION

The I^{2}C (Inter-IC) bus is becoming a popular concept which implements an innovative serial bus protocol that needs to be understood. On the hardware level I^{2}C is a collection of microcomputers (MAB8400, PCD3343, 83C351, 84CXX) and peripherals (LCD/LED drivers, RAM, ROM, clock/timer, A/D, D/A, IR transcoder, I/O, DTMF generator, and various tuning circuits) that communicate serially over a two-wire bus, serial data (SDA) and serial clock (SCL). The I^{2}C structure is optimized for hardware simplicity. Parallel address and data buses inherent in conventional systems are replaced by a serial protocol that transmits both address and bidirectional data over a 2-line bus. This means that interconnecting wires are reduced to a minimum; only V_{CC}, ground and the two-wire bus are required to link the controller(s) with the peripherals or other controllers. This results in reduced chip size, pin count, and interconnections. An I^{2}C system is therefore smaller, simpler, and cheaper to implement than its parallel counterpart.

The data rate of the I^{2}C bus makes it suited for systems that do not require high speed. An I^{2}C controller is well suited for use in systems such as television controllers, telephone sets, appliances, displays or applications involving human interface. Typically an I^{2}C system might be used in a control function where digitally-controllable elements are adjusted and monitored via a central processor.

The I^{2}C bus is an innovative hardware interface which provides the software designer the flexibility to create a truly multi-master environment. Built into the serial interface of the controllers are status registers which monitor all possible bus conditions: bus free/busy, bus contention, slave acknowledgement, and bus interference. Thus an I^{2}C system might include several controllers on the same bus each with the ability to asynchronously communicate with peripherals or each other. This provision also provides expandability for future add-on controllers. (The I^{2}C system is also ideal for use in environments where the bus is subject to noise. Distorted transmissions are immediately detected by the hardware and the information presented to the software.) A slave acknowledgement on every byte also facilitates data integrity.

An I^{2}C system can be as simple or sophisticated as the operating environment demands. Whether in a single master or multi-master system, noisy or 'safe', correct system operation can be insured under software control.

CONTROLLERS

Currently the family of I^{2}C controllers include the MAB8400, and the PCD 3343 (the PCD3343 is basically a CMOS version of the MAB8400). The MAB8400 is based on the 8048 architecture with the I^{2}C interface built-in. The instruction set for the MAB8400 is similar to the 8048, with a few instructions added and a few deleted. Tables 1 and 2 summarize the differences.

Programs for the MAB8400 and PCD 3343 may be assembled on an 8048-assembler using the macros listed in Appendix A. The serial I/O instructions involve moving data to and from the S0, S1, and S2 serial I/O control registers. The block diagram of the I^{2}C interface is shown in Figure 1.

SERIAL I/O INTERFACE

A block diagram of the Serial Input/Output (SIO) is shown in Figure 1. The clock line of the serial bus (SCL) has exclusive use of Pin 3, while the Serial Data (SDA) line shares Pin 2 with parallel I/O signal P23 of port 2. Consequently, only three I/O lines are available for port 2 when the I^{2}C interface is enabled.

Communication between the microcomputer and interface takes place via the internal bus of the microcomputer and the Serial Interrupt Request line. Four registers are used to store data and information controlling the operation of the interface:

- data shift register S0
- address register S0′
- status register S1
- clock control register S2.

THE I^{2}C BUS INTERFACE: SERIAL CONTROL REGISTERS S0, S1

All serial I^{2}C transfers occur between the accumulator and register S0. The I^{2}C hardware takes care of clocking out/in the data, and receiving/generating an acknowledge. In addition, the state of the I^{2}C bus is controlled and monitored via the bus control register S1. A definition of the registers is as follows:

Data Shift Register S0 — S0 is the data shift register used to perform the conversion between serial and parallel data format. All transmissions or receptions take place through register S0 MSB first. All I^{2}C bus receptions or transmissions involve moving data to/from the accumulator from/to S0.

Table 1. MAB8400 Family Instructions not in the MAB8048 Instruction Set

SERIAL I/O	REGISTER	CONTROL	CONDITIONAL BRANCH

MOV A,Sn
MOV Sn,A
MOV Sn,#data
EN SI
DIS SI
	DEC @Rr
	DJNZ @Rr,addr
		SEL MB2
		SEL MB3
			JNTF addr

Table 2. MAB8048 Instructions not in the MAB8400 Family Instruction Set

DATA MOVES	FLAGS	BRANCH	CONTROL

MOVX A,@R
MOVX @R,A
MOVP3 A,@A
MOVD A,P
MPVD P,A
ANLD P,A
ORLD P,A
	CLR F0
	CPL F0
	CLR F1
	CPL F1
		*JNI addr
		JF0 addr
		JF1 addr
		
		*replaced by
		JT0, JNT0
			ENTOCLK

The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

AN168

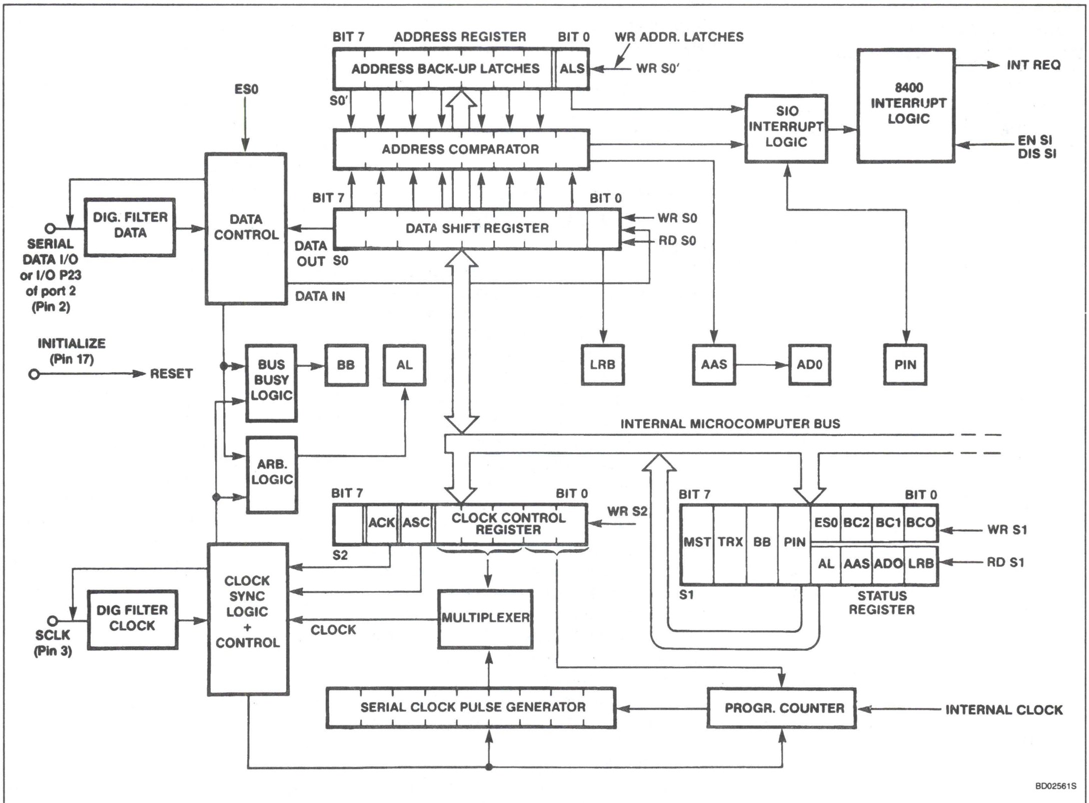

BIT 7
ADDRESS REGISTER
BIT 0
WR ADDR. LATCHES
ADDRESS BACK-UP LATCHES
ALS
WR S0′
INT REQ
8400 INTERRUPT LOGIC
ES0
S0′
SIO INTERRUPT LOGIC
ADDRESS COMPARATOR
EN SI
DIS SI
BIT 7
BIT 0
DIG. FILTER DATA
DATA CONTROL
DATA SHIFT REGISTER
WR S0
RD S0
SERIAL DATA I/O or I/O P23 of port 2 (Pin 2)
DATA OUT S0
DATA IN
INITIALIZE (Pin 17)
RESET
BUS BUSY LOGIC
BB
AL
LRB
AAS
AD0
PIN
INTERNAL MICROCOMPUTER BUS
ARB. LOGIC
BIT 7
BIT 0
ACK
ASC
CLOCK CONTROL REGISTER
WR S2
BIT 7
BIT 0
MST
TRX
BB
PIN
ES0
BC2
BC1
BC0
AL
AAS
AD0
LRB
WR S1
RD S1
S2
S1
STATUS REGISTER
DIG FILTER CLOCK
CLOCK SYNC LOGIC + CONTROL
SCLK (Pin 3)
CLOCK
MULTIPLEXER
SERIAL CLOCK PULSE GENERATOR
PROGR. COUNTER
INTERNAL CLOCK
BD02561S

Figure 1. Block Diagram of the MAB8400 SIO Interface

Address Register S0′ — In multi-master systems, this register is loaded with a controller's slave address. When activated, (ALS = 0), the hardware will recognize when it is being addressed by setting the AAS (Addressed As Slave) flag. This provision allows a master to be treated as a slave by other masters on the bus.

Status Register S1 — S1 is the bus status register. To control the SIO interface, information is written to the register. The lower 4 bits in S1 serve dual purposes; when written to, the control bits ES0, BC2, BC1, BC0 are programmed (Enable Serial Output and a 3-bit counter which indicates the current number of bits left in a serial transfer). When reading the lower four bits, we obtain the status information AL, AAS, AD0, LRB (Arbitration Lost, Addressed As Slave, Address Zero (the general call has been received), the Last Received Bit (usually the acknowledge bit)). The upper 4 bits are the MST, TRX, BB, and PIN control bits (Master, Transmitter, Bus Busy, and Pending Interrupt Not). These bits define what role the controller has at any particular time. The values of the master and transmitter bits define the controller as either a master or slave (a master initiates a transfer and generates the serial clock; a slave does not), and as a transmitter or receiver. Bus Busy keeps track of whether the bus is free or not, and is set and reset by the 'Start' and 'Stop' conditions which will be defined. Pending Interrupt Not is reset after the completion of a byte transfer + acknowledge, and can be polled to indicate when a serial transfer has been completed. An alternative to polling the PIN bit is to enable the serial interrupt; upon completion of a byte transfer, an interrupt will vector program control to location 07H.

SERIAL CLOCK/ACKNOWLEDGE CONTROL REGISTER S2

Register S2 contains the clock-control register and acknowledge mode bit. Bits S20 – S24 program the bus clock speed. Bit S26 programs the acknowledge or not-acknowledge mode (1/0). The various I^2C bus clock speed possibilities are shown in Table 3.

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Table 3. Clock Pulse Frequency Control When Using a 4.43MHz Crystal

HEX S20 – S24 CODE	DIVISOR	APPROX. f_{CLOCK} (kHz)
0	Not Allowed	
1	39	114
2	45	98
3	51	87
4	63	70
5	75	59
6	87	51
7	99	45
8	123	36
9	147	30
A	171	26
B	195	23
C	243	18
D	291	15
E	339	13
F	387	11
10	483	9.2
11	579	7.7
12	675	6.6
13	771	5.8
14	963	4.6
15	1155	3.8
16	1347	3.3
17	1539	2.9
18*	1923	2.3
19*	2307	1.9
1A*	2691	1.7
1B*	3075	1.4
1C	3843	1.2
1D	4611	1.0
1E	5379	0.8
1F	6147	0.7

*only values that may be used in the low speed mode (ASC = 1).

These speeds represent the frequency of the serial clock bursts and do not reflect the speed of the processor's main clock (i.e. it controls the bus speed and has no effect on the CPU's execution speed).

BUS ARBITRATION

Due to the wire-AND configuration of the I^2C bus, and the self-synchronizing clock circuitry of I^2C masters, controllers with varying clock speeds can access the bus without clock contention. During arbitration, the resultant clock on the bus will have a low period equal to the longest of the low periods; the high period will equal the shortest of the high periods. Similarly, when two masters attempt to drive the data line simultaneously, the data is 'ANDed', the master generating a low while the other is driving a high will win arbitration. The resultant bus level will be low, and the loser will withdraw from the bus and set its 'Arbitration Lost' flag (S1 bit 3).

The losing Master is now configured as a slave which could be addressed during this very same cycle. These provisions allow for a number of microcomputers to exist on the same bus. With properly written subroutines, software for any one of the controllers may regard other masters as transparent.

I^2C PROTOCOL AND ASSEMBLY LANGUAGE EXAMPLES

I^2C data transfers follow a well-defined protocol. A transfer always takes place between a master and a slave. Currently a microcomputer can be master or slave, while the 'CLIPS' peripherals are always slaves. In a 'bus-free' condition, both SCL and SDA lines are kept logical high by external pull-up resistors. All bus transfers are bounded by a 'Start' and a 'Stop' condition. A 'Start' condition is defined as the SDA line making a high-to-low transition **while the SCL line is high**. At this point, the internal hardware on all slaves are activated and are prepared to clock-in the next 8 bits and interpret it as a 7-bit address and a $R/\overline{W}$ control bit (MSB first). All slaves have an internal address (most have 2 – 3 programmable address bits) which is then compared with the received address. The slave that recognized its address will respond by pulling the data line low during a ninth clock generated by the master (all I^2C byte transfers require the master to generate 8 clock pulses plus a ninth acknowledge-related clock pulse). The slave-acknowledge will be registered by the master as a '0' appearing in the LRB (Last Received Bit) position of the S1 serial I/O status register. If this bit is high after a transfer attempt, this indicates that a slave did not acknowledge, and that the transfer should be repeated.

After the desired slave has acknowledged its address, it is ready to either send or receive data in response to the master's driving clock. All other slaves have withdrawn from the bus. In addition, for multi-master systems, the start condition has set the 'Bus Busy' bit of the serial I/O register S1 on all masters on the bus. This gives a software indication to other masters that the bus is in use and to wait until the bus is free before attempting an access.

There are two types of I^2C peripherals that now must be defined: there are those with only a chip address such as the I/O expander, PCF8574, and those with a chip address plus an internal address such as the static RAM, PCF8570. Thus after sending a start condition, address, and $R/\overline{W}$ bit, we must take into account what type of slave is being addressed. In the case of a slave with only a chip address, we have already indicated its address and data direction ($R/\overline{W}$) and are therefore ready to send or receive data. This is performed by the master generating bursts of 9 clock pulses for each byte that is sent or received. The transaction for writing one byte to a slave with a chip address only is shown in Figure 3.

In this transfer, all bus activity is invoked by writing the appropriate control byte to the serial I/O control register S1, and by moving data to/from the serial bus buffer register S0. Coming from a known state (MOV S1,#18H-Slave, Receiver, Bus not Busy) we first load the serial I/O buffer S0 with the desired

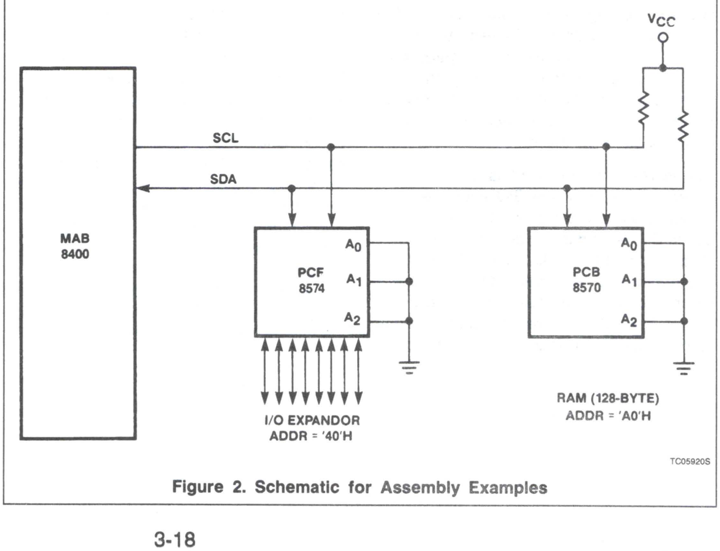
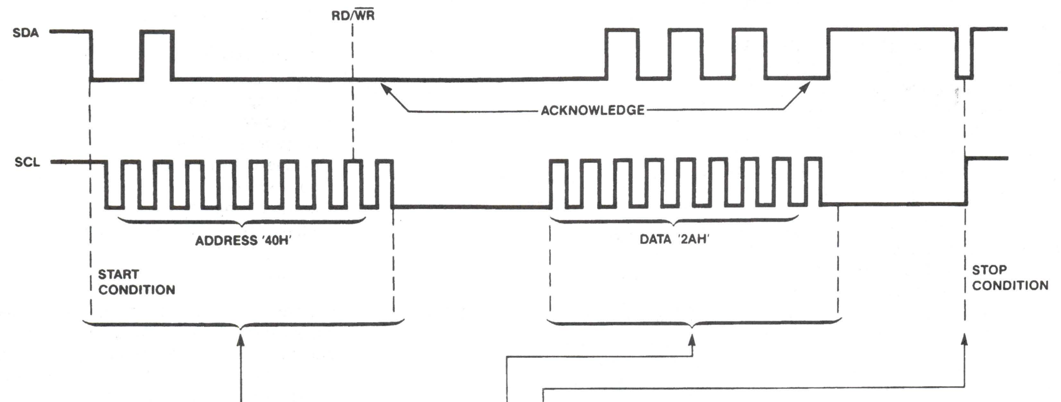


Figure 2. Schematic for Assembly Examples



```
MOV S1,#18H          ;Initialize S1-Slave, Receiver, Bus not
                     ;Busy, Enable Serial I/O.
MOV S0,#40H          ;Preload S0 with Slave's address &
                     ;R/W bit.
MOV S1,#0F8H         ;Invoke start condition & slave address
                     ;(Master, Transmitter, Bus Busy, Enable
                     ;Serial I/O, Bit Counter = 000).
CALL ACKWT:          ;Check for transmission complete, ack.
                     ;received, no arbitration, etc.
MOV A,#2AH           ;Get a data byte.
MOV S0,A             ;Transmit data byte.
CALL ACKWT:          ;Wait for transmission complete again.
MOV S1,#0D8H         ;Generate Stop condition
                     ;(Master, Transmitter, Bus not Busy).
```

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Figure 3

slave's address (MOV S0,#40H). To transmit this preceded by a start condition, we must first examine the control register S1, which, after initialization, looks like this:

MASTER	TRANS	BUS BUSY	PIN	ES0	BC2	BC1	BC0
0	0	0	1	1	0	0	0

To transmit to a slave, the Master, Transmitter, Bus Busy, PIN (Pending Interrupt Not), and ESO (Enable Serial Output) must be set to a 1. This results in an 'F8H' being written to S1. This word defines the controller as a Master Transmitter, invokes the transfer by setting the 'Bus Busy' bit, clears the Pending Interrupt Not (an inverted flag indicating the completion of a complete byte transfer), and activates the serial output logic by setting the Enable Serial Output (ESO) bit.

BIT COUNTER S12, S11, S10

BC2, BC1, and BC0 comprise a bit-counter which indicates to the logic how long the word is to be clocked out over the serial data line. By setting this to a 000H, we are telling it to produce 9 clocks (8 bits plus an acknowledge clock) for this transfer. The bit counter will then count off each bit as it is transmitted. The bit counter possibilities are shown in Table 4.

Thus the bit counter keeps track of the number of clock pulses remaining in a serial transfer. Additionally, there is a not-acknowledge mode (controlled through bit 6 of clock control register S2) which inhibits the acknowledge clock pulse, allowing the possibility of straight serial transfer. We may thus define the word size for a serial transfer (by preloading BC2, BC1, BC0 with the appropriate control number), with or without an acknowledge-related clock pulse being generated. This makes the controller able to transmit serial data to most any serial device regardless of its protocol (e.g., C-bus devices).

CHECKING FOR SLAVE ACKNOWLEDGE

After a 'Start' condition and address have been issued, the selected slave will have recognized and acknowledged its address by

Table 4. Binary Numbers in Bit-Count Locations BC2, BC1 and BC0

BC2	BC1	BC0	BITS/BYTE WITHOUT ACK	BITS/BYTE WITH ACK
0	0	1	1	2
0	1	0	2	3
0	1	1	3	4
1	0	0	4	5
1	0	1	5	6
1	1	0	6	7
1	1	1	7	8
0	0	0	8	9

pulling the data line low during the ninth clock pulse. During this period, the software (which runs on the processor's 4MHz clock) will have been either waiting for the transfer to be completed by polling the PIN bit in S1 which goes low on completion of a transfer/reception (whose length is defined by the preloaded Bit-counter value), or by the hardware in Serial Interrupt mode. The serial interrupt (vectored to 07H) is enabled via the EN SI (enable serial interrupt) instruction.

At the point when PIN goes low (or the serial interrupt is received) the 9-bit transfer has been completed. The acknowledgement bit will now be in the LRB position of register S1, and may be checked in the routine 'ACKWT' (Wait for Acknowledge) as shown in Figure 4.

This routing must go one step further in multimaster systems; the possibility of an Arbitration Lost situation may occur if other masters are present on the bus. This condition may be detected by checking the 'AL' bit (bit 3). If arbitration has been lost, provisions for reattempting the transmission should be taken. If arbitration is lost, there is the possibility that the controller is being addressed as a Slave. If this condition is to be recognized, we must test on the 'AAS' bit (bit 2). A 'General Call' address (00H) has also been defined as an 'all-call' address for all slaves; bit 1, AD0, must be tested if this feature is to be recognized by a Master.

After a successful address transfer/acknowledge, the slave is ready to be sent its data. The instruction MOV SO,A will now automatically send the contents of the accumulator out on the bus. After calling the ACKWT routine once more, we are ready to terminate the transfer. The Stop condition is created by the instruction 'MOV S1, #0D8H'. This resets the bus-busy bit, which tells the hardware to generate a Stop — the data line makes a low-to-high transition while the clock remains high. All bus-busy flags on other masters on the bus are reset by this signal.

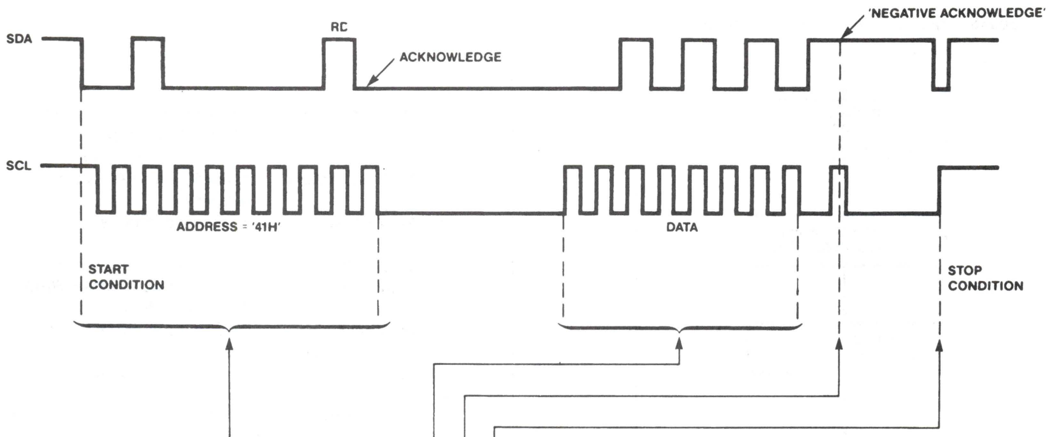
The transfer is now complete — PCF8574 I/O Expandor will transfer the serial data stream to its 8 output pins and latch them until further update.

```
ACKWT:    MOV A,S1          ;Get bus status word
                            ;from S1.
          JB4 ACKWT         ;Poll the PIN bit
                            ;until it goes low
                            ;indicating transfer
                            ;completed
          JBO BUSERR        ;Jump to BUSERR
                            ;routine if acknowledge
                            ;not received.
          RET               ;transfer complete,
                            ;acknowledge received - return.
```

Figure 4

MASTER READS ONE BYTE FROM SLAVE

A read operation is a similar process; the address, however, will be 41H, the LSB indicating to the I/O device that a read is to be performed. During the data portion of a read, the I/O port 8574 will transmit the contents of its latches in response to the clock generated by the master. The Master/Receiver in this case generates a low-level acknowledge on reception of each byte (a 'positive' acknowledge). Upon completion of a read, the master must generate a 'negative' acknowledge during the ninth clock to indicate to the slaves that the read operation is finished. This is necessary because an arbitrary number of bytes may be read within the same transfer. A negative acknowledge consists of a high signal on the data line during the ninth clock of the last byte to be read. To accomplish this, the master 8400 must leave the acknowledge mode just before the final byte, read the final byte (producing only 8 clock pulses), program the bit-counter with 001 (preparing for a one-bit negative acknowledge pulse), and simply move the contents of S0 to the accumulator. This final instruction accomplishes two things simultaneously: it transfers the final byte to the accumulator and produces one clock pulse on the SCL line. The structure of the serial I/O register S0 is such that a read from it causes a double-buffered transfer from the I^2C bus to S0, while the original contents of S0 are transferred to the accumulator. Because the number of clocks produced on the bus is determined by the control number in the Bit Counter, by presetting it to 001, only one clock is generated. At this point in time the slave is still waiting for an acknowledge; the bus is high due to the pull-up, as single clock pulse in this condition is interpreted as a 'negative' acknowledge. The slave has now been informed that reading is completed; a Stop condition is now generated as before. The read process (one byte from a slave with only a chip address) is shown in Figure 5.


SDA
RC
ACKNOWLEDGE
'NEGATIVE ACKNOWLEDGE'
SCL
ADDRESS = '41H'
DATA
START CONDITION
STOP CONDITION

```
           MOV S1,#18H      ;Initialize serial I/O control
                            ;register.
           MOV S0,#41H      ;Preload serial register S0
                            ;with slave address and RD
                            ;control bit.
           MOV S1,#0F8H     ;Send address to bus along with
                            ;start condition.
           CALL ACKWT       :Wait for acknowledge (as
                            ;before).
           MOV S2,#01H      ;Leave acknowledge mode.
           MOV S0,A         ;Read data from slave to S0.
WAIT:      MOV A,S1         ;Test for byte received by
                            ;testing S1 PIN bit.
           JB4 Wait         ;Wait until PIN received.
           MOV S1,#0A9H     ;Set Bit Counter to 1 and
                            ;become a receiver (A9 =
                            ;Mst,Rec,Bus Busy,Bit Coutner =
                            ;001).
           MOV A,S0         ;Move data to accumulator and
                            ;clock out a negative
           MOV S1,#0D8H     ;acknowledge.
                            ;Generate Stop Condition.
```

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Figure 5

The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

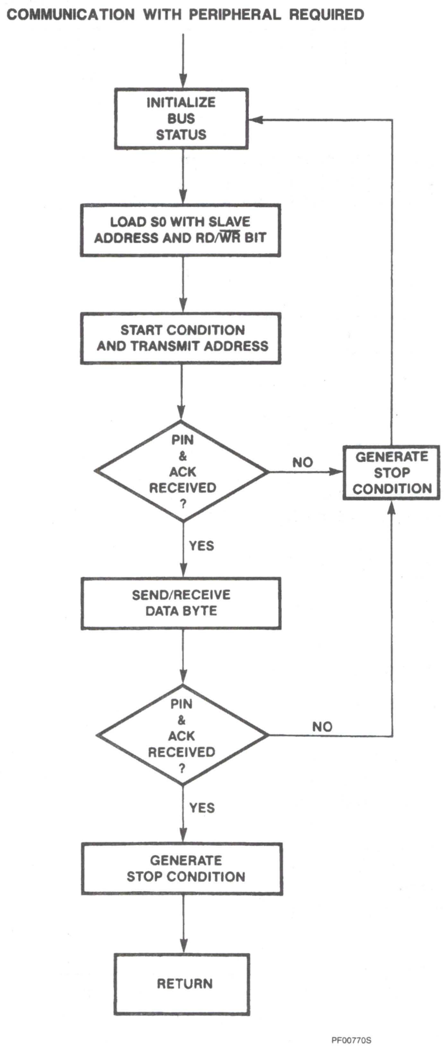

Figure 6. Flowchart for Reading/Writing One Byte to an I^2C Peripheral; Single-Master, Single-Address Slave

```
        MOV S1, #18H      ;Initialize bus-status register
                          ;Master, Transmitter,
                          ;Bus-not-Busy, Enable SIO.
        MOV S0, #0A0H     ;Load S0 with RAM's chip
                          ;address.
        MOV S1, #0F8H     ;Start cond. and transmit
                          ;address.
        CALL ACKWT        ;Wait until address received.
        MOV A,#00H        ;Set up for transmitting RAM
                          ;location address.
        MOV S0,A          ;Transmit first RAM address.
        CALL ACKWT        ;Wait.
        MOV S1, #18H      ;Set up for a repeated Start
                          ;condition.
        MOV A,#0A1H       ;Get RAM chip address & RD bit.
        MOV S0,A          ;Send out to bus
        MOV S1,#0F8H      ;preceded by repeated Start.

        CALL ACKWT        ;Wait.
        MOV A,S0          ;First data byte to S0.
        CALL ACKWT        ;Wait.
        MOV A,S0          ;Second data byte to S0.
                          ;And First data byte to Acc.
        CALL ACKWT        ;Wait.
        MOV R0,A          ;Save first byte in R0.
        MOV A,S0          ;Third data byte to S0
                          ;and second data byte to Acc.
        CALL ACKWT        ;Wait.
        MOV R1,A          ;Save second data byte
                          ;in R1.
        MOV S2,#01H       ;Leave ack. mode.
                          ;Bit Counter=001 for neg ack.
        MOV A,S0          ;Third data byte to acc
                          ;negative ack. generated.
        MOV R2,A          ;Save third data byte in R2.
WAIT1:  MOV A,S1          ;Get bus status.
        JB4 WAIT1         ;Wait until transfer complete.
        MOV S1,#0D8H      ;Stop condition.
        MOV S2,#41H       ;Restore acknowledge mode.
```

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Figure 7

These examples apply to a slave with a chip address — more than one byte can be written/read within the same transfer; however, this option is more applicable to I^2C devices with sub-addresses such as the static RAMs or Clock/Calendar. In the case of these types of devices, a slightly different protocol is used. The RAM, for example, requires a chip address and an internal memory location before it can deliver or accept a byte of information. During a write operation, this is done by simply writing the secondary address right after the chip address — the peripheral is designed to interpret the second byte as an internal address. In the case of a Read operation, the slave peripheral must send data back to the Master after it has been addressed and sub-addressed. To accomplish this, first the Start, Address, and Sub-address is transmitted. Then we have a **repeated** start condition to reverse the direction of the data transfer, followed by the chip address and RD, then a data string (w/ acknowledges). This repeated Start does not affect other peripherals — they have been deactivated and will not reactivate until a Stop condition is detected. I^2C peripherals are equipped with auto-incrementing logic which will automatically transmit or receive data in consecutive (increasing) locations. For example, to read 3 consecutive bytes to PCB8571 RAM locations 00, 01 and 02, we use the following format as shown in Figure 7.

This routine reads the contents of location 00, 01 and 02 of the PCB8571 128-byte RAM and puts them in registers R0, R1, and R2. The auto-incrementing feature allows the programmer to indicate only a starting location, then read an arbitrary block of consecutive memory addresses. The WAIT 1 loop is required to poll for the completion of the final byte because the ACKWT routine will not recognize the negative acknowledge as a valid condition.

BUS ERROR CONDITIONS: ACKNOWLEDGE NOT RECEIVED

In the above routines, should a slave fail to acknowledge, the condition is detected during the 'ACKWT' routine. The occurrence may indicate one of two conditions: the slave has failed to operate, or a bus disturbance has occurred. The software response to either event is dependent on the system application. In either case, the 'BusErr' routine should reinitialize the bus by issuing a 'Stop' condition. Provision may then be taken to repeat the transfer an arbitrary number of times. Should the symptom persist, either an error condition will be entered, or a backup device can be activated.

These sample routines represent single-master systems. A more detailed analysis of multi-master/noisy environment systems will be treated in further application notes. Examples of more complex systems can be found in the 'Software Examples' manual; publication 9398 615 70011.

APPENDIX A

Only the 8048 assembler is capable of assembling MAB8400 source code when it has at least a "DATA" or "Define Byte" assembler directive, possibly in combination with a MACRO facility.

The new instructions can be simply defined by MACROs. The instructions which are not in the MAB8400 should not be in the MAB8400 source program.

An example of a macro definitions list is given here for the Intel Macro Assembler.

This list can be copied in front of a MAB8400 source program; the new instructions are added to the MAB8400 source program by calling the MACRO via its name in the op-code field and (if required) followed by an operand in the operand field.

MACRO DEFINITIONS

LINE SOURCE STATEMENT

```
$MACROFILE
;MACROS FOR 8048 ASSEMBLER RECOGNITION
;OF 8400 COMMANDS
                              MOVS0A     MACRO      ;MOV S0,A
                              DB 3CH
                              ENDM
                              MOVAS0     MACRO      ;MOV A,S0
                              DB 0CH
                              ENDM
                              MOVS1A     MACRO      ;MOV S1,A
                              DB 3DH
                              ENDM
                              MOVAS1     MACRO      ;MOV A,S1
                              DB 0DH
                              ENDM
                              MOVS2A     MACRO      ;MOV S2,A
                              DB 3EH
                              ENDM
                              MOVS0      MACRO L    ;MOV S0,#DATA
                              DB 9CH,L
                              ENDM
                              MOVS1      MACRO L    ;MOV S1,#DATA
                              DB 9DH,L
                              ENDM
                              MOVS2      MACRO L    ;MOV S2,#DATA
                              DB 9EH,L
                              ENDM
                              ENSI       MACRO      ;EN SI
                              DB 85H
                              ENDM
                              DISSI      MACRO      ;DIS SI (Disable serial
                                                     interrupt)
                              DB         95H
                              ENDM
;
; PORT 0 INSTRUCTIONS:
;                             INAP0      MACRO      ;IN A,P0
                              DB         08H
                              ENDM
;
                              OUTP0A     MACRO      ;OUTL P0,A
                              DB         38H
                              ENDM
;
                              ORLP0      MACRO L    ;ORL P0,#DATA
                              DB         88H,L
                              ENDM
;
                              ANLP0      MACRO L    ;ANL P0,#DATA
                              DB         98H,L
                              ENDM
;
```

MACRO DEFINITIONS (Continued)

LINE	SOURCE STATEMENT		
52; DATA MEMORY INSTRUCTIONS:			
53	DECARO	MACRO	;DEC @R0
54	DB	0COH	
55	ENDM		
56;			
57	DECAR1	MACRO	;DEC @R1
58	DB	OC1H	
59	ENDM		
60;			
61; SELECT MEMORY BANK INSTRUCTIONS:			
62	SELMB2	MACRO	;SEL MB2
63	DB	0A5H	
64	ENDM		
65;			
66	SELMB3	MACRO	;SEL MB3
67	DB	0B5H	
68	ENDM		
69;			
70; CONDITIONAL JUMP INSTRUCTIONS:			
71	DJNZA0	MACRO L	;DJNZ @R0,ADDR
72	DB	0E0H,L AND 0FFH	
73	ENDM		
74;			
75	DJNZA1	MACRO L	;DJNZ @R1,ADDR
76	DB	0E1H,L AND 0FFH	
77	ENDM		
78;			
79	JNTF	MACRO L	;JUMP IF TIMERFLAG IS NON ZERO
80	DB	06H,L AND 0FFH	
81	ENDM		
82			
83; END OF MACRO DEFINITIONS			

THE 8400 INSTRUCTIONS BUILT FROM THE MACRO LIST

```
LOC/OBJ    LINE              SOURCE STATEMENT
 0000       1                    ORG 0
            2                    MOVAS0                        ;MACRO for MOV A,S0
 0000 0C    3 +                  DB          0CH
            4                    MOVAS1                        ;MACRO for MOV A,S1
 0001 0D    5 +                  DB          0DH
            6                    MOVS0A                        ;MACRO for MOV S0,A
 0002 3C    7 +                  DB          3CH
            8                    MOVS1A                        ;MACRO For MOV S1,A
 0003 3D    9 +                  DB          3DH
            10                   MOVS2A                        ;MACRO For MOV S2,A
 0004 3E    11 +                 DB          3EH
            12                   MOVS0       56H               ;MACRO For MOV S0,
                                                                #56H
 0005 9C    13 +                 DB          9CH,56H
 0006 56
            14                   MOVS1       9FH               ;MACRO for MOV S1,
                                                                #9FH
 0007 9D    15 +                 DB          9DH,9FH
 0008 9F
            16                   MOVS2       0E8H              ;MACRO for MOV S2,
                                                                #0E8H
 0009 9E    17 +                 DB          9EH,0E8H
 000A E8
            18                   ENS1                          ;MACRO for EN S1
 000B 85    19 +                 DB          85H
            20                   DISSI                         ;MACRO for DIS SI
 000C 95    21 +                 DB          95H
            22                   INAP0                         ;MACRO for IN A,P0
 000D 08    23 +                 DB          08H
            24                   OUTP0A                        ;MACRO for OUTL P0,A
 000E 38    25 +                 DB          38H
            26                   ORLP0       5AH               ;MACRO for ORL P0,A
 000F 88    27 +                 DB          88H,5AH
 0010 5A
            28                   ANLP0       2FH               ;MACRO for ANL P0,A
 0011 98    29 +                 DB          98H,2FH
 0012 2F
            30                   DECAR0                        ;MACRO for DEC @R0
 0013 C0    31 +                 DB          0C0H
            32                   DECAR1                        ;MACRO for DEC @R1
 0014 C1    33 +                 DB          0C1H
            34                   SELMB2                        ;MACRO for SEL MB2
 0015 A5    35 +                 DB          0A5H
            36                   SELMB3                        ;MACRO for SEL MB3
 0016 B5    37 +                 DB          0B5H
            38                   DJNZA0      567H              ;MACRO for DJNZ @R0,
                                                                567H
 0017 E0    39 +                 DB          0E0H,567H AND
                                             0FFH
 0019 67
            40                   DJNZA1      0EFEH             ;MACRO for DJNZ @R1,
                                                                0EFEH
 0019 E1    41 +                 DB          0E1H,0EFEH AND
                                             0FFH
 001A FE
            42                   JNTF        789H              ;MACRO for JNTF 789H
 001B 06    43 +                 DB          06H, 789H AND
                                             0FFH
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Signetics

Section 4
Amplifiers

Linear Products

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Amplifier Selector Guide

Linear Products

Amplifier Selector Guide

DEVICE	COM-PLEXITY	TEMP RANGE[1]	MAX. INPUT VOLTAGE[2]		MAX. INPUT CURRENT		$R_L = 2k\Omega$ MIN. A_{VOL} (V/mV)	TYP. BW $A_V = 1$ (MHz)	TYP. SLEW RATE (V/µs)	MAX. DIFF. INP. VOLT[3] (V)	MIN. CMRR RATIO (dB)	MIN. PSRR (dB)	SUPPLY VOLTAGE MAX. (V)	MAX. SUPPLY CURR. (mA)	MIN. OUTPUT VOLTAGE SWING (V) $R_L = 2k\Omega$	INTERNAL COMPEN-SATION	INPUT NOISE VOLTAGE (nV√Hz) $f_O = 1kHz$
			OFFSET (mV)	DRIFT (µV/°C TYP.)	OFFSET (nA)	BIAS (nA)											
NE530	Single	Comm.	6	6°	40	150	50	3	35	±30	70	76	±18	3	±10	Yes	
SE530	Single	Mil.	4	6°	20	80	50	3	35	±30	70	76	±22	3	±10	Yes	
NE531	Single	Comm.	6	10°	200	1500	20^{5}	1	35	±15	70	76	±21	10	$\pm 10^{5}$	No	
SE531	Single	Mil.	5	10°	20	500	50^{5}	1	35	±15	70	76	±22	7	$\pm 10^{5}$	No	
NE538	Single	Comm.	6	6°	40	150	50	6	60	±30	70	76	±18	3	±10	Yes[7]	
SE538	Single	Mil.	4	15	20	80	50	6	60	±30	70	76	±22	3	±10	Yes[7]	
µA741	Single	Mil.	5	10°	200	500	50	1	0.5	±30	70	76	±22	2.8	±10	Yes	
µ741C	Single	Comm.	6	12°	200	500	20	1	0.5	±30		76	±18	2.8	±10	Yes	
NE5534/A	Single	Comm.	4	5°	300	1500	25^{6}	10	13	±0.5	70	80	±22	8	$\pm 12^{6}$	Yes[8]	4.5
SE5534/A	Single	Mil.	2	5°	200	800	50^{6}	10	13	±0.5	80	86	±22	6.5	$\pm 12^{6}$	Yes[8]	4■
NE5539	Single	Comm.	5		2.000	20.000		1200^{4}	600		70	60	±12	33	2.3^{9}	Yes[10]	4■
NE5205	Single	Comm.					20^{11}	500^{12}	2000	5V			8	30		Yes	6^{13}
SE5539	Single	Mil.	3		1.000	13.000		1200^{4}	600		70	60	±12	31	2.5	Yes[10]	4■
NE5230	Single	Comm.	4		30 – 100	60 – 200	150	0.2 – 0.6	0.09 – 0.25	±9	80	75	±9	0.15 – 0.8	±0.7	Yes	23
LM158	Dual	Mil.	5	7°	30	150	50	1	0.3	32	70	65	32	2	26	Yes	50
LM258	Dual	Ind.	5	7°	30	150	50	1	0.3	32	70	65	32	2	26	Yes	50■
LM358	Dual	Comm.	7	7°	50	250	25	1	0.3	32	65	65	32	2	26	Yes	50■
NE532	Dual	Comm.	7	7°	50	250	25	1	0.3	32	65	65	32	2	26	Yes	50■
SA532	Dual	Auto	7	7.5°	50	250	25	1	0.3	32	65	65	32	2	26	Yes	50■
SE532	Dual	Mil.	5	7°	30	150	50	1	0.3	32	70	65	32	2	26	Yes	50■
µA747	Dual	Mil.	5	10°	200	500	50	1	0.5	±30	70	76	±22	2.8	±10	Yes	
µA747C	Dual	Comm.	6	12°	200	500	25	1	0.5	±30	70	76	±18	2.8	±10	Yes	
MC1458	Dual	Comm.	6	12°	200	500	25	1	0.8	±30	70	76	±18	5.6▲	±10	Yes	
SA1458	Dual	Auto	6	12°	200	500	20	1	0.8	±30	70	76	±18	5.6	±10	Yes	
MC1558	Dual	Mil.	5	10°	200	500	50	1	0.8	±30	70	76	±22	5▲	±10	Yes	30■
NE4558	Dual	Comm.	6	4°	200	500	20	3	1	±30	70	76	±18	5.6	±10	Yes	30■
SA4558	Dual	Auto	6	4°	200	500	50	3	1	±30	70	76	±18	5.6	±10	Yes	30■
SE4558	Dual	Mil.	5	4°	200	500	50	3	1	±30	70	76	±22	5.6	±10	Yes	30■
NE5512	Dual	Comm.	5	5°	20	20	50	3	1	32	70	80	±16	5	±13	Yes	30■
SE5512	Dual	Mil.	2	4°	10	10	50	3	1	±32	70	80	±16	5	±13	Yes	30■
NE5532/A	Dual	Comm.	4	5°	150	800	25	10	9	±0.5	70	80	±22	16	$\pm 12^{6}$	Yes	6
SE5532/A	Dual	Mil.	2	5°	100	400	50	10	9	±0.5	80	86	±22	13	$\pm 12^{6}$	Yes	5■
NE5533	Dual	Comm.	4		300	1500	25	10	13	±0.5	70	80	±22	16	$\pm 12^{6}$	Yes[8]	4.5▲
NE5535	Dual	Comm.	6	6°	40	150	50	1	15	±30	70	76	±18	5.6	±10	Yes	50■
SE5535	Dual	Mil.	4	15	20	80	50	1	15	±30	70	76	±22	5.6	±10	Yes	
LM124	Quad	Mil.	5	7°	30	150	50	1	0.3	32	70	65	32	3	26	Yes	50■
LM224	Quad	Ind.	5	7°	30	150	50	1	0.3	32	70	65	32	3	26	Yes	50■
LM324	Quad	Comm.	7	7°	50	250	25	1	0.3	32	65	65	32	3	26	Yes	50■
SA534	Quad	Auto	7	7°	50	250	25	1	0.3	32	65	65	32	3	26	Yes	50■
MC3303	Quad	Auto	8	10	75	500	20	1	0.6	±36	70	76	±18	7	±10	Yes	
MC3403	Quad	Comm.	10	10	50	500	20	1	0.6	±36	70	76	±18	7	±10	Yes	
MC3503	Quad	Mil.	5	10	50	500	50	1	0.6	±36	70	76	±18	4	±10	Yes	
NE5514	Quad	Comm.	5	5°	20	20	50	3	1	32	70	80	±16	10	±13	Yes	30■
SE5514	Quad	Mil.	2	4°	10	10	50	3	1	32	70	80	±16	10	±13	Yes	30■

See notes on next page

Amplifier Selector Guide

NOTES:

1. Military: −55°C to +125°C
   Industrial: −25°C to +85°C
   Commercial: 0°C to +70°C
   Automotive: −40°C to +85°C
2. Specifications guaranteed at 25°C unless otherwise indicated by the following marks:
   ° Typical over full temperature range
   ▲ Guaranteed over full temperature range
   ■ Typical at 25°C
3. Unless otherwise stated, maximum negative input voltage cannot exceed negative power supply voltage.
4. $A_V = 7$
5. $R = 10k\Omega$
6. $R_L = 600\Omega$
7. $A_V \geqslant 5$
8. $A_V \geqslant 3$
9. $R_L = 150\Omega$
10. $A_V \geqslant 7$
11. Fixed gain, stated in dB.
12. Bandwidth to −0.5dB pt.
13. Noise specification in dB, not volts.

Symbols and Definitions for Amplifiers

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Average Input Offset Current Temperature Coefficient (TCI_{OS})

The change in input offset current divided by the change to ambient temperature producing it.

Average Input Offset Voltage Temperature Coefficient (TCV_{OS})

The change in input offset voltage divided by the change in ambient temperature producing it.

Bandwidth

The frequency at which the gain is down 3dB from its DC value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Common-Mode Input Resistance

The resistance looking into both inputs, with inputs tied together.

Common-Mode Rejection Ratio (CMRR)

The ratio of the change of input offset voltage to the input common-mode voltage change producing it.

Full Power Bandwidth

The maximum frequency at which the full sine wave output might be obtained.

1dB Gain Compression and Saturated Output Power

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large-signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

Input Bias Current (I_B)

The average of the two input currents at zero output voltage. In some cases, the input current is measured for either input independently.

Input Capacitance

The capacitance looking into either input terminal with the other grounded.

Input Current

The current into an input terminal.

Input Noise Voltage

The square root of the mean square narrow-band noise voltage referred to the input.

Input Offset Current

The difference in the currents into the two input terminals with the output at 0V.

Input Offset Voltage

That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

Input Resistance

The resistance looking into either input terminal with the other grounded.

Input Voltage Range

The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

Intermodulation Intercept Tests

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select levels that are too low because the test equipment may not be able to recover the signal from the noise.

Large-Signal Voltage Gain

The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

Output Resistance

The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

Output Short-Circuit Current

The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Symbols and Definitions for Amplifiers

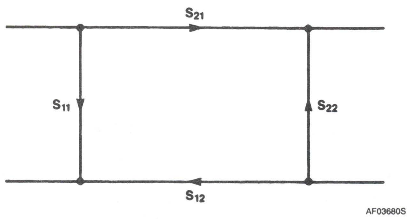


Figure 1. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

Figure 2

Output Voltage Swing

The peak output swing, referred to zero, that can be obtained.

Package Type Designation

See full package designations in Appendix.

Phase Margin

180° minus the absolute value of the phase shift measured at the frequency at which the gain is unity.

Power Consumption

The DC power required to operate the amplifier with the input at zero and with the output at zero and with no load current.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Power Supply Rejection Ratio

The ratio of the change in input offset voltage to the change in supply voltages producing it.

Rise Time

The time required for an output voltage step to change from 10% to 90% of its final value.

Scattering Parameters

S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figures 1 and 2.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

$$\text{INPUT RETURN LOSS} = S_{11}\text{dB}$$

$$S_{11}\text{dB} = 20 \text{ Log } |S_{11}|$$

$$\text{OUTPUT RETURN LOSS} = S_{22}\text{dB}$$

$$S_{22}\text{dB} = 20 \text{ Log } |S_{22}|$$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

Additional Reading on Scattering Parameters

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

S-Parameter Techniques for Faster, More Accurate Network Design, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, HP App Note 154, 1972.

Slew Rate

The maximum rate of change of output voltage under large-signal conditions.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10s).

Temperature Stability of Voltage Gain

The maximum variation of the voltage gain over the specified temperature range.

V_{CC} ($-V_{CC}$)

Supply voltage. The range of power supply voltage over which the device will operate safely.

Signetics

AN164
Explanation of Noise

Application Note

Linear Products

INTRODUCTION TO NOISE

Since fabrication techniques in the integrated circuit industry have improved so tremendously in the past few years, input offset voltages and bias currents are being minimized and noise parameters (whether measured at the output or referred to the input) have become a major source of concern. Reducing noise by improved process techniques and by use of peripheral component control will be the thrust of this application as a secondary effort, in understanding the noise components themselves.

An inspection of industry specifications show several methods of rating amplifier noise performance.

1. Output signal-to-noise ratio.
2. Output noise level (with specified loads and bandwidth).
3. Output noise level referenced to normal operating level.
4. Equivalent input noise (at a specified gain, source impedance and bandwidth).
5. Noise figure.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrow-band or wide-band, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common sources are shown in Figure 1. Some observations to be made from Figure 1 are that noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency; noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally-caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be identified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16ms sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, there are several preamplifiers available with variable bandwidth and frequency which allow quick noise source frequency identification. Another basic identification tool is the simple low-pass filter, as shown in Figure 2, where the bandpass is calculated by:

$$f_O = \frac{1}{2\pi RC} \qquad (1)$$

With such a filter, measurement bandpass can be changed from 10Hz to 100Hz (C = 4.7μF to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 1, the external noise chart.

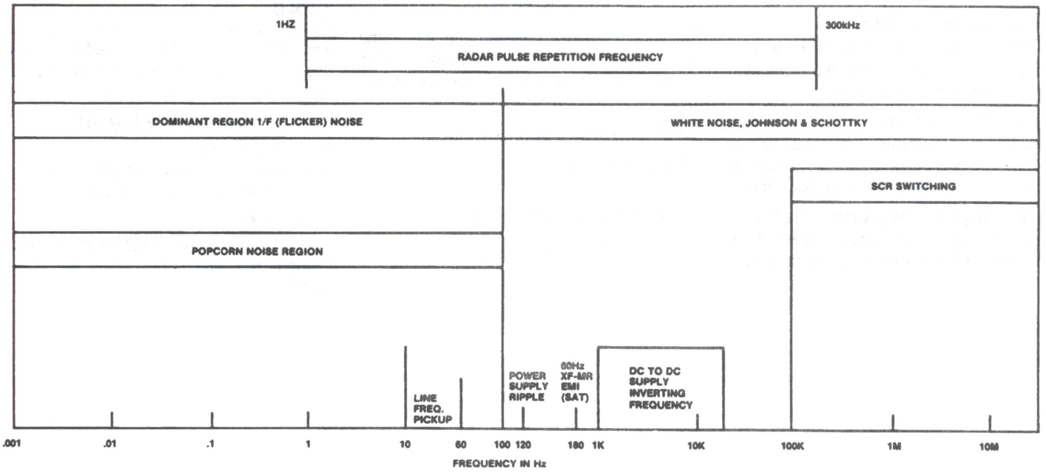


Figure 1. Frequency Spectrum of Noise Sources Affecting Operational Amplifiers and Low Noise Preamplifiers

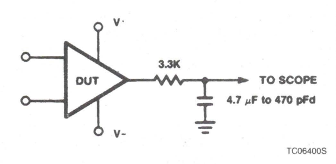


Figure 2. Noise Frequency Analysis RC Low-Pass Filter

POWER SUPPLY RIPPLE

Power supply ripple at 120Hz is not usually thought of as noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply rejection ratio (PSRR), the regulator's ripple rejection ratio, and, finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3. For the amplifier shown, 120Hz PSRR is about 74dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than 5mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to 0.5V.

Externally-compensated low noise op amps can provide improved 120Hz PSRR in high close-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 5. When compensated for a closed-loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies, allowing low ripple noise operation in exceptionally severe environments.

POWER SUPPLY DECOUPLING

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator outputs typically contain at least 150µV of noise in the 100Hz to 10kHz range, switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher frequency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 6, will adequately filter most wide-band noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage as the op amp's supply pins.

POWER SUPPLY REGULATION

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3, PSRR at DC is 110dB (3µV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp, and through careful selection and application of the peripheral components.

Noise voltage, e_n, or more properly, equivalent short-circuit input RMS noise voltage, is simply that noise voltage which would appear to originate at the input of a noiseless amplifier (referring to Figure 4) if the input terminals were shorted. It is expressed in nanovolts per root Hertz ($nV/\sqrt{Hz}$) at specified frequency, or in microvolts (µV) for a given frequency band. It is determined, or measured, by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristics is used in

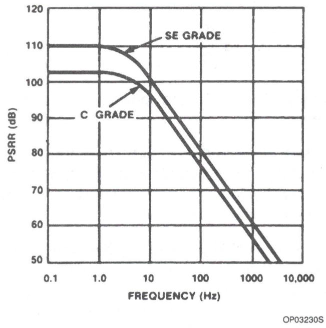


Figure 3. PSRR vs Frequency

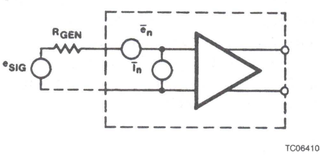


Figure 4. Noise Characterization of Amplifier

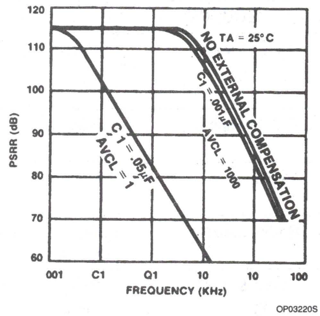


Figure 5. PSRR vs Frequency (Externally-Compensated Device)

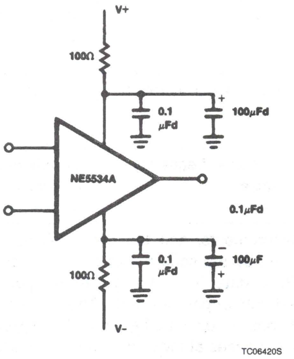


Figure 6. RC Decoupling

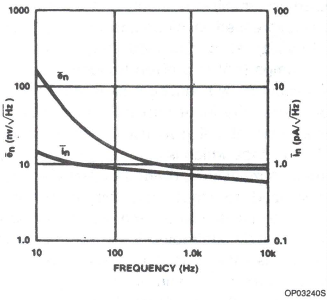


Figure 7. Noise Voltage and Current for an Op Amp

Table 1. External Noise Chart

SOURCE	NATURE	CAUSES	MINIMIZATION METHODS
60Hz Power	Repetitive Interference	Power lines physically close to op amp inputs. Poor CMRR at 60Hz.	Reorientation of power wiring. Shielded transformers.
120Hz Ripple	Repetitive	Inadequate ripple consideration. Poor RSRR at 120Hz.	Thorough design to minimize ripple. RC decoupling at the op amp.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio stations	Standard AM broadcast through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay & switch arcing	High frequency burst at switching rate.	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed circuit board contamination	Random low frequency	Dirty boards or sockets.	Thorough cleaning and humidity sealant.
Radar transmitters	High frequency gated at radar pulse repetition rate.	Radar transmitters from long range surface search to short range navigational especially near airports.	Shielding. Output filtering of frequencies >>PRR.
Mechanical vibration	Random < 100Hz	Loose connections, intermittent metallic contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper frequency noise	Common-mode input current at chopping frequency	Abnormally high noise chopper amplifier in system	Balanced source resistors. Use bipolar input op amps instead.

measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$, if data is to be expressed per unit bandwidth or per root Hertz. The level of $\overline{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in Figure 7. This increase is $1/f_{NOISE}$ (flicker).

Noise current, i_n, or more properly, equivalent open-circuit RMS noise current, is that noise which occurs apparently at the input of a noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz (pA/$\sqrt{Hz}$) at a specified frequency or in nanoamps (nA) in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is $i_n \times R_{IN}$ (or X_{CIN}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\overline{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the input, there is only $\overline{e}_n$ and $\overline{i}_n$ X_{CIN}. The $\overline{i}_n$ is measured with a bandpass filter and converted to pA/$\sqrt{Hz}$, if appropriate; typically, it increases at lower frequencies for bipolar op amps and transistors, but it increases at higher frequencies for field-effect transistors and Bi-FET/Bi-MOS op amps.

Noise Figure, NF, is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \log \frac{(S/N)_{in}}{(S/N)_{out}} \quad (2)$$

where: S and N are power or (voltage)^2 levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{GEN} and any X_{GEN} as well as frequency must be known to properly express NF in meaningful terms. This is because the amplifier $i_n \times Z_{GEN}$ as well as R_{GEN} itself produces input noise. The signal source contains some noise. However, e_{SIG} is generally considered to be noise-free and input noise is present as the thermal noise of the resistive component of the signal generator impedance R_{GEN}. This thermal noise is white in nature as it contains constant noise power density per unit bandwidth. It is easily seen that the $\overline{e}_n{}^2$ has the units V^2/Hz and that ($\overline{e}_n$) has the units V/$\sqrt{Hz}$

$$\overline{e}_R{}^2 = 4kTRB \quad (3)$$

where: T is temperature in °K
R is resistor value in Ω
B is bandwidth in Hz
k is Boltzman's constant

OPERATIONAL AMPLIFIER INTERNAL NOISE

OP AMP NOISE SPECIFICATIONS

Most completely specified low noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth and low frequency noise over a range of 0.1Hz to 10Hz. To minimize total noise, a knowledge of the derivation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

RANDOM NOISE CHARACTERISTICS

Op amp associated noise currents and voltages are random. They are aperiodic, not correlated to each other, and have Gaussian amplitude distributions; the highest noise amplitudes having the lowest probability. Gaussian amplitude distribution allows random noises to be expressed as RMS quantities;

Explanation of Noise

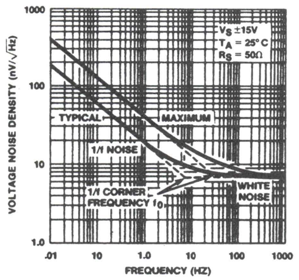


Figure 8. Noise Voltage

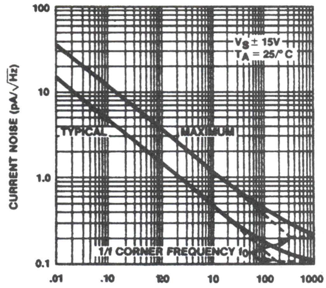


Figure 9. Noise Current

multiplying a Gaussian RMS quantity by six results in a peak-to-peak value that will not be exceeded 99.73% of the time.

The two basic types of op amp associated noises are white noise and flicker noise (l/f). White noise contains equal amounts of power in each Hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each decade of bandwidth. This is best illustrated by spectral noise density plots such as in Figures 8 and 9. Above a certain corner frequency, white noise dominates; below that frequency, flicker (l/f) noise is dominant. Low noise corner frequencies distinguish low noise op amps from general purpose devices.

SPECTRAL NOISE DENSITY

To utilize Figures 8 and 9, let us consider the definition of spectral noise density: the square root of the rate of change of mean-square noise voltage (or current) with frequency (Equation 4a).

$$e_n{}^2 = \frac{d}{df}(E_n)^2 \tag{4a}$$

$$i_n{}^2 = \frac{d}{df}(1_n)^2 \tag{4b}$$

$$E_n = \sqrt{\int_{f_L}^{f_H} e_n{}^2\,dF} \tag{5a}$$

$$I_N = \sqrt{\int_{f_L}^{f_H} i_n{}^2\,dF} \tag{5b}$$

where e_n, i_n = Spectral noise density
E_n, I_n = Total RMS noise
f_H = Upper frequency limit
f_L = Lower frequency limit

Conversely, the RMS noise value within a given frequency band is the square root of the definite integral of the spectral noise density over the frequency band (Equation 5b). This means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

WHITE NOISE

White noise sources are defined to have a noise content that is equal in each Hertz of bandwidth, and Equation 5b may be rewritten for white noise sources as:

$$E_n(\omega) = e_n\sqrt{f_H - f_L} \qquad I_n(\omega) = i_n\sqrt{f_H - f_L} \tag{6}$$

It is therefore convenient to express spectral noise density in V/√Hz or A/√Hz where $f_H - f_L = 1\text{Hz}$. When $f_H \geqslant 10f_L$, the white noise expressions may be further reduced to:

$$E_n(\omega) = e_n\sqrt{f_H} \qquad I_n(\omega) = i_n\sqrt{f_H} \tag{7}$$

FLICKER NOISE & WHITE NOISE

Since flicker noise content is equal in each decade of bandwidth, total flicker noise may be calculated if noise in one decade is known. The 0.1Hz to 1Hz decade noise content (K) is widely used for this purpose because the white noise contribution below 10Hz is usually negligible.

$$E_n(f) \cong K\sqrt{\frac{1}{f}}, \quad I_n(f) \cong K\sqrt{\frac{1}{f}} \tag{8}$$

When substituted in Equation 3, the expressions may be rewritten to:

$$E_n(f) = K\sqrt{\ln\left(\frac{f_H}{f_L}\right)} \tag{9}$$

$$I_n(f) = K\sqrt{\ln\left(\frac{f_H}{f_L}\right)}$$

When corner frequencies are known, simplified expressions for total voltage and current noise, (E_N and I_N), may be written:

$$E_N(f_H - f_L) = e_n\sqrt{f_{CE}\ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \tag{10}$$

$$I_N(f_H - f_L) = i_n\sqrt{f_{CI}\ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \tag{11}$$

where:

e_n = White noise voltage in a 1Hz bandwidth
i_n = White noise current in a 1Hz bandwidth
f_{CE} = Voltage noise corner frequency
f_{CI} = Current noise corner frequency
f_H = Upper frequency limit
f_L = Lower frequency limit

The two most important internally-generated noise minimization rules are: limit the circuit bandwidth, and use operational amplifiers with low corner frequencies.

NOISE SUMMATION

In the spectral density discussions, the concepts of white noise and flicker noise were introduced. In Figure 10, the complete input-referred op amp noise model, internal white and flicker noise sources are combined into three equivalent input noise generators, E_n, I_{N1} and I_{N2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1} and E_{t2}. Total RMS input-referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage sources over that bandwidth.

$$E_{NT}(f_H - f_L) = \sqrt{E_N{}^2 + (I_{N1}\cdot R_{S1})^2 + (I_{N2}\cdot R_{S2})^2 + E_{t1}{}^2 + E_{t2}{}^2} \tag{12}$$

Explanation of Noise

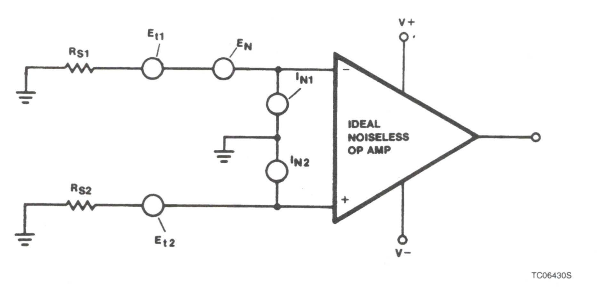


Figure 10. Op Amp Noise Mode[1]

THERMAL NOISE

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits this is the type of noise produced by the source resistances in series with each input. Its RMS value over a given bandwidth is calculated by:

$$E_t = \sqrt{4kTR\,(f_H - f_L)} \qquad (13)$$

Where:

k = Boltzman's constant = 1.38×10^{-23} joules/°K
T = Absolute temperature, °K
R = Resistance in Ω
f_H = Upper frequency limit in Hz
f_L = Lower frequency limit in Hz

At room temperature, Equation 13 simplifies to:

$$E_t = 1.28 \times 10^{-10}\sqrt{R(f_H - f_L)} \qquad (14)$$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from r_{bb}, the base-spreading resistances in the input stage transistors. These noises are included in E_N, the total equivalent input voltage noise generator.

SHOT NOISE

Shot noise (Shottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons). In Figure 10, I_{N1} and I_{N2} above the 1/f frequency are shot noise currents which are related to the amplifier's DC input bias currents:

$$I_{SH} = \sqrt{2qI_{BIAS}\,(f_H - f_L)} \qquad (15)$$

where:

I_{SH} = RMS shot noise value in amps
q = charge of an electron
= 1.602×10^{-19} Coulombs
I_{BIAS} = Bias current in amps
f_H = Upper frequency limit in Hz
f_L = Lower frequency limit in Hz

At room temperature, Equation 15 simplifies to:

$$I_{SH} = 5.64 \times 10^{-10}\sqrt{I_{BIA\ S}\,(f_h - f_L)} \qquad (16)$$

Shot noise currents also flow in the input stage emitter dynamic resistances, (r_e), producing input noise voltages. These voltages, along with the r_{bb}, thermal noise, make up the white noise portion of E_N, the total equivalent input noise voltage generator.

FLICKER NOISE

In limited bandwidth applications, flicker (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltages noise. Equation 17 illustrates this relationship:

$$\frac{i_n \text{ second stage}}{g_M \text{ first stage}} = e_n \text{ input} \qquad (17)$$

Another critical factor is corner frequency. For minimum noise, the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 11, low noise corner frequencies distinguish low noise op amps from ordinary industry-standard 741 types.

POPCORN NOISE

Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Minimization of this problem can be accomplished through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation".

Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be significantly reduced in almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated

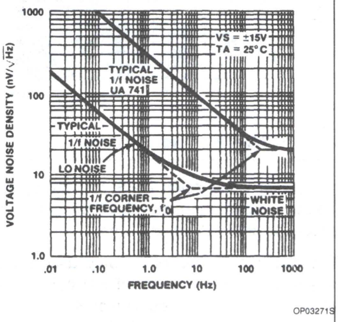


Figure 11. Noise Voltage Comparison

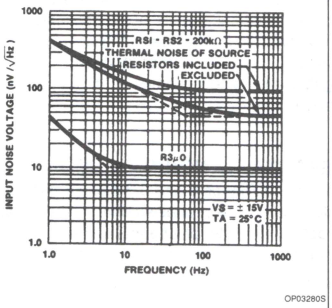


Figure 12. Input Noise Voltage vs Frequency

for a given application. To illustrate the method, noise information from a data sheet is reproduced in Figure 12. The first step is to determine the current and voltage noise corner frequencies so that the E_N and I_N terms of Equation 12 may be calculated using Equations 10 and 11.

CORNER FREQUENCY DETERMINATION

In the input shot noise versus frequency curves of Figure 12, it may be seen that voltage noise ($R_S = 0$) begins to rise at about 10Hz. Lines projected from the horizontal (white noise) portion and sloped (flicker noise) portion intersect at 6Hz, the voltage noise corner frequency (f_{CE}). In the center curve, excluding thermal noise multiplied by 200Ω is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 60Hz, the current noise corner frequency (f_{CI}). Equations 10 and 11 also require e_n and i_n for calculation of E_N and I_N. To find e_n and i_n, use the data sheet specification a decade or more above the respective corner frequencies; in this case e_n is 9.6 $nV/\sqrt{Hz}$ (1000Hz), and i_n is 0.12 $pA/\sqrt{Hz}$ (1000Hz).

BANDWIDTH OF INTEREST

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, $(f_H - f_L)$. At this time, assume f_H to be the highest frequency component that must be amplified without distortion. Note that e_n, i_n, corner frequencies and bandwidth are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

TYPICAL APPLICATION EXAMPLE

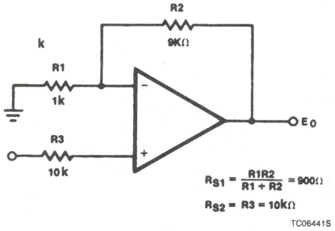
Figure 13a shows a typical ×10 gain stage with a 10kΩ source resistance. In Figure 13b, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

$e_n = 9.6nV/\sqrt{Hz}$
$I_n = 0.12pA/\sqrt{Hz}$
$f_{CE} = 6Hz$
$f_{CI} = 60Hz$

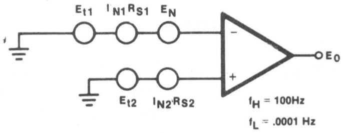
Using Equation 14: $E_t = \sqrt{4kTR(f_H - f_L)}$

$$E_{t1} = 1.28 \times 10^{10}\sqrt{(900\Omega)(100Hz)} = 0.4\mu V_{RMS}$$

$$E_{t2} = 1.28 \times 10^{10}\sqrt{(10k\Omega)(100Hz)} = 0.128\mu V_{RMS}$$


R2
9KΩ
k
R1
1k
R3
10k
−
+
E0
$R_{S1} = \frac{R1R2}{R1 + R2} = 900\Omega$
$R_{S2} = R3 = 10k\Omega$
TC06441S

a. Noise Analysis Circuit



b. Noise Analysis Equivalent Circuit

Figure 13

Next, Calculate I_N Using Equation 11

$$I_N = i_n\sqrt{f_{CI}\,l_n\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= 0.12pA\sqrt{60\,l_n\left(\frac{100Hz}{0.01Hz}\right) + (100 - 0.01)}$$

$$= 3.066pA_{RMS}$$

and:

$$I_{N1} \cdot R_{S1} \geqslant 3.066pA\ (900\Omega) = 0.0027\mu V_{RMS}$$

$$I_{N2} \cdot R_{S2} = 3.066pA\ (10k\Omega) = 0.0306\mu V_{RMS}$$

Finally, E_N from Equation 10

$$E_N = e_n\sqrt{f_{CE}\,l_n\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= 9.6nV\sqrt{6\,l_n\left(\frac{100Hz}{0.01Hz}\right) + (100 - 0.01)}$$

$$= 0.120\mu V_{RMS}$$

Substituting in Equation 12

$$E_{NT}\,(f_H - f_L) =$$

$$\sqrt{E_N{}^2 + I_{N1}{}^2R_{S1}{}^2 + (I_{N2}R_{S2})^2 + E_{t1}{}^2 + E_{t2}{}^2}$$

$$= \sqrt{(0.120\mu V)^2 + (0.0027\mu V)^2 + (0.0306\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 0.183\mu V_{RMS}$$

Using the factor of 6, total input-referred noise = $1.1\mu V_{P\text{-}P}$ (0.01Hz to 100Hz).

741 CALCULATION EXAMPLE

The preceding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 13 is useful. Once again the starting point is corner frequency determination, using the data sheet curves:

$f_{CE} = 200Hz$; $f_{CI} = 2kHz$;

$e_n = 20nV/\sqrt{Hz}$; $i_n = 0.5pA/\sqrt{Hz}$.

Using these corner frequencies and noise magnitudes, E_N and I_N are calculated to be $0.88\mu V_{RMS}$ and $68pA_{RMS}$, respectively. Multiplying this noise current by the source resis-

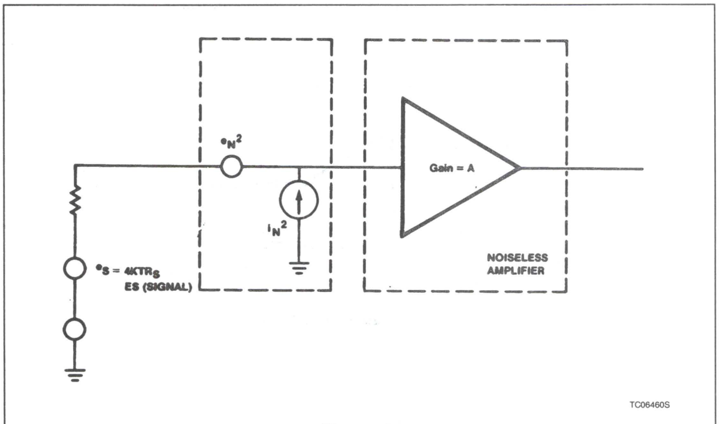


Figure 14

tance gives terms 2 and 3 of Equation 12 as shown below.

$$E_{NT}\ (f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2 R_{S1}^2 + I_{N2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2} \quad (12)$$

Substituting in Equation 12

$$= \sqrt{(0.88\mu V)^2 + (0.061\mu V)^2 + (0.68\mu V)^2 + (0.4\mu V)^2 + (0.128\mu V)^2}$$

$$= 1.12\mu V_{RMS}$$

Total input-referred noise = $6.7\mu V_{P\text{-}P}$ (0.01Hz to 100Hz).

This is 5.9 times that of the low noise op amp example.

The calculation examples illustrate three rules for minimizing noise in operational amplifier applications:

RULE 1. Use an op amp with low corner frequencies.

RULE 2. Keep source resistances as low as possible.

RULE 3. Limit circuit bandwidth to signal bandwidth.

NOISE PERFORMANCE

This segment shall be concerned with determining the signal-to-noise characteristics and the noise figure of amplifiers.

The amplifier noise is composed of thermal noise generated in the base resistance shot noise caused by the arrival of discrete charges at diode junction and 1/f noise.

For simplification, these noise sources can be combined and the amplifier modeled by a noise source and a noiseless amplifier as in Figure 14.

e_n = Amplifier's equivalent mean square noise voltage/$\sqrt{Hz}$

i_n = Amplifier's equivalent mean square noise current/$\sqrt{Hz}$

The total output noise can now be computed by Equation 8:

$$e_t = (e_n^2 + i_n^2 R_S^2 + 4kTR_S)^{1/2} B^{1/2} A_{RMS} \text{Volts} \quad (8)$$

Assuming R_S small compared to amplifier input.

* See Note 1.

If we now compare the total output noise to the output signal, $A - E_S$, we find the output signal-to-noise ratio.

$$S/N = \frac{E_s}{(e_n^2 + i_n^2 R_S^2 + 4kTR_S)^{1/2} B^{1/2}} \quad (13)$$

The denominator of the S/N ratio is the total output noise divided by the midband gain or the equivalent input noise as shown on the NE542 specification sheet.

$$E_{IN} = (e_n^2 + i_n^2 R_S^2 + 4kTR_S)^{1/2} B^{1/2} \text{RMS Volts} \quad (14)$$

The S/N ratio may now be computed independently of the amplifier gain. However, the gain should be chosen to maintain linear operation of the amplifier. For example, if the input signal to the NE542 is $400\mu V_{RMS}$ from a source resistance of 680Ω with a bandwidth of 100Hz to 10kHz, the S/N ratio becomes, in dB:

$$S/N = 20 \log \frac{400\mu V}{0.77\mu V} = 54.3\text{dB}$$

An amplifier gain of 68dB yields an output signal voltage of $1V_{RMS}$.

For an input signal of $10mV_{RMS}$, 40dB of gain, and $1V_{RMS}$ output, the NE542 gives a S/N ratio:

$$S/N = 20 \log \frac{10{,}000}{0.77} = 82.3\text{dB}$$

Another popular figure of merit for measuring the noise performance of an amplifier is noise figure. We first define noise factor (F) as

$$F = \frac{\text{Noise power input (Total)}}{\text{Thermal noise power}}$$

In terms of voltage this can be expressed as:

$$F = \frac{4kTR_S + (e_n^2 + i_n^2 R_S^2)}{4kTR_S} = 5.34,$$

$$R_S = 680\Omega \quad (15)$$

The noise figure is now defined as:

$$NF = 10 \log F \text{ (dB)}$$

or

$$NF = 10 \log \frac{4kTR_S + e_n^2 + i_n^2 R_S^2}{4kTR_S} \text{ (dB)} \quad (16)$$

Table 2. Spectral Voltage and Current Noise Densities

	μA741	5534	LF357	NE542	LM387
e_n (nV/$\sqrt{Hz}$)	40	4	12	7	9
i_n (pA/$\sqrt{Hz}$)	0.25	0.6	0.01	0.25	0.7
e_n f_{CE} (Hz)	200	90	50	800	850
i_n f_{CI} (Hz)	1.5k	200	1	700	2

NOTES:

1. The current spectral noise is omitted for the LF series since current noise levels in JFET devices are insignificant.
2. The spectral current noise for the LM387 is relatively linear over the frequency spectrum of 100Hz to 10kHz and is not specified below 100Hz.

A noiseless amplifier will, therefore, have a noise figure of "0" dB. Although the bandwidth has been eliminated from this calculation, it is still an influencing factor on the noise figure since the value of e_n and i_n will be dependent on the bandwidth of interest. This is especially true if I/f or high frequency noise is in this bandwidth.

From Figures 15 and 16 we can calculate the noise figure. For the NE542, the noise figure for 100Hz to 10Hz, 3dB bandwidth (15.7kHz equivalent noise bandwidth) and a source resistance of 5kΩ is:

$$NF = 10 \log \left(1 + \frac{e_n{}^2 + i_n{}^2 R_S{}^2}{4kTR_S} \right) \qquad (17)$$

$$NF = 10 \log$$

$$\left(1 + \frac{(7)^2 \times 10^{-18} + (0.25)^2 \times 10^{-24} \times R_S{}^2}{75 \times 10^{-18}} \right)$$

$4 \times 1.38 \times 10^{-23} \times 300° \text{K} \times R_S$

$= 10 \log$

$= 7.27 \text{ @ } R_S = 680\Omega$

$= 2.07 \text{ @ } R_S = 5k\Omega$

$= 1.25 \text{ @ } R_S = 10k\Omega$

To this point, the discussion has been limited to flat band response and no mention of the effect of equalization networks has been made. In instances where the gain of the amplifier is changing significantly across the frequency band of interest, as is the case for NAB and RIAA equalization, the noise performance is significantly improved.

The following table lists the spectral voltage and current noise densities and the respective corner frequencies for several different operational amplifiers and low noise preamplifiers.

where

I_N = total current noise over a specified bandwidth.

E_N = total voltage noise over a specified bandwidth.

E_{ti} = thermal (Johnson) noise of the source resistance.

*R_S = equivalent input source (or generator) resistance.

NOTE:

1. If R_S is a complex function, Z_S, then this function must be calculated for the R_{SS} mean of each bandwidth considered. For example, the input is a capacitor in parallel with a resistor; the input impedance is therefore:

$$Z_{IN} = \frac{R}{1 + jwCR}$$

Therefore as the frequency varies, the absolute value of Z_{IN} will vary and will affect the $I_N R_S$*, input noise value.

GENERAL EQUATIONS

Total Spectral Voltage Noise

$$E_N (f_H - f_L) = e_n \sqrt{f_{CE} \ln \left(\frac{f_H}{f_L} \right) + (f_H - f_L)} \qquad (18)$$

Total Spectral Noise Current

$$I_N (f_H - f_L) = i_n \sqrt{f_{CI} \ln \left(\frac{f_H}{f_L} \right) + (f_H - f_L)} \qquad (19)$$

Thermal

$E_t = 4 \text{ kTR } (f_H - f_L)$

$k = 1.38 \times 10^{-23}$ joules/°K

T = absolute temp in °K

$R = \Omega$

$f_t = 1.28 \times 10^{-10} \sqrt{R(f_H - f_L)}$ at room temperature (20)

Shot at Room Temperature

$$I_{SH} = 5.64 \times 10^{-10} \sqrt{I_{BIAS} (f_H - f_L)} \qquad (21)$$

Total Noise*

$$\left| \text{ENT} \right|_{f_L}^{f_H} = \sqrt{E_n{}^2 + (I_N R_{S1})^2 + I_{N2} R_{S2}{}^2 + E_{t1}{}^2 + E_{t2}{}^2}$$

Example:

In order to determine the total noise of any device the following basic procedures can be used:

1. Determine the spectral voltage noise value $\bar{e}_n$ and the 3dB corner frequency. (If the value is not listed, but a curve given, the spectral noise value will be that value above the 3dB corner frequency on the flat portion of the curve.)

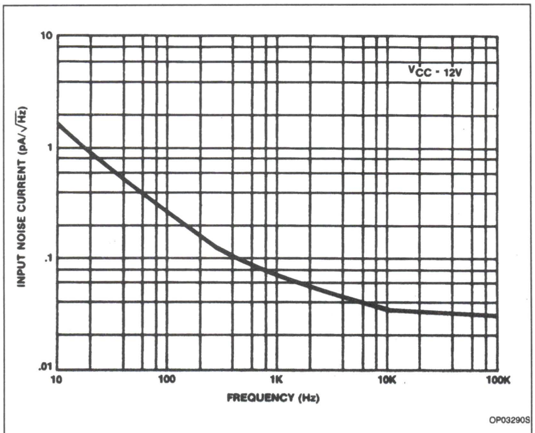


Figure 15. Input Noise Current vs Frequency

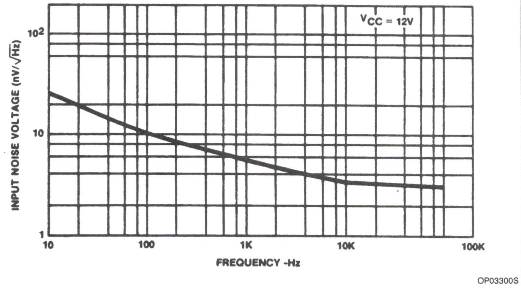


Figure 16. Input Noise Voltage vs Frequency

Explanation of Noise

AN164

2. Determine the spectral current noise value $\overline{i_n}$ and the 3dB corner frequency. (The same note holds true as for the spectral voltage noise, except that the corner frequencies are generally not the same.)
3. Determine the thermal noise of the input port source resistances by using the basic equal at room temperature of $E_T = 1.28 \times 10^{-10} \sqrt{R}/\sqrt{Hz}$
4. Using Equations 1, 2, and 4 and using Figure 1 as a basic block, we then can determine the total current and voltage noise at the input ports.
5. Employing Equation 5 we can then determine the total R_{SS} voltage noise referred to the input of the amplifier.
6. If the closed-loop gain of the system is known, then the total output noise is then $E_{Nout} = E_{Nin} \times A_{CL}$

Given: From Table 2, the NE5534 operating over the range of 10Hz to 1kHz and 1kHz to 10kHz, with $R_S = 10k\Omega$: determine total input noise over each bandwidth.

$$E_N(f_H - f_L) = e_n \sqrt{f_{CE} \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \qquad (18)$$

$$I_N(f_H - f_L) = i_n \sqrt{f_{CI} \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \qquad (19)$$

$$E_t = 1.28 \times 10^{-10} \sqrt{R\,(f_H - f_L)} \qquad (20)$$

$$\left| \mathrm{ENT} \right|_{f_L}^{f_H} = \sqrt{(E_n)^2 + (I_{N1} R_{S1})^2 + (E_t)^2} \qquad (21)$$

For the first band (10Hz to 1kHz):

$$E_n = 4 \times 10^{-9} \sqrt{90\ 1n\,(100) + (990)}$$
$$= 0.15\mu V_{RMS}$$

$$I_N R_S = 0.6 \times 10^{-12} \sqrt{200\ 1n\ (100) + (990) \times (10^4)}$$
$$= 0.26\mu V_{RMS}$$

$$E_T = 1.28 \times 10^{-8} \sqrt{990} = 0.4\mu V_{RMS}$$

$$E_{TH}\Big|_{10}^{1000} = \sqrt{(E_N)^2 + (I_N R_S)^2 + {E_T}^2}$$
$$= 0.50\mu V_{RMS}$$

Using the factor of 6:

$f_{NOISE\ P\text{-}P} = 3.00\mu V_{P\text{-}P}$ will never be exceeded in 99.73% of all cases.

For the second band (1kHz to 10kHz):

$${}^{*}E_N = 4 \times 10^{-9} \sqrt{9000} = 0.38\mu V_{RMS}$$

$$ {}^{*}I_N R_S = 0.6 \times 10^{-12} \sqrt{9000 \times (10^4)}$$
$$= 0.58\mu V_{RMS}$$

$$E_T = 1.28 \times 10^{-10} \sqrt{10^4 (9000)}$$
$$= 1.21\mu V_{RMS}$$

NOTE:
* For frequencies above 1kHz only WHITE noise is a consideration.

$$\left| E_{TH} \right|_{f_{1kHz}}^{f_{10kHz}} = \sqrt{(0.38)^2 + (0.57)^2 + (1.21)^2 \mu V_{RMS}}$$

$$\mathrm{RSS} \left| E_{TH} \right|_{f_{1kHz}}^{f_{10kHz}} = \sqrt{1.39\mu V_{RMS}}$$

$$E_{THmax} = 8.34\mu V_{P\text{-}P}$$

CONCLUSION

The designer should look at the previous application note as a reasonable approach to determine system noise levels. The variations of parameters, such as resistance values, temperature and bandwidth, are controllable by design procedure; however, the parametric variations of the monolithic op amps are controlled by the IC manufacturer. Signetics manufactures a wide variety of operational amplifiers designed to meet all contingencies.

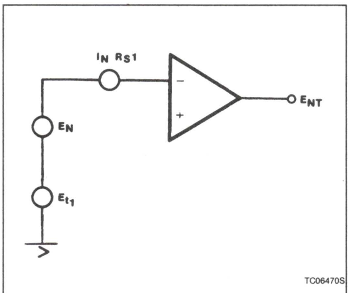

I_N R_S1
E_NT
E_N
E_t1
−
+
TC06470S

Figure 17. Total Noise Configuration

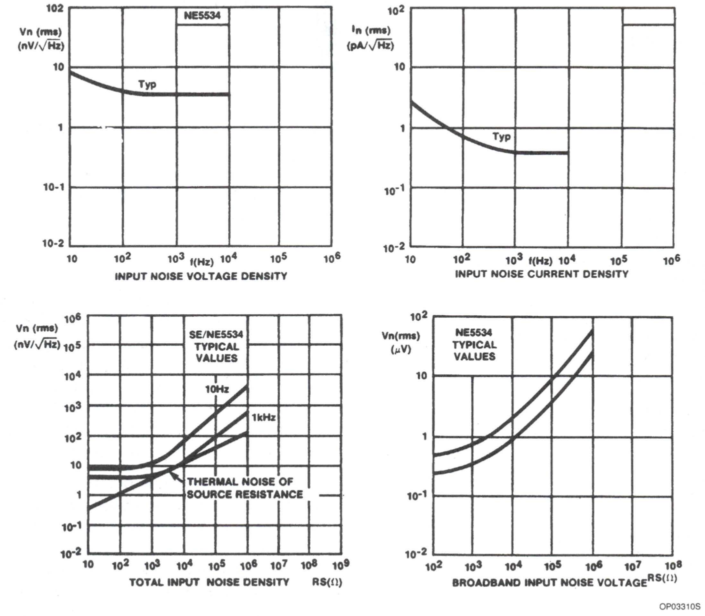


Figure 18. NE5534 Noise Characteristics

Signetics

Linear Products

AN165

Integrated Operational Amplifier Theory

Application Note

INTRODUCTION

The operational amplifier was first introduced in the early 1940s. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity, this application note will cover the basic op amp as it is defined, along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 1.

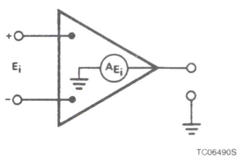


Figure 1. Ideal Operational Amplifier

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common-mode input signals.

Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed, the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. In bipolar devices, for instance, input bias currents are in the pA range for FET input amplifiers while offset voltages have been reduced to less than 1mV in many cases.

Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak-to-peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage, while output current is internally limited to approximately 25mA. Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

DEFINITION OF TERMS

Earlier, the ideal operational amplifier was defined. No circuit is ideal, of course, so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored, it would be beneficial to define those parameters commonly referenced.

INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0V out for 0V input. But, since the practical case is not perfect, a small DC voltage will appear at the output, even though no differential voltage is applied. This DC voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 2.

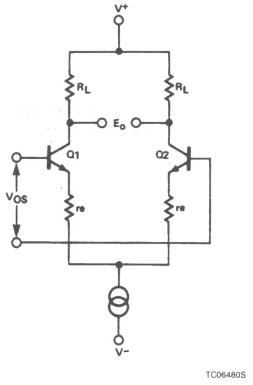


Figure 2. Differential Input Stage

An operational amplifier's performance is, in large part, dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage which also determines DC parameters such as offset voltage, since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions, the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

$$E_{OS} = I_{C2}R_L - I_{C1}R_L = 0 \tag{1}$$

In practice, small differences in geometries of the base-emitter regions of Q1 and Q2 will cause E_{OS} not to equal 0. Thus, for balance to be restored, a small DC voltage must be added to one V_{BE} or

$$V_{OS} = V_{BE}1 - V_{BE}2 \tag{2}$$

where the V_{BE} of the transistor is found by

$$V_{BE} = \frac{kT}{q} l_n \left(\frac{I_E}{I_s} \right) \tag{3}$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is 'that differential DC voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of V_{OS}. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is V_{OS} drift with temperature. Present-day amplifiers usually possess V_{OS} drift levels in the range of 5μV/°C to 40μV/°C. The magnitude of V_{OS} drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per °C will be 3.3μV for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.

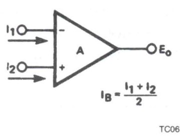


Figure 3. Input Bias Current

INPUT BIAS CURRENT

Referring to Figure 3, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a DC current path to ground in order for the input to function. Input bias current, then, is 'the DC current required by the inputs of the amplifier to properly drive the first stage.'

The magnitude of I_{BIAS} is calculated as the average of both currents flowing into the inputs and is calculated from

$$I_B = \frac{I_1 + I_2}{2} \qquad (4)$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little I_{OS} as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to I_{OS} can be calculated by

$$V_{OUT} = A_{CI}(I_{OS}R_S) \qquad (5)$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current. Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for I_{OS} drift with values ranging in the 0.5nA/°C area. Obviously, those applications requiring low input offset currents also require low drift with temperature.

INPUT IMPEDANCE

Differential and common-mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other, while common-mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

COMMON-MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon *both inputs* which will not cause the output to misbehave is called the common-mode range. Most amplifiers possess common-mode ranges of ±12V with supplies of ±15V.

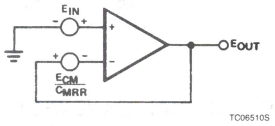


Figure 4. Effects of CMRR on Voltage-Follower

COMMON-MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common-mode signals. The classic definition for common-mode rejection ratio of an amplifier is the ratio of the differential signal gain to the common-mode signal gain expressed in dB as shown in equation 6a.

$$\text{CMRR(dB)} = 20\ \log\frac{e_O/e_I}{e_O/e_{CM}} \qquad (6a)$$

The measurement CMRR as in 6a requires 2 sets of measurements. However, note that if e_o in equation 6a is held constant, CMRR becomes:

$$\text{CMRR(dB)} = 20\ \log\frac{e_{CM}}{e_I} \qquad (6b)$$

A new alternate definition of CMRR based on 6b is the ratio of the change of input offset voltage to the input common-mode voltage change producing it.

Figure 4 illustrates the application of the equivalent common-mode error generator to the voltage-follower circuit. The gain of the voltage-follower with error contributions caused by both finite gain and finite common-mode rejection ratio is shown in equation 7.

$$\frac{e_O}{e_{IN}} = \frac{1 \pm 1/\text{CMRR}}{1 + 1/A} \qquad (7)$$

where A equals open-loop gain and is frequency-dependent.

AC PARAMETERS

Parameter definition has, up to this point, been dealing primarily with DC quantities of voltages currents, etc. Several important AC, or frequency-dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open-loop gain with low frequency gains in excess of 100dB. The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open-loop gain, the cascading of stages results in the need for frequency compensation in closed-loop configurations and reduces the open-loop.

LARGE-SIGNAL BANDWIDTH

The large-signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$f_{PL} = \frac{\text{Slew Rate}}{2\pi \cdot E_{OUT}} \qquad (8)$$

where f_{PL} is the upper power bandwidth frequency and E_{OUT} is the peak output swing of the amplifier.

SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components, to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease frequency response. In general, the worst case slew rate is in the unity gain non-inverting mode (see Figure 5a). Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each gain stage. Monolithic PNP transistors, used for level shifting, possess poor upper frequency characteristics. Cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 6, the open-loop frequency response of the op amps shown crosses unity gain at approximately 10MHz. Closed-loop response is unstable without compensation, however, so typical unity gain frequencies are readjusted by the effects of phase compensation, in this case 1MHz.

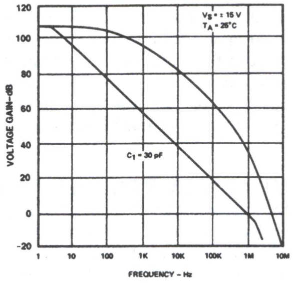


Figure 6. Open-Loop Voltage Gain as a Function of Frequency

From Figure 6, it is also apparent that an amplifier has a trade-off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade-off is a constant figure called the gain bandwidth product.

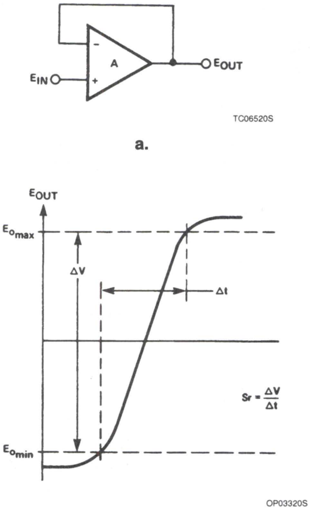
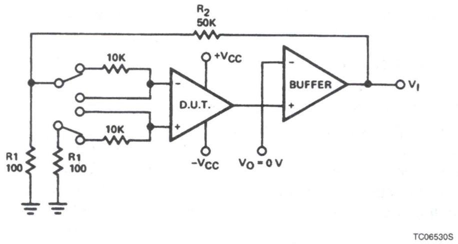
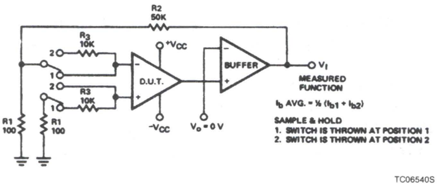


Figure 5. Amplifier Slew Rate Limitations



NOTE:
All resistor values are in ohms.

Figure 7. Circuit Diagram Used for CMRR Measurement



NOTE:
All resistor values are in ohms.

Figure 8. Circuit Diagram Used for Average Bias Current Measurement

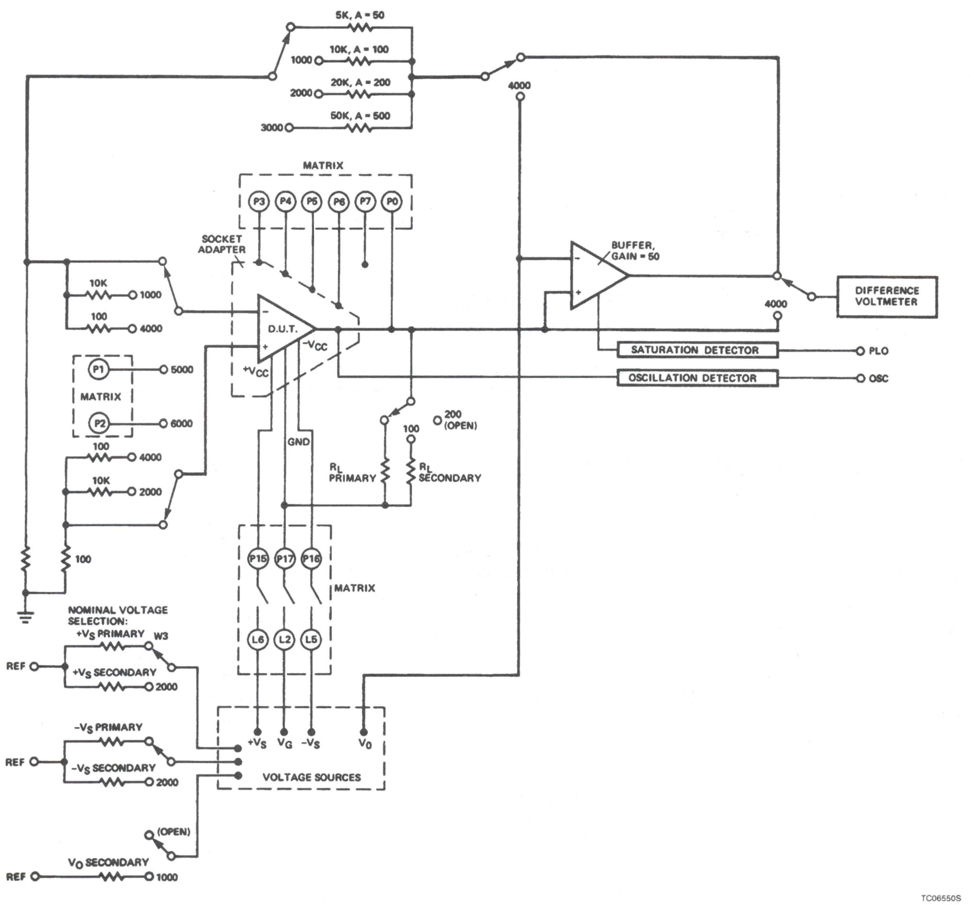
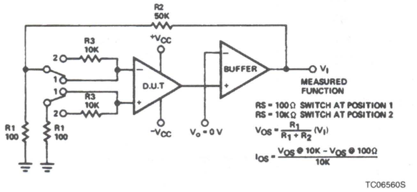
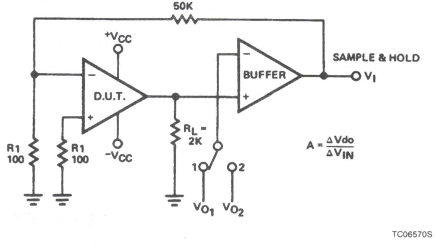

5K, A = 50
10K, A = 100
1000
20K, A = 200
2000
50K, A = 500
3000
4000
MATRIX
P3
P4
P5
P6
P7
P0
SOCKET ADAPTER
BUFFER, GAIN = 50
DIFFERENCE VOLTMETER
10K
1000
100
4000
D.U.T.
-VCC
+VCC
SATURATION DETECTOR
PLO
OSCILLATION DETECTOR
OSC
P1
5000
MATRIX
P2
6000
100
4000
10K
2000
GND
200 (OPEN)
100
RL PRIMARY
RL SECONDARY
100
P15
P17
P16
MATRIX
L6
L2
L5
NOMINAL VOLTAGE SELECTION:
+VS PRIMARY
W3
REF
+VS SECONDARY
2000
-VS PRIMARY
REF
-VS SECONDARY
2000
+VS
VG
-VS
VO
VOLTAGE SOURCES
(OPEN)
VO SECONDARY
REF
1000
TC06550S

Figure 9. A Typical Op Amp Test Circuit (Simplified)


R2
50K
R3
10K
+VCC
2
1
1
2
R3
10K
D.U.T
BUFFER
V1
MEASURED FUNCTION
RS = 100Ω SWITCH AT POSITION 1
RS = 10KΩ SWITCH AT POSITION 2
VOS = R1 / (R1 + R2) (V1)
IOS = (VOS @ 10K - VOS @ 100Ω) / 10K
R1
100
R1
100
-VCC
Vo = 0 V
TC06560S

NOTE:
All resistor values are in ohms.

Figure 10. Circuit Diagram Used for Offset Voltage and Offset Current


R2
50K
+VCC
BUFFER
SAMPLE & HOLD
V1
D.U.T.
RL = 2K
A = ΔVdo / ΔVIN
R1
100
R1
100
-VCC
1
2
VO1
VO2
TC06570S

NOTE:
All resistor values are in ohms.

Figure 11. Circuit Diagram Used for Large-Signal Open-Loop Gain Measurement

TEST METHODS

Product testing of integrated circuits uses automatic test equipment. Large computer-controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

A typical simplified op amp test configuration is depicted by Figure 9. Units may be classed in several categories according to selected parameters. Even failures may be classified categorically, depending upon their mode of failure.

Figures 7, 8, 10 and 11 illustrate the general test setups commonly used to measure CMRR, average bias current, offset voltage and current, and open-loop gain, respectively.

In general, the following parameters are tested under the following conditions.

COMMON-MODE REJECTION

The test setup for CMRR is given in Figure 7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

The positive common-mode input voltage within the range V_{CM1} is algebraically subtracted from all supply voltages and from V_O. Then V_1 is measured (V_{11}). The most negative common-mode voltage within the range, V_{CM2}, is then subtracted from all the supply voltages and V_O, and V_1 is again measured (V_{12}).

Then

$$CMRR = (R1 + R2)/R1(V_{CM1} - V_{CM2})/V_{11} - V_{12} \tag{9}$$

This operation is equivalent to swinging both inputs over the full common-mode range, and holding the output voltage constant, but it makes the V_1 measurement much simpler.

BIAS CURRENT

Bias current is measured in the configuration of Figure 8.

With switches at position 1 and $V_O = 0V$, measure V_{11}. Move switches to position 2 and again measure V_{12}. Calculate I_{BIAS} (average), by

$$I_{B1} = \frac{R1}{R1 + R2}\left(\frac{V1}{R3}\right) \tag{10a}$$

$$I_{B2} = \frac{R1}{R1 + R2}\left(\frac{V1}{R3}\right) \tag{10b}$$

$$I_{BIAS}(avg) = \frac{I_{B1} + I_{B2}}{2} = \frac{R1}{R1 + R2}\;\frac{V_{11} - V_{12}}{2R3} \tag{10c}$$

OFFSET VOLTAGE

Figure 10 is used for both offset voltage and current. With V_O at 0V and the switches selecting the source impedance of 100Ω, the offset voltage is measured at V_1 and is equal to

$$V_{OS} = \frac{R1V_1}{R1 + R2} \tag{11}$$

OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure V_{12}. Calculate the contribution of I_{OS} by

$$I_{OS} = \frac{V_{12} - V_I}{R3} \tag{12}$$

SIGNAL GAIN

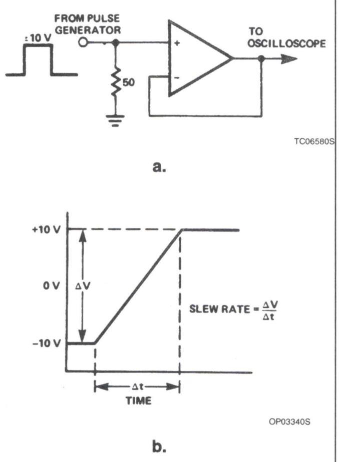
The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 11. Usually specified under a specific load determined by R_L, a signal equal to the maximum swing of the output voltage is applied to V_O in both positive and negative directions. V_{11} and V_{12} are measured values of V_1 and V_O = maximum positive and maximum negative signals, respectively. The gain of the device under test then becomes

$$A_{VO} = \left(\frac{R1 + R2}{R1}\right)\left(\frac{V_{O1} - V_{O2}}{V_{11} - V_{12}}\right) \tag{13}$$

SLEW RATE

Many other parameters are checked automatically by similar means. Only the most important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.

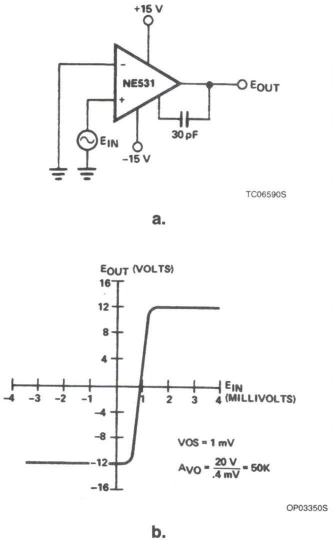


a.

b.

Figure 12. Measuring Slew

Figure 12 shows a typical bench setup for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, V_{IN} must be less



a.

b.

Figure 13. Transfer Curve of 531

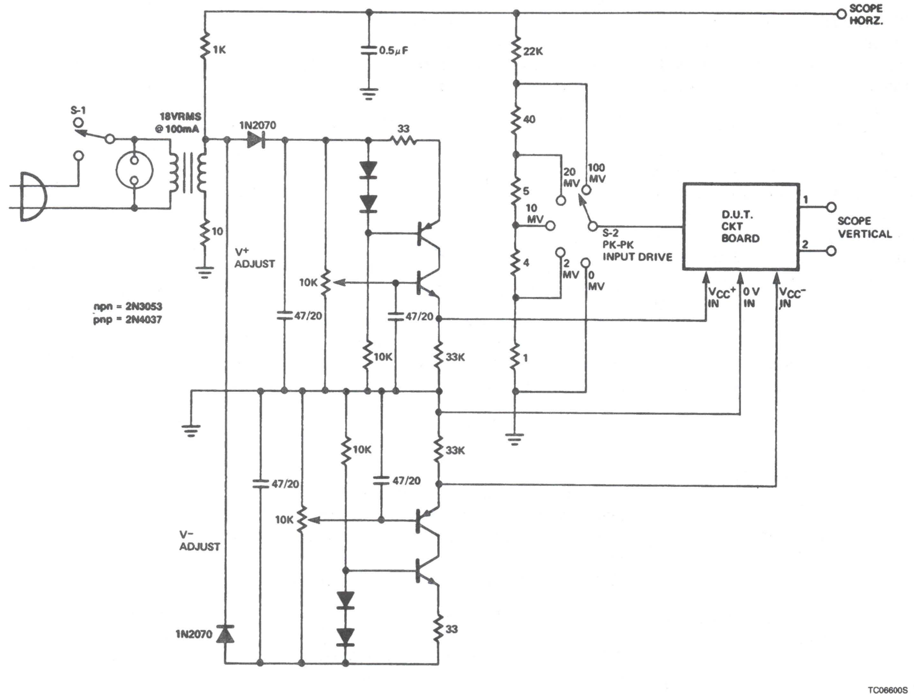


Figure 14. Curve Tracer Schematic

than absolute maximum input voltage and the waveform should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$SR = \frac{\Delta V_{OUT}}{\Delta T} \text{ in V/}\mu\text{s} \qquad (14)$$

OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Signetics linear devices.

Figure 13 shows the transfer characteristics of a typical linear device, the Signetics NE531. Note that the unit saturates at approximately +12V and −12V and exhibits a linear transfer characteristic between −10V and +10V.

From the slope of this linear portion of the transfer characteristic, and from the point and +10V where it crosses the E_{IN} axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (DUT), is 50,000 and its input offset voltage is 1.0mV.

A simple circuit to display the curves of Figure 13 on an oscilloscope is shown in Figure 14. A 60Hz, $44V_{P-P}$ sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the DUT.

The output of the DUT drives the vertical input of the scope. For providing V+ and V− to the DUT, the tester uses two simple adjustable regulators, both current-limited at 25mA. Input drive to the DUT may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V+ and V− supplies with an accurate meter. The supply voltages are somewhat dependent on AC line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak DUT input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 13.

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will, in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

AMPLIFIER DESIGN

Linear operational amplifier ICs were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short-circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three-stage approach requiring both input and output stage compensation. In addition, the output stage was not short-circuit proof and the input stage latched-up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally-compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage-to-current converter, with a small g_M and the second stage a current-to-voltage converter with a high r_M, the second stage can be rolled off at 6dB octave with a small value capacitor in the order of 30pF, which can then be built into the device itself. This concept is shown in Figure 15.

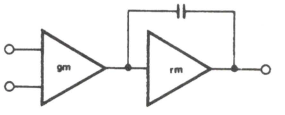


Figure 15. Basic Two-Stage Op Amp Design

The frequency and phase response of the PNP devices in the first stage dictate a roll-off in the second stage to give a loop gain of unity at about 1.0MHz. For the unity gain feedback configuration, this implies an open-loop gain of unity at this frequency. The capacitor C_C controls this parameter by looking much smaller than r_M at frequencies above a few cycles, giving a clean 6dB/octave roll-off over 5 decades.

The overall gain at frequencies where the impedance of C_C dominates r_m is given by

$$A_{V(\omega)} = \frac{qI_{S1}}{4kT} \cdot \frac{1}{\omega C_C} \qquad (15)$$

Substituting the value given, we find that a capacitance of $C_C = 30\text{pF}$ gives a unity gain frequency of about 1.0MHz.

First-stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the C_C by the expression

$$SR = \frac{dV}{dT} = \frac{I_{LS}}{C_C} \qquad (16)$$

where I_{LS} is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first-stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000. Bias currents under 2nA can be achieved in this way. Even though the B_{VCEO} of such transistors can be as low as 1V, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

The second limitation of 741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal g_M of the first stage as depicted by Figure 18, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source I_4 causes the first-stage transfer function to change as shown in Figure 19. The compensation capacitor is returned to the output of the NE531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large-signal bandwidths with this input structure will be essentially the same as the small-signal response. Full bandwidth possibilities of this configuration are still limited by the beta and f_t of the lateral PNP devices used for collector loads in the first stage. Even so, the slew rate of the NE531 and NE538 is a factor of 40 better than general purpose devices.

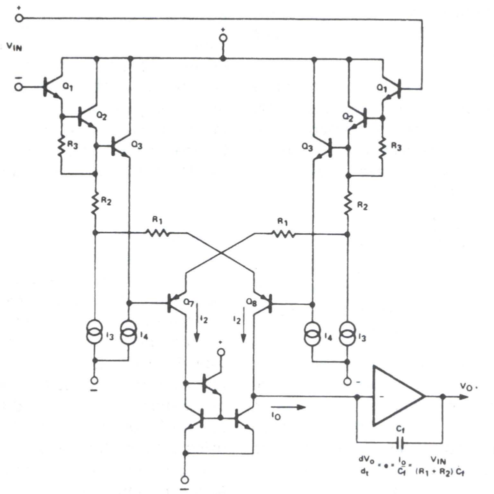

+
VIN
-
+
Q1
Q2
Q3
R3
R2
R1
R1
R2
R3
Q3
Q2
Q1
Q7
Q8
I2
I2
I3
I4
I4
I3
+
-
-
IO
CF
VO
$\frac{dV_O}{d_t} = \bullet = \frac{I_O}{C_f} = \frac{V_{IN}}{(R_1 + R_2)C_f}$
LD05940S

Figure 18. Input Structure of 531

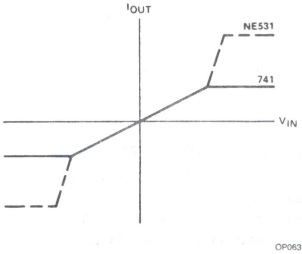


Figure 19. Voltage/Current Curves of First Stage

Signetics

AN166
Basic Feedback Theory

Application Note

Linear Products

BASIC FEEDBACK THEORY

In AN165, the ideal op amp was defined. The ideal parameters are never fully realized but they present a very convenient method for the preliminary analysis of circuitry. So important are these ideal definitions that they are repeated here. The ideal amplifier possesses

1. Infinite gain
2. Infinite input impedance
3. Infinite bandwidth
4. Zero output impedance

From these definitions two important theorems are developed.

1. No current flows into or out of the input terminals.
2. When negative feedback is applied, the differential input voltage is reduced to zero.

Keeping these rules in mind, the basic concept of feedback can be explored.

VOLTAGE-FOLLOWER

Perhaps the most often used and simplest circuit is that of a voltage-follower. The circuit of Figure 1 illustrates the simplicity.

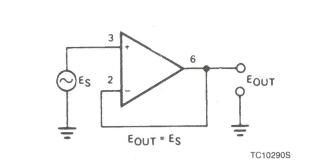


Figure 1. Voltage-Follower

Applying the zero differential input theorem, the voltages of Pins 2 and 3 are equal, and since Pins 2 and 6 are tied together, their voltage is equal; hence, $E_{OUT} = E_{IN}$. Trivial to analyze, the circuit nevertheless does illustrate the power of the zero differential voltage theorem. Because the input impedance is multiplied and the output impedance divided by the loop gain, the voltage-follower is extremely useful for buffering voltage sources and for impedance transformation.

The basic configuration in Figure 1 has a gain of 1 with extremely high input impedance. Setting the feedback resistor equal to the source impedance will cancel the effects of bias current if desired.

However, for most applications, a direct connection from output to input will suffice. Errors arise from offset voltage, common-mode rejection ratio, and gain. The circuit can be used with any op amp with the required unity gain compensation, if it is required.

NON-INVERTING AMPLIFIER

Only slightly more complicated is the non-inverting amplifier of Figure 2.

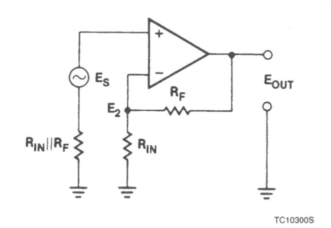


Figure 2. Non-Inverting Amplifier

The voltage appearing at the inverting input is defined by

$$E_2 = \frac{E_{OUT} \cdot R_{IN}}{R_F + R_{IN}} \quad (1a)$$

Since the differential voltage is zero, $E_2 = E_S$, and the output voltage becomes

$$E_{OUT} = E_S\left(1 + \frac{R_F}{R_{IN}}\right) \quad (1b)$$

It should be noted that as long as the gain of the closed-loop is small compared to open-loop gain, the output will be accurate, but as the closed-loop gain approaches the open-loop value more error will be introduced.

The signal source is shown in Figure 2 in series with a resistor equal in size to the parallel combination of R_{IN} and R_F. This is desirable because the voltage drops due to bias currents to the inputs are equal and cancel out even over temperature. Thus overall performance is much improved.

The amplifier does not phase-invert and possesses high input impedance. Again the impedances of the two inputs should be equal to reduce offsets due to bias currents.

INVERTING AMPLIFIER

By slightly rearranging the circuit of Figure 2, the non-inverting amplifier is changed to an inverting amplifier. The circuit gain is found by applying both theorems; hence, the voltage at the inverting input is 0 and no current flows into the input. Thus the following relationships hold:

$$\frac{E_S}{R_{IN}} + \frac{E_O}{R_F} = 0 \quad (2a)$$

Solving for the output E_O

$$E_O = -E_S\frac{R_F}{R_{IN}} \quad (2b)$$

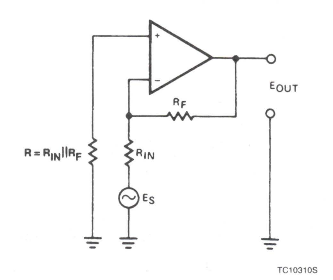


Figure 3. Inverting Amplifier

As opposed to the non-inverting circuits the input impedance of the inverting amplifier is not infinite but becomes essentially equal to R_{IN}. This circuit has found widespread acceptance because of the ease with which input impedance and gain can be controlled to advantage, as in the case of the summing amplifier.

With the inverting amplifier of Figure 3, the gain can be set to any desired value defined by R divided by R_{IN}. Input impedance is defined by the value of R_{IN} and R should equal the parallel combination of R_{IN} and R to cancel the effect of bias current. Offset voltage, offset current, and gain contribute most of the errors. The ground may be set anywhere within the common-mode range and any op amp will provide satisfactory response.

CURRENT-TO-VOLTAGE CONVERTER

The transfer function of the current-to-voltage converter is

$$V_{OUT} = I_{IN} R_1 \quad (3)$$

Evaluation of the circuit depends upon the virtual ground theorem developed earlier. The current flowing into the input must be the same as that flowing across R1, hence, the output voltage is the IR drop of R1.

Limitations, of course, are output saturation voltage and output current capability. The inputs may be biased anywhere within the common-mode range.

DIFFERENTIAL AMPLIFIER

This circuit of Figure 5 has a gain with respect to differential signals of R2/R1.

The common-mode rejection is dominated by the accuracy of the resistors. Other errors arise from the offset voltage, input offset current, gain and common-mode rejection. The circuit can be used with any op amp discussed in this chapter with the proper compensation.

SUMMING AMPLIFIER

The summing amplifier is a variation of the inverting amplifier. The output is the sum of the input voltages, each being weighed by R_F/R_{IN}.

The value of R4 may be chosen to cancel the effects of bias current and is selected equal to the parallel combination of R_F and all the input resistors.

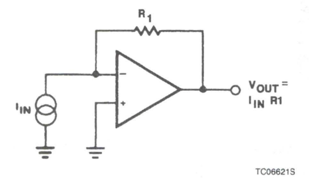


Figure 4. Current-to-Voltage Converter

INTEGRATOR

Integration can be performed with a variation of the inverting amplifier by replacing the feedback resistor with a capacitance. The transfer function is defined by

$$V_{OUT} = -\frac{1}{RC}\int_{0}^{t} V_{IN}\cdot dt \tag{4}$$

The gain of the circuit falls at 6dB per octave over the range in which strays and leakages are small.

Since the gain at DC is very high a method for resetting initial conditions is necessary. Switch S1 removes the charge on the capacitor. A relay or FET may be used in the practical circuit. Bias and offset currents and offset voltage of the switch should be low in such an application.

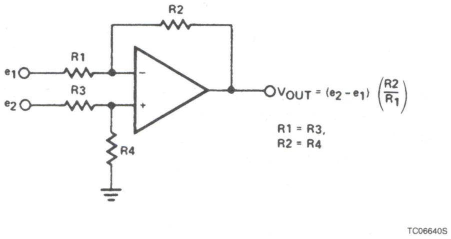


Figure 5. Differential Amplifier

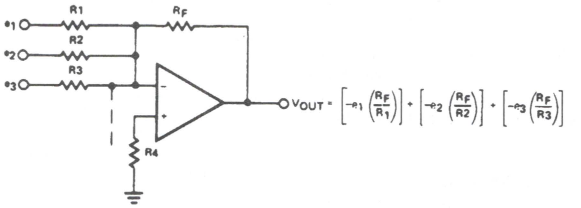


Figure 6. Summing Amplifier

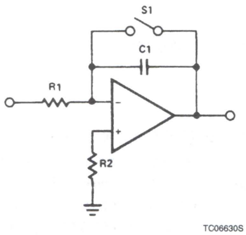


Figure 7. Integrator

DIFFERENTIATOR

The differentiator of Figure 8 is another variation of the inverting amplifier. The gain increases at 6dB per octave until it intersects the amplifier open-loop gain, then decreases because of the amplifier bandwidth. This characteristic can lead to instability and high frequency noise sensitivity.

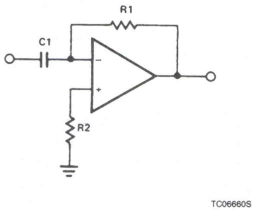


Figure 8. Differentiator

A more practical circuit is shown in Figure 9. The gain has been reduced by R3 and the high frequency gain reduced by C2, allowing better phase control and less high frequency noise. Compensation should be for unity gain.

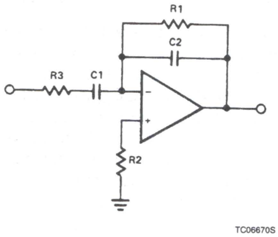


Figure 9. Practical Differentiator

COMPENSATION

Present-day operational amplifiers are comprised of multiple stages, each of which has a 3dB point or pole associated with it. Referring to Figure 10, the 3dB breakpoints of a two-stage amplifier are approximated by the Bode plot.

Basic Feedback Theory AN166

As with any feedback loop, the op amp must be protected from phase shifts in excess of 360°. A steady 180° phase shift is developed by the amplifier from output to inverting input. In addition, the sum of all additional shifts due to amplifier poles or feedback component poles will cause the necessary additional 180° to sustain oscillation if the gain of the amplifier is greater than one for the frequency at which the 180° phase shift is reached. By adding poles and zeros to the amplifier response externally, the phase shift can be controlled to insure stability.

Many op amps now include internal compensation. These are single capacitors of 30pF, typically, and the amplifier will remain stable for all gains. However, since they are unconditionally stable, the compensation is larger than required for most applications. The resultant loss of bandwidth and slew rate may be acceptable in the general case, but selection of an externally-compensated device can add a great deal to the amplifier response if the compensation is handled properly.

In order to fully develop the point at which instability occurs, a fuller understanding of phase response is necessary.

The diagram of Figure 11 depicts the phase shift of a single pole. Note that at the pole position the phase shift is 45° and that phase shift becomes 0° for a decade below the pole and −90° for a decade above the pole location. This is a Bode approximation which possesses a 5.7° error at 0° and 90°, but this error is usually considered small enough to be ignored. The single pole produces a maximum of 90° phase shift and also produces a frequency roll-off of 20dB per decade. The addition of the second pole of Figure 12 produces an additional 90° phase shift and increases the roll-off slope to −40dB per decade.

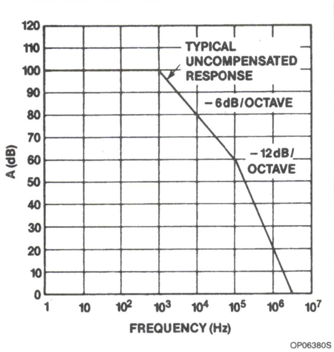


Figure 10. Frequency Compensation

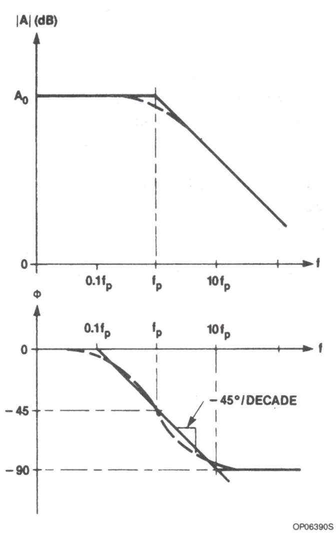


Figure 11. Single-Pole Amplitude and Phase Response

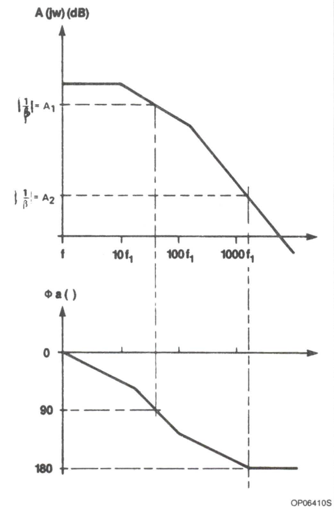


Figure 12. Two-Pole Closed-Loop Response

At this point, phase shift could exceed 180° because unity gain is reached, causing stability. For gain levels equal to A1 or 1/β, the phase shift is only 90° and the amplifier is stable. However, the gain of A2 the phase shift is 180° and the loop is unstable. Gains in between A1 and A2 are marginally stable. However, as shown in Figure 13, the phase shift as it approaches 180° causes increasing frequency peaking and overshoot until sustained oscillations occur.

It is generally accepted in the interest of minimized frequency peaking to limit the phase shift of the amplifier to 135° or a phase margin of 45°. At this margin the second-order response of the system is critically damped and oscillation is prevented.

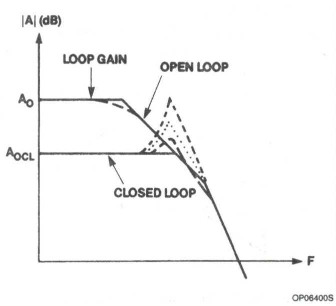


Figure 13. Frequency Peaking Due to Insufficient Phase Margin

Referring to Figure 14, the required compensation can be determined. Given the open-loop response of the amplifier, the desired gain is plotted until it intercepts the open-loop curve as shown.

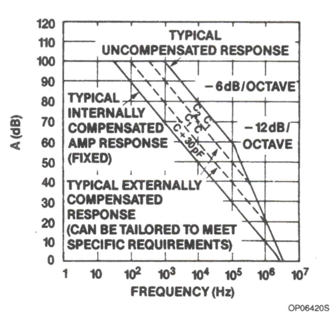


Figure 14. Frequency Compensation

The phase shift for minimum peaking is 135°. Remembering that phase shift is 45° at the frequency pole, the example of Figure 14 will be unstable at gains less than 20dB where phase shift exceeds 180°, and will possess excessive overshoot and ringing at gains I_{SS} than 60dB where phase shift exceeds 135°. Thus, the desired compensation will move the second pole of the amplifier out in frequency until the closed-loop gain intersects the open-loop response before the second break of the amplifier occurs. Selecting only enough compensation to do the job assures the maximum bandwidths and slew rates of the amplifier. Additional in-depth information on compensation can be found in the reference material.

FEED-FORWARD COMPENSATION

External compensation has been shown to improve amplifier bandwidth over internal compensation in the preceding section. Additional bandwidth can be realized if feed-forward compensation is used. Bandwidth is limited in monolithic design by the poor frequency response of the PNP level shifters of the first stage.

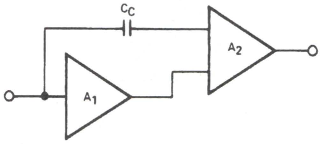


Figure 15. Technique of Feed-Forward Around 1st Stage

The concept of feed-forward compensation bypasses the input stage at high frequencies driving the higher frequency second stage directly as pictured by Figure 15. The Bode plot of Figure 16 shows the additional response added by the feed-forward technique. The response of the original amplifier requires less compensation at lower frequencies allowing an order of magnitude improvement in bandwidth. Standard compensation and feed-forward are both plotted to illustrate the bandwidth improvement. Unfortunately, the use of feed-forward compensation is restricted to the inverting amplifier mode.

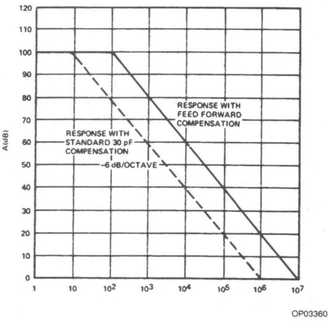


Figure 16. Frequency Response With Feed-Forward Compensation

REFERENCES

1. OPERATIONAL AMPLIFIERS-*Design & Applications*, Jerald Graeme and Gene Tobey, McGraw Hill Book Company.

Signetics

LM124/224/324/A* /SA534/LM2902

Low Power Quad Op Amps

Product Specification

Linear Products

DESCRIPTION

The LM124/SA534/LM2902 series consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

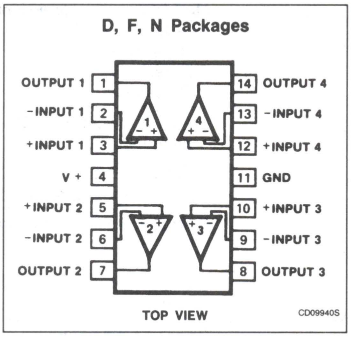
In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency and the input bias current ACC are temperature-compensated.

FEATURES

- **Internally frequency-compensated for unity gain**
- **Large DC voltage gain — 100dB**
- **Wide bandwidth (unity gain) — 1MHz (temperature-compensated)**
- **Wide power supply range**
  Single supply — $3V_{DC}$ to $30V_{DC}$ or dual supplies — $\pm 1.5V_{DC}$ to $\pm 15V_{DC}$
- **Very low supply current drain — essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)**
- **Low input biasing current — $45nA_{DC}$ (temperature-compensated)**
- **Low input offset voltage — $2mV_{DC}$ and offset current — $5nA_{DC}$**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage — $0V_{DC}$ to $V\pm 1.5V_{DC}$ swing**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	-55°C to +125°C	LM124N
14-Pin Ceramic DIP	-55°C to +125°C	LM124F
14-Pin Plastic DIP	-25°C to +85°C	LM224N
14-Pin Ceramic DIP	-25°C to +85°C	LM224F
14-Pin Plastic DIP	0 to +70°C	LM324N
14-Pin Ceramic DIP	0 to +70°C	LM324F
14-Pin Plastic SO	0 to +70°C	LM324D
14-Pin Plastic DIP	-40°C to +85°C	SA534N
14-Pin Ceramic DIP	-40°C to +85°C	SA534F
14-Pin Plastic SO	-40°C to +85°C	SA534D
14-Pin Plastic SO	-40°C to +85°C	LM2902D
14-Pin Plastic DIP	-40°C to +85°C	LM2902N

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*Please contact your local Signetics Sales Office or the Signetics factory for information on the LM324A offered in 14-Pin Plastic DIP or SO.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	−0.3 to +32	V_{DC}
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1]		
	N package	1190	mW
	F package	1420	mW
	D package	1040	mW
	Output short-circuit to GND 1 amplifier[2] $V_{CC} < 15V_{DC}$ and $T_A = 25°C$	Continuous	
V_{IN}	Input current ($V_{IN} < -0.3V$)[3]	50	mA
T_A	Operating ambient temperature range		
	LM324	0 to +70	°C
	LM224	−25 to +85	°C
	SA534/LM2902	−40 to +85	°C
	LM124	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short-circuits from the output to V_{CC} + can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$ continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/ LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$ $R_S = 0\Omega$, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	$R_S = 0\Omega$		7			7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$ $I_{IN}(+)$ or $I_{IN}(-)$, over temp.		45 40	150 300		45 40	250 500	nA
I_B	Drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$ $I_{IN}(+0 - I_{IN}(-)$, over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift	Over temp.		10			10		pA/°C
V_{CM}	Common-mode voltage range[3]	$V_{CC} = 30V$ $V_{CC} = 30V$, over temp.	0 0		V±1.5 V±2	0 0		V±1.5 V±2	V V
CMRR	Common-mode rejection ratio	$V_{CC} = 30V$	70	85		65	70		dB

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*Please contact your local Signetics Sales Office or the Signetics factory for information on the LM324A offered in 14-Pin Plastic DIP or SO.

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 5V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V_{CC} = +30V$, over temp.	26			26			V
V_{OH}	Output voltage high	$R_L \leqslant 10k\Omega$, over temp.	27	28		27	28		V
V_{OL}	Output voltage low	$R_L \leqslant 10k\Omega$, $V_{CC} = 5V$, over temp.		5	20		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp.		1.5	3		1.5	3	mA
		$R_L = \infty$, on all op amps, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	$V_{CC} = +15V$ (for large V_O swing) $R_L \geqslant 2k\Omega$	50	100		25	100		V/mV
		$V_{CC} = +15V$ (for large V_O swing), $R_L \geqslant 2k\Omega$, over temp.	25			15			V/mV
	Amplifier-to-amplifier coupling[5]	f = 1kHz to 20kHz, input referred		−120			−120		dB
PSRR	Power supply rejection ratio	$R_S \leqslant 0\Omega$	65	100		65	100		dB
I_{OUT}	Output current source	$V_{IN}+ = +1V_{DC}$, $V_{IN}- = 0V_{DC}$, $V_{CC} = 15V_{DC}$	20	40		20	40		mA
		$V_{IN}+ = +1V_{DC}$, $V_{IN}- = 0V_{DC}$, $V_{CC} = 15V_{DC}$, over temp.	10	20		10	20		mA
	sink	$V_{IN}- = +1V_{DC}$, $V_{IN}+ = 0V_{DC}$, $V+ = 15V_{DC}$	10	20		10	20		mA
		$V_{IN}- = +1V_{DC}$, $V_{IN}+ = 0V_{DC}$, $V_{CC} = 15V_{DC}$, over temp.	5	8		5	8		mA
		$V_{IN}+ = 0V_{DC}$, $V_{IN}- = +1V_{DC}$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short-circuit current[4]		10	40	60	10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}			V_{CC}	
GBW	Unity gain bandwidth	$T_A = 25°C$		1			1		MHz
SR	Slew rate	$T_A = 25°C$		0.3			0.3		V/μs
V_{NOISE}	Input noise voltage	$T_A = 25°C$, f = 1kHz		40			40		nV/$\sqrt{Hz}$

NOTES:

1. $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V_{CC} from 5V to 30V and over full input common-mode range ($0V_{DC}+$ to $V_{CC} - 1.5V$).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC} - 1.5$, but either or both inputs can go to +32V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

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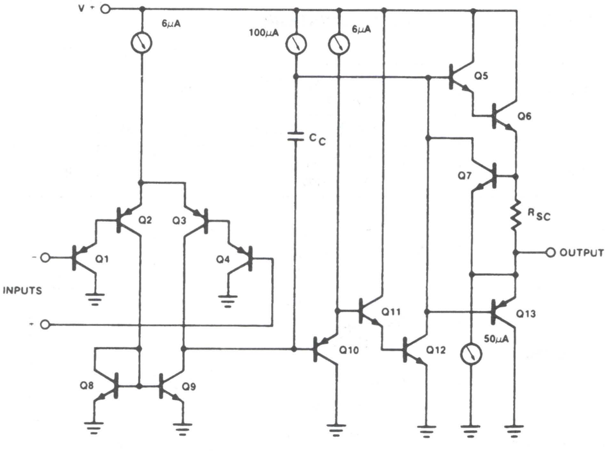
*Please contact your local Signetics Sales Office or the Signetics factory for information on the LM324A offered in 14-Pin Plastic DIP or SO.

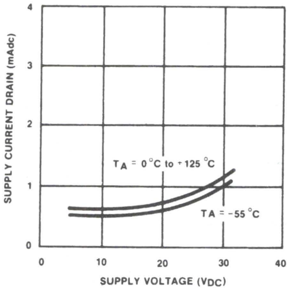
EQUIVALENT SCHEMATIC


V+
6μA
100μA
6μA
Q5
Q6
C_C
Q7
R_{SC}
Q2
Q3
Q1
Q4
OUTPUT
INPUTS
-
+
Q11
Q13
50μA
Q10
Q12
Q8
Q9

TC08890S

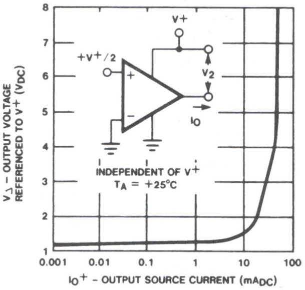
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



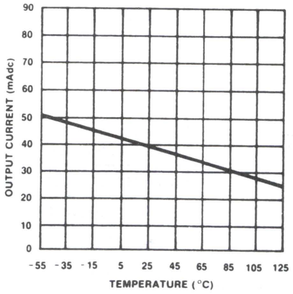
OP05450S

Output Characteristics Current Sourcing



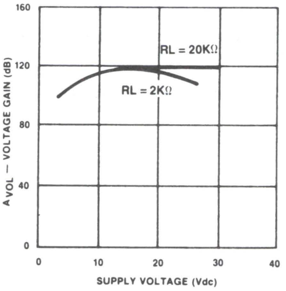
OP05460S

Current Limiting



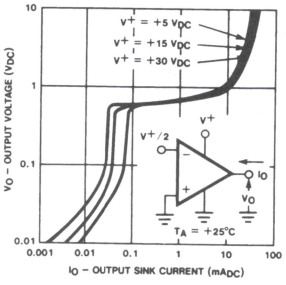
OP05470S

Voltage Gain



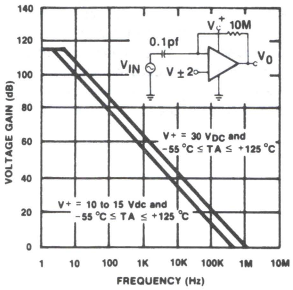
OP05480S

Output Characteristics Current Sinking



OP05490S

Open-Loop Frequency Response



OP05500S

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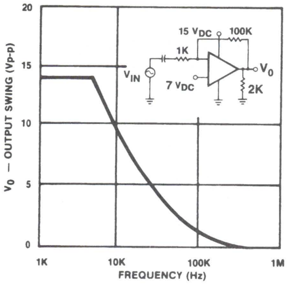
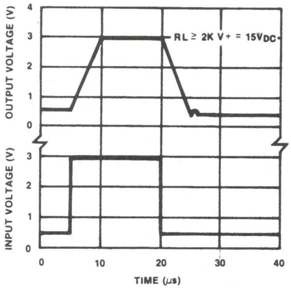
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Large-Signal Frequency Response



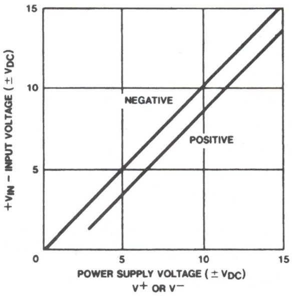
OP05510S

Voltage-Follower Pulse Response



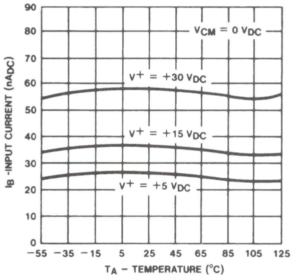
OP05520S

Input Voltage Range



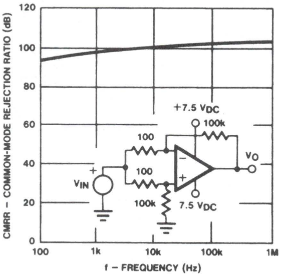
OP05530S

Input Current



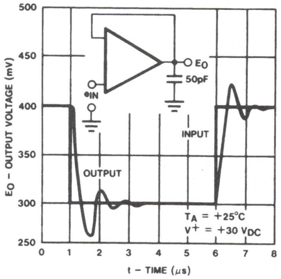
OP05540S

Common-Mode Rejection Ratio



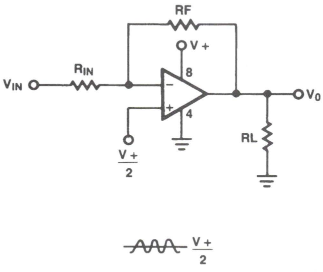
OP05550S

Voltage-Follower Pulse Response (Small-Signal)



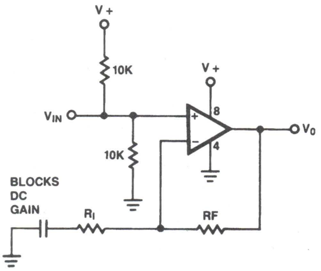
OP05560S

TYPICAL APPLICATIONS


RF
V+
8
V_{IN}
R_{IN}
4
V_O
RL
V+
2
V+
2

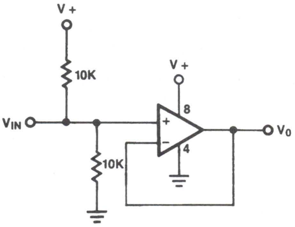
TC08900S

Single Supply Inverting Amplifier


V+
10K
V+
V_{IN}
8
4
V_O
10K
BLOCKS
DC
GAIN
R_I
RF

TC08910S

Non-Inverting Amplifier


V+
10K
V+
8
V_{IN}
V_O
4
10K

TC08920S

Input Biasing Voltage-Follower

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*Please contact your local Signetics Sales Office or the Signetics factory for information on the LM324A offered in 14-Pin Plastic DIP or SO.

Signetics

MC/SA1458/MC1558
General-Purpose Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The MC1458 is a high-performance operational amplifier with high open-loop gain, internal compensation, high common-mode range and exceptional temperature stability. The MC1458 is short-circuit protected.

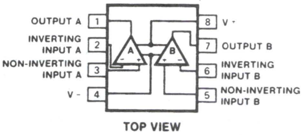
The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short-circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**

PIN CONFIGURATION

D, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	MC1458D
8-Pin Plastic DIP	0 to +70°C	MC1458N
8-Pin Plastic SO	-40°C to +85°C	SA1458D
8-Pin Plastic DIP	-40°C to +85°C	SA1458N
8-Pin Plastic DIP	-55°C to +125°C	MC1558N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage MC1458 SA1458 MC1558	 ±18 ±18 ±22	 V V V
T_J	Junction temperature	+150	°C
P_{MAX}	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] N package D package	 1160 780	 mW mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
	Output short-circuit duration	Continuous	
T_A	Operating ambient temperature range MC1458 SA1458 MC1558	 0 to +70 -40 to +85 -55 to +125	 °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

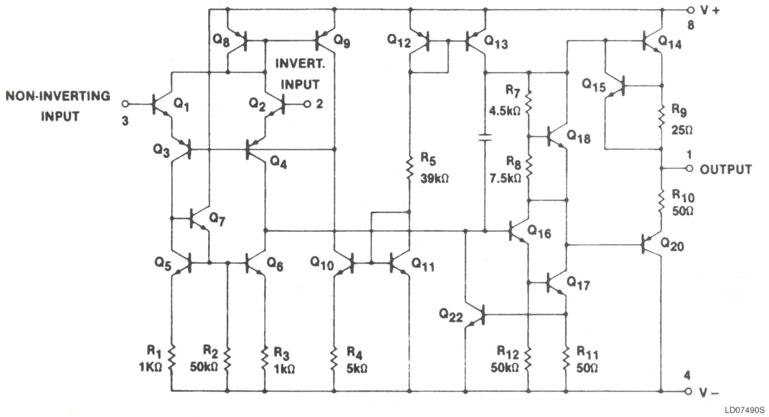
NOTES:

1. The following derating factors should be applied above 25°C:
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

General-Purpose Operational Amplifier

MC/SA1458/MC1558

EQUIVALENT SCHEMATIC


V +
8
Q8
Q9
Q12
Q13
Q14
INVERT. INPUT
NON-INVERTING INPUT
3
Q1
Q2
2
R7
4.5kΩ
Q15
R9
25Ω
Q18
Q3
Q4
R5
39kΩ
R8
7.5kΩ
1
OUTPUT
R10
50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
Q17
Q22
R1
1KΩ
R2
50kΩ
R3
1kΩ
R4
5kΩ
R12
50kΩ
R11
50Ω
4
V −
LD07490S

Amplifier "A" of MC1458, SA1458, MC1558

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0	mV
		$R_S = 10k\Omega$, over temperature			6.0	mV
ΔV_{OS}	Offset voltage	Over temperature		10		μV/°C
I_{OS}	Offset current			20	200	nA
		Over temperature			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10		nA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temperature			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temperature	±12	±14		V
		$R_L = 2k\Omega$, over temperature	±10	±13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2k\Omega, V_O = \pm 10V$	50	100		V/mV
		$R_L = 2k\Omega$, $V_O = \pm$ temperature	20			V/mV
	Offset voltage adjustment range			±30		mV
SVRR	Supply voltage rejection ratio	$R_S \leqslant 10k\Omega$		30	150	μV/V
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		±12	±13		V
P_D	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current		10	26	60	mA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.

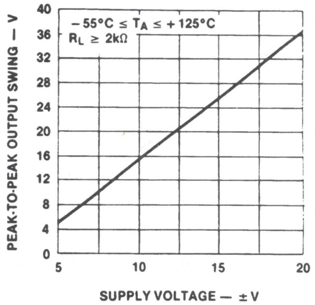
SYMBOL	PARAMETER	TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.			7.5			7.5	mV
ΔV_{OS}	Offset voltage	Over temperature		12			12		µV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temperature			300			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10			0.10		nA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temperature			800			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0			1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
		$R_L = 2k\Omega$, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	25	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, Over temperature	15			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
SVRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	150		30	150	µV/V
CMRR	Common-mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	1		0.3	1		MΩ
P_D	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f = 20Hz	0.3			MΩ
	Common-mode input impedance	f = 20Hz		200		MΩ
	Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0kHz$, f = 1.0kHz		30		$nV/\sqrt{Hz}$
BW	Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD ≤ 5%, $V_{OUT} = 20V_{P-P}$		14		kHz
	Phase margin			65		degrees
A_V	Gain margin			11		dB
	Unity gain crossover frequency	Open loop		1.0		MHz
	Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$				
t_R	Rise time			0.3		µs
	Overshoot			5.0		%
SR	Slew rate	$C \leq 100pF$, $R_L \geq 2k\Omega$, $V_{IN} = \pm 10V$		0.8		V/µs

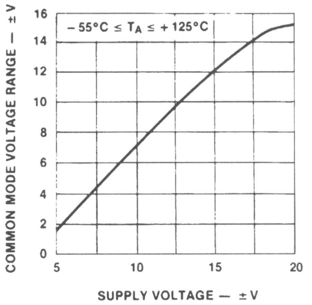
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing as a Function of Supply Voltage



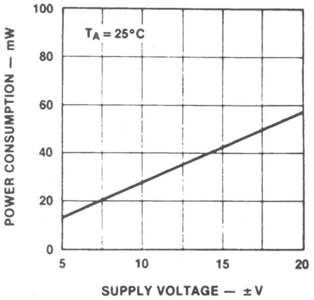
OP13620S

Input Common-Mode Voltage Range as a Function of Supply Voltage



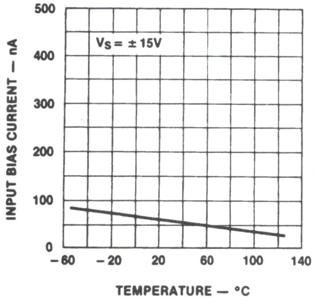
OP13630S

Power Consumption as a Function of Supply Voltage



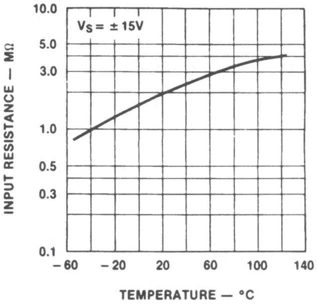
OP13640S

Input Bias Current as a Function of Ambient Temperature



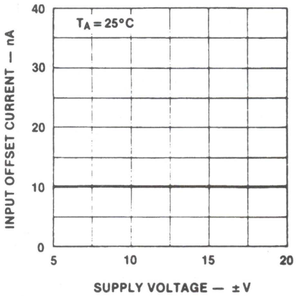
OP13650S

Input Resistance as a Function of Ambient Temperature



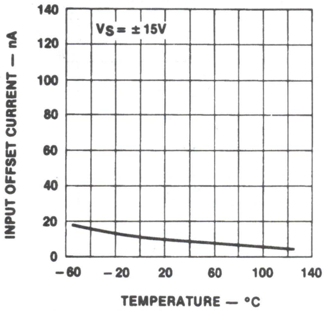
OP13660S

Input Offset Current as a Function of Supply Voltage



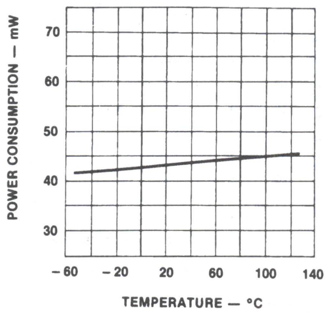
OP13670S

Input Offset Current as a Function of Ambient Temperature



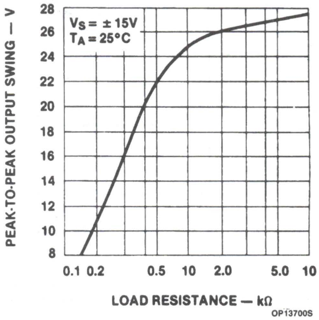
OP13680S

Power Consumption as a Function of Ambient Temperature



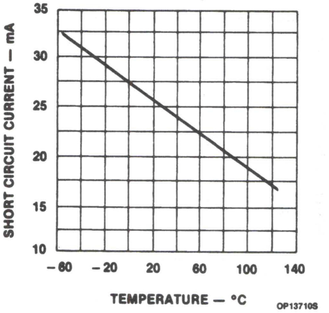
OP13690S

Output Voltage Swing as a Function of Load Resistance

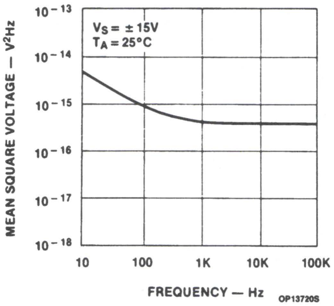


OP13700S

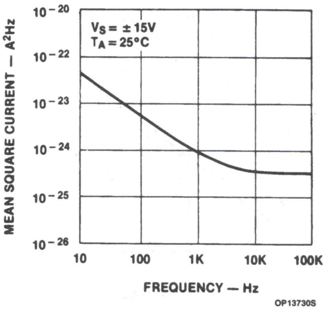
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



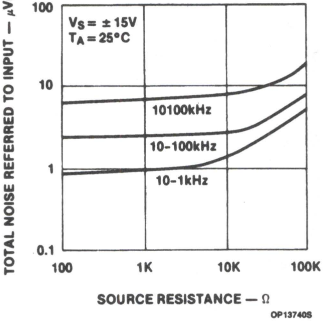
Output Short-Circuit Current as a Function of Ambient Temperature



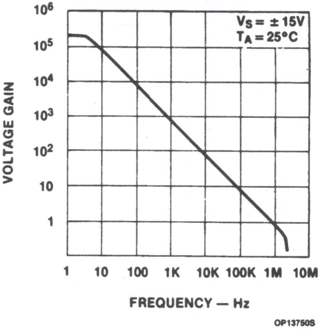
Input Noise Voltage as a Function of Frequency



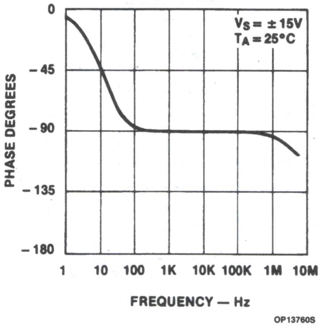
Input Noise Current as a Function of Frequency



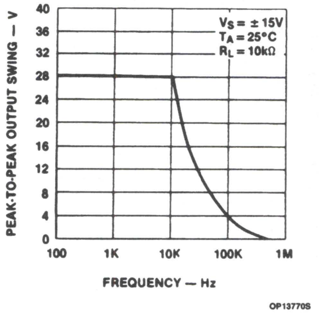
Broadband Noise for Various Bandwidths



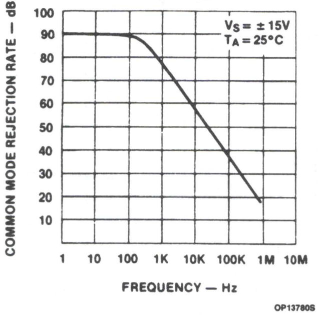
Open-Loop Voltage Gain as a Function of Frequency



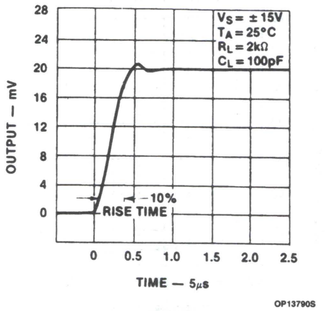
Open-Loop Phase Response as a Function of Frequency



Output Voltage Swing as a Function of Frequency



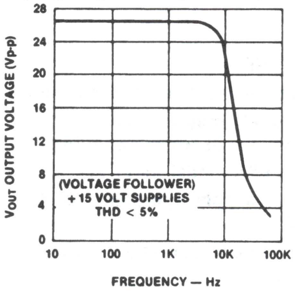
Common-Mode Rejection Ratio as a Function of Frequency



Transient Response

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Power Bandwidth (Large-Signal Swing vs Frequency)



OP13800S

Signetics

MC3303/3403/3503
Quad Low Power Operational Amplifiers

Product Specification

Linear Products

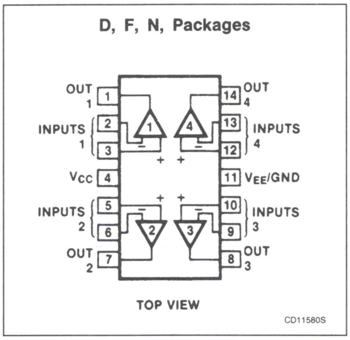
DESCRIPTION

The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 32V. The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

FEATURES

- **Short-circuit protected outputs**
- **Class AB output stage for minimal crossover distortion**
- **True differential input stage**
- **Single supply operation: 3.0 to 32V**
- **Split supply operation: ± 1.5 to ± 16V**
- **Low input bias currents: 500nA max**
- **Four amplifiers per package**
- **Internally compensated**

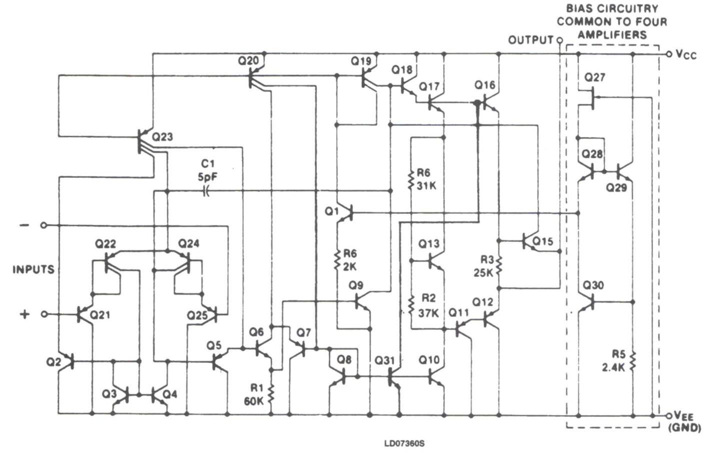
PIN CONFIGURATION

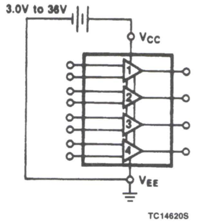

D, F, N, Packages
OUT 1
1
INPUTS 1
2
3
Vcc
4
INPUTS 2
5
6
OUT 2
7
OUT 4
14
13
INPUTS 4
12
11
VEE/GND
10
INPUTS 3
9
OUT 3
8
TOP VIEW
CD11580S

ORDERING INFORMATION

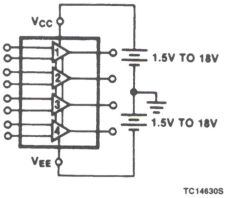
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Ceramic DIP	-40°C to +85°C	MC3303F
14-Pin Plastic DIP	-40°C to +85°C	MC3303N
14-Pin Plastic SO	0 to +70°C	MC3403D
14-Pin Ceramic DIP	0 to +70°C	MC3403F
14-Pin Plastic DIP	0 to +70°C	MC3403N
14-Pin Ceramic DIP	-55°C to +125°C	MC3503F

CIRCUIT SCHEMATIC (1/4 Shown)


BIAS CIRCUITRY COMMON TO FOUR AMPLIFIERS
OUTPUT
Vcc
Q20
Q19
Q18
Q17
Q16
Q27
Q23
C1 5pF
R6 31K
Q28
Q29
Q1
−
INPUTS
+
Q22
Q24
Q21
Q25
R6 2K
Q13
Q15
R3 25K
Q9
R2 37K
Q11
Q12
Q30
Q2
Q5
Q6
Q7
Q8
Q31
Q10
R1 60K
Q3
Q4
R5 2.4K
VEE (GND)
LD07360S


3.0V to 36V
Vcc
1
2
3
4
VEE
TC14620S

Single Supply


Vcc
1
2
3
4
1.5V TO 18V
1.5V TO 18V
VEE
TC14630S

Split Supplies

Quad Low Power Operational Amplifiers

MC3303/3403/3503

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[3]		
V_{CC}	Single supply	36	V_{DC}
V_{CC}	Split supplies	+18	V_{DC}
V_{EE}		−18	V_{DC}
V_{IDR}	Input differential voltage range[1]	±36	V_{DC}
V_{ICR}	Input common-mode voltage range[1, 2]	±18	V_{DC}
P_{MAX}	Maximum power dissipation, $T_A = 25°C$ (still-air)[4]		
	F package	1.20	mW
	D package	1.04	mW
	N package	1.45	mW
T_{STG}	Storage temperature range		
	Ceramic	−65 to +150	°C
	Plastic	−55 to +125	
T_A	Operating ambient temperature range		
	MC3503	−55 to +125	°C
	MC3403	0 to +70	°C
	MC3303	−40 to +85	°C
T_J	Junction temperature	150	°C

NOTES:

1. Split power supplies.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Device not functional for single supply >32V or split supply >±16V.
4. Derate above 25°C at the following rates:
    - F package at 9.5mW/°C
    - D package at 8.7mW/°C
    - N package at 11.6mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +15V$, $V_{EE} = -15V$ for MC3503, MC3403; $V_{CC} = +14V$, $V_{EE} = GND$ for MC3303. $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage			2.0	5.0		2.0	10		2.0	8.0	mV
		$T_A = T_{HIGH}$ to T_{LOW}			6.0			12			10	
I_{IO}	Input offset current			10	50		10	50		30	75	nA
		$T_A = T_{HIGH}$ to T_{LOW}			200		200		250			
A_{VOL}	Large-signal open-loop voltage gain	$V_O = \pm 10V$,	50	200		20	200		20	200		V/mV
		$V_O = \pm 10V$ $R_L = 2.0k\Omega$	50	200		20			20			
		$T_A = T_{HIGH}$ to T_{LOW}	25	300		15			15			
I_{BIAS}	Input bias current	$T_A = T_{HIGH}$ to T_{LOW}		−30	−500		−30	−500		−30	−500	nA
				−40	−1200			−800			−1000	
Z_O	Output impedance	f = 20Hz		75			75			75		Ω
Z_I	Input impedance	f = 20Hz	0.3	1.0		0.3	1.0		0.3	1.0		MΩ
V_{OR}	Output voltage range	$R_L = 10k\Omega$	±12	±13.5		±12	±13.5		+12	+12.5		V
		$R_L = 2.0k\Omega$	±10	±13		±10	±13		+10	+12		
		$R_L = 2.0k\Omega$ $T_A = T_{HIGH}$ to T_{LOW}	±10			±10			+10			

Quad Low Power Operational Amplifiers MC3303/3403/3503

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = +15V$, $V_{EE} = -15V$ for MC3503, MC3403; $V_{CC} = +14V$, $V_{EE} = GND$ for MC3303. $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ICR}	Input common-mode voltage range		+13 $-V_{EE}$	+13.5 $-V_{EE}$		+13 $-V_{EE}$	+13.5 $-V_{EE}$		+12 $-V_{EE}$	+12.5 $-V_{EE}$		V
CMRR	Common-mode rejection ratio	$R_S \leqslant 10k\Omega$	70	90		70	90		70	90		dB
I_{CC}, I_{EE}	Power supply current ($V_O = 0$)	$R_L = \infty$		25	4.0		2.5	7.0		2.5	7.0	mA
$\Delta I_B/\Delta T$		$T_A = T_{HIGH}$ to T_{LOW}		3.5	5		3.5	7		3.5	7	mA
$I_{OS}\pm$	Individual output short-circuit current[2]		±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
PSSR+	Positive power supply rejection ratio			30	150		30	150		30	150	μV/V
PSSR−	Negative power supply rejection ratio			30	150		30	150				μV/V
$\Delta I_B/\Delta T$		$T_A = T_{HIGH}$ to T_{LOW}		50			50			50		pA/°C
$\Delta I_{IO}/\Delta T$	Average temperature coefficient of input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}		50			50			50		pA/°C
$\Delta V_{IO}/\Delta T$	Average temperature coefficient of input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}		10			10			10		μV/°C
BW_P	Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, $V_O = 20V_{P-P}$ THD = 5%		9.0			9.0			9.0		kHz
BW	Small-signal bandwidth	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$		1.0			1.0			1.0		MHz
SR	Slew rate	$A_V = 1$, $V_I = -10V$ to $+10V$		0.6			0.6			0.6		V/μs
t_{TLH}	Rise time	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$		0.35			0.35			0.35		μs
t_{THL}	Fall time	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$		0.35			0.35			0.35		μs
OS	Overshoot	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$		20			20			20		%
θm	Phase margin	$A_V = 1$, $R_L = 2.0k\Omega$, $C_L = 200pF$		50			50			50		°
	Crossover distortion	$V_{IN} = 30mV_{P-P}$, $V_{OUT} = 2.0V_{P-P}$, f = 10kHz		1.0			1.0			1.0		%

DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V$, $V_E = GND$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage			2.0	5.0		2.0	10			10	mV
I_{IO}	Input offset current			30	50		30	50			75	nA
I_{BIAS}	Input bias current			−200	−500		−200	−500			−500	nA
A_{VOL}	Large-signal open-loop voltage gain	$R_L = 2.0k\Omega$	10	200		10	200		10	200		V/mV
PSRR	Power supply rejection ratio				150			150			150	μV/V
V_{OR}	Output voltage range[3]	$R_L = 10k\Omega$, $V_{CC} = 5.0V$ $R_L = 10k\Omega$, $5.0V \leqslant V_{CC} \leqslant 30V$	3.3 V_{CC} −1.7	3.5 V_{CC} −1.5		3.3 V_{CC} −1.7	3.5 V_{CC} −1.5		3.3 V_{CC} −1.7	3.5 V_{CC} −1.5		V_{P-P}
I_{CC}	Power supply current			2.5	4.0		2.5	7.0		2.5	7.0	mA
	Channel separation	f = 1.0kHz to 20kHz (input referenced)		−120			−120			−120		dB

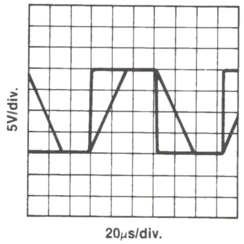
NOTES:

1. $T_{HIGH} = 125°C$ for MC3503, 70°C for MC3303. $T_{LOW} = -55°C$ for MC3503, 0°C for MC3403, −40°C for MC3303.
2. Not to exceed maximum package power dissipation.
3. Output will swing to ground.

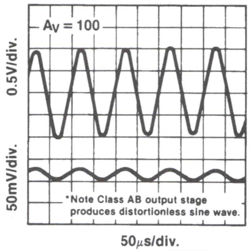
Quad Low Power Operational Amplifiers MC3303/3403/3503

TYPICAL PERFORMANCE CHARACTERISTICS

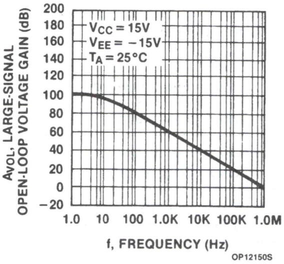
Inverter Pulse Response



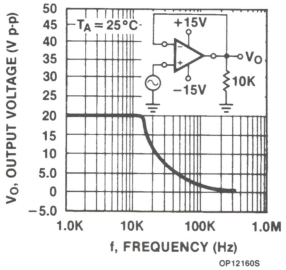
Sine Wave Response



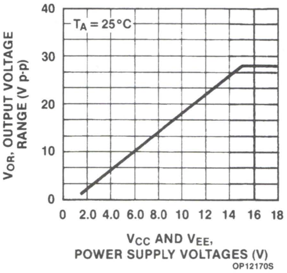
Open-Loop Frequency Response



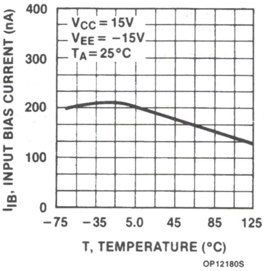
Power Bandwidth



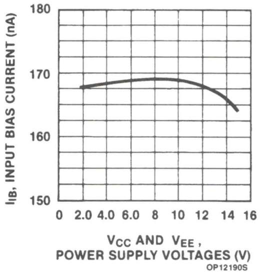
Output Swing vs Supply Voltage



Input Bias Current vs Temperature



Input Bias Current vs Supply Voltage



Signetics

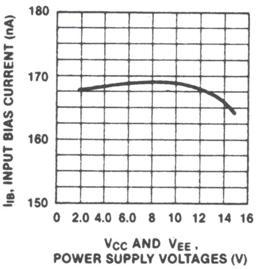
AN160
Applications for the MC3403

Application Note

Linear Products

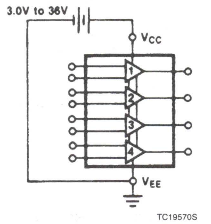
MC3403 DESCRIPTION

The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular µA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 36V. The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.



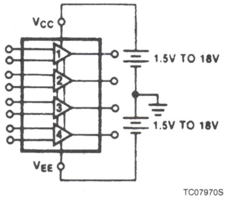
OP03210S

Input Bias Current vs Supply Voltage


3.0V to 36V
V_CC
1
2
3
4
V_EE

TC19570S

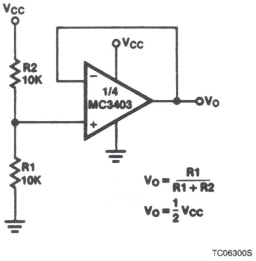
Single Supply


V_CC
1
2
3
4
1.5V TO 18V
1.5V TO 18V
V_EE

TC07970S

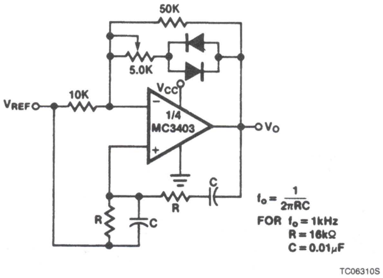
Split Supplies

APPLICATIONS


V_CC
V_CC
R2 10K
R1 10K
1/4 MC3403
V_O
V_O = R1 / (R1 + R2)
V_O = 1/2 V_CC

TC06300S

Voltage Reference


50K
5.0K
V_CC
10K
V_REF
1/4 MC3403
V_O
R
C
R
C
f_o = 1 / 2πRC
FOR f_o = 1kHz
R = 16kΩ
C = 0.01µF

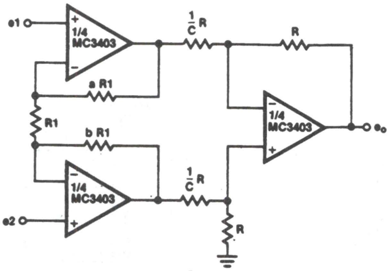
TC06310S

Wein Bridge Oscillator

Applications for the MC3403

AN160

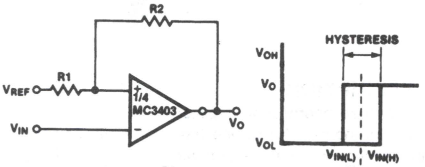
APPLICATIONS (Continued)


e1
+
1/4 MC3403
−
$\frac{1}{C}$R
R
a R1
R1
b R1
1/4 MC3403
−
+
e₀
1/4 MC3403
$\frac{1}{C}$R
R
e2

$e_o = C(1 + a + b)(e2 - e1)$

TC06320S

High Impedance Differential Amplifier


R2
R1
VREF
VIN
+
1/4 MC3403
−
VO
VOH
VO
VOL
HYSTERESIS
VIN(L)
VIN(H)
VREF

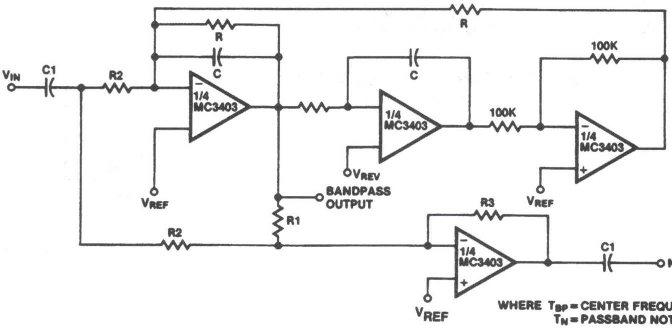
$V_{IN(L)} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$

$V_{IN(H)} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

TC06330S

Comparator With Hysteresis


R
R
C
VIN
C1
R2
1/4 MC3403
C
1/4 MC3403
VREV
100K
100K
1/4 MC3403
VREF
BANDPASS OUTPUT
R1
R3
VREF
R2
1/4 MC3403
C1
NOTCH OUTPUT
VREF

$f_o = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$

$C1 = 10C$

$V_{REF} = \frac{1}{2} V_{CC}$

FOR $f_o = 1kHz$

$Q = 10$

$T_{BP} = 1$

$T_N = 1$

R = 160kΩ

C = 0.001μF

R1 = 1.6MΩ

R2 = 1.6MΩ

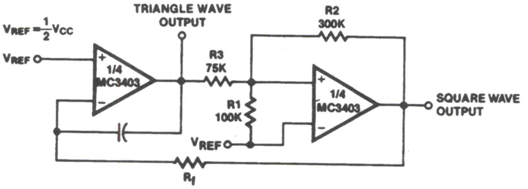
R3 = 1.6MΩ

WHERE T_{BP} = CENTER FREQUENCY GAIN

T_N = PASSBAND NOTCH GAIN

TC06340S

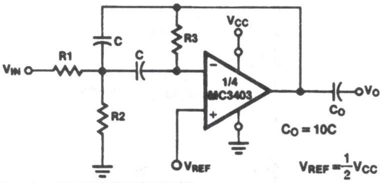
Bi-Quad Filter


VREF = ½VCC
VREF
1/4 MC3403
TRIANGLE WAVE OUTPUT
R3 75K
R2 300K
R1 100K
1/4 MC3403
SQUARE WAVE OUTPUT
VREF
Rf

$f = \frac{R1 + R_C}{4CR_f\,R1}$ IF $R3 = \frac{R2\,R1}{R2 + R1}$

TC06350S

Function Generator


VCC
C
R3
VIN
R1
C
1/4 MC3403
Vo
Co
R2
VREF
Co = 10C
VREF = ½VCC

GIVEN f_o = CENTER FREQUENCY

$A(f_o)$ = GAIN AT CENTER FREQUENCY

CHOOSE VALUE f_o, C

THEN:

$R3 = \frac{Q}{\pi f_o C}$

$R1 = \frac{R3}{2\,A(f_o)}$

$R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$

FOR LESS THAN 10% ERROR FROM OPERATIONAL AMPLIFIER

$\frac{Q_o\,f_o}{BW} < 0.1$ WHERE f_o AND BW ARE EXPRESSED IN Hz.

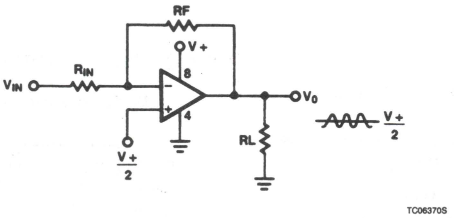
IF SOURCE IMPEDANCE VARIES, FILTER MAY BE PRECEDED WITH VOLTAGE FOLLOWER BUFFER TO STABILIZE FILTER PARAMETERS.

TC06360S

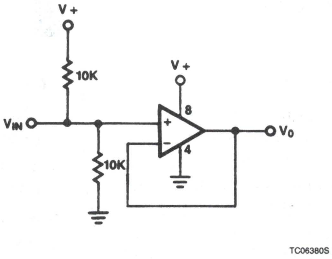
Multiple Feedback Bandpass Filter

Applications for the MC3403 AN160

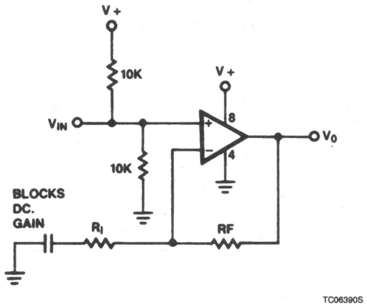
TYPICAL APPLICATIONS


RF
V+
R_IN
V_IN
8
4
V_O
RL
V+/2
V+/2
TC06370S

Single Supply Inverting Amplifier


V+
10K
V+
V_IN
8
4
V_O
10K
TC06380S

Input Biasing Voltage-Follower


V+
10K
V+
V_IN
8
4
V_O
10K
BLOCKS
DC.
GAIN
R_I
RF
TC06390S

Non-Inverting Amplifier

Signetics

Linear Products

NE/SA/SE4558
Dual General-Purpose Operational Amplifier

Product Specification

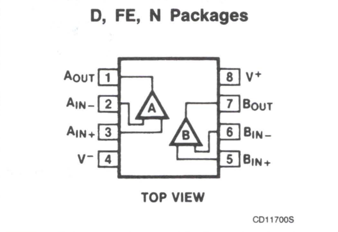
DESCRIPTION

The 4558 is a dual operational amplifier that is internally compensated. Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The NE/SA/SE4558 is a pin-for-pin replacement for the RC/RM/RV4558.

FEATURES

- **2MHz unity gain bandwidth guaranteed**
- **Supply voltage ±22V for SE4558 and ±18V for NE4558**
- **Short-circuit protection**
- **No frequency compensation required**
- **No latch-up**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**

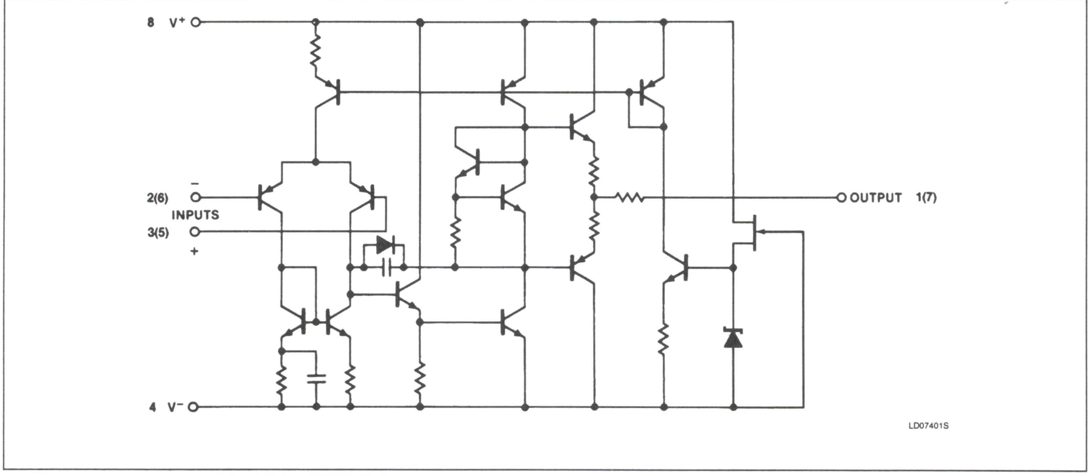
PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE4558D
8-Pin Ceramic DIP	0 to +70°C	NE4558FE
8-Pin Plastic DIP	0 to +70°C	NE4558N
8-Pin Plastic DIP	−40°C to +85°C	SA4558N
8-Pin Ceramic DIP	−40°C to +85°C	SA4558FE
8-Pin Ceramic DIP	−55°C to +125°C	SE4558FE

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE4558	±22	V
	NE4558, SA4558	±18	V
P_D	Maximum power dissipation		
	$T_A = 25°C$ (Still air)[1]		
	F package	780	mW
	N package	1160	mW
	D package	780	mW
	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range		
	SE4558	−55 to +125	°C
	SA4558	−40 to +85	°C
	NE4558	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	Indefinite	

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for NE4558 and to +85°C ambient temperature for SA4558.

DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

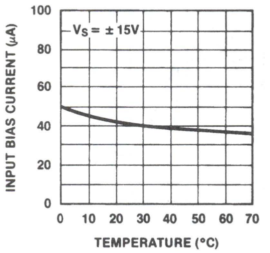
SYMBOL	PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leqslant 10k\Omega$		1.0	5.0		2.0	6.0	mV
	$\Delta V_{OS}/\Delta T$	Over temp.		4			4		μV/°C
I_{OS}	Input offset current			50	200		30	200	nA
	$\Delta I_{OS}/\Delta T$	Over temp.		20			20		pA/°C
I_{BIAS}	Input bias current			40	500		200	500	nA
	$\Delta I_B/\Delta T$	Over temp.		40			40		pA/°C
R_{IN}	Input resistance		0.3	1.0		0.3	1.0		MΩ
A_V	Large-signal voltage gain	$R_L \geqslant 2k\Omega$ $V_{OUT} = \pm 10V$	50,000	300,000		20,000	300,000		V/V
	Output voltage swing	$R_L \geqslant 10k\Omega$ $R_L \geqslant 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V
V_{IN}	Input voltage range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio	$R_S \leqslant 10k\Omega$	70	100		70	100		dB
SVRR	Supply voltage rejection ratio	$R_S \leqslant 10k\Omega$		10	150		10	150	μV/V
	Power consumption (all amplifiers)	$R_L =$ •		100	170		100	170	mW
	Transient response (unity gain)	$V_{IN} = 20mV$ $R_L = 2k\Omega$ $C_L \leqslant 100pF$							
t_R	Rise time Overshoot			100 15.0			100 15.0		ns %
SR	Slew rate (unity gain)	$R_L \geqslant 2k\Omega$		1.0			1.0		V/μs
	Channel separation (gain = 100)	f = 10kHz $R_S = 1k\Omega$		90			90		dB
BW	Unity gain bandwidth (gain = 1)		2.0	3.0		2.0	3.0		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degree
V_{NOISE}	Input noise voltage	f = 1kΩ		25			25		$nV/\sqrt{Hz}$
I_{SC}	Short-circuit current	$T_A = 25°C$	5	25	60	5	25	60	mA
NOTE: The following specifications apply over operating temperature range.									
V_{OS}	Input offset voltage	$R_S \leqslant 10k\Omega$			6.0			7.5	mV
I_{OS}	Input offset current				500			300/500[1]	nA
I_{BIAS}	Input bias current				1500			800/1500[1]	nA
A_V	Large-signal voltage gain	$R_L \geqslant 2k\Omega$ $V_{OUT} = \pm 10$	25,000			15,000			V/V
	Output voltage swing	$R_L \geqslant 2k\Omega$	±10			±10			V
P_C	Power consumption	$V_S = \pm 15V$ T_A = HIGH T_A = LOW		90 120	150 200		90 120	150 200	mW

NOTE:

1. SA4558 only.

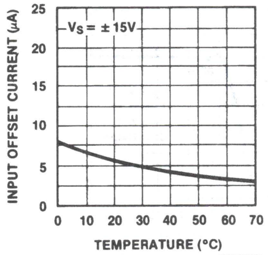
TYPICAL PERFORMANCE CURVES

Input Bias Current as a Function of Ambient Temperature



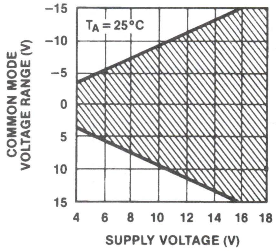
OP12430S

Input Offset Current as a Function of Ambient Temperature



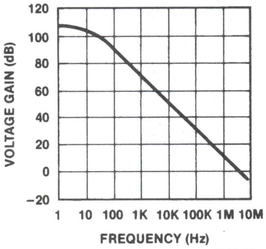
OP12440S

Common-Mode Range as a Function of Supply Voltage



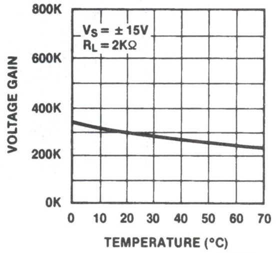
OP12450S

Open-Loop Voltage Gain as a Function of Frequency



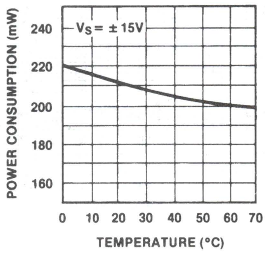
OP12460S

Open-Loop Gain as a Function of Temperature



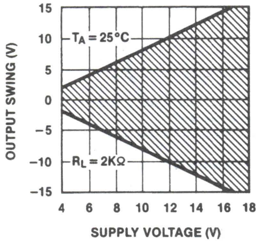
OP12470S

Power Consumption as a Function of Ambient Temperature



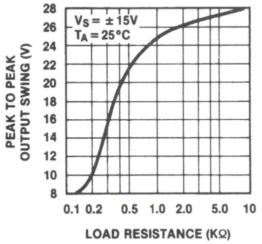
OP12480S

Typical Output Voltage as a Function of Supply Voltage



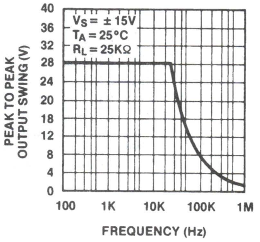
OP12490S

Output Voltage Swing as a Function of Load Resistance



OP12500S

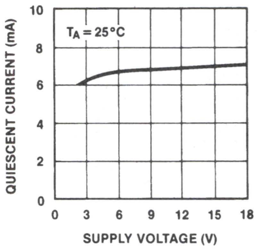
Output Voltage Swing as a Function of Frequency



OP12510S

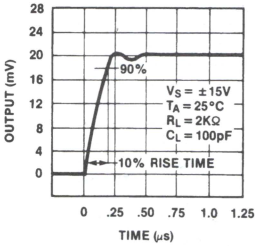
TYPICAL PERFORMANCE CURVES (Continued)

Quiescent Current as a Function of Supply Voltage



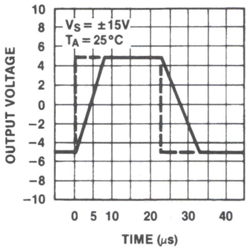
OP12520S

Transient Response



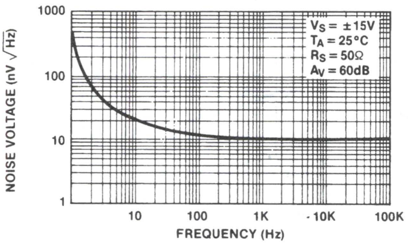
OP12530S

Voltage-Follower Large-Signal Pulse Response



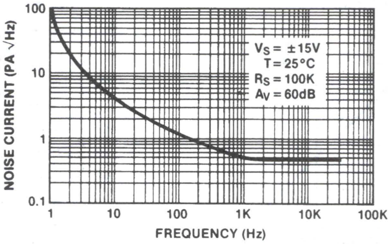
OP12540S

Input Noise Voltage as a Function of Frequency



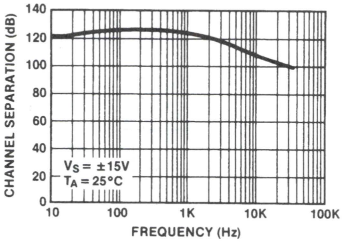
OP12550S

Input Noise Current as a Function of Frequency



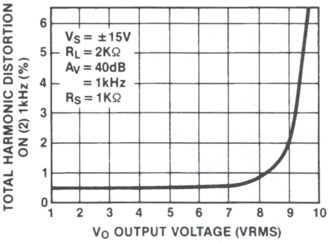
OP12560S

Channel Separation



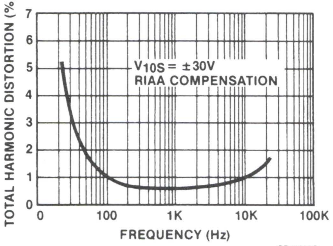
OP12570S

Total Harmonic Distortion vs Output Voltage



OP12580S

Distortion vs Frequency $V_O = 1V_{RMS}$



OP12590S

Signetics

NE/SE530
High Slew Rate Operational Amplifier

Product Specification

Linear Products

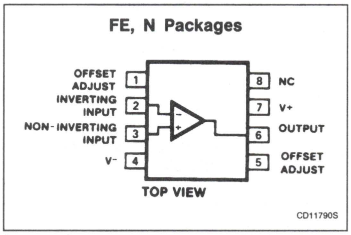
DESCRIPTION

The 530 is a new generation operational amplifier featuring a high slew rate combined with improved input characteristics. Internally compensated, the SE530 guarantees slew rates of 25V/μs with 2mV typical offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741 and LF356 types.

FEATURES

- **Gain bandwidth product — 3MHz**
- **35V/μs slew rate (gain = −1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV max.**
- **Low input bias current — 60nA max.**
- **Short-circuit protection**
- **Offset null capability**
- **Large common-mode and differential voltage ranges**

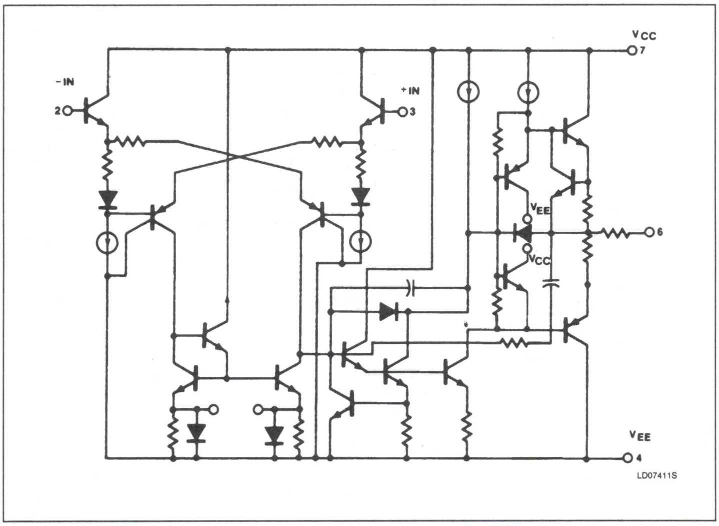
PIN CONFIGURATION


FE, N Packages
OFFSET ADJUST
1
INVERTING INPUT
2
NON-INVERTING INPUT
3
V−
4
8
NC
7
V+
6
OUTPUT
5
OFFSET ADJUST
−
+
TOP VIEW
CD11790S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE530N
8-Pin Ceramic DIP	0 to +70°C	NE530FE
8-Pin Plastic DIP	−55°C to +125°C	SE530N
8-Pin Ceramic DIP	−55°C to +125°C	SE530FE

EQUIVALENT SCHEMATIC EACH AMPLIFIER


VCC
7
−IN
2
+IN
3
VEE
VCC
6
VEE
4
LD07411S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE530	±22	V
	NE530	±18	V
P_D	Maximum power dissipation $T_A = 25°C$ (still air)[1]		
	F package	780	mW
	N package	1160	mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage	±15	V
T_A	Operating temperature range		
	SE530	−55 to +125	°C
	NE530	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
I_{SC}	Output short circuit	Indefinite	

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.

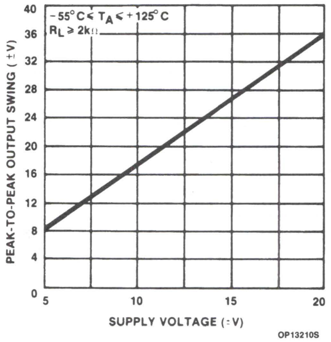
SYMBOL	PARAMETER	TEST CONDITIONS	SE530			NE530			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
		Over temperature			5.0			7.0	mV
ΔV_{OS}	Temperature coefficient of input offset voltage	Over temperature		3	15		6		µV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temperature			40			80	nA
ΔI_{OS}	Input offset current	Over temperature		25			40		pA/°C
I_{BIAS}	Input bias current			45	80		65	150	nA
		Over temperature			200			200	nA
ΔI_{BIAS}	Input current	Over temperature		50			80		pA/°C
R_{IN}	Input resistance		3	10		1	6		MΩ
V_{CM}	Input common mode voltage range		±12	±13		±12	±13		V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	200		50	200		V/mV
		Over temperature	25			25			V/mV
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
I_{SC}	Output short-circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω
I_{CC}	Supply current	Each amplifier		2.0	3.0		2.0	3.0	mA
		Over temperature		2.2	3.6		2.2		mA
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$ Over temperature	70	90		70	90		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$ Over temperature		30	150		30	150	µV/V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.

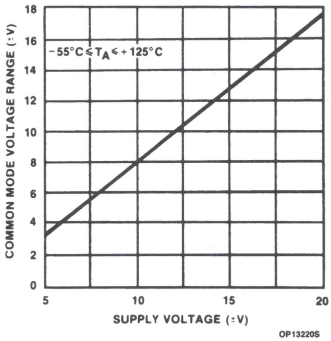
SYMBOL	PARAMETER	TEST CONDITIONS	SE530			NE530			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Transient Response								
t_R	Small-signal rise time			0.06			0.06		μs
	Small-signal overshoot			13			13		%
t_S	Settling time	To 0.1% (10V step)		0.9			0.9		μs
SR	Slew rate	±15V supply, $V_O = \pm 10V$, $R_L \geqslant 2k\Omega$							
	Unity gain inverting		25	35		20	35		V/μs
	Unity gain non-inverting		18	25		12	25		V/μs
BW	Power bandwidth	5% THD, $V_O = \pm 10V$, $R_L \geqslant 2k\Omega$	360	500		280	500		kHz
	Small-signal bandwidth	Open-loop		3			3		MHz
V_{NOISE}	Input noise voltage	f = 1kHz		30			30		$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

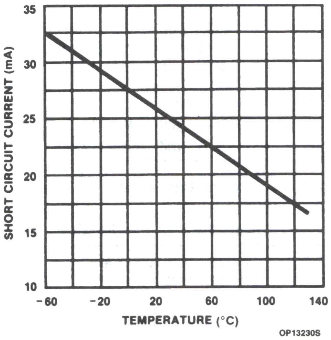
Output Voltage Swing as a Function of Supply Voltage



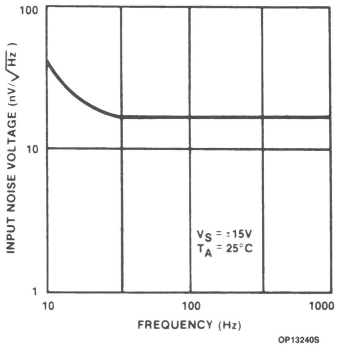
Input Common-Mode Voltage Range as a Function of Supply Voltage



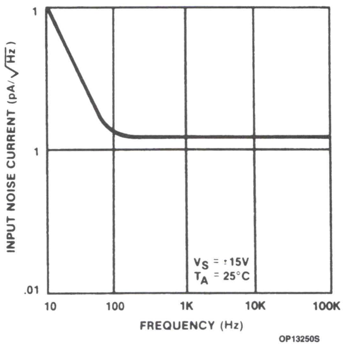
Output Short-Circuit Current as a Function of Ambient Temperature



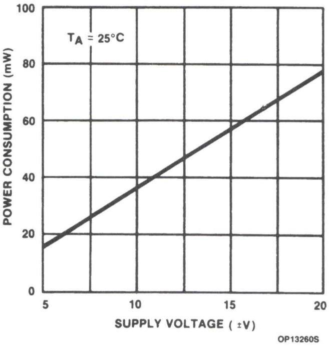
Input Noise Voltage as a Function of Frequency



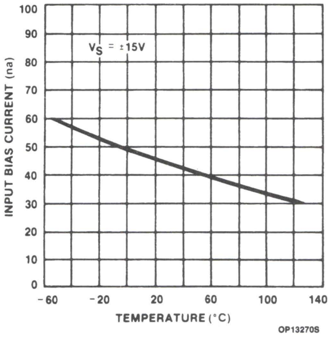
Input Noise Current as a Function of Frequency



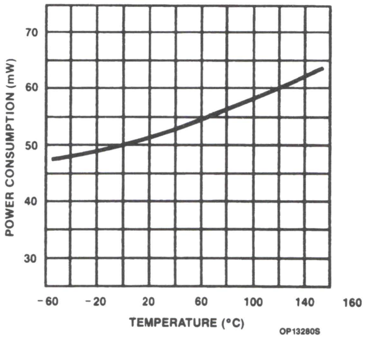
Power Consumption as a Function of Supply Voltage (Each Amplifier)



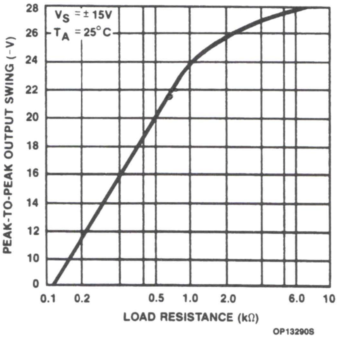
Input Bias Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature (Each Amplifier)

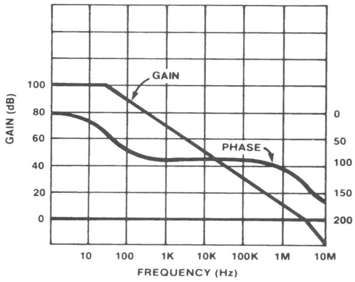


Output Voltage Swing as a Function of Load Resistance



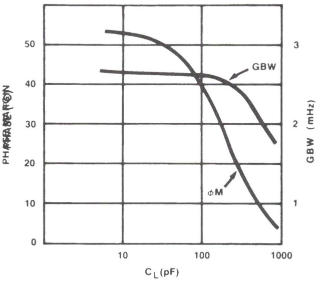
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE530 Open-Loop Gain and Phase vs Frequency



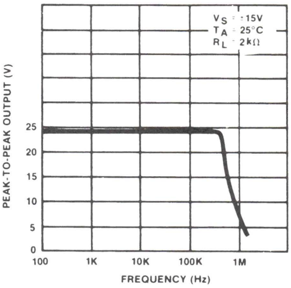
OP13300S

Gain Bandwidth Product and Phase Margin vs Load Capacity



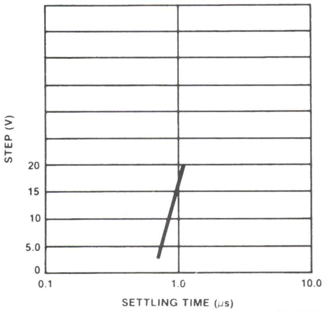
OP13310S

Power Bandwidth



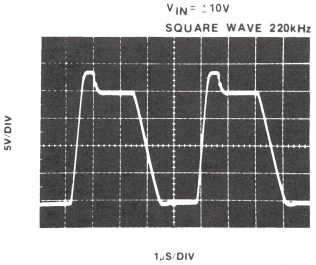
OP13320S

Input Voltage Step vs Settling Time to 10mV



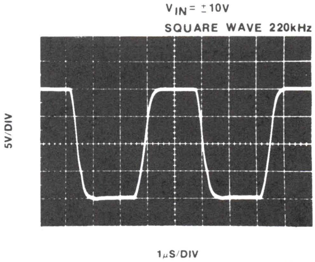
OP13330S

Slew Rate — Voltage-Follower



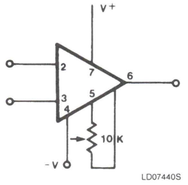
OP13340S

Slew Rate (−1 Amplifier)



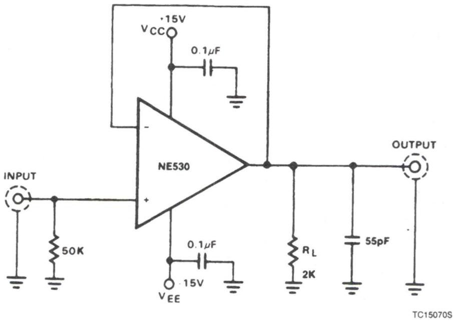
OP13350S

TYPICAL CIRCUIT CONNECTION



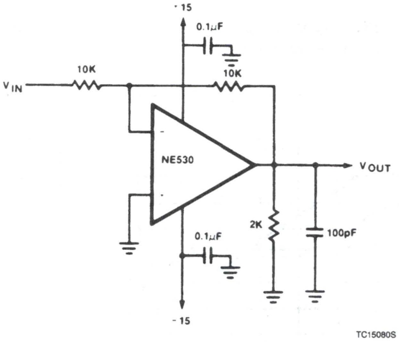
Offset Adjust Circuit

TEST LOAD CIRCUITS

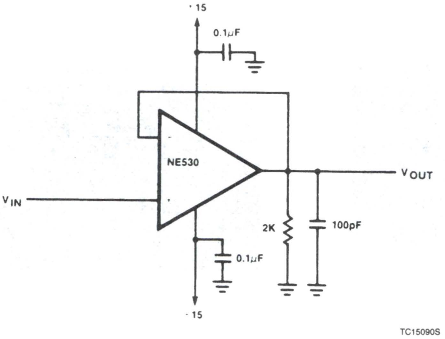

+15V
VCC
0.1µF
NE530
INPUT
50K
0.1µF
15V
VEE
RL
2K
55pF
OUTPUT
TC15070S

NOTES:
Pins not shown are not connected.
All resistor values are typical and in ohms.

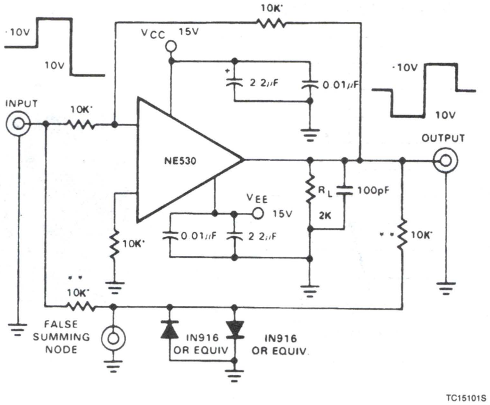
Slew Rate and Settling Time


+15
0.1µF
10K
VIN
10K
NE530
VOUT
0.1µF
2K
100pF
- 15
TC15080S

High Slew Rate — Inverting Amplifier


+15
0.1µF
NE530
VIN
VOUT
2K
100pF
0.1µF
- 15
TC15090S

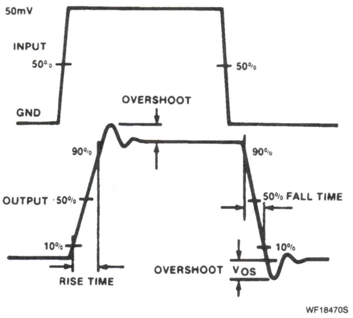
High Slew Rate — Voltage-Follower


+10V
10V
10K*
VCC 15V
2.2µF
0.01µF
-10V
10V
INPUT
10K*
OUTPUT
NE530
RL
100pF
VEE
15V
2K
0.01µF
2.2µF
10K*
**10K*
**
10K*
FALSE SUMMING NODE
IN916 OR EQUIV
IN916 OR EQUIV
TC15101S

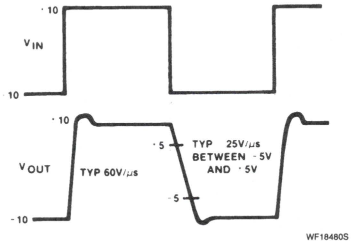
NOTES:
Pins not shown are not connected.
All resistor values are typical and in ohms.
*Match to within 0.01%.
**Open for slew rate.

Testing Slew Rate and Settling Time

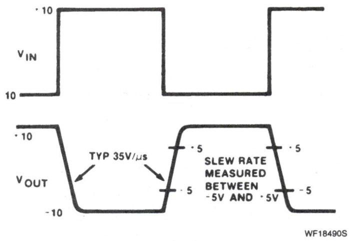
VOLTAGE WAVEFORMS


50mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT 50%
50% FALL TIME
10%
10%
RISE TIME
OVERSHOOT
V_{OS}
WF18470S

Small-Signal Transient Response Definitions


+10
V_{IN}
10
+10
V_{OUT}
TYP 60V/µs
+5
TYP 25V/µs
BETWEEN -5V
AND +5V
-5
-10
WF18480S

Slew Rate — Voltage-Follower


+10
V_{IN}
10
+10
V_{OUT}
TYP 35V/µs
+5
-5
SLEW RATE
MEASURED
BETWEEN
-5V AND +5V
+5
-5
-10
WF18490S

Slew Rate — Inverting Amplifier

Signetics

Linear Products

NE/SE531
High Slew Rate Operational Amplifier

Product Specification

DESCRIPTION

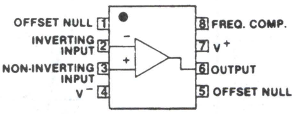
The 531 is a fast slewing high performance operational amplifier which retains DC performance equal to the best general purpose types while providing far superior large-signal AC performance. A unique input stage design allows the amplifier to have a large-signal response nearly identical to its small-signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large-signal bandwidths are required, the amplifier out-performs conventional designs which have much better small-signal response. Also, because the small-signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation, and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μs slew rate at unity gain**
- **Pin-for-pin replacement for μA709, μA748, or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small-signal bandwidth 1MHz**
- **Large-signal bandwidth 500kHz**
- **True op amp DC characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications**

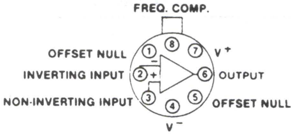
PIN CONFIGURATIONS

N, FE Packages



CD11770S

H Package[1]



CD11780S

NOTE:

1. Metal cans (H) not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

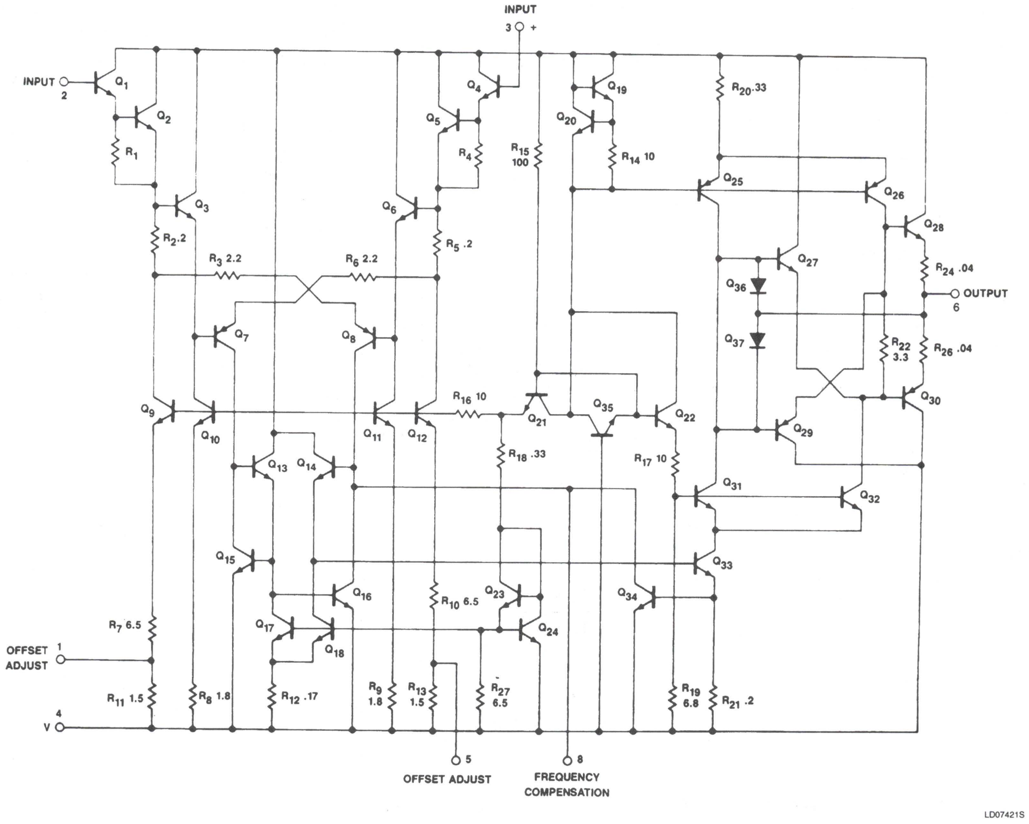
SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
P_{MAX}	Maximum power dissipation T_A = 25°C (still-air)[1] FE package N package H package	 780 1160 830	 mW mW mW
	Differential input voltage	±15	V
V_{CM}	Common-mode input voltage[2]	±15	V
	Voltage between offset null and V−	±0.5	V
T_A	Operating ambient temperature range NE531 SE531	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	indefinite	

NOTES:

1. The following derating factors should be applied above 25°C:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   H package at 6.7mW/°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

High Slew Rate Operational Amplifier NE/SE531

EQUIVALENT SCHEMATIC


INPUT
3 +
INPUT 2
Q1
Q2
R1
Q3
R2 .2
R3 2.2
R6 2.2
Q4
Q5
R4
Q6
R5 .2
Q7
Q8
Q9
Q10
Q11
Q12
R16 10
R15 100
Q19
Q20
R14 10
R20 .33
Q25
Q26
Q27
Q28
R24 .04
OUTPUT 6
Q36
Q37
R22 3.3
R26 .04
Q21
Q35
Q22
Q29
Q30
R18 .33
R17 10
Q13
Q14
Q31
Q32
Q15
Q33
Q16
R10 6.5
Q23
Q34
Q17
Q18
Q24
R7 6.5
OFFSET ADJUST 1
R11 1.5
R8 1.8
R12 .17
R9 1.8
R13 1.5
R27 6.5
R19 6.8
R21 .2
4 V
5 OFFSET ADJUST
8 FREQUENCY COMPENSATION
LD07421S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE531N
8-Pin Ceramic DIP	0 to +70°C	NE531FE
8-Pin Metal Can	0 to +70°C	NE531H
8-Pin Plastic DIP	−55°C to +125°C	SE531N
8-Pin Ceramic DIP	−55°C to +125°C	SE531FE
8-Pin Metal Can	−55°C to +125°C	SE531H

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE531			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp			6.0			7.5	mV
ΔV_{OS}		Over temp		10			10		μV/°C
I_{OS}	Offset current	$T_A = 25°C$		30	200		50	200	nA
		$T_A = High$			200			200	nA
		$T_A = Low$			500			300	nA
ΔI_{OS}		Over temp		0.4			0.4		nA/°C
I_{BIAS}	Input bias current	$T = 25°C$		300	500		400	1500	nA
		$T_A = High$			500			1500	nA
		$T_A = Low$			1500			2000	nA
ΔI_{BIAS}		Over temp		2			2		nA/°C
V_{CM}	Common-mode voltage range	$T_A = 25°C$	±10			±10			V
CMRR	Common-mode rejection ratio	$T_A = 25°C$, $R_S \leq 10k\Omega$				70	100		dB
		Over temp $R_S \leq 10k\Omega$	70	90					dB
R_{IN}	Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	$T_A = 25°C$			7.0			10	mA
		T_{MAX}			7.0			10	mA
P_D	Power consumption	$T_A = 25°C$			210			300	mW
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp		10	150				μV/V
R_{OUT}	Output resistance	$T_A = 25°C$		75			75		Ω
		$T_A = 25°C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$	50	100		20	60		V/mV
A_{VOL}	Large-signal voltage gain	$R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	25			15			V/mV
V_{INN}	Input noise voltage	25°C, f = 1kHz		20			20		$nV/\sqrt{Hz}$
I_{SC}	Short-circuit current	25°C	5	15	45	5	15	45	mA

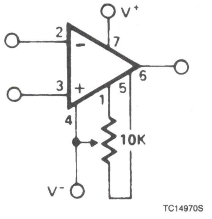
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1]

SYMBOL	PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Full power bandwidth			500			500		kHz
t_S	Settling time (1%)	$A_V = +1$, $V_{IN} = \pm 10V$		1.5			1.5		μs
	(0.1%)			2.5			2.5		μs
	Large-signal overshoot	$A_V = +1$, $V_{IN} = \pm 10V$		2			2		%
	Small-signal overshoot	$A_V = +1$, $V_{IN} = 400mV$		5			5		%
t_R	Small-signal rise time	$A_V = +1$, $V_{IN} = 400mV$		300			300		ns
SR	Slew rate	$A_V = 100$		35			35		V/μs
		$A_V = 10$		35			35		V/μs
		$A_V = 1$ (non-inverting)		30		20	30		V/μs
		$A_V = 1$ (inverting)		35		25	35		V/μs

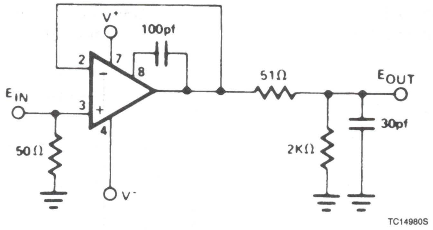
NOTE:

1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

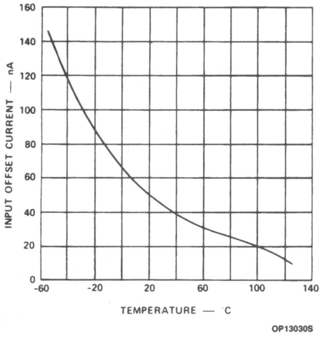

V⁺
2
7
3
6
5
1
4
10K
V⁻
TC14970S

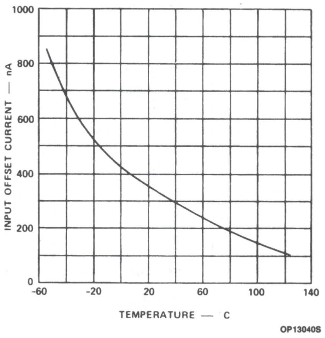
Offset Null Circuit

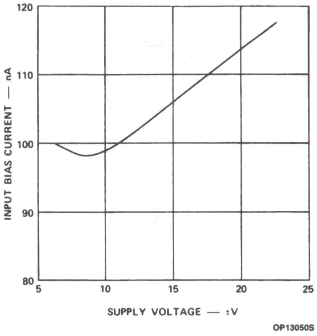

V⁺
100pf
2
7
8
3
4
E_IN
50Ω
V⁻
51Ω
E_OUT
2KΩ
30pf
TC14980S

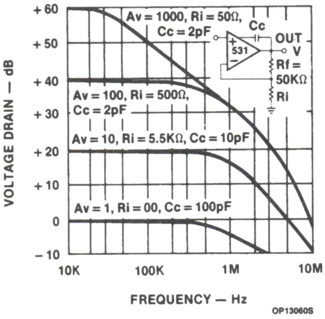
Transient Response Circuit

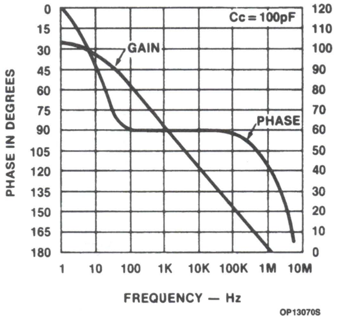
TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.

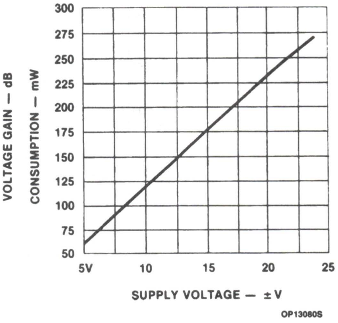

Input Offset Current as a Function of Ambient Temperature


Input Bias Current as a Function of Ambient Temperature


Input Bias Current as a Function of Supply Voltage

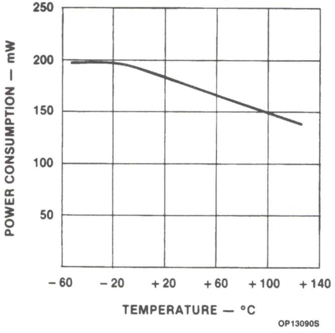

Closed-Loop Non-Inverting Voltage Gain as a Function of Frequency


Open-Loop Phase Response and Voltage Gain as a Function of Frequency

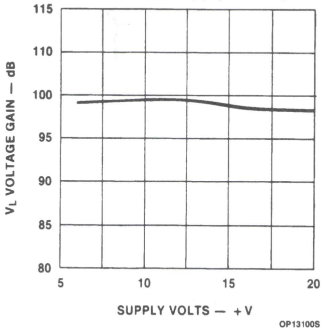

Power Consumption as a Function of Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued) $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.

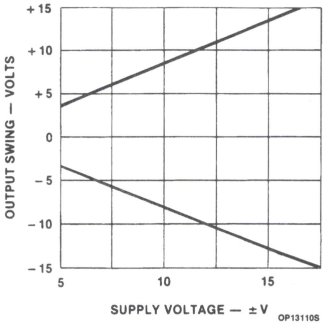
Power Consumption as a Function of Ambient Temperature



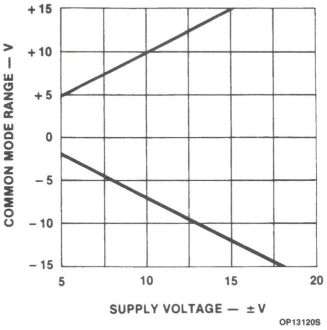
Open-Loop Voltage Gain as a Function of Supply Voltage



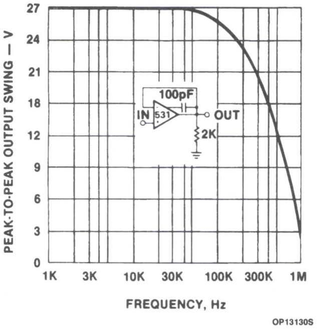
Output Voltage Swing as a Function of Supply Voltage



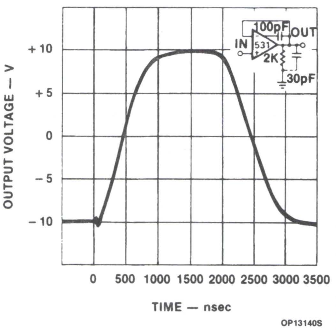
Input Voltage Range as a Function of Supply Voltage



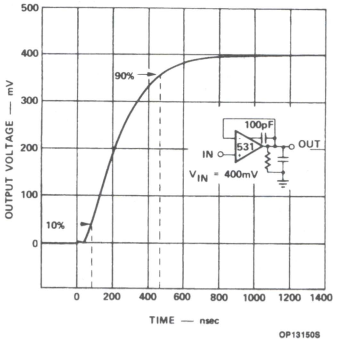
Output Voltage Swing as a Function of Frequency



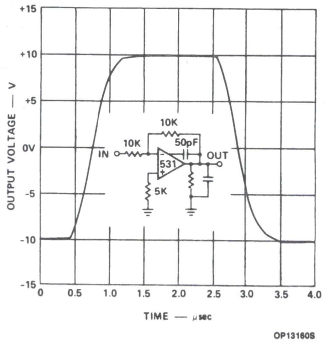
Voltage-Follower Large-Signal Response



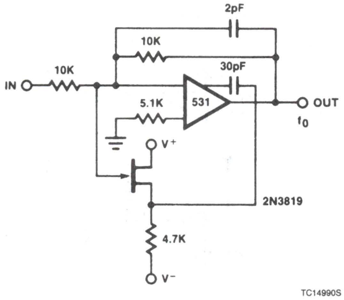
Voltage-Follower Transient Response



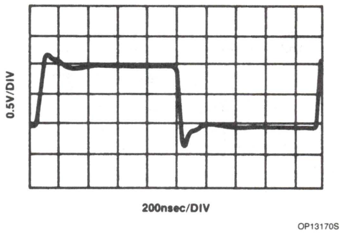
Unity Gain Inverting Amplifier Large-Signal Response



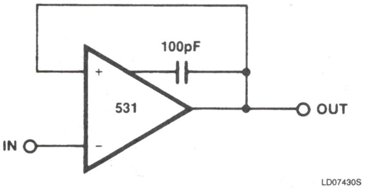
TYPICAL APPLICATIONS


2pF
10K
10K
30pF
IN
5.1K
531
OUT
f0
V+
2N3819
4.7K
V−
TC14990S

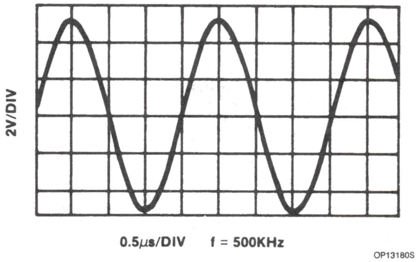
High-Speed Inverter
(10MHz Bandwidth)



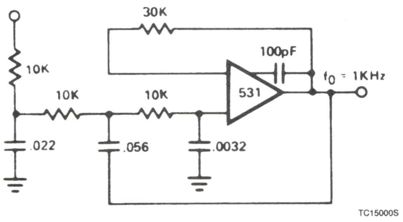
Pulse Response
High-Speed Inverter


100pF
+
531
−
IN
OUT
LD07430S

Fast Settling Voltage-Follower

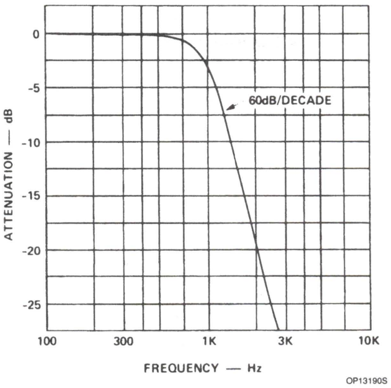


Large-Signal Response Voltage-Follower


30K
100pF
10K
10K
10K
531
f0 = 1KHz
.022
.056
.0032
TC15000S

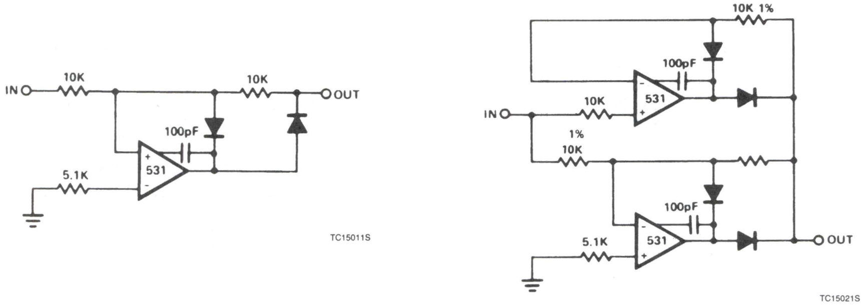
NOTES:
1. Reference — EDN Dec. 15, 1970
Simplify 3-pole active filter design
A. Paul Brokow

Three-Pole Active Low-Pass Filter Butterworth Maximally Flat Response[1]



Response of 3-Pole Active Butterworth Maximally Flat Filter

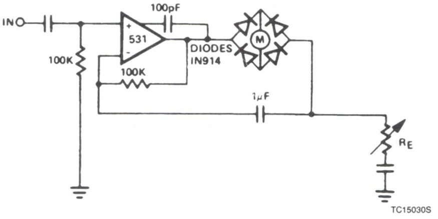
TYPICAL APPLICATIONS (Continued)


IN
10K
10K
OUT
100pF
531
5.1K
TC15011S
10K 1%
100pF
531
IN
10K
1%
10K
100pF
5.1K
531
OUT
TC15021S

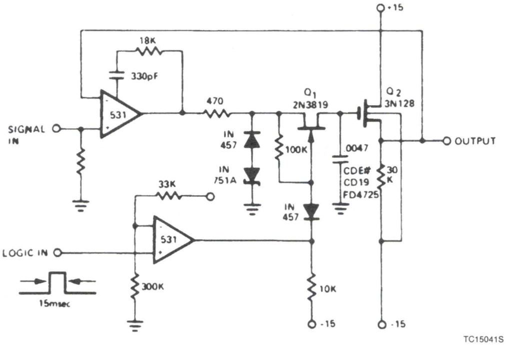
a. Half-Wave

b. Full-Wave

Precision Rectifiers


IN
100pF
531
100K
DIODES
IN914
M
100K
1μF
RE
TC15030S

AC Millivoltmeter


+15
18K
330pF
531
SIGNAL IN
470
Q1
2N3819
Q2
3N128
IN 457
100K
.0047
OUTPUT
IN 751A
CDE#
CD19
FD4725
30 K
33K
IN 457
531
LOGIC IN
15msec
300K
10K
-15
-15
TC15041S

Sample-and-Hold

CYCLIC A-TO-D CONVERTER

One interesting, but much ignored, A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{REF} from the input and doubles the remainder if the polarity was correct. In Figure 1, the signal is full-wave rectified and the remainder of $V_{IN} - V_{REF}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{REF}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5μs.

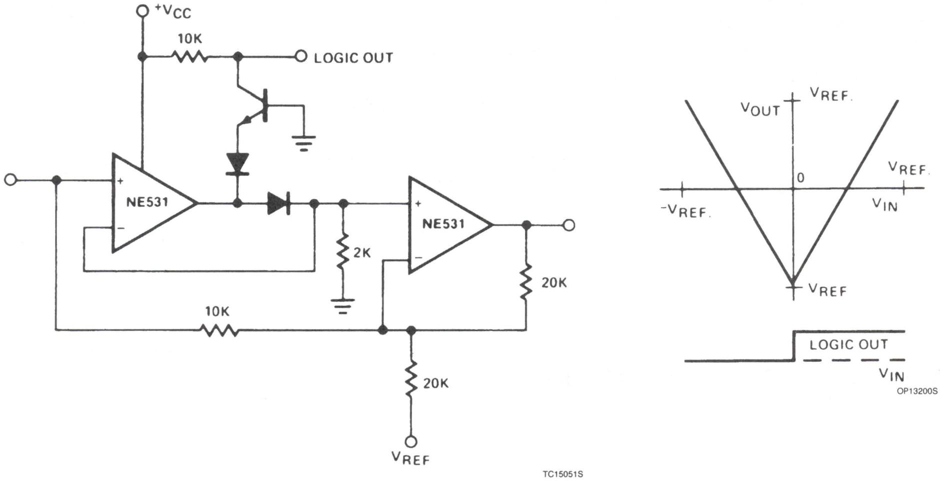
TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 2 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of op amp A-1, and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is:

$$f = \frac{1}{4RC} \cdot \frac{R2}{R1} \qquad (1)$$

The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open-loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The NE5535 device can be used as well, except for the lower frequency response.


+VCC
10K
LOGIC OUT
NE531
NE531
2K
20K
10K
20K
VREF
TC15051S
VOUT
VREF
VREF
0
-VREF
VIN
VREF
LOGIC OUT
VIN
OP13200S

a. b.

Figure 1. Cyclic A-to-D Converter

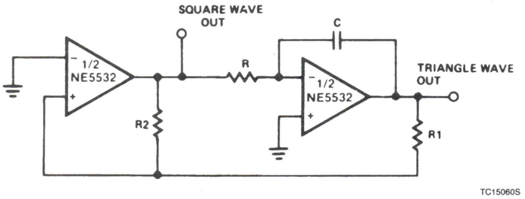

SQUARE WAVE OUT
C
R
1/2 NE5532
1/2 NE5532
TRIANGLE WAVE OUT
R2
R1
TC15060S

Figure 2. Triangle and Square Wave Generator

Signetics

NE/SE538
High Slew Rate Op Amp

Product Specification

Linear Products

DESCRIPTION

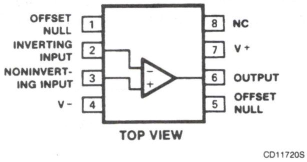
The NE/SE538 is a new generation operational amplifier featuring high slew rates combined with improved input characteristics. Internally-compensated for gains of 5 or larger, the SE538 offers guaranteed minimum slew rates of 40V/μs or larger. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A and 741.

FEATURES

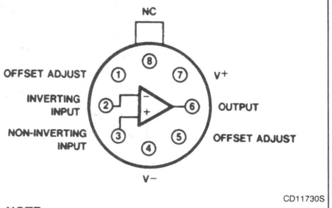
- **2mV typical input offset voltage**
- **80nA max input offset current**
- **Short-circuit protected**
- **Offset null capability**
- **Large common-mode and differential voltage ranges**
- **60V/μs typical slew rate (gain of +5, −4 min)**
- **6MHz typical gain bandwidth product (gain +5, −4 minimum)**
- **Internal frequency compensation (gain of +5, −4 minimum)**
- **Pinout: standard single op amp (748, 101A, 741, etc).**

PIN CONFIGURATIONS

FE, N Packages

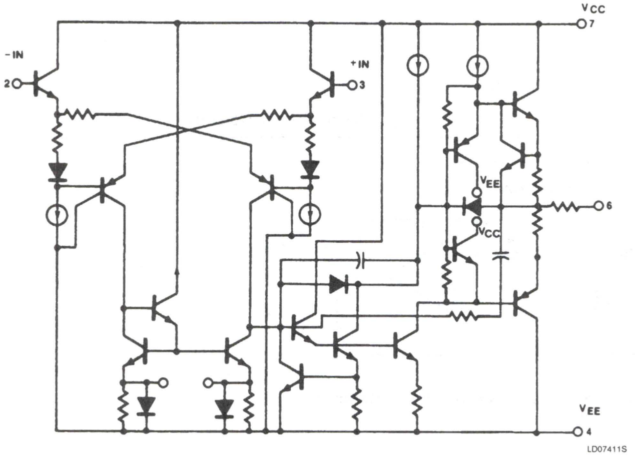

OFFSET NULL
INVERTING INPUT
NONINVERT-ING INPUT
V−
1
2
3
4
8
7
6
5
NC
V+
OUTPUT
OFFSET NULL
−
+
TOP VIEW
CD11720S

H Package[1]


NC
OFFSET ADJUST
INVERTING INPUT
NON-INVERTING INPUT
V+
OUTPUT
OFFSET ADJUST
V−
①
②
③
④
⑤
⑥
⑦
⑧
−
+
CD11730S

NOTE:
1. Metal cans not recommended for new designs.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)


−IN
2
+IN
3
V_{CC}
7
V_{EE}
V_{CC}
6
V_{EE}
4
LD07411S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE538N
8-Pin Ceramic DIP	0 to +70°C	NE538FE
8-Pin Metal Can	0 to +70°C	NE538H
8-Pin Plastic DIP	−55°C to +125°C	SE538N
8-Pin Ceramic DIP	−55°C to +125°C	SE538FE
8-Pin Metal Can	−55°C to +125°C	SE538H

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE military grade NE commercial grade	 ±22 ±18	 V V
P_D	Maximum power dissipation, T_A=25°C (still air)[1] F package N package	 780 1160	 mW mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
T_A	Operating ambient temperature range SE military grade NE commercial grade	 −55 to +125 0 to 70	 °C °C
	Output short-circuit[3]	indefinite	
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

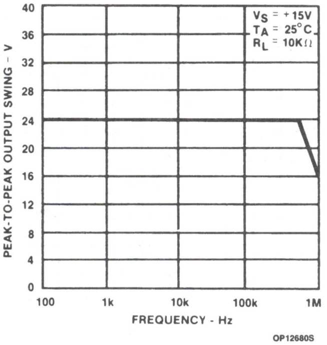
SYMBOL	PARAMETER	TEST CONDITIONS	SE538			NE538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp.			5.0			7.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		µV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temp.			40			80	nA
ΔI_{OS}	Input offset current	Over temp.		25			40		pA/°C
I_B	Input current			45	80		65	150	nA
		Over temp.			200			200	nA
ΔI_B	Input current	Over temp.		50			80		pA/°C
V_{CM}	Input common-mode voltage range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	µV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, , $V_{OUT} = \pm 10V$	50	200		50	200		V/mV
		Over temp., $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25			25			V/mV
V_{OUT}	Output voltage	Over temp., $R_L \geq 2k\Omega$	±10	±13		±10	±13		V
		Over temp., $R_L \geq 10k\Omega$	±12	±14		±12	±14		V
I_{CC}	Supply current	Per amplifier		2	3		2	3	mA
		Over temp., per amplifier		2.2	3.6		2.2	3.6	mA
P_D	Power dissipation	Per amplifier		60	90		60	90	mW
		Over temp., per amplifier		66	108		66	108	mW
I_{SC}	Output short-circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.

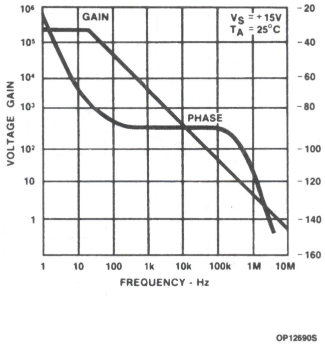
SYMBOL	PARAMETER	TEST CONDITIONS	SE538			NE538			UNIT
			Min	Typ	Max	Min	Typ	Max	
GBW	Gain bandwidth product (Gain +5, −4 minimum)			6			6		MHz
t_R	Transient response								
	Small-signal rise time			0.25			0.25		µs
	Small-signal overshoot			6			6		%
t_S	Settling time	To 0.1%		1.2			1.2		µs
SR	Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/µs
V_{NOISE}	Input noise voltage	f = 1kHz, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

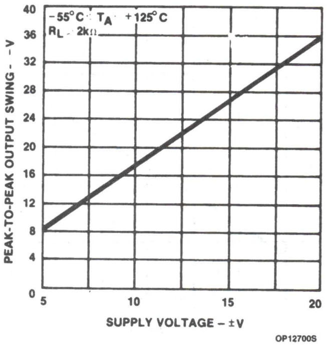
Output Voltage Swing as a Function of Frequency



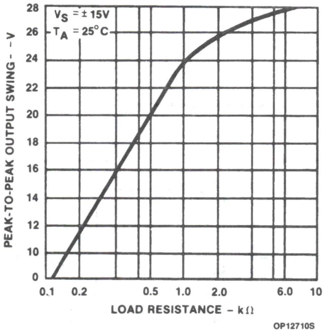
Open Loop Voltage Gain as a Function of Frequency



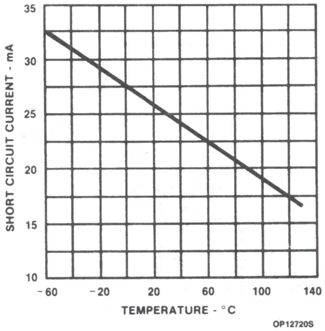
Output Voltage Swing as a Function of Supply Voltage



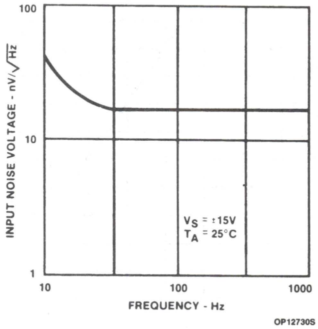
Output Voltage Swing as a Function of Load Resistance



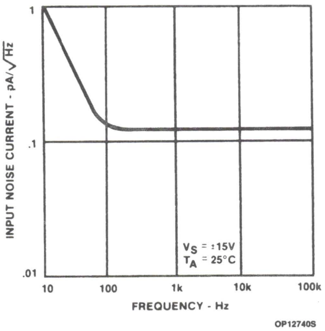
Output Short-Circuit Current as a Function of Ambient Temperature



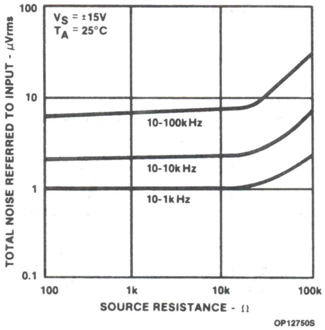
Input Noise Voltage as a Function of Frequency



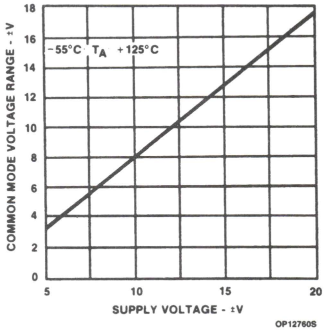
Input Noise Current as a Function of Frequency



Broadband Noise for Various Bandwidths

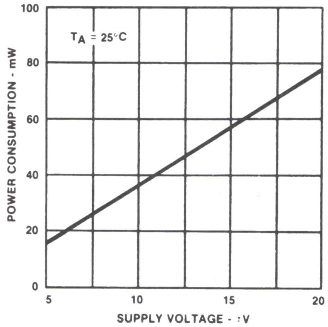


Input Common-Mode Voltage Range as a Function of Supply Voltage



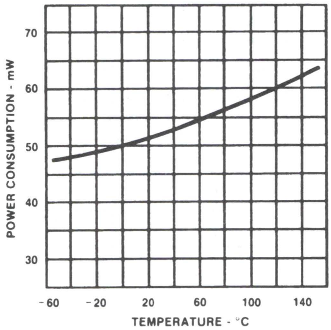
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Power Consumption as a Function of Supply Voltage



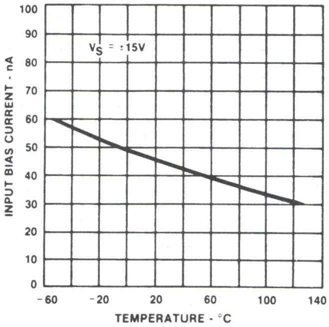
OP12770S

Power Consumption as a Function of Ambient Temperature



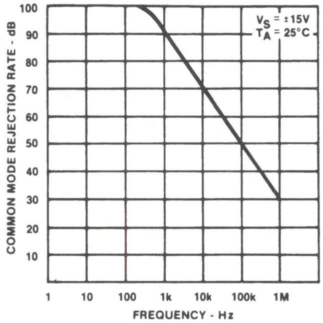
OP12780S

Input Bias Current as a Function of Ambient Temperature



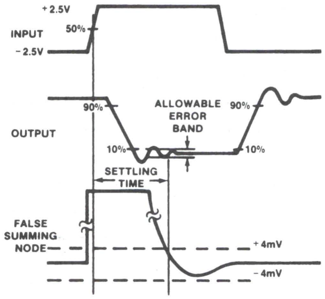
OP12790S

Common-Mode Rejection Ratio as a Function of Frequency



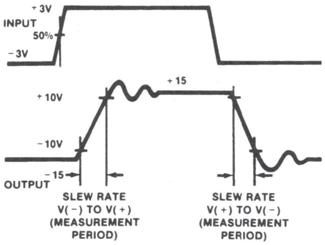
OP12800S

Settling Time Measurement Waveforms


+2.5V
INPUT
50%
-2.5V
OUTPUT
90%
ALLOWABLE ERROR BAND
90%
10%
10%
SETTLING TIME
FALSE SUMMING NODE
+4mV
-4mV

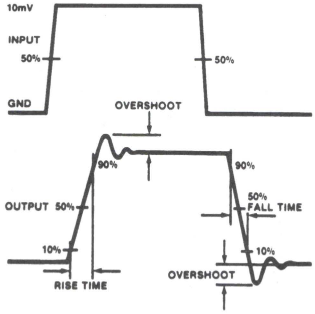
WF18440S

Slew Rate Measurement $V_{CC} = \pm 20V$


+3V
INPUT
50%
-3V
+15
+10V
-10V
-15
OUTPUT
SLEW RATE V(-) TO V(+) (MEASUREMENT PERIOD)
SLEW RATE V(+) TO V(-) (MEASUREMENT PERIOD)

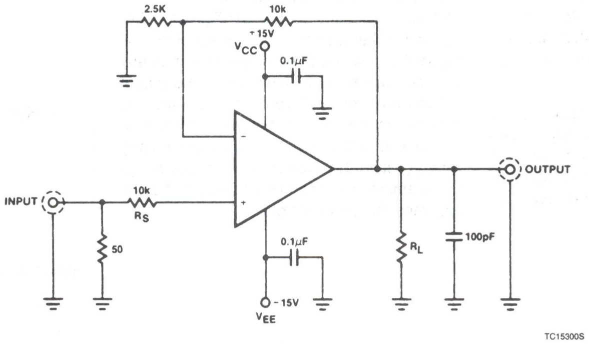
WF18450S

Small-Signal Transient Response Definitions


10mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT 50%
50% FALL TIME
10%
10%
RISE TIME
OVERSHOOT

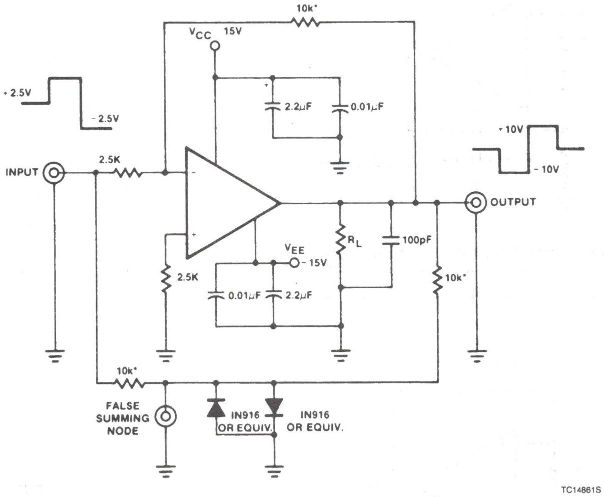
WF18460S

TEST LOAD CIRCUITS


2.5K
10k
+15V
V_{CC}
0.1μF
INPUT
10k
R_S
50
0.1μF
-15V
V_{EE}
R_L
100pF
OUTPUT
TC15300S

NOTES:
Pins not shown are not connected.
All resistor values are typical and in ohms.

Slew Rate and Small-Signal Transient Response Test Circuit


10k*
V_{CC} 15V
+2.5V
-2.5V
2.2μF
0.01μF
+10V
-10V
INPUT
2.5K
OUTPUT
R_L
100pF
V_{EE}
-15V
2.5K
0.01μF
2.2μF
10k*
10k*
FALSE SUMMING NODE
IN916 OR EQUIV.
IN916 OR EQUIV.
TC14861S

NOTES:
*Match to within 0.01%.
Pins not shown are not connected.
All resistor values are typical and in ohms.

Settling Time Test Circuit

APPLICATIONS

The internal frequency compensation is designed for a minimum inverting gain of 4 and a minimum non-inverting gain of 5. Below these gains the NE538 will be unstable and will need external compensation (see Figures 1 and 2).

The higher slew rate of the NE538 has made this device quite appealing for high-speed designs, and the fact that it has a standard pinout will allow it to be used to upgrade existing systems that now use the μA741 or μ748.

Equations:

$$f_{LAG} = \frac{1\ (6MHz)}{10} = \frac{1}{2^{\pi} R_L C_L}$$

$$f_{LEAD} = 6MHz = \frac{1}{2^{\pi} R_F C_F}$$

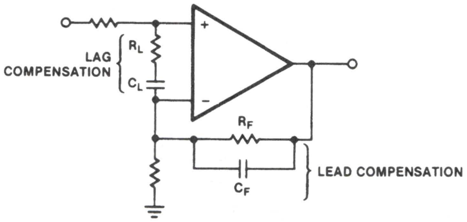

LAG COMPENSATION
R_L
C_L
+
−
R_F
C_F
LEAD COMPENSATION
TC14870S

Figure 1. Non-Inverting Configuration

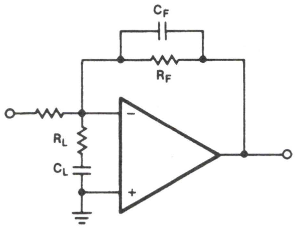

C_F
R_F
R_L
C_L
−
+
TC14920S

Figure 2. Inverting Configuration

VOLTAGE COMPARATOR

Inexpensive voltage comparators with only modest parameters are often needed. The op amp is often used in the configuration because the high gain provides good selectivity. Figure 6 shows a circuit usable with most any op amp. The zener is selected for the output voltage required (5.1 volt for TTL), and the resistor provides some current protection to the op amp output structure. V_{REF} can be any voltage within the wide common-mode range of the amplifier — another advantage of using op amps for comparators.

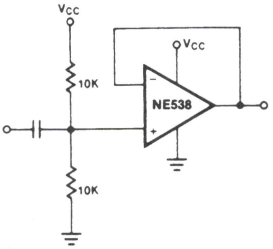

Vcc
Vcc
10K
10K
NE538
−
+
TC14880S

Figure 3. Voltage-Follower With Single Power Source

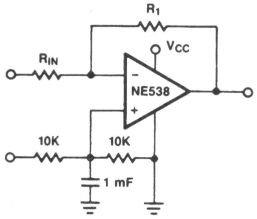

R1
Vcc
RIN
NE538
−
+
10K
10K
1 mF
TC14890S

Figure 4. Inverting Amp With Single Power Supply

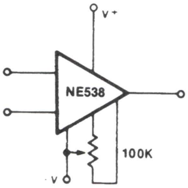
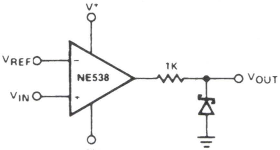

V+
NE538
100K
V
TC14900S

Figure 5. Offset Adjust Circuit


V+
VREF
VIN
NE538
−
+
1K
VOUT
V−
TC14910S

NOTE:
All resistor values are in ohms.

Figure 6. Voltage Comparator

Signetics

NE/SE5512
Dual High-Performance Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The 5512 series of high-performance operational amplifiers provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability, yet have low supply quiescent current.

APPLICATIONS

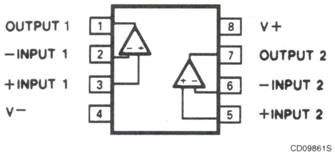
- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Battery operation**
- **Instrumentation amplifiers**

FEATURES

- **Low input bias $< \pm 20nA$**
- **Low input offset current $< \pm 20nA$**
- **Low input offset voltage $< 1mV$**
- **Low V_{OS} temperature drift 5μV/°C**
- **Low input bias temperature drift 40pA/°C**
- **Low input voltage noise 30nV/$\sqrt{Hz}$**
- **Low supply current 1.5mA/amp**
- **High slew rate 1.0V/μs**
- **High CMRR 100dB**
- **High input impedance 100MΩ**
- **High PSRR 110dB**
- **High differential input voltage limit**
- **No crossover distortion**
- **Indefinite output short circuit protection**
- **Internally-compensated for unity gain**
- **600Ω drive capability**

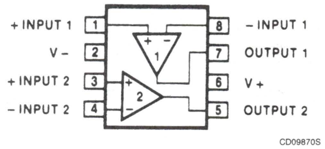
PIN CONFIGURATIONS

FE, N Packages


OUTPUT 1
1
−INPUT 1
2
+INPUT 1
3
V−
4
8
V+
7
OUTPUT 2
6
−INPUT 2
5
+INPUT 2
CD09861S

TOP VIEW

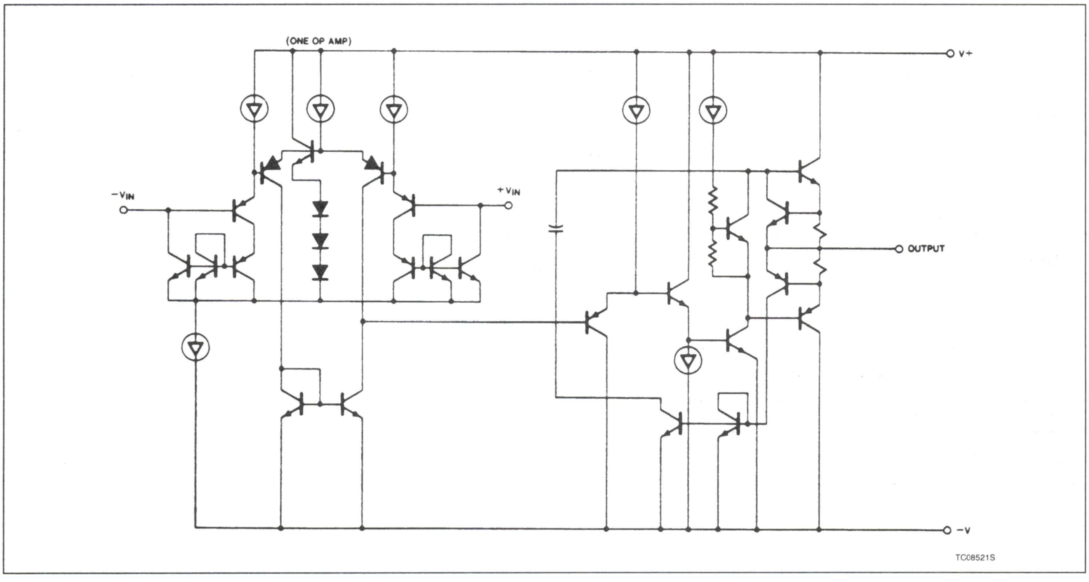
D Package[1]


+INPUT 1
1
V−
2
+INPUT 2
3
−INPUT 2
4
8
−INPUT 1
7
OUTPUT 1
6
V+
5
OUTPUT 2
1
2
CD09870S

TOP VIEW

NOTE:
1. The D package pinout is not functionally identical to the FE or N pinout.

EQUIVALENT SCHEMATIC


(ONE OP AMP)
V+
−VIN
+VIN
OUTPUT
−V
TC08521S

Dual High-Performance Operational Amplifier NE/SE5512

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0°C to +70°C	NE5512D
8-Pin Ceramic DIP	0°C to +70°C	NE5512FE
8-Pin Plastic DIP	0°C to +70°C	NE5512N
8-Pin Ceramic DIP	−55°C to +125°C	SE5512FE
8-Pin Plastic DIP	−55°C to +125°C	SE5512N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
P_D	Power dissipation	500	mW
T_A	Operating ambient temperature range NE5512 SE5512	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

ELECTRICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_A = 25°C$ over temperature range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5512			NE5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$ $T_A = +25°C$ Over temp.		0.7 1	2 3		1 1.5	5 6	mV
$\Delta V_{OS}/\Delta T$				4			5		µV/°C
I_{OS}	Input offset current	$R_S = 100k\Omega$ $T_A = +25°C$ Over temp.		3 4	10 20		6 8	20 30	nA
$\Delta I_{OS}/\Delta T$				30			40		pA/°C
I_{BIAS}	Input bias current	$R_S = 100k\Omega$ $T = +25°C$ Over temp.		3 4	10 20		6 8	20 30	nA
$\Delta I_{BIAS}/\Delta T$				30			40		pA/°C
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$ Over temp.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$ $V_{IN} = \pm 13.5V$ (RM) $T_A = 25°C$ $V_{IN} = \pm 13V$ (FR) Over temp.	70	100		70	100		dB
A_V	Large-signal voltage gain	$R_L = 2k\Omega$ $T_A = 25°C$ $V_O = \pm 10V$ over temp.	50 25	200		50 25	200		V/mV
SR	Slew rate	$T_A = 25°C$	0.6	1			1		V/µs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz

ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued) $V_{CC} = \pm 15V$, $T_A = 25°C$ over temperature range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5512			NE5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
θ_M	Phase margin	$T_A = 25°C$		45			45		degree
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ $T_A = 25°C$ Over temp.	 ±13 ±12.5	 ±13.5 ±13		 ±13 ±12.5	 ±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega^1$ $T_A = 25°C$ Over temp.	 ±10 ±7.5	 ±11.5 ±9		 ±10 ±8	 ±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open $T_A = 25°C$ Over temp.		 3.4 3.6	 5 5.5		 3.4 3.6	 5 5.5	mA
PSRR	Power supply rejection ratio	$T_A = 25°C$ Over temp.	80 80	110 100		80 80	110 100		dB
AA	Amplifier-to-amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		−120			−120		dB
THD	Total harmonic distortion	f = 10kHz $T_A = 25°C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V_{NOISE}	Input noise voltage	f = 1kHz $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$
I_{NOISE}	Input noise current	f = 1kHz $T_A = 25°C$		0.2			0.2		$pA/\sqrt{Hz}$
I_{SC}	Short-circuit current	±15V, $T_A = 25°C$		40			40		mA

NOTE:

1. For operation at elevated temperature, N package must be derated based on a thermal resistance of 120°C/W junction-to-ambient. Thermal resistance of the FE package is 125°C/W.

Signetics

AN144
Applications for the NE5512

Application Note

Linear Products

DESCRIPTION

The NE/SE5512 series of high-performance operational amplifiers provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability, yet have low supply quiescent current.

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors, a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a possible solution to these general requirements (Figure 1).

For $V_S = 10V$, the common-mode voltage is approximately +5V, well within the common-mode limits of the NE5512.

The sensitivity of the input stage is approximately

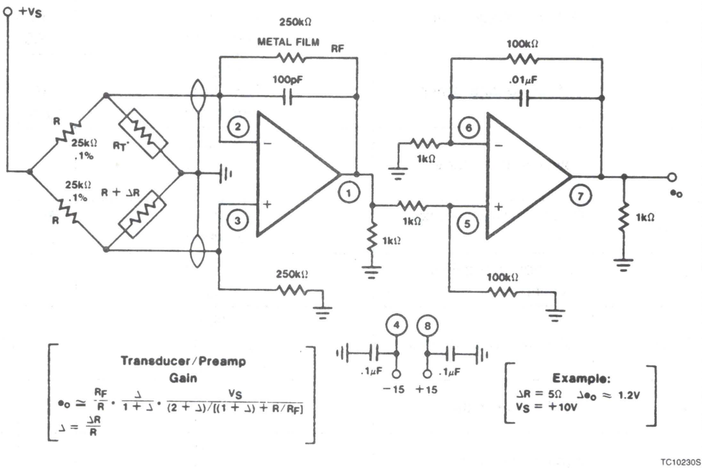
$$\frac{R_F \cdot V_S}{2R}$$

to a change in transducer resistance ΔR. This gives a gain factor of ≅50 for $V_S = 10V$ and $R = 25k\Omega$. The second stage gain is ×100 giving a total gain of ≅5000.

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground. Common-mode noise rejection is particularly important, making matched differential impedance critical. The NE5512 typically provides 100dB of common-mode rejection and will considerably reduce this undesirable effect.

The following are sensitivity figures for the transducer circuits.

	ΔR	ΔE_{OUT}
Leg 1	10Ω	−2.6V
	5Ω	−1.3V
Leg 2	10Ω	+2.4V
	5Ω	+1.2V



$$e_o \simeq \frac{R_F}{R} \cdot \frac{\Delta}{1+\Delta} \cdot \frac{V_S}{(2+\Delta)/[(1+\Delta)+R/R_F]}$$

$$\Delta = \frac{\Delta R}{R}$$

$\Delta R = 5\Omega \quad \Delta e_o \approx 1.2V$
$V_S = +10V$

NOTE:
Thermal compensation transducer (non-active)

Figure 1. NE/SE5512 Bridge Transducer Amplifier

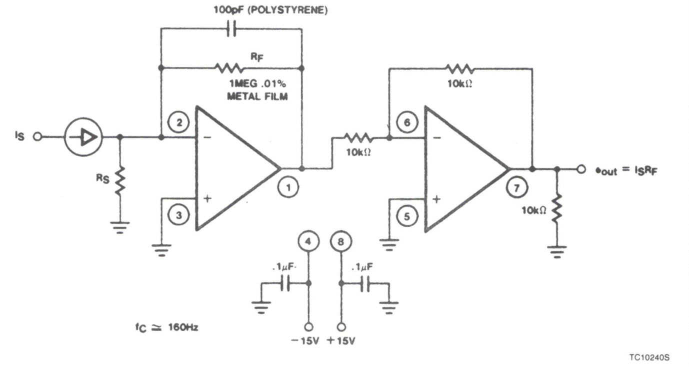


Figure 2. NE/SE5512 Current-to-Voltage Converter With 1% Accuracy [Sensitivity: 1V/μA]

Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

CURRENT-TO-VOLTAGE CONVERTER

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in

Applications for the NE5512 AN144

its adaptation to a current-to-voltage converter as shown in Figure 2.

The lower limit of measuring accuracy is determined by I_B (inverting), which is typically 6nA. In order to attain a measurement accuracy of 1%, the following inequality must hold:

$$I_B \leqslant (0.01)\ I_{Smin}$$

Where I_B = input bias current and I_{Smin} = minimum measured current. For I_B = 6nA and I_{Smin} = 1μA,

6nA ⩽ (0.01) 1μA = 10nA and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≅ 1 for $R_S >> R_F$.

The measured results for this circuit appear below (V_{CC} = ±15V).

INPUT CURRENT	OUTPUT VOLTAGE
1μA	1.008V
5μA	5.00V
10.00μA	10.00V

NE5512 OPERATIONAL DIFFERENTIATOR

By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the waveforms in Figures 4, 5 and 6. One of the primary problems with such circuits is the tendency towards instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency, requiring low input noise in the amplifier.

The relative stability is shown by the output signal waveforms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC, must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC, which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.

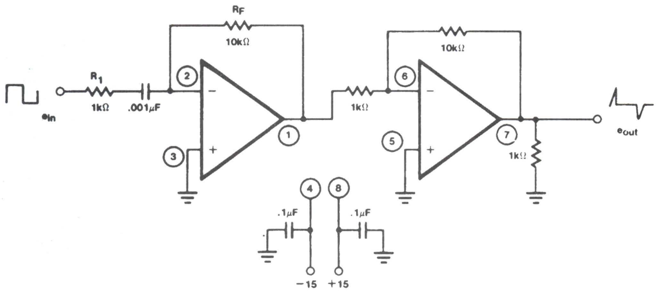


Figure 3. NE/SE5512 Active Differentiator With Inverting × 10 Buffer

DIFFERENTIATOR WAVEFORMS

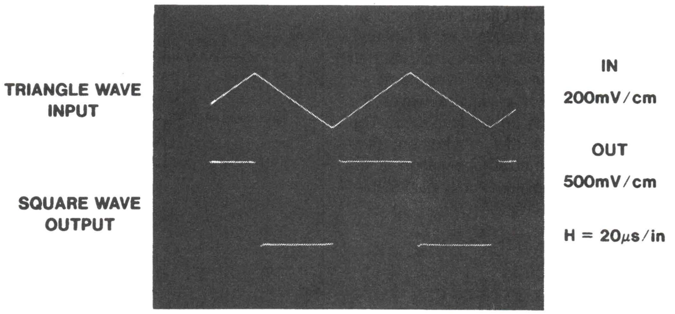


Figure 4

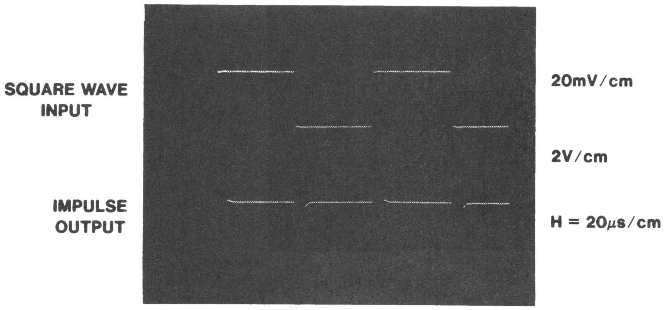


Figure 5

Applications for the NE5512 AN144

THE OPERATIONAL INTEGRATOR

The operational complement of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). To obtain satisfactory integration, the time constant must fulfill the following requirement:

$RC \geqslant 15T$

Where T is the period of the input waveform.

For the ideal integrator

$$e_{out} = \frac{1}{RC}\int e_{in}\, dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The waveforms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of ≥89° for sine wave input over the active frequency range. For a square wave, the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

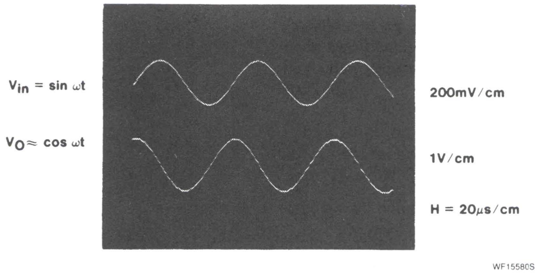


Figure 6

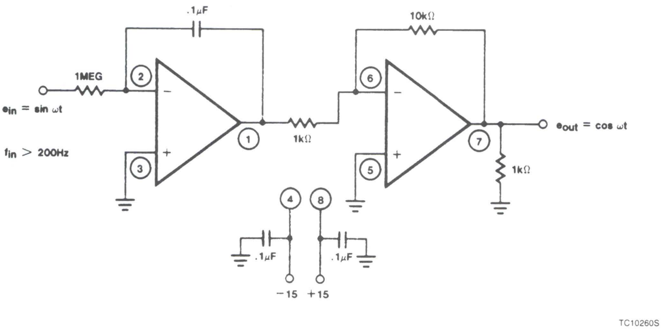


Figure 7. NE/SE5512 Active Integrator

INTEGRATOR WAVEFORMS

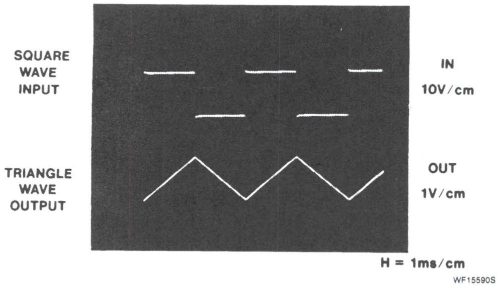


Figure 8

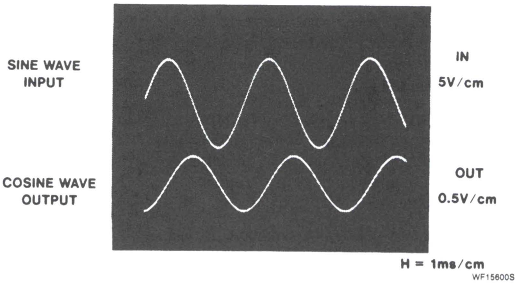


Figure 9

Signetics

Linear Products

NE/SE5514
Quad High-Performance Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5514 family of quad operational amplifiers sets new standards in bipolar quad amplifier performance. The amplifiers feature low input bias current and low offset voltages. Pinout is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FEATURES

- **Low input bias current:** < ±3nA
- **Low input offset current:** < ±3nA
- **Low input offset voltage:** < 1mV
- **Low supply current: 1.5mA/A**
- **1V/μs slew rate**
- **High input impedance: 100MΩ**
- **High common-mode impedance: 10GΩ**
- **Internal compensation for unity gain**
- **600Ω drive capability ($7V_{RMS}$)**

APPLICATIONS

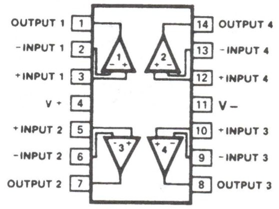
- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Instrumentation amplifier**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL package	0 to +70°C	NE5514D
14-Pin Ceramic DIP	0 to +70°C	NE5514F
14-Pin Plastic DIP	0 to +70°C	NE5514N
14-Pin Ceramic DIP	-55°C to +125°C	SE5514F
14-Pin Plastic DIP	-55°C to +125°C	SE5514N

PIN CONFIGURATIONS

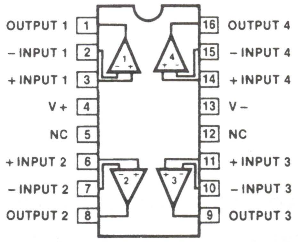
F, N Packages


OUTPUT 1 1
-INPUT 1 2
+INPUT 1 3
V+ 4
+INPUT 2 5
-INPUT 2 6
OUTPUT 2 7
14 OUTPUT 4
13 -INPUT 4
12 +INPUT 4
11 V-
10 +INPUT 3
9 -INPUT 3
8 OUTPUT 3
1
2
3
4

TOP VIEW

CD11660S

D Package[1]

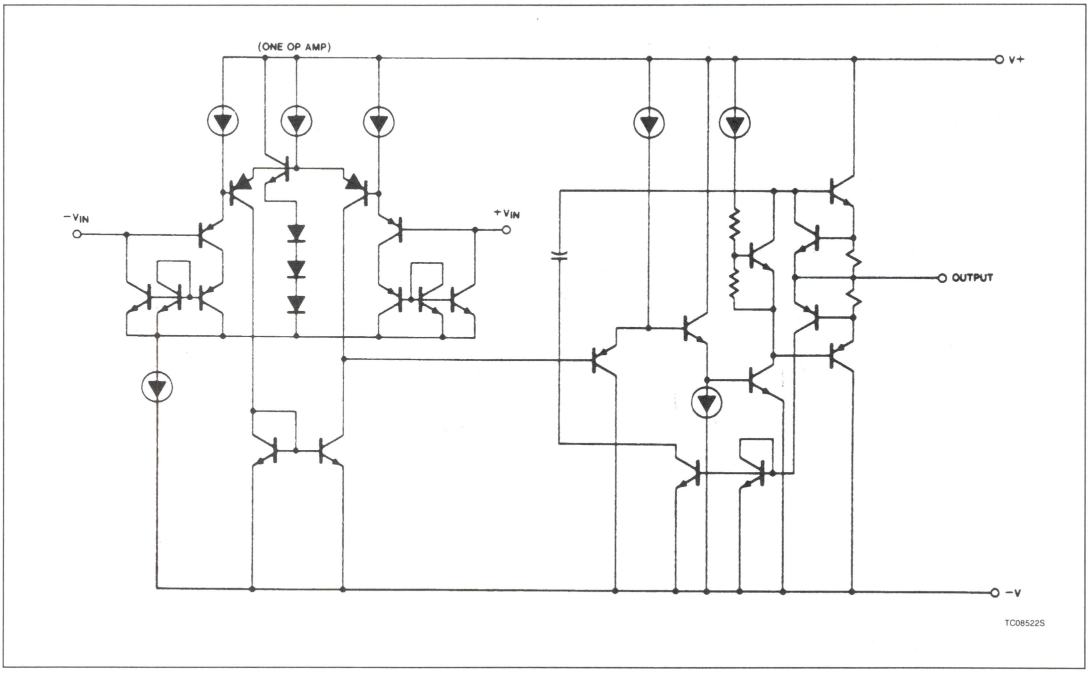

OUTPUT 1 1
-INPUT 1 2
+INPUT 1 3
V+ 4
NC 5
+INPUT 2 6
-INPUT 2 7
OUTPUT 2 8
16 OUTPUT 4
15 -INPUT 4
14 +INPUT 4
13 V-
12 NC
11 +INPUT 3
10 -INPUT 3
9 OUTPUT 3
1
4
2
3

TOP VIEW

CD11670S

NOTE:
1. SOL – Released in 16-lead large SO package only. Pinout is different than F, N packages.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating ambient temperature range		
	NE5514	0 to 70	°C
	SE5514	−55 to +125	°C
P_{MAX}	Maximum power disspation T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1250	mW

NOTE:

1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 10.0mW/°C.

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$, $T_A = +25°C$,		0.7	2		1	5	mV
		Over temp.		1	3		1.5	6	
ΔV_{OS}		Over temp.		4			5		μV/°C
I_{OS}	Input offset current	$R_S = 100k\Omega$, $T_A = +25°C$,		3	10		6	20	nA
		Over temp.		4	20		8	30	
ΔI_{OS}		Over temp.		30			40		pA/°C
I_{BIAS}	Input bias current	$R_S = 100k\Omega$, $T_A = +25°C$,		3	10		6	20	nA
		Over temp.		4	20		8	30	
ΔI_{BIAS}		Over temp.		30			40		pA/°C
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$, Over temp.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$, c, $V_{IN} = \pm 13.5V$ @ $T_A = 25°C$, $V_{IN} = \pm 13V$ @ Over temp.	70	100		70	100		dB
A_V	Large-signal voltage gain	$R_L = 2k\Omega$, $T_A = 25°C$ $V_C = \pm 10V$, Over temp.	50 25	200		50 25	200		V/mV
SR	Slew rate	$T_A = 25°C$	0.6	1		0.6	1		V/μs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degr
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $T_A = 25°C$, Over temp.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$, $T_A = 25°C$, Over temp.	±10 ±7.5	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open, $T_A = 25°C$, Over temp.		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio	Over temp.	80	110		80	110		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		−120			−120		dB
THD	Total harmonic distortion	f = 10kHz, $T_A = 25°C$, $V_O = 7V_{RMS}$		0.01			0.01		%
V_{NOISE}	Input noise voltage	f = 1kHz, $T_A = 25°C$		30			30		nV/$\sqrt{Hz}$
I_{SC}	Short-circuit current	$T_A = 25°C$	10	40	60	10	40	60	mA

Signetics

AN1441
Applications for the NE5514

Application Note

Linear Products

NE5514 DESCRIPTION

The SE/NE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pinout is identical to LM324/LM348, which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FOUR-QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photoconductive mode (reverse-biased) very small currents in the microampere range must be sensed in the photo active operating region. Dark currents in the nanoamperes are common. Generally, for this reason, JFET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6nA) to allow its use under these circuit constraints as shown in a possible design used to sense four-quadrant motion of a light source. By proper summing of the signals from the X and Y axes, four-quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation (see Figure 1).

The wide input common-mode voltage range of the device allows a +10V supply to be used to drive the signal bridge giving high sensitivity and improved signal-to-noise. Obviously, input balancing is critical to achieving common-mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick-up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems, a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method, the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. DC offset is then adjusted using the balance pot on the output amplifier under dark field conditions.

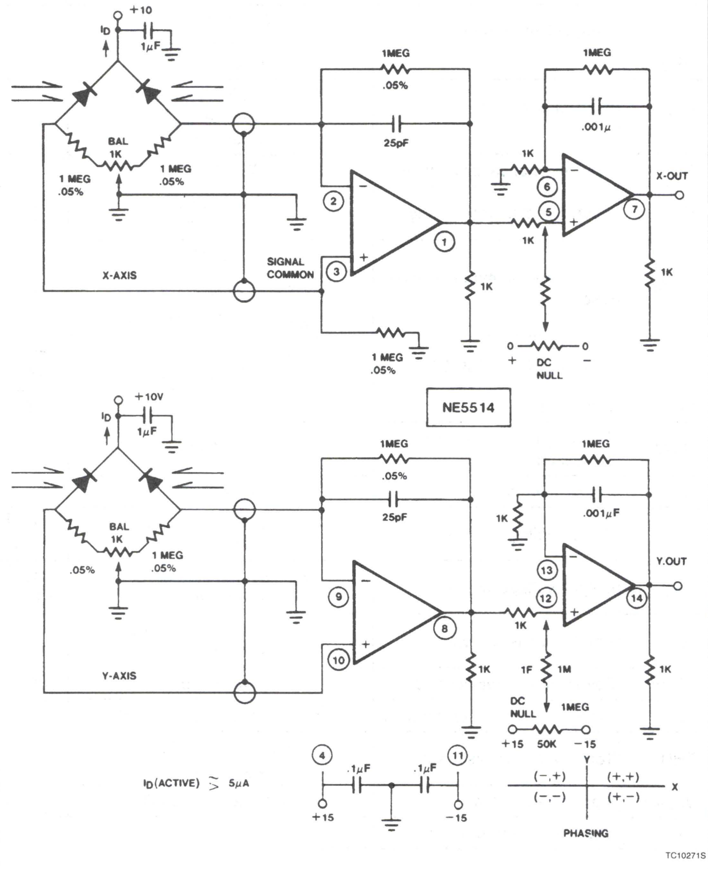


Figure 1. Four-Quadrant Photo Detector

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications.

By the use of narrow-band active pre-filters to attain selectivity and gain, the effective signal to noise ratio is greatly improved. The NE/SE5514 is easily adapted to such filter configurations due to its inherent stability. In addition, its very high input impedance drastically reduces loading to the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 2 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from the filter configuration were as follows:

Wide-band signal-to-noise	63dB
Gain (Mid band)	30dB
Q (effective)	≈ 30
Output	0dBM (0.775V_{RMS})

Note that the amplifiers are operated from a single +12V supply and are biased to half V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

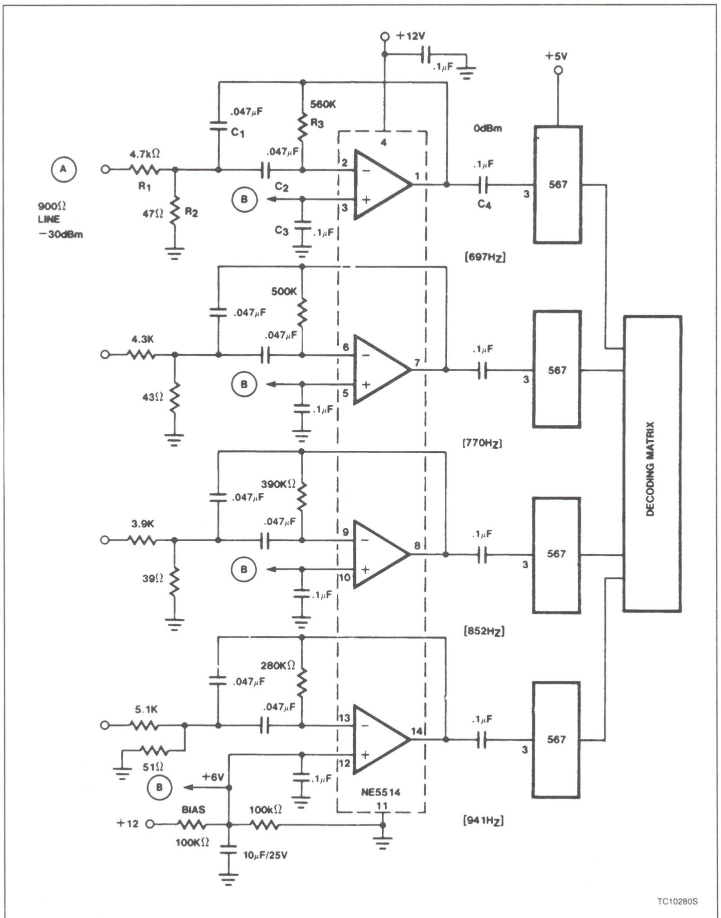

+12V
.1μF
+5V
.047μF
C1
560K
R3
0dBm
4
4.7kΩ
.047μF
.1μF
A
R1
2
1
567
C2
B
3
C4
900Ω
LINE
−30dBm
47Ω
R2
3
C3
.1μF
[697Hz]
500K
.047μF
.047μF
4.3K
6
.1μF
7
567
B
5
3
43Ω
.1μF
[770Hz]
DECODING MATRIX
390KΩ
.047μF
3.9K
.047μF
9
.1μF
8
567
B
10
3
39Ω
.1μF
[852Hz]
280KΩ
.047μF
5.1K
.047μF
13
.1μF
14
567
51Ω
3
+6V
12
.1μF
B
NE5514
BIAS
100kΩ
11
+12
100KΩ
10μF/25V
[941Hz]
TC10280S

Figure 2. NE5514 MFB Bandpass Filter for Multi-Channel Tone Decoder

4-STATION 0 – 50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 3. The principle used is fundamental to the current voltage relationship of a forward-biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

$$\text{and} \quad I_E \infty I_S \exp (V_{BE}/V_T); \; V_T = \frac{kt}{q}$$

$$\text{therefore,} \quad V_{BE} \infty V_T \ln I_E/I_S$$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E >> I_S$). I_S is typically 0.05pA, therefore, setting I_E to 1 or 2μA gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "0" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100mV/°C output.

Only the transistor need be placed in the temperature-controlled environment. Figure 4 shows the addition of an A/D converter and display to give a digital thermometer.

Applications for the NE5514

AN1441

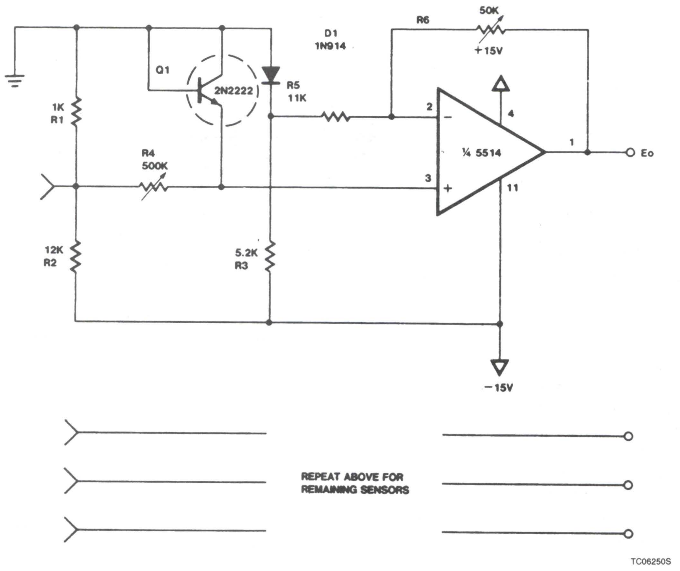

R6
50K
D1
1N914
+15V
Q1
2N2222
R5
11K
1K
R1
R4
500K
2
4
¼ 5514
1
Eo
3
11
12K
R2
5.2K
R3
−15V
REPEAT ABOVE FOR REMAINING SENSORS
TC06250S

Figure 3. 4-Channel Temperature Sensor (0 – 50°C)

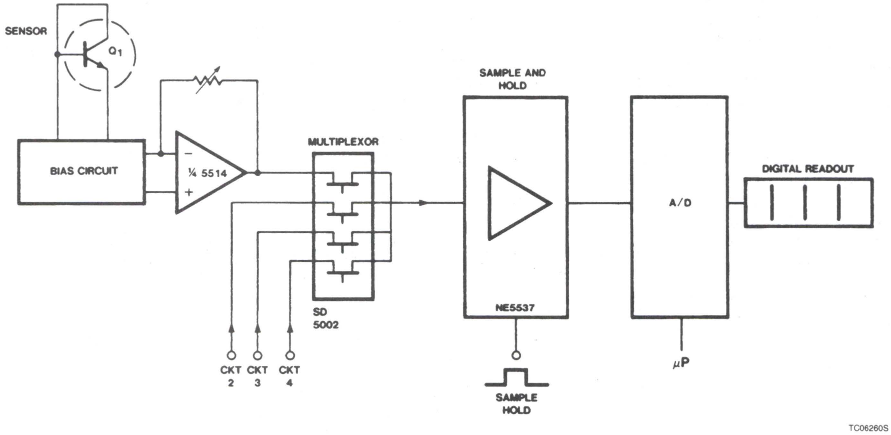

SENSOR
Q1
SAMPLE AND HOLD
BIAS CIRCUIT
¼ 5514
MULTIPLEXOR
DIGITAL READOUT
A/D
SD 5002
NE5537
μP
CKT 2
CKT 3
CKT 4
SAMPLE HOLD
TC06260S

Figure 4. Microprocessor-Controlled Digital Thermometer

Signetics

Linear Products

NE/SE5532/5532A

Internally-Compensated Dual Low Noise Operational Amplifier

Product Specification

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

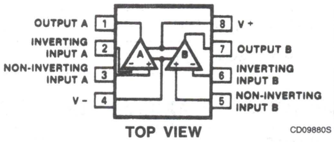
This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used because it has guaranteed noise voltage specifications.

FEATURES

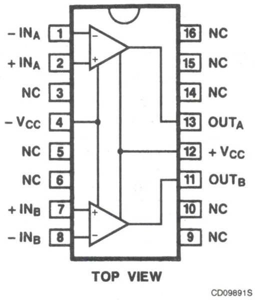
- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V_{RMS}**
- **Input noise voltage: 5nV/$\sqrt{\text{Hz}}$ (typical)**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**
- **Compensated for unity gain**

PIN CONFIGURATIONS

FE, N Packages

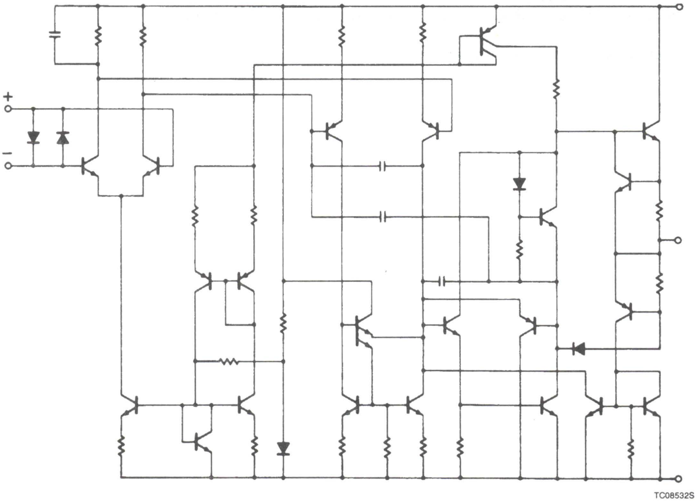

OUTPUT A
1
INVERTING INPUT A
2
NON-INVERTING INPUT A
3
V-
4
A
B
8
V+
7
OUTPUT B
6
INVERTING INPUT B
5
NON-INVERTING INPUT B
TOP VIEW
CD09880S

D Package[1]


-IN_A
1
+IN_A
2
NC
3
-V_CC
4
NC
5
NC
6
+IN_B
7
-IN_B
8
16
NC
15
NC
14
NC
13
OUT_A
12
+V_CC
11
OUT_B
10
NC
9
NC
TOP VIEW
CD09891S

NOTE:
1. SOL and *non-standard* pinout.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



Internally-Compensated Dual Low Noise Operational Amplifier

NE/SE5532/5532A

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE5532N
8-Pin Ceramic DIP	0 to 70°C	NE5532FE
8-Pin Plastic DIP	0 to 70°C	NE5532AN
8-Pin Ceramic DIP	0 to 70°C	NE5532AFE
8-Pin Ceramic DIP	−55°C to +125°C	SE5532FE
8-Pin Ceramic DIP	−55°C to +125°C	SE5532AFE
16-Pin Plastic SOL	0 to 70°C	NE5532D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	$\pm V_{SUPPLY}$	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range		
	NE5532/A	0 to 70	°C
	SE5532/A	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[2]		
	N package	1200	mW
	F package	1000	mW
	D package	1200	mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. Thermal resistances of the above packages are as follows:
   N package at 100°C/W.
   F package at 125°C/W.
   D package at 100°C/W.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
$\Delta I_B/\Delta T$				5			5		mA/°C
I_{CC}	Supply current						8	16	mA
		Over temperature			13				mA
V_{CM}	Common-mode input range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50			25	100		V/mV
		Over temperature	25			15			V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	40			15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$				±12	±13		V
		Over temperature				±10	±12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	±15	±16					V
		Over temperature				±12	±14		V
		$R_L \geq 2k\Omega$ over temp.	±12	±13		±10	±13		V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current		10	38	60	10	38	60	mA

NOTES:

1. Diodes protect the inputs against overvoltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the package thermal resistance.
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532/5532A Min	NE/SE5532/5532A Typ	NE/SE5532/5532A Max	UNIT
R_{OUT}	Output resistance	$A_V = 30dB$ Closed-loop $f = 10kHz$, $R_L = 600\Omega$		0.3		Ω
	Overshoot	Voltage-follower $V_{IN} = 100mV_{P-P}$ $C_L = 100pF$, $R_L = 600\Omega$		10		%
	Gain	f = 10kHz		2.2		V/mV
BW	Gain bandwidth product	$C_L = 100pF$, $R_L = 600\Omega$		10		MHz
SR	Slew rate			9		V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$ $V_{OUT} = \pm 14V$, $R_L = 600\Omega$, $V_{CC} = \pm 18V$		140 100		kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

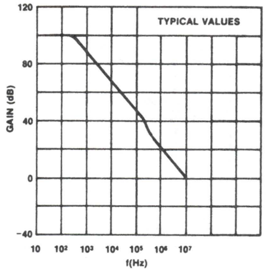
SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532 Min	NE/SE5532 Typ	NE/SE5532 Max	NE/SE5532A Min	NE/SE5532A Typ	NE/SE5532A Max	UNIT
V_{NOISE}	Input noise voltage	$f_O = 30Hz$ $f_O = 1kHz$		8 5			8 5	12 6	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
I_{NOISE}	Input noise current	$f_O = 30Hz$ $f_O = 1kHz$		2.7 0.7			2.7 0.7		$pA/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Channel separation	$f = 1kHz$, $R_S = 5k\Omega$		110			110		dB

Internally-Compensated Dual Low Noise Operational Amplifier

NE/SE5532/5532A

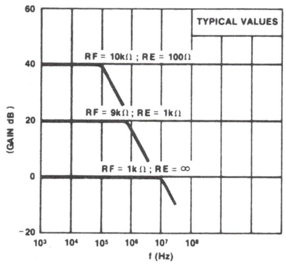
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Frequency Response



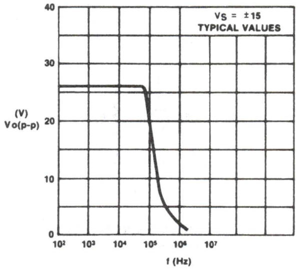
OP04870S

Closed-Loop Frequency Response



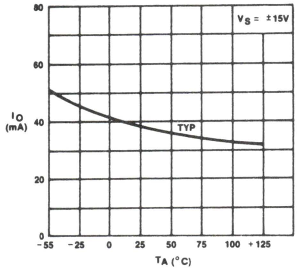
OPT4880S

Large-Signal Frequency Response



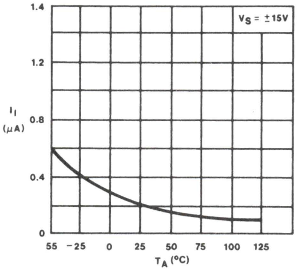
OPT4890S

Output Short-Circuit Current



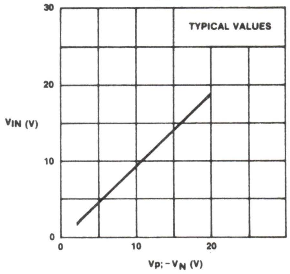
OP04900S

Input Bias Current



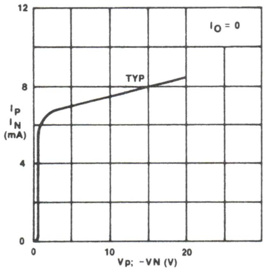
OP04910S

Input Common-Mode Voltage Range



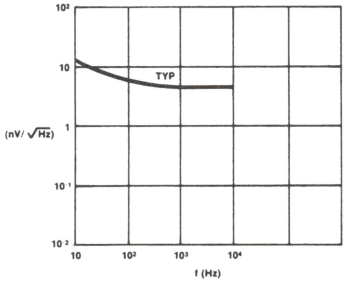
OP04920S

Supply Current



OP04930S

Input Noise Voltage Density

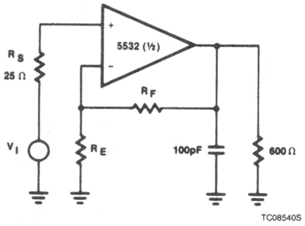


OP04940S

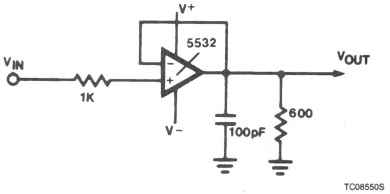
Internally-Compensated Dual Low Noise Operational Amplifier

NE/SE5532/5532A

TEST CIRCUITS


+
-
5532 (½)
R_S
25 Ω
R_F
V_I
R_E
100pF
600 Ω
TC08540S

Closed-Loop Frequency Response


V+
5532
-
+
V_{IN}
1K
V−
100pF
600
V_{OUT}
TC08550S

Voltage-Follower

Signetics

Linear Products

NE5533/5533A
NE/SA/SE5534/5534A
Dual and Single Low Noise Op Amp

Product Specification

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5533N
16-Pin Plastic SO package	0 to +70°C	NE5533AD
14-Pin Plastic DIP	0 to +70°C	NE5533AN
16-Pin Plastic SO package	0 to +70°C	NE5533D
8-Pin Plastic SO package	0 to +70°C	NE5534D
8-Pin Hermetic Cerdip	0 to +70°C	NE5534FE
8-Pin Plastic DIP	0 to +70°C	NE5534N
8-Pin Plastic SO package	0 to +70°C	NE5534AD
8-Pin Hermetic Cerdip	0 to +70°C	NE5534AFE
8-Pin Plastic DIP	0 to +70°C	NE5534AN
8-Pin Plastic DIP	-40°C to +85°C	SA5534N
8-Pin Plastic DIP	-40°C to +85°C	SA5534AN
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534AFE
8-Pin Plastic DIP	-55°C to +125°C	SE5534N
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534AFE
8-Pin Plastic DIP	-55°C to +125°C	SE5534AN

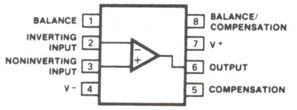
FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, $10V_{RMS}$ at $V_S = \pm 18V$**
- **Input noise voltage: $4nV/\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwith: 200kHz**
- **Slew rate: 13V/µs**
- **Large supply voltage range: ±3 to ±20V**

PIN CONFIGURATIONS

NE/SA/SE5534/5534A

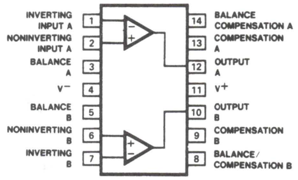
D, FE, N Packages


BALANCE 1
INVERTING INPUT 2
NONINVERTING INPUT 3
V- 4
8 BALANCE/ COMPENSATION
7 V+
6 OUTPUT
5 COMPENSATION
−
+

CD09900S

NE5533/5533A

N Package

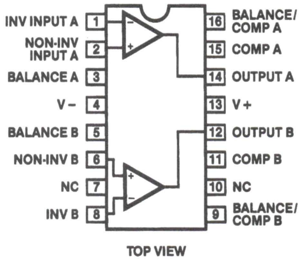

INVERTING INPUT A 1
NONINVERTING INPUT A 2
BALANCE A 3
V− 4
BALANCE B 5
NONINVERTING B 6
INVERTING B 7
14 BALANCE COMPENSATION A
13 COMPENSATION A
12 OUTPUT A
11 V+
10 OUTPUT B
9 COMPENSATION B
8 BALANCE/ COMPENSATION B

CD09910S

NE5533/5533A

D Package

D2


INV INPUT A 1
NON-INV INPUT A 2
BALANCE A 3
V− 4
BALANCE B 5
NON-INV B 6
NC 7
INV B 8
16 BALANCE/ COMP A
15 COMP A
14 OUTPUT A
13 V+
12 OUTPUT B
11 COMP B
10 NC
9 BALANCE/ COMP B
TOP VIEW

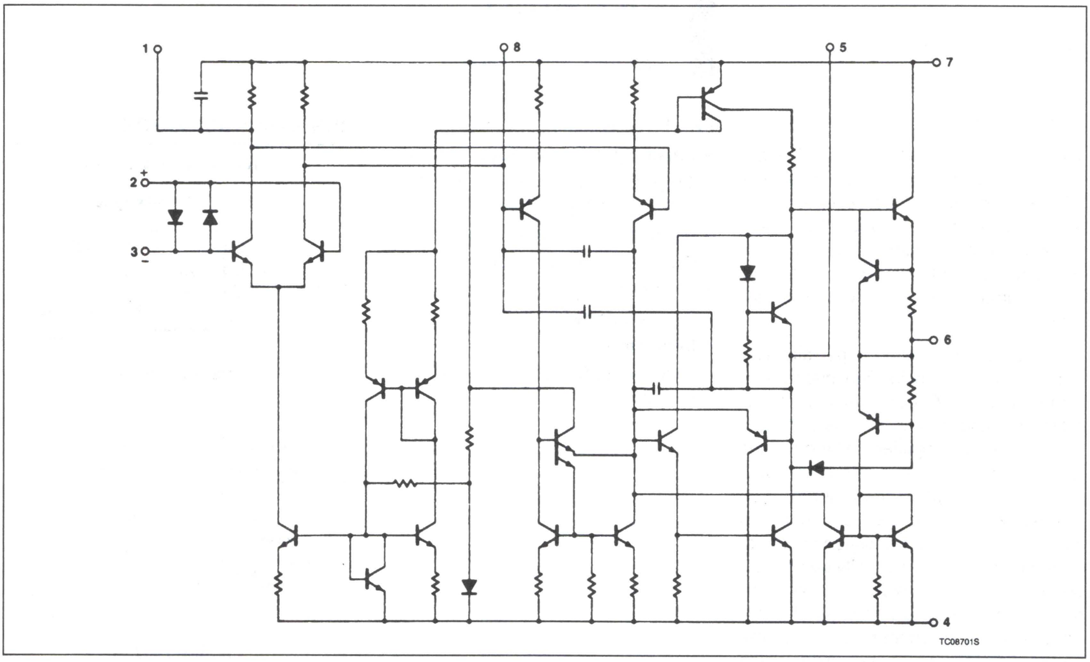
CD11390S

NOTE:
This device may not be symboled in standard format.

Dual and Single Low Noise Op Amp

NE5533/5533A NE/SA/SE5534/5534A

EQUIVALENT SCHEMATIC


1
8
5
7
2 +
3 −
6
4
TC08701S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range SE SA NE	 −55 to +125 −40 to +85 0 to +70	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2] 5533N, 5534N, 5534FE	 800	 mW
	Output short-circuit duration[3]	Indefinite	
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistance:
   - 8-pin ceramic DIP 150°C/W
   - 8-pin plastic DIP 105°C/W
   - 8-pin plastic SO 160°C/W
   - 14-pin ceramic DIP 100°C/W
   - 14-pin plastic DIP 80°C/W
   - 16-pin plastic SO 90°C/W
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A/ 5534/5534A			UNIT
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current per op amp			4	6.5		4	8	mA
		Over temperature			9			10	mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	$R_L \geqslant 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing 5534 only	$R_L \geqslant 600\Omega$	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		V
		$R_L \geqslant 600\Omega$, $V_S = \pm 18V$	±15	±16		±15	±16		V
		$R_L \geqslant 2k\Omega$	±13	±13.5		±13	±13.5		V
		Over temperature	±12	±12.5		±12	±12.5		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES:

1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$.
2. For SE5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 15V$, unless otherwise specified.

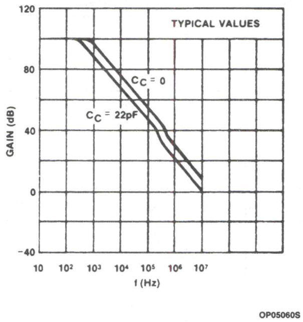
SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A/ 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ closed-loop $f = 10kHz$, $R_L = 600\Omega$, $C_C = 22pF$		0.3			0.3		Ω
	Transient response	Voltage-follower, $V_{IN} = 50mV$ $R_L = 600\Omega$, $C_C = 22pF$, $C_L = 100pF$							
t_R	Rise time			20			20		ns
	Overshoot			20			20		%
	Transient response	$V_{IN} = 50mV$, $R_L = 600\Omega$ $C_C = 47pF$, $C_L = 500pF$							
t_R	Rise time			50			50		ns
	Overshoot			35			35		%
A_V	Gain	$f = 10kHz$, $C_C = 0$ $f = 10kHz$, $C_C = 22pF$		6 2.2			6 2.2		V/mV V/mV
BW	Gain bandwidth product	$C_C = 22pF$, $C_L = 100pF$		10			10		mHz
SR	Slew rate	$C_C = 0$ $C_C = 22pF$		13 6			13 6		V/μs V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$, $C_C = 0$ $V_{OUT} = \pm 10V$, $C_C = 22pF$ $V_{OUT} = \pm 14V$, $R_L = 600\Omega$ $C_C = 22pF$, $V_{CC} = \pm 18V$		200 95 70			200 95 70		kHz kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 15V$, unless otherwise specified.

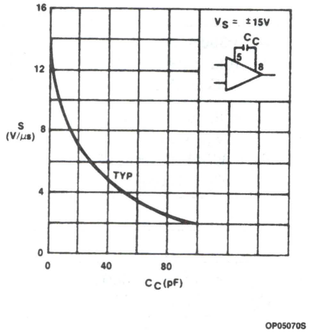
SYMBOL	PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	$f_O = 30Hz$ $f_O = 1kHz$		7 4			5.5 3.5	7 4.5	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
I_{NOISE}	Input noise current	$f_O = 30Hz$ $f_O = 1kHz$		2.5 0.6			1.5 0.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Broadband noise figure	$f = 10Hz - 20kHz$, $R_S = 5k\Omega$					0.9		dB
	Channel separation	$f = 1kHz$, $R_S = 5k\Omega$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

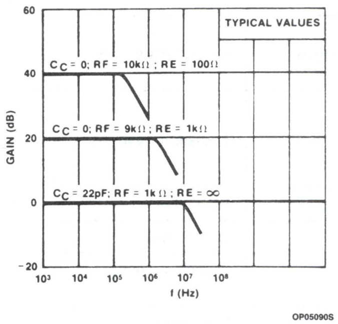
Open-Loop Frequency Response



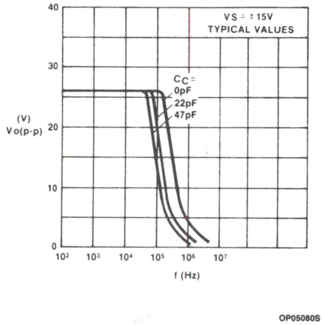
Slew Rate as a Function of Compensation Capacitance



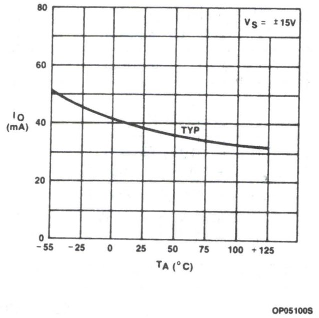
Closed-Loop Frequency Response



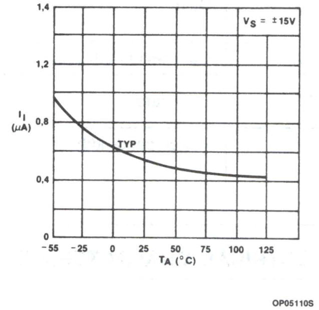
Large-Signal Frequency Response



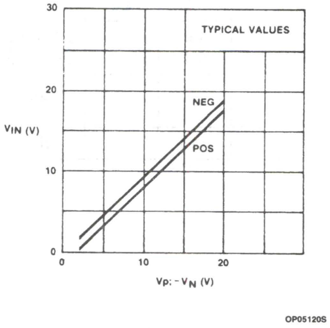
Output Short-Circuit Current



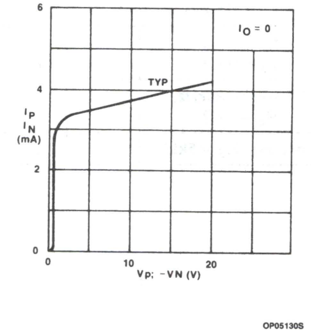
Input Bias Current



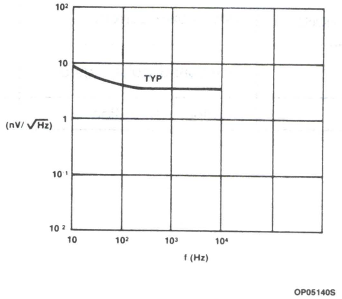
Input Common-Mode Voltage Range



Supply Current per Op Amp

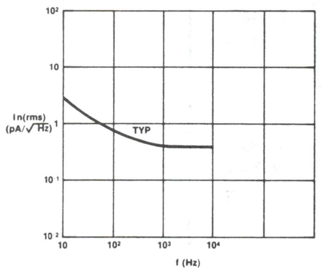


Input Noise Voltage Density



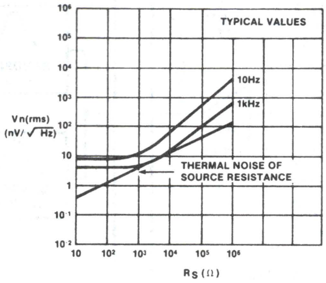
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Input Noise Current Density



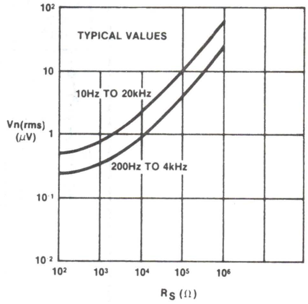
OP05150S

Total Input Noise Density



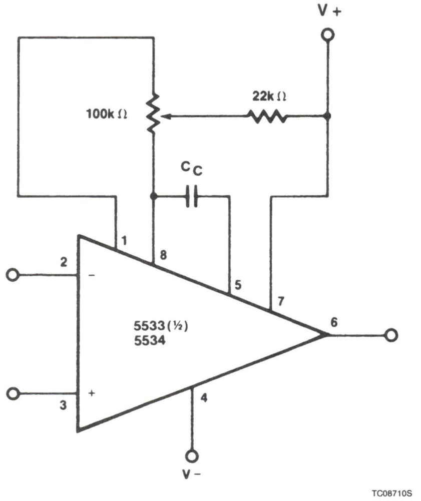
OP05160S

Broadband Input Noise Voltage

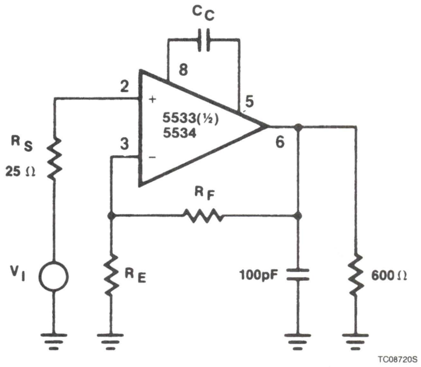


OP05170S

TEST LOAD CIRCUITS

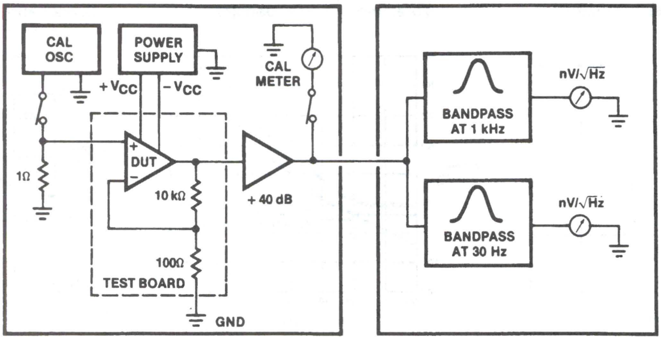

V+
100kΩ
22kΩ
CC
1
8
5
7
2
3
4
6
5533(½)
5534
V−
TC08710S

Frequency Compensation and Offset Voltage Adjustment Circuit


CC
8
2
5
5533(½)
5534
3
6
RS
25 Ω
RF
VI
RE
100pF
600Ω
TC08720S

Closed-Loop Frequency Response

NOISE TEST BLOCK DIAGRAM


CAL OSC
POWER SUPPLY
CAL METER
+VCC
−VCC
DUT
1Ω
10 kΩ
100Ω
TEST BOARD
GND
+40 dB
BANDPASS AT 1 kHz
BANDPASS AT 30 Hz
nV/√Hz
nV/√Hz

BD02960S

Signetics

Linear Products

AN142
Audio Circuits Using the NE5532/33/34

Application Note

AUDIO CIRCUITS USING THE NE5532/33/34

The following will explain some of Signetics' low noise op amps and show their use in some audio applications.

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally-compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

APPLICATIONS

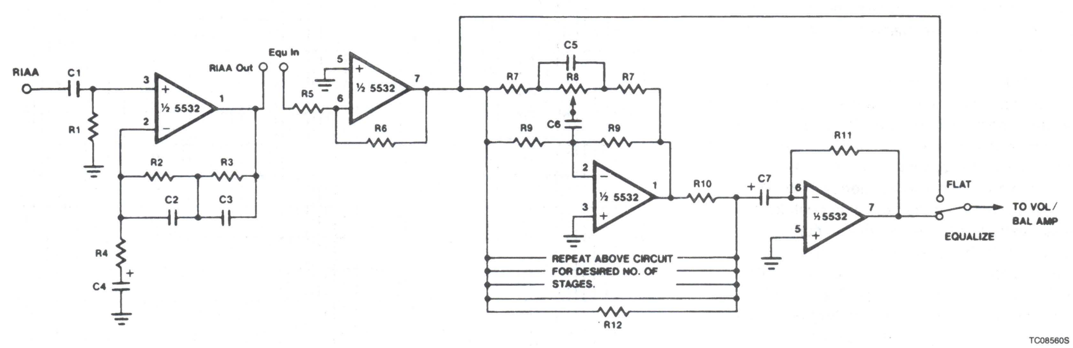
The Signetics 5532 High-Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion. The circuit included in this application note has been assembled on a PC board, and tested with actual audio input devices (Tuner and Turntable). It consists of an RIAA (Recording Industry Association of America) preamp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA preamp section is a standard compensation configuration with low frequency boost provided by the Magnetic cartridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the preamplifier and the equalizer section. Because the 5532 is internally-compensated, no external compensation is required. The 5-band active filter section is actually five individual active filters with the same feedback design for all five. The main difference in all five stages is the values of C5 and C6, which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5 equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

RIAA EQUALIZATION AUDIO PREAMPLIFIER USING NE5532A

With the onset of new recording techniques with sophisticated playback equipment, a new breed of low noise operational amplifiers was developed to complement the state-of-the-art in audio reproduction. The first ultra-low noise op amp introduced by Signetics was called the NE5534A. This is a single operational amplifier with less than $4nV/\sqrt{Hz}$ input noise voltage. The NE5534A is internally-compensated at a gain of three. This device has been used in many audio preamp and equalizer (active filter) applications since its introduction early last year.



COMPONENT VALUES

R1	1meg	C1	0.22µF	R5	100k	C5	SEE TABLE	R9	SEE TABLE
R2	100k	C2	750pF	R6	100k	C6	SEE TABLE	R10	100k
R3	1meg	C3	0.0033µF	R7	SEE TABLE	C7	2.2µF	R11	100k
R4	1.1k	C4	33µF	R8	(pot) SEE TABLE			R12	20k (5 STAGES)

Figure 1. RIAA — Equalizer Schematic

Audio Circuits Using the NE5532/33/34

COMPONENT VALUES FOR FIGURE 1

R8 = 25k R7 = 2.4k R9 = 240k			R8 = 50k R7 = 5.1k R9 = 510k			R8 = 100k R7 = 10k R9 = 1meg		
f_O	C5	C6	f_O	C5	C6	f_O	C5	C6
23Hz	1µF	0.1µF	25Hz	0.47µF	0.047µF	12Hz	0.47µF	0.047µF
50Hz	0.47µF	0.047µF	36Hz	0.33µF	0.033µF	18Hz	0.33µF	0.033µF
72Hz	0.33µF	0.033µF	54Hz	0.22µF	0.022µF	27Hz	0.22µF	0.022µF
108Hz	0.22µF	0.022µF	79Hz	0.15µF	0.015µF	39Hz	0.15µF	0.015µF
158Hz	0.15µF	0.015µF	119Hz	0.1µF	0.01µF	59Hz	0.1µF	0.01µF
238Hz	0.1µF	0.01µF	145Hz	0.082µF	0.0082µF	72Hz	0.082µF	0.0082µF
290Hz	0.082µF	0.0082µF	175Hz	0.068µF	0.0068µF	87Hz	0.068µF	0.0068µF
350Hz	0.068µF	0.0068µF	212Hz	0.056µF	0.0056 µF	106Hz	0.056µF	0.0056µF
425Hz	0.056µF	0.0056µF	253Hz	0.047µF	0.0047µF	126Hz	0.047µF	0.0047µF
506Hz	0.047µF	0.0047µF	360Hz	0.033µF	0.0033µF	180Hz	0.033µF	0.0033µF
721Hz	0.033µF	0.0033µF	541Hz	0.022µF	0.0022µF	270Hz	0.022µF	0.0022µF
1082Hz	0.022µF	0.0022µF	794Hz	0.015µF	0.0015µF	397Hz	0.015µF	0.0015µF
1588Hz	0.015µF	0.0015µF	1191Hz	0.01µF	0.001µF	595Hz	0.01µF	0.001µF
2382Hz	0.01µF	0.001µF	1452Hz	0.0082µF	820pF	726Hz	0.0082µF	820pF
2904Hz	0.0082µF	820pF	1751Hz	0.0068µF	680pF	875Hz	0.0068µF	680pF
3502Hz	0.0068µF	680pF	2126Hz	0.0056µF	560pF	1063Hz	0.0056µF	560pF
4253Hz	0.0056µF	560pF	2534Hz	0.0047µF	470pF	1267Hz	0.0047µF	470pF
5068Hz	0.0047µF	470pF	3609Hz	0.0033µF	330pF	1804Hz	0.0033µF	330pF
7218Hz	0.0033µF	330pF	5413Hz	0.0022µF	220pF	2706Hz	0.0022µF	220pF
10827Hz	0.0022µF	220pF	7940Hz	0.0015µF	150pF	3970Hz	0.0015µF	150pF
15880Hz	0.0015µF	150pF	11910Hz	0.001µF	100pF	5955Hz	0.001µF	100pF
23820Hz	0.001µF	100pF	14524Hz	820pF	82pF	7262Hz	820pF	82pF
			17514Hz	680pF	68pF	8757Hz	680pF	68pF
			21267Hz	560pF	56pF	10633Hz	560pF	56pF
						12670Hz	470pF	47pF
						18045Hz	330pF	33pF

Many of the amplifiers that are being designed today are DC-coupled. This means that very low frequencies (2 – 15Hz) are being amplified. These low frequencies are common to turntables because of rumble and tone arm resonancies. Since the amplifiers can reproduce these sub-audible tones, they become quite objectionable because the speakers try to reproduce these tones. This causes non-linearities when the actual recorded material is amplified and converted to sound waves.

The RIAA has proposed a change in its standard playback response curve in order to alleviate some of the problems that were previously discussed. The changes occur primarily at the low frequency range with a slight modification to the high frequency range (See Figure 2). Note that the response peak for the bass section of the playback curve now occurs at 31.5Hz and begins to roll off below that frequency. The roll-off occurs by introducing a fourth RC network with a 7950µs time constant to the three existing networks that make up the equalization circuit. The high end of the equalization curve is extended to 20kHz, because recordings at these frequencies are achievable on many current discs.

NE5533/34 DESCRIPTION

the 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers.

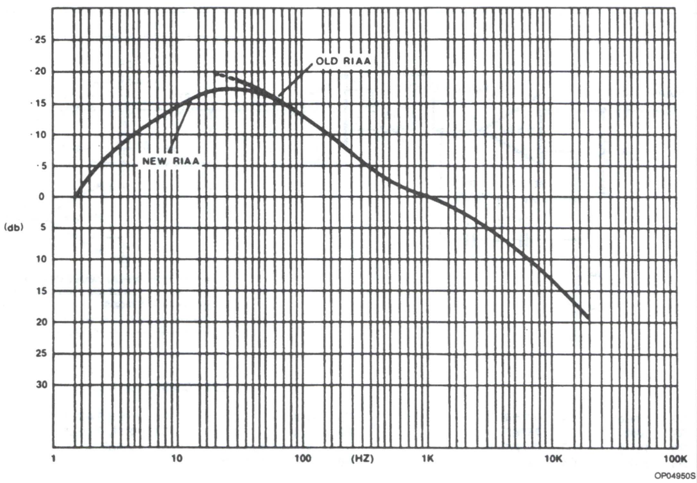
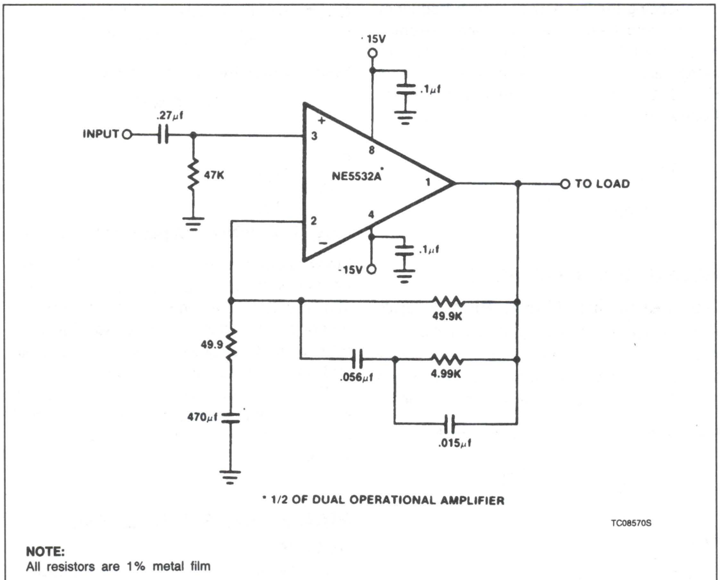


Figure 2. Proposed RIAA Playback Equalization

Audio Circuits Using the NE5532/33/34 AN142


15V
.1µf
.27µf
INPUT
47K
NE5532A*
3
8
1
2
4
TO LOAD
.1µf
-15V
49.9K
49.9
.056µf
4.99K
470µf
.015µf
* 1/2 OF DUAL OPERATIONAL AMPLIFIER
TC08570S

NOTE:
All resistors are 1% metal film

Figure 3. RIAA Phonograph Preamplifier Using the NE5532A

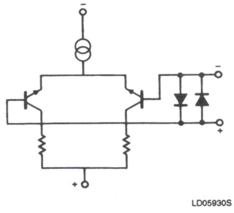
The op amps are internally-compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

APPLICATIONS

Diode Protection of Input

The input leads of the device are protected from differential transients above ±0.6V by internal back-to-back diodes. Their presence imposes certain limitations on the amplifier dynamic characteristics related to closed-loop gain and slew rate.

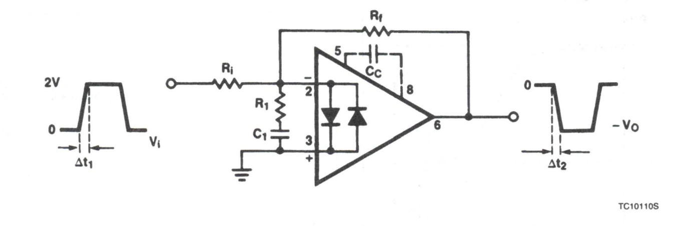
Consider the unity gain follower as an example:



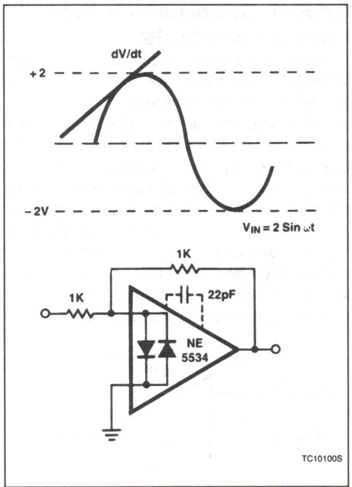
Assume a signal input square wave with dV/dt of 250V/µs and 2V peak amplitude as shown. If a 22pF compensation capacitor is inserted and the R_1 C_1 circuit deleted, the device slew rate falls to approximately 7V/µs. The input waveform will reach 2V/250V/µs or 8ns, while the output will have changed (8×10^{-3}) only 56mV. The differential input signal is then ($V_{IN} - V_O$) $R_I/R_I + R_F$ or approximately 1V.

The diode limiter will definitely be active and output distortion will occur; therefore, $V_{IN} < 1V$ as indicated.

Next, a sine wave input is used with a similar circuit.


2V
0
Δt₁
Vᵢ
Rᵢ
R_f
5
Cc
R₁
C₁
2
3
8
6
0
-V₀
Δt₂
TC10110S

NOTE
$R_F = R_I = 1k\Omega$


dV/dt
+2
-2V
V_IN = 2 Sin ωt
1K
1K
22pF
NE 5534
TC10100S

The slew rate of the input waveform now depends on frequency and the exact expression is

$$\frac{dv}{dt} = 2\omega \cos \omega t$$

The upper limit before slew rate distortion occurs for *small-signal* ($V_{IN} < 100mV$) conditions is found by setting the slew rate to 7V/µs. That is:

$$7 \times 10^6 V/\mu s = 2\omega \cos \omega t$$

at $\omega t = 0$

$$\omega_{LIMIT} = \frac{7 \times 10^6}{2} = 3.5 \times 10^6 \text{ rad/s}$$

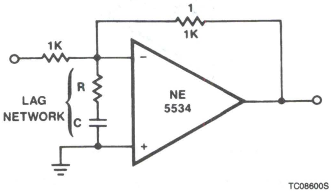
$$f_{LIMIT} = \frac{3.5 \times 10^6}{2\pi} \cong 560kHz$$

Audio Circuits Using the NE5532/33/34

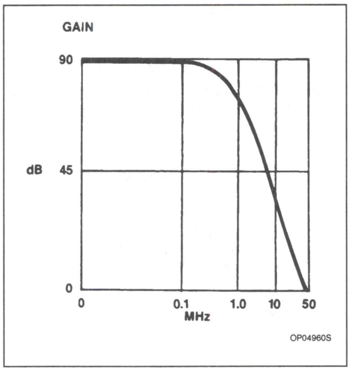
AN142

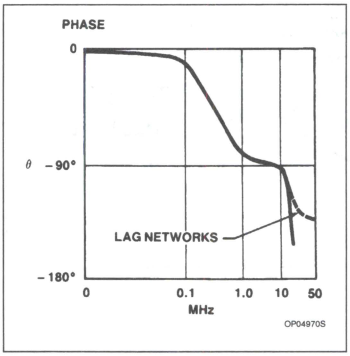
External Compensation Network Improves Bandwidth

By using an external lead-lag network, the follower circuit slew rate and small-signal bandwidth can be increased. This may be useful in situations where a closed-loop gain less than 3 to 5 is indicated. A number of examples are shown in subsequent figures. The principle benefit of using the network approach is that the full slew rate and bandwidth of the device is retained, while impulse-related parameters such as damping and phase margin are controlled by choosing the appropriate circuit constants. For example, consider the following configuration:



The major problem to be overcome is poor phase margin leading to instability.





By choosing the lag network break frequency one decade below the unity gain crossover frequency (30 – 50MHz), the phase and gain margin are improved. An appropriate value for R is 270Ω. Setting the lag network break frequency at 5MHz, C may be calculated

$$C = \frac{1}{2\pi \cdot 270 \cdot 5 \times 10^6}$$

$$= 118\text{pF}$$

RULES AND EXAMPLES

Compensation Using Pins 5 and 8 (Limited Bandwidth and Slew Rate)

A single-pole and zero inserted in the transfer function will give an added 45° of phase margin, depending on the network values.

Calculating the Lead-Lag Network

$$C_1 = \frac{1}{2\pi F_1 R_1} \quad \text{Let } R_1 = \frac{R_{IN}}{10}$$

where

$$F_1 = \frac{1}{10}\,(\text{UGBW})$$

UGBW = 30MHz

External Compensation for Wide-Band Voltage-Follower

Shunt Capacitance Compensation

$$C_F = \frac{1}{2\pi F_F R_F},\ F_F \cong 30\text{MHz}$$

or

$$C_F \cong \frac{C_{DIST}}{A_{CL}}$$

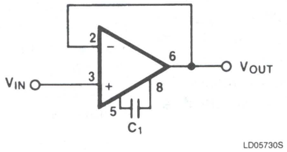
$C_{DIST} \cong$ Distributed Capacitance $\cong$ 2 – 3pF

Many audio circuits involve carefully-tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 7. Operational amplifiers are well suited to these applications because of their high gain and easily-tailored frequency response.

RIAA PREAMP USING THE NE5534

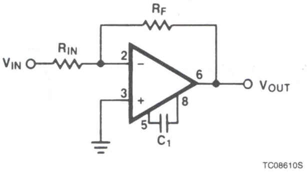
The preamplifier for phono equalization is shown in Figure 8 with the theoretical and actual circuit response.

Low frequency boost is provided by the inductance of the magnetic cartridge with the



NOTES:
$C_1 = C_C(1)$
C_C = 22pF for NE5533/34
C_C = 22pF [See graph under typical performance characteristics]

Figure 4. Unity Gain Non-Inverting Configuration



NOTES:
$R_F = R_{IN}$

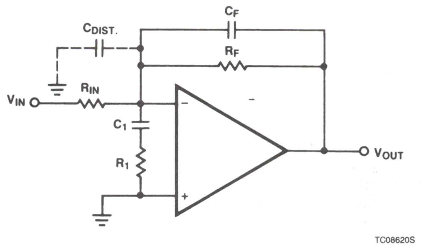
$$C_1 = C_C\left[\frac{R_{IN}}{R_F + R_{IN}}\right] = \frac{C_C}{2} \text{ therefore, } C_1 = 11\text{pF}$$

Figure 5. Unity Gain Inverting Configuration

RC network providing the necessary break points to approximate the theoretical RIAA curve.

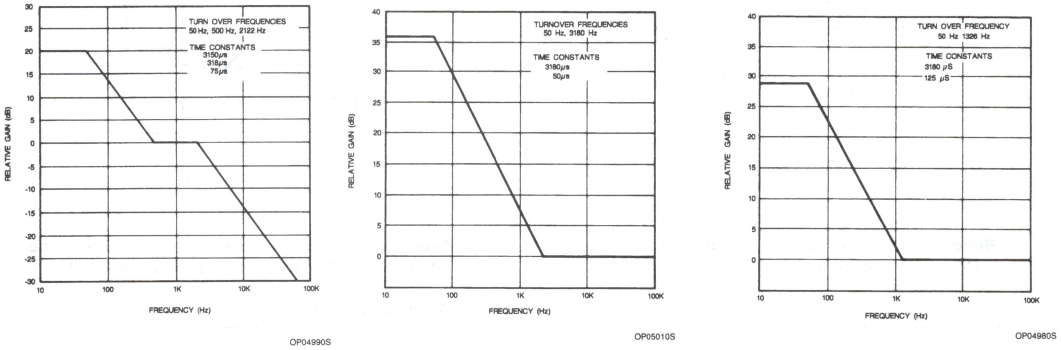
RUMBLE FILTER

Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2-pole Butterworth approach and features switchable break points. With the circuit of Figure 9, any degree of filtering from fairly sharp to none at all is switch-selectable.



NOTE:
Input diodes limit differential to < 0.5V

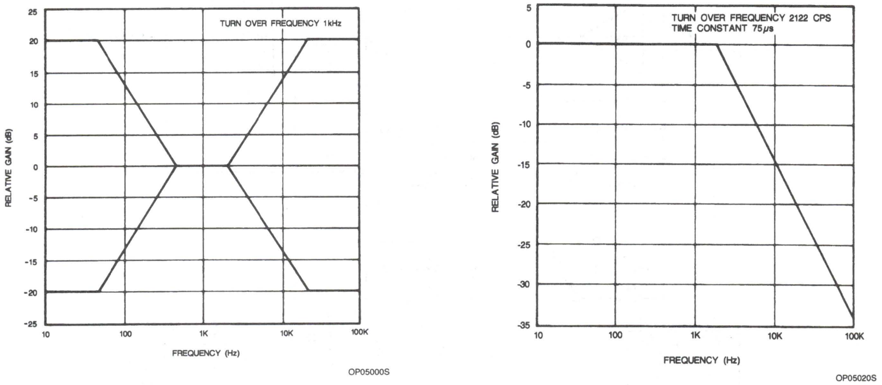
Figure 6. External Compensation for Wideband Voltage Follower



a. RIAA Equalization

b. NAB Standard Playback 7½ IPS

c. 3.75 IPS Tape Equalization



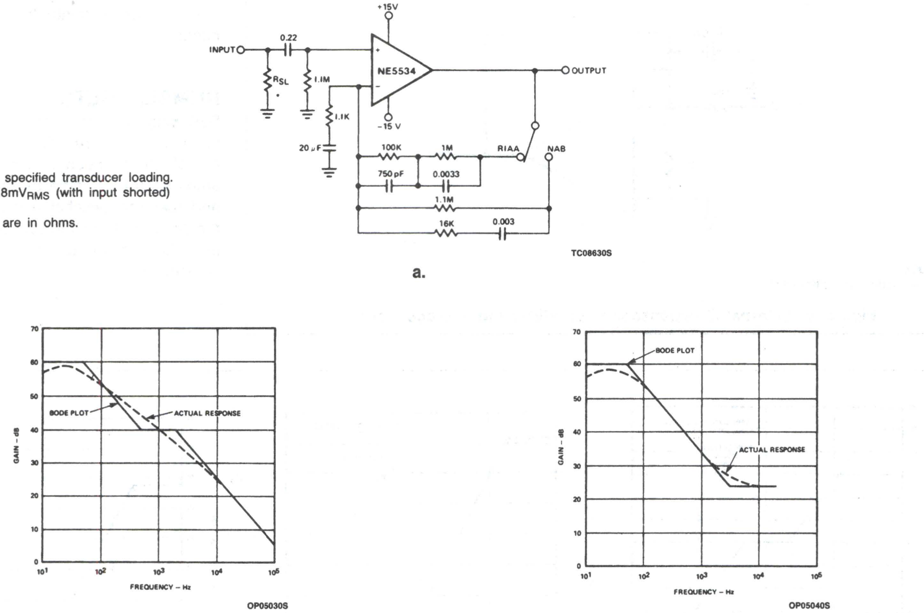
d. Base Treble Control Curve

e. Standard FM Broadcast Equalization

Figure 7

NOTES:
*Select to provide specified transducer loading.
Output Noise ≅ 0.8mV$_{RMS}$ (with input shorted)

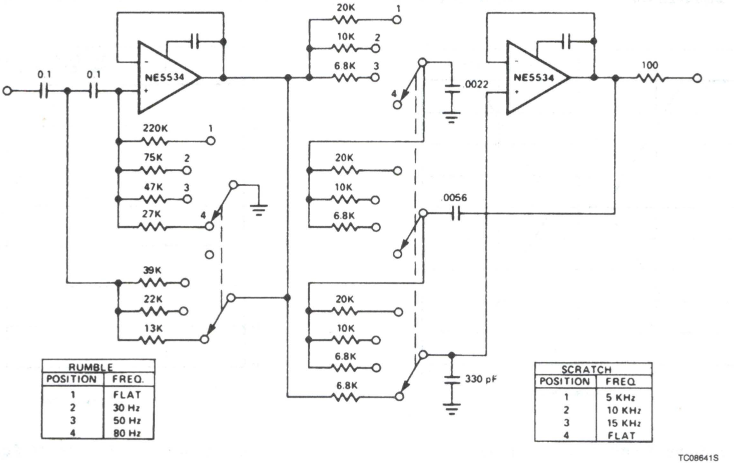
All resistor values are in ohms.


+15V
INPUT
0.22
R_SL
*
1.1M
NE5534
1.1K
20 µF
−15 V
OUTPUT
100K
1M
RIAA
NAB
750 pF
0.0033
1.1M
16K
0.003
TC08630S
a.
70
60
50
40
30
20
10
0
GAIN – dB
BODE PLOT
ACTUAL RESPONSE
10¹
10²
10³
10⁴
10⁵
FREQUENCY – Hz
OP05030S
OP05040S

b. Bode Plot of RIAA Equalization and the Response Realized in an Actual Circuit Using the 531

c. Bode Plot of NAB Equalization and the Response Realized in the Actual Circuit Using the 531

Figure 8. Preamplifier — RIAA/NAB Compensation

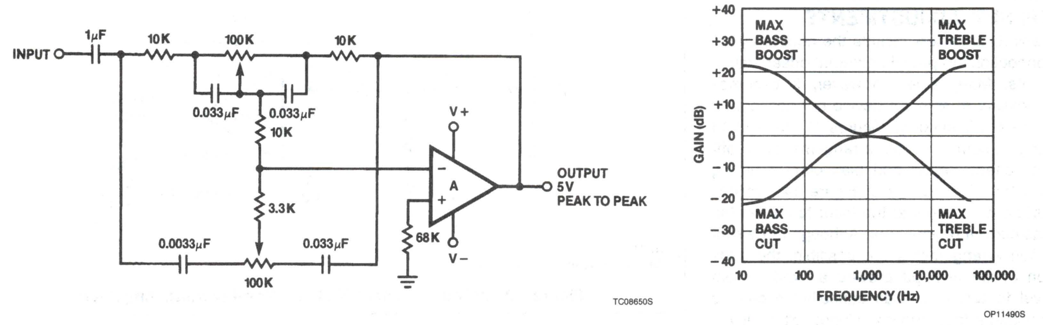

0 1
0 1
NE5534
220K
75K
47K
27K
39K
22K
13K
20K
10K
6.8K
1
2
3
4
0022
0056
330 pF
100
TC08641S

RUMBLE	
POSITION	FREQ.
1	FLAT
2	30 Hz
3	50 Hz
4	80 Hz

SCRATCH	
POSITION	FREQ.
1	5 KHz
2	10 KHz
3	15 KHz
4	FLAT

NOTE:
All resistor values are in ohms.

Figure 9. Rumble/Scratch Filter


INPUT
1µF
10K
100K
10K
0.033µF
0.033µF
10K
3.3K
0.0033µF
0.033µF
100K
V+
V−
A
68K
OUTPUT
5V
PEAK TO PEAK
TC08650S
GAIN (dB)
+40
+30
+20
+10
0
−10
−20
−30
−40
MAX BASS BOOST
MAX TREBLE BOOST
MAX BASS CUT
MAX TREBLE CUT
10
100
1,000
10,000
100,000
FREQUENCY (Hz)
OP11490S

NOTES:

1. Amplifier A may be a NE531 or 301. Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over frequency — 1kHz.
3. Bass boost + 20dB at 20Hz, bass cut − 20dB at 20Hz, treble boost + 19dB at 20Hz, treble cut − 19dB at 20Hz.

All resistor values are in ohms.

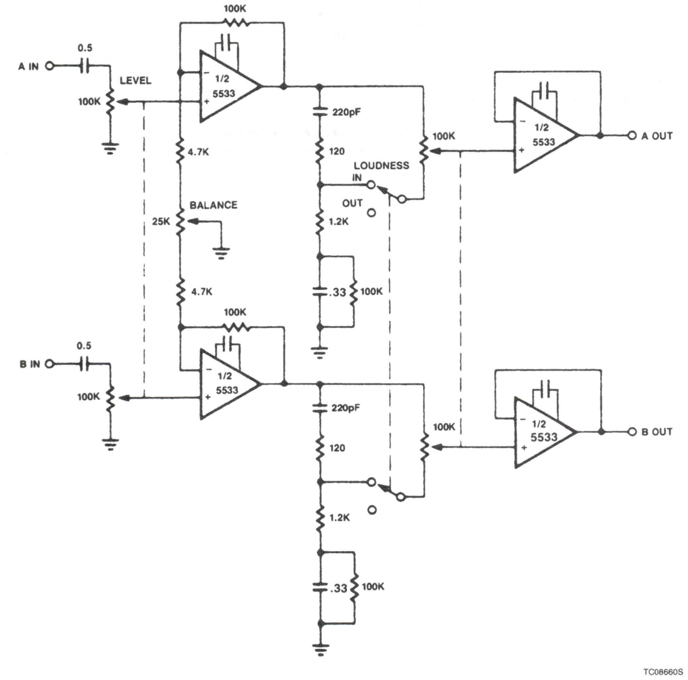
Figure 10. Tone Control Circuit for Operational Amplifiers

TONE CONTROL

Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones, dependent upon listener preference. The circuit of Figure 10 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

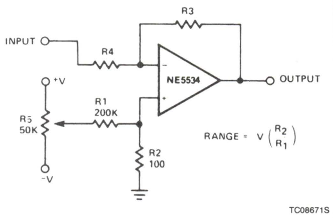
BALANCE AND LOUDNESS AMPLIFIER

Figure 11 shows a combination of balance and loudness controls. Due to the non-linearity of the human hearing system, the low frequencies must be boosted at low listening levels. Balance, level, and loudness controls provide all the listening controls to produce the desired music response.


A IN
0.5
100K
LEVEL
100K
1/2
5533
220pF
4.7K
120
LOUDNESS
IN
OUT
BALANCE
25K
1.2K
4.7K
.33
100K
100K
1/2
5533
A OUT
B IN
0.5
100K
100K
1/2
5533
220pF
120
1.2K
.33
100K
100K
1/2
5533
B OUT
TC08660S

NOTE:
All resistor values are in ohms.

Figure 11. Balance Amplifier With Loudness Control

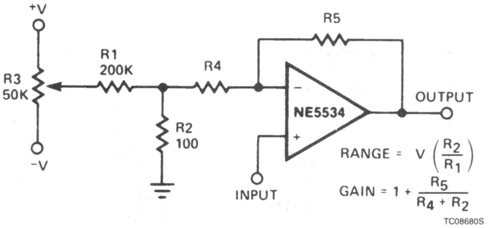

INPUT
R3
R4
NE5534
OUTPUT
+V
R1
200K
R5
50K
−V
R2
100
RANGE = V (R2/R1)
TC08671S

NOTE:
All resistor values are in ohms.

Figure 12. Universal Offset Null for Inverting Amplifiers

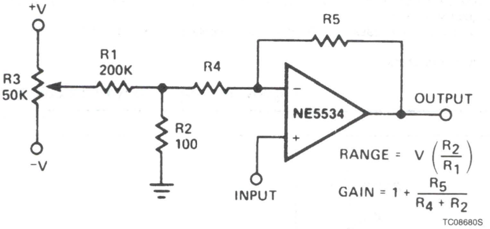
VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times, however, it becomes necessary to select a device not possessing external adjustments. Figures 12, 13, and 14 suggest some possible arrangements for offset voltage adjust and bias current nulling circuitry. The circuitry of Figure 14 provides sufficient current into the input to cancel the bias current requirement. Although more simplified arrangements are possible, the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.


+V
R3
50K
-V
R1
200K
R4
R2
100
R5
NE5534
OUTPUT
INPUT
RANGE = $V\left(\frac{R_2}{R_1}\right)$
GAIN = $1 + \frac{R_5}{R_4 + R_2}$
TC08680S

NOTE:
All resistor values are in ohms.

Figure 13. Universal Offset Null for Non-Inverting Amplifiers


+V
R3
50K
-V
R1
200K
R4
R2
100
R5
NE5534
OUTPUT
INPUT
RANGE = $V\left(\frac{R_2}{R_1}\right)$
GAIN = $1 + \frac{R_5}{R_4 + R_2}$
TC08680S

NOTE:
Select R_2 & R_3 for desired current

Figure 14. Bias Current Compensation

Signetics

Linear Products

NE/SA5230
Low Voltage Operational Amplifier

Product Specification

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 115dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and $23nV/\sqrt{Hz}$ noise specification.

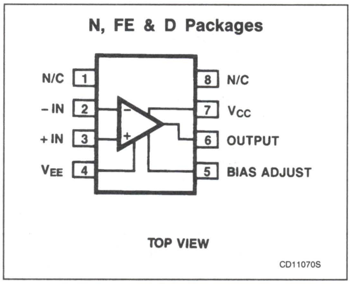
FEATURES

- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **V_{OUT} within 100mV of both rails**

APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO package	0 to +70°C	NE5230D
8-Pin Ceramic DIP	0 to +70°C	NE5230FE
8-Pin Plastic DIP	0 to +70°C	NE5230N
8-Pin Plastic SO package	−40°C to +85°C	SA5230D
8-Pin Plastic DIP	−40°C to +85°C	SA5230N

Low Voltage Operational Amplifier

NE/SA5230

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	
V_{EE}	Dual supply voltage	±9	V
	Differential input voltage[1]	±9 (18)	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	$V_{CC} + 0.5$	V
V_{CM}	Common-mode voltage (negative)	$V_{EE} - 0.5$	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	Output short-circuit duration to either power supply pin[2, 3]	Indefinite	sec
T_{STG}	Storage temperature	-65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	$V_{CC} + 0.25$	V
Common-mode voltage (negative)	$V_{EE} - 0.25$	V
Temperature		
NE grade	0 to 70	°C
SA grade	-40 to 85	°C

NOTES:

1. Can exceed the supply voltages when $V_S \leqslant \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions.
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

DC ELECTRICAL CHARACTERISTICS Unless otherwise specified, ±0.9V ⩽ V_S ⩽ ±7.5V or equivalent single supply, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS	BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
V_{OS}	Offset voltage		T_A = 25°C	Any		0.4	3	mV
						3	4	mW
V_{OS}	Drift			Any		2	5	μV/°C
I_{OS}	Offset current		T_A = 25°C	High		3	50	nA
			T_A = 25°C	Low		3	30	nA
				High			100	nA
				Low			60	nA
I_{OS}	Drift			High		0.5	1.4	nA/°C
				Low		0.3	1.4	nA/°C
I_B	Bias current		T_A = 25°C	High		40	150	nA
			T_A = 25°C	Low		20	60	nA
				High			200	nA
				Low			150	nA
I_B	Drift			High		2	4	nA/°C
				Low		2	4	nA/°C
I_S	Supply current		V_S = ±0.9V, T_A = 25°C	Low		110	160	μA
			T_A = 25°C	High		600	750	μA
				Low			250	μA
				High			800	μA
			V_S = ±7.5V, T_A = 25°C	Low		320	550	μA
			T_A = 25°C	High		1.1	1.6	mA
				Low			600	μA
				High			1.7	mA
V_{CM}	Common-mode input range		V_{OS} ⩽ 6mV, T_A = 25°C	Any	$V^- -0.25$		$V^+ +0.25$	V
				Any	V^-		V^+	V
CMRR	Common-mode rejection ratio		R_S = 10kΩ, V_{CM} = ±7.5V, T_A = 25°C	Any	85	95		dB
			V_S = ±7.5V	Any	80			dB
PSRR	Power supply rejection ratio		T_A = 25°C	High	90	105		dB
			T_A = 25°C	Low	85	95		dB
				High	75			dB
				Low	80			dB
I_L	Load current	source	V_S = ±7.5V	Any	4	8		mA
		sink	V_S = ±7.5V	Any	5	9		mA
		source	V_S = ±0.9V	Any	1	4		mA
		sink	V_S = ±0.9V	Any	3	5		mA
		T_A = 25°C, source	V_S = ±0.9V	High	4	5		mA
		T_A = 25°C, sink	V_S = ±0.9V	High	5	11		mA

DC ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise specified, ±0.9V $\leqslant V_S \leqslant$ ±7.5V or equivalent single supply, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS	BIAS	NE/SA5230			UNIT
				Min	Typ	Max	
A_{VOL}	Large-signal open-loop gain	$R_L = 10k\Omega$, $T_A = 25°C$	High	120	200		V/mV
		$R_L = 10k\Omega$, $T_A = 25°C$	Low	60	150		V/mV
			High	100			V/mV
			Low	50			V/mV
V_{OUT}	Output voltage swing	$V_S = \pm 0.9V$, $R_L = 10k\ \Omega$ $T_A = 25°C$, +SW	Any	750	800		mV
		$T_A = 25°C$, −SW	Any	750	800		mV
		+SW	Any	700			mV
		−SW	Any	700			mV
		$V_S = \pm 7.5V$, $R_L = 10k\Omega$ $T_A = 25°C$, +SW	Any	7.30	7.35		V
		$T_A = 25°C$, −SW	Any	7.32	7.35		V
		+SW	Any	7.25	7.30		V
		−SW	Any	7.30	7.35		V
SR	Slew rate		High		0.25		V/μs
			Low		0.09		V/μs
BW	Inverting unity gain bandwidth	$R_L = 10k\Omega$, $C_L = 1\ 00pF$ $T_A = 25°C$	High		0.6		MHz
		$T_A = 25°C$	Low		0.25		MHz
θ_M	Phase margin	$T_A = 25°C$	Any		70		Deg.
t_S	Settling time	0.1%	High		2		μs
			Low		5		μs
V_{INN}	Input noise	$R_S = 0\Omega$, f = 1kHz	High		22		$nV/\sqrt{Hz}$
			Low				

NOTES:

1. $R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$, $T_A = 25°C$.
2. $V_S = \pm 7.5V$.
3. $V_{CM} = V_S/2$ for SE grade only.

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, $V_{B1} = 0.8V$ at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

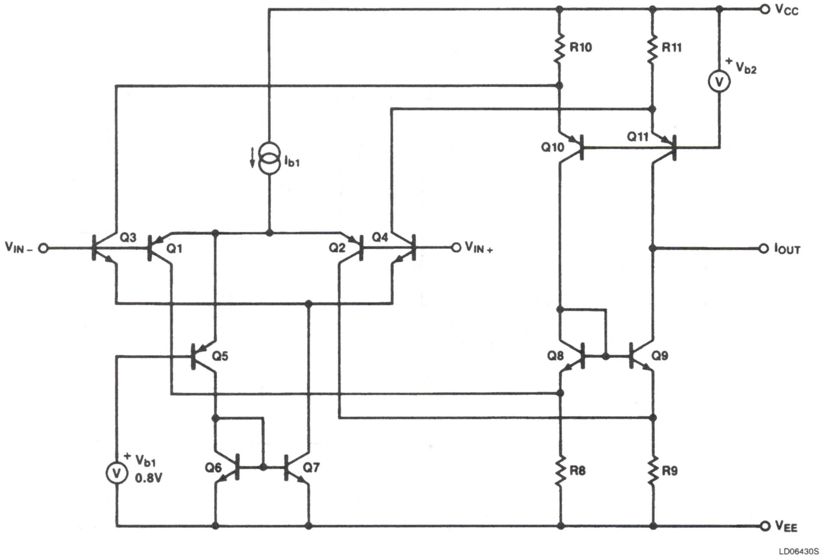


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Signetics does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad (1)$$

Where $T_A \equiv$ Ambient Temperature
T_J = Die Temperature
$P_D \equiv$ Power Dissipation
$= (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv$ Package thermal resistance
= 270°C/W for SO-8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

θ_{JA} = 100°C/W for the plastic DIP;
θ_{JA} = 110°C/W for the ceramic DIP.

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply voltages other than the maximum, see the data

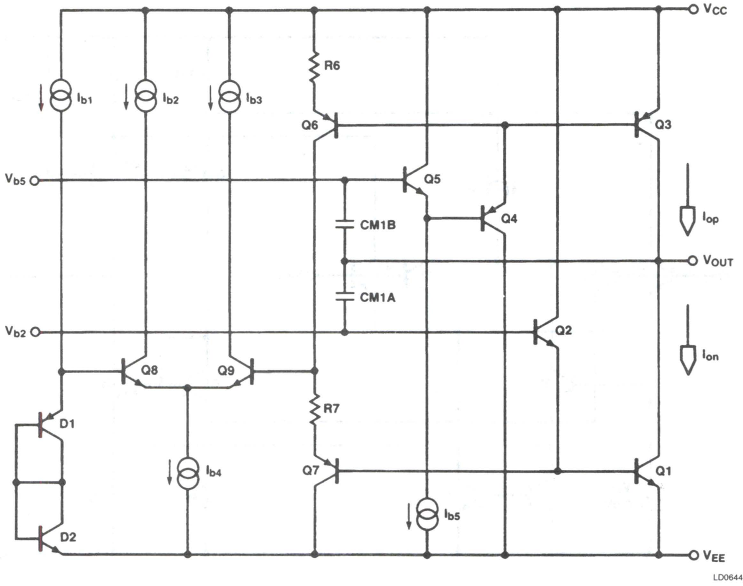


Figure 2. Output Stage

sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100μA to 600μA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5μs at low bias to 2μs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is 0.08V/μs at low bias and 0.25V/μs at high bias.

The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

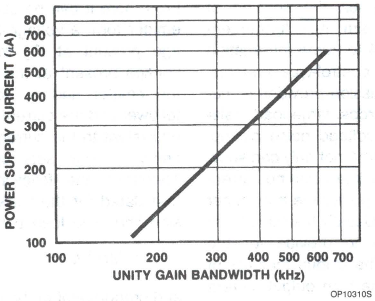
If extremely low signal distortion (< 0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

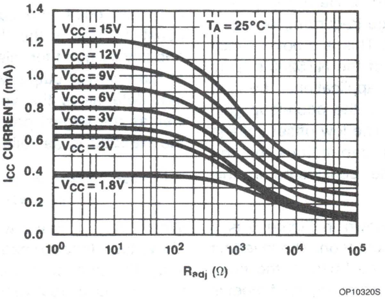
There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is



a. Unity Gain Bandwidth vs Power Supply Current for $V_{CC} = \pm 0.9V$



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3

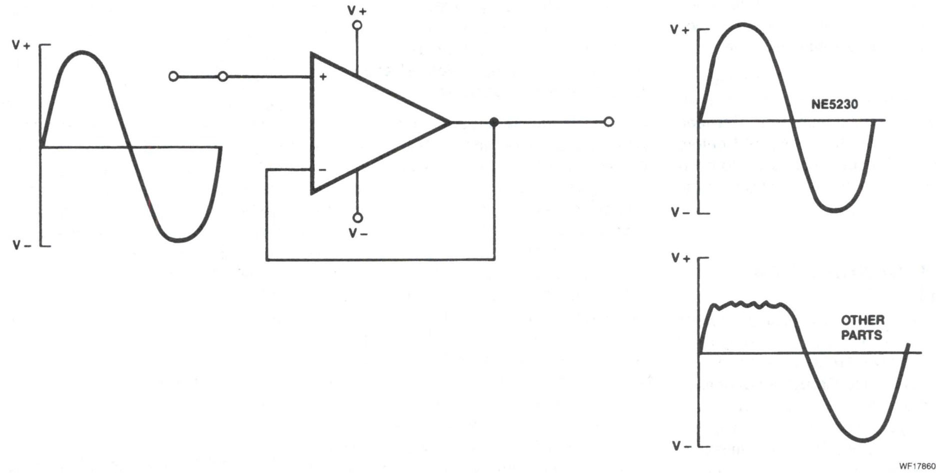


Figure 4. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability

the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4 to 20mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 5. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

The NE5230 circuit shown in Figure 5 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non-inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN}/R_C \qquad (2)$$

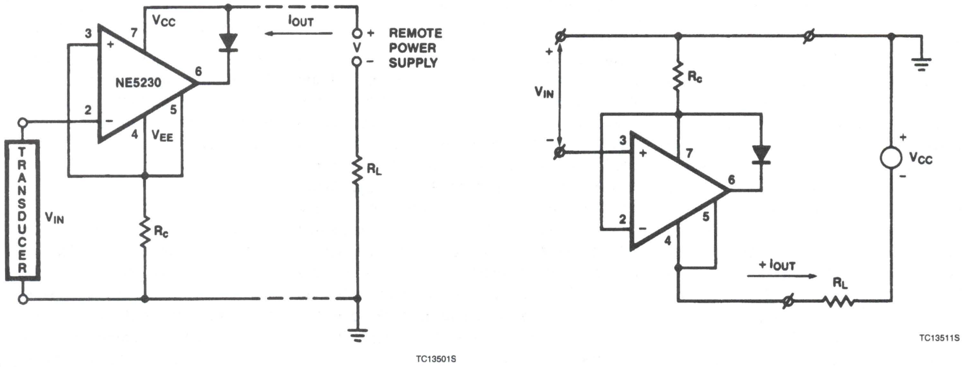
and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

$$R_{L\ max} = [V_{remote\ supply}) - V_{CC\ min} - V_{IN\ max}]/I_L \qquad (3)$$

Where $V_{CC\ min}$ is the worst-case power supply voltage (approximately 1.8V) that will still keep the part operational. As an example, when using a 15V remote power supply, a current sensing resistor of 1Ω, and an input voltage (V_{IN}) of 20mV, the output current (I_L) is 20mA. Furthermore, a load resistance of zero to approximately 650Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8V. With a 15V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20mA output into the 650Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NE5230 transconductance configuration. The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 5 can be used



NOTES:
1. $I_{OUT} = V_{IN/RC}$
2. $R_{L\ max} \simeq \frac{V_{REMOTE} - 1.8V - V_{IN\ max}}{I_{OUT}}$

For $R_C = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

a. The NE5230 as a Remote Transducer Transconductance Amp With 4 – 20mA Current Transmission Output Capability

b. The Same Type of Circuit as Figure 5a, but for Sourcing Current to the Load

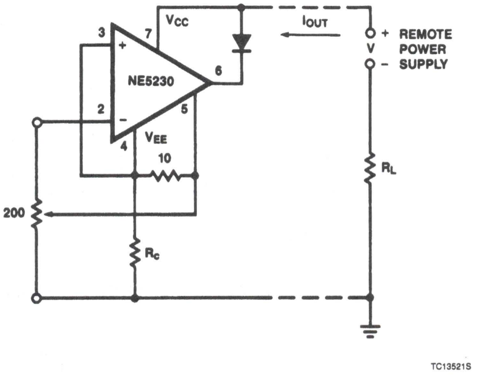
Figure 5

with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 6). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.



NOTES:
1. $I_{OUT} = V_{IN/RC}$
2. $R_L Max \simeq \frac{V_{REMOTE} - 1.8V - V_{IN}Max}{I_{OUT}}$

For $RC = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

Figure 6. NE5230 Remote Temperature Transducer Utilizing 4 – 20mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell in the Device to Make the Part, Itself, a Transducer

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 7. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 8 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

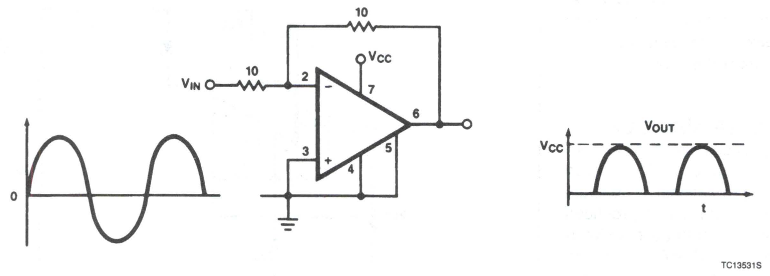
By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 9. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

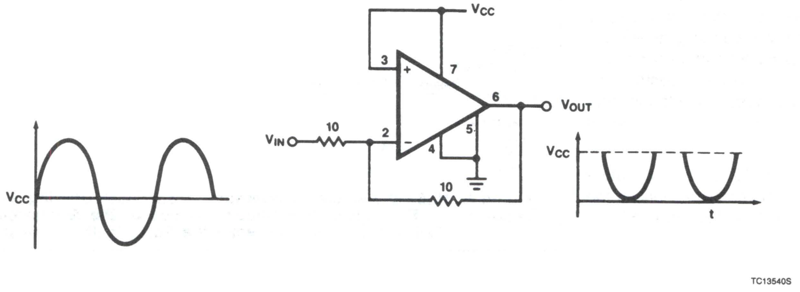
CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs



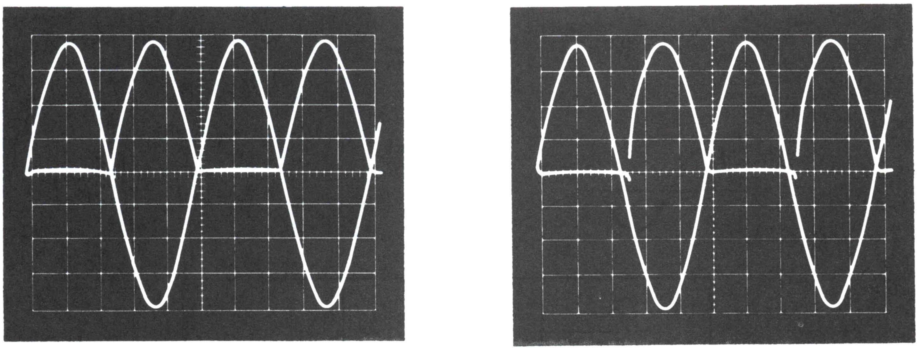
a. Rail-to-Ground Output Swing Referenced to Ground



b. Negative-Going Output Referenced to V_{CC}

Figure 7. Half-Wave Rectifier With Positive-Going Output Swings

where S/N ratios are important. The wide full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105dB.

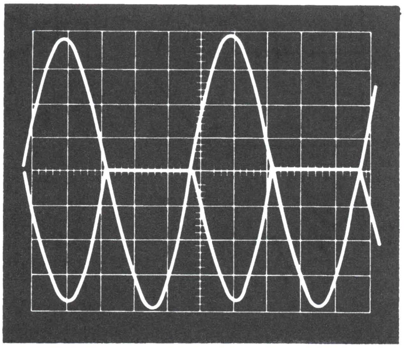


WF17870S

WF17880S

500mV/DIV 200µS/DIV
Biased to Ground

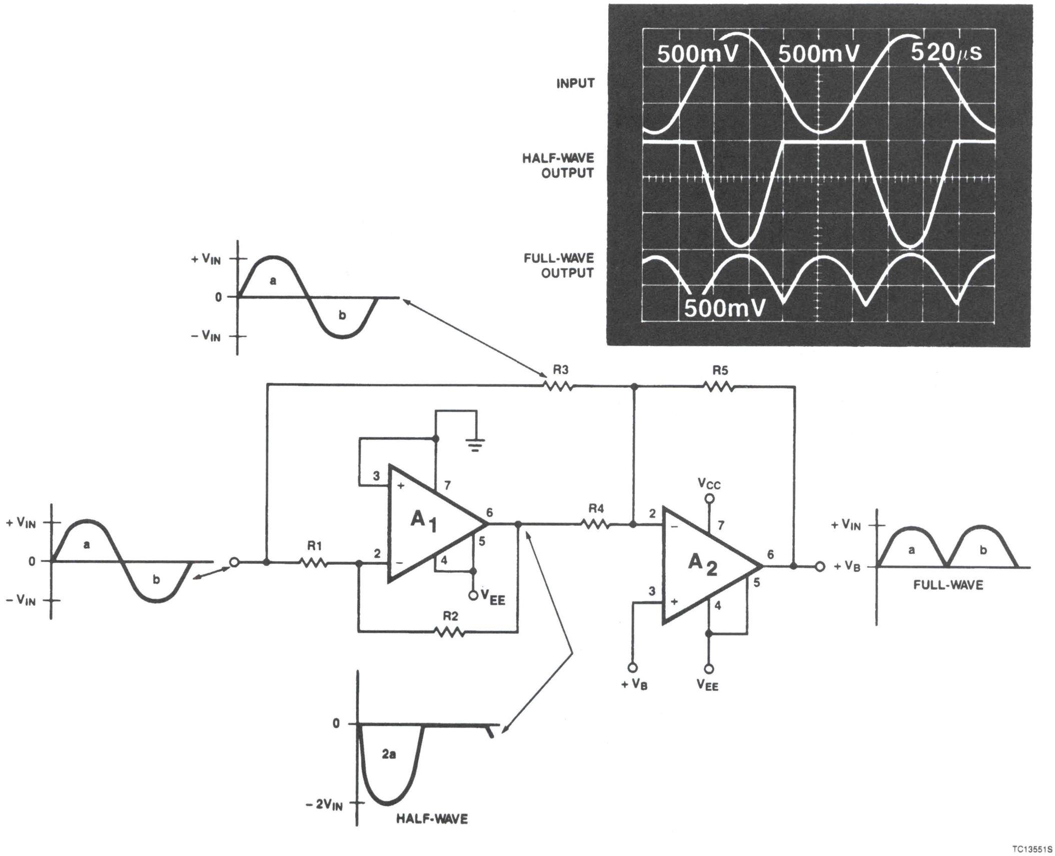
500mV/DIV 20µS/DIV
Biased to Ground



WF17890S

500mV/DIV 20µS/DIV
Biased to Positive Rail

Figure 8. Performance Waveforms for the Circuits in Figure 7. Good Response is Shown at 1 and 10kHz for Both Circuits Under Full Swing With a 2V Supply


500mV
500mV
520µs
INPUT
HALF-WAVE OUTPUT
FULL-WAVE OUTPUT
500mV
+VIN
0
-VIN
a
b
R3
R5
R1
R2
R4
A1
A2
VEE
VCC
+VB
VEE
2
3
4
5
6
7
0
-2VIN
2a
HALF-WAVE
FULL-WAVE
+VIN
+VB
TC13551S

NOTES:
R2 = 2 R1
R4 = R5 = R3
+V$_B$ will vary output reference.
For single supply operation V$_{EE}$ can be grounded on A2.

Figure 9. Adding an Inverting Summer to the Input and Output of the Half-Wave Rectifier will Result in Full-Wave

REFERENCES

Johan H. Huijsing, "Multi-stage Amplifier with Capacitive Nesting for Frequency Compensation," U.S. Patent Application Serial No. 602.234, filed April 19, 1984.

Bob Blauschild, "Differential Amplifier with Rail-to-Rail Capability," U.S. Patent Application Serial No. 525.181, filed August 23, 1983.

Operational Amplifiers — Characteristics and Applications, Robert G. Irvine, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 1981.

Transducer Interface Handbook — A Guide to Analog Signal Conditioning, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

Signetics

Linear Products

AN1511

Low-Voltage Gated Function Generator: NE5230

Application Note

Author: Tony Aguilar

INTRODUCTION

Described herein is a low-voltage, gated function generator using the NE5230 and two AA batteries. The outputs are a square, triangular and sine wave. The sine wave-generating circuit and the square and triangular circuits are independent. Some ideas for refinement of the circuits are also presented.

APPLICATIONS

The use of signal sources is universal. Over the years, a great many practical circuits have been developed which have numerous desirable features. These circuits are typified by high power outputs, or speed, or precision, or combinations of these. They are housed in rugged, handsome cases and are available for a few hundred dollars. Most require AC line cords and are somewhat cumbersome to use. With the advent of low-voltage op amps such as the NE5230, it is now possible to design good, stable, battery-operated signal sources.

SINE WAVE GENERATOR

The circuit used is a Wien bridge sine wave oscillator. This circuit has been used since the days of vacuum tubes (see Figure 1). It is simple, stable and requires few components. The circuit utilizes both positive and negative feedback to achieve balanced operation. The oscillator will stop working if too much negative feedback is used and will saturate in both states if too much positive feedback is used. In the practical implementation, some non-linear element must be employed to realize this stable condition. The gain of the amplifier must be large enough at the frequency of oscillation to make the input excursions small enough to be compensable by this non-linear element. Among others, diodes and FETs have been used to accomplish this. One of the most popular is the lamp; small, inexpensive and readily available, its voltage variable resistance makes it an ideal candidate for this application. It works like this: as the negative feedback voltage increases across the lamp, its resistance increases, and thereby reduces the output voltage. When the output voltage decreases, the amount of negative feedback voltage across the lamp decreases and thereby increases the resistance of the lamp. This balancing act continues until a stable condition is achieved. It is important to note that the lamp resistance is changing due to the thermal effects caused by the changing voltage across it. The frequency of oscillation is determined by:

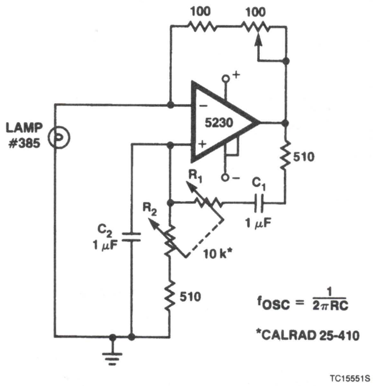


Figure 1. Sine Wave Generator

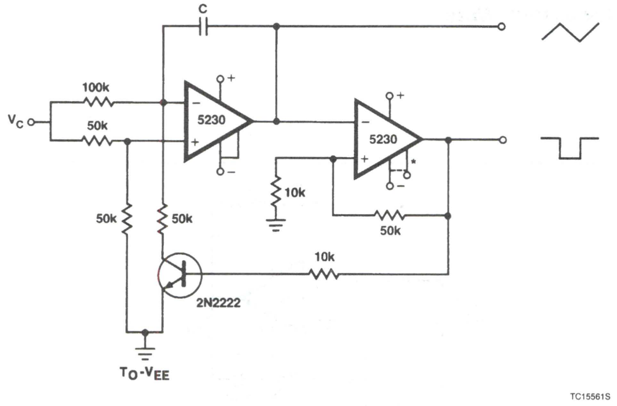
$$f_{OSC} = \frac{1}{2\pi RC}$$

VCO

Another classic oscillator circuit uses a comparator and an integrator. The output of the comparator is fed back to the input of the integrator. The output of the integrator is connected to the input of the comparator. Upon application of power, the comparator output goes into one state or the other. This comparator output voltage is fed back into the input of the integrator which begins ramping up or down, depending on the polarity of the first pulse from the comparator. When the voltage threshold of the comparator is reached, the output changes state. The cycle then repeats.

If an inversion in the feedback loop can be achieved, and external energy can be introduced at the right time, some interesting modifications of the previously described circuit will result — namely, a voltage-controlled oscillator. It works as follows: the transistor inverts the output of the comparator. This voltage is presented to the inverting input of the integrator to begin the cycle. When the comparator threshold is reached, the comparator changes state as before. This time, however, because the external applied voltage to the same inverting input is present, the amount of current available to the input is controlled by the external voltage and not by the feedback voltage. Once the component values are selected, the applied voltage, V_C, sets the frequency of oscillation because the current available to the integrating capacitor determines the charging time constant and, therefore, the frequency. The more positive the V_C, the more current that is available and the higher the frequency of oscillation. The converse is also true with minor differences. It is interesting to note here that other low-voltage amplifiers are not able to perform as well as the NE5230 in this circuit. One reason is that the NE5230 input voltage swing is able to exceed the rails by 250mV and still operate within its linear region. For a given set of conditions, then, the frequency range of the NE5230 is wider than conventional low-voltage op amps. The frequency of this circuit can also be changed by changing the value of the integrating capacitor. The smaller the capacitor, the higher the frequency for a given set of conditions.

Low-Voltage Gated Function Generator: NE5230 AN1511



NOTE:
*See text.

Figure 2. Function Generator

PERFORMANCE

The circuit in Figure 2 is the complete low-voltage function generator. The measurements were taken at room temperature with only two AA batteries supplying the power. The outputs were loaded with 200Ω for the sine and triangular wave outputs and 50Ω for the square wave output. The output voltage for the sine wave was ± 1V. The square wave output swung from rail to rail while the output voltage of the triangular wave varied with the input voltage, V_C. This was due, of course, to the collector-emitter voltage requirements of the transistor.

The distortion of the Wien bridge was 0.015% at the lowest frequency and 0.09% at the highest. Using the different capacitor values, the frequency was varied from minimum to maximum using the ganged 10kΩ pot. The frequencies could be changed from 20Hz to 2.5kHz. It was necessary to include a 500Ω resistor in each leg of the bridge to prevent the complete saturation of the amplifier when the potentiometer was in one extreme of its travel. In addition, a small adjustment resistor was used in the negative feedback loop to adjust the gain and to compensate for the slow thermal time constant of the lamp.

The maximum frequency obtained by the VCO was 9.7kHz with $V_C = 1.65V$ with ± 1.4V batteries. The frequency varied from 8.4kHz to 1.6kHz with ± 1 (V_C) applied with a 0.001μF integrating capacitor.

CONCLUSIONS

Some things could have been done differently to improve the operation of these circuits. The thermal time constant of the non-linear elements was an inhibiting factor in the low-frequency operation of the Wien bridge. A diode or FET will work better here. Extreme ambient temperature will change the operating point of the lamp and, therefore, the output amplitude. Some non-symmetrical output was seen when operating the VCO at the lower frequencies. This is due to the influence of the transistor, as described previously.

Finally, the NE5230 has yet another feature: the bias adjust pin. This pin is intended to be used to control the power supply current. The power supply current is controlled by decreasing the internal bias current of the op amp. When the bias current is decreased, the transconductance, g_M, of the input stage is reduced; this, in turn, lowers the −3dB bandwidth. In addition, this pin can be used to turn the op amp on or off. If the voltage at the bias adjust pin is moved to 50mV above the voltage at the V_{EE} pin, the output becomes severely attenuated. The op amp, for all intents and purpose, is off. If, on the other hand, the bias adjust pin is moved to 50mV below the voltage at the V_{EE} pin, the band width and the slew rate are increased. The user should exercise care when doing this.

The NE5230 is a versatile, low-voltage op amp. It has been demonstrated that the device can be used in a variety of different ways. Its ability to swing within 100mV of the output, its input voltage which can exceed the power supply voltage, and its programmable power supply current, make it a leader of low-voltage op amps.

REFERENCES:

Modern Electronic Circuit Reference Manual, John Markus

Raytheon 1984 Data Manual

Signetics

Linear Products

NE/SA/SE532/ LM158/258/358/2904

Low Power Dual Operational Amplifiers

Product Specification

DESCRIPTION

The 532/358/LM2904 consists of two independent, high gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

UNIQUE FEATURES

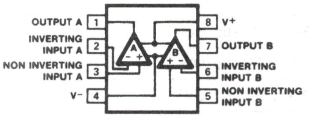
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature-compensated. The input bias current is also temperature-compensated.

FEATURES

- **Internally frequency-compensated for unity gain**
- **Large DC voltage gain — 100dB**
- **Wide bandwidth (unity gain) — 1MHz (temperature-compensated)**
- **Wide power supply range single supply — $3V_{DC}$ to $30V_{DC}$ or dual supplies — $\pm 1.5V_{DC}$ to $\pm 15V_{DC}$**
- **Very low supply current drain ($400\mu A$) — essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)**
- **Low input biasing current — $45nA_{DC}$ temperature-compensated**
- **Low input offset voltage — $2mV_{DC}$ and offset current — $5nA_{DC}$**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage — $0V_{DC}$ to V+ $1.5V_{DC}$ swing**

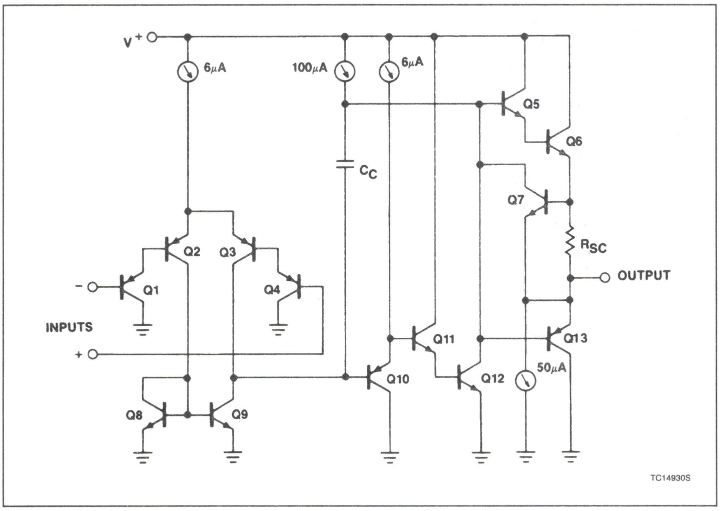
PIN CONFIGURATIONS

D, FE, N Packages


OUTPUT A
1
INVERTING INPUT A
2
NON INVERTING INPUT A
3
V-
4
A
B
8
V+
7
OUTPUT B
6
INVERTING INPUT B
5
NON INVERTING INPUT B

CD11750S

EQUIVALENT CIRCUIT


V+
6μA
100μA
6μA
Q5
Q6
C_C
Q7
R_{SC}
OUTPUT
Q2
Q3
Q1
Q4
INPUTS
-
+
Q11
Q13
Q10
Q12
50μA
Q8
Q9
TC14930S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE532D
8-Pin Plastic DIP	0 to +70°C	NE532N
8-Pin Ceramic DIP	0 to +70°C	NE532FE
8-Pin Plastic SO	-40°C to +85°C	SA532D
8-Pin Plastic DIP	-40°C to +85°C	SA532N
8-Pin Ceramic DIP	-40°C to +85°C	SA532FE
8-Pin Plastic SO	-40°C to +85°C	LM2904D
8-Pin Plastic DIP	-40°C to +85°C	LM2904N
8-Pin Plastic DIP	-25°C to +85°C	LM158N
8-Pin Ceramic DIP	-25°C to +85°C	LM158FE
8-Pin Plastic DIP	-25°C to +85°C	LM258N
8-Pin Ceramic DIP	-25°C to +85°C	LM258FE
8-Pin Plastic SO	-25°C to +85°C	LM358D
8-Pin Plastic DIP	-25°C to +85°C	LM358N
8-Pin Ceramic DIP	-25°C to +85°C	LM358FE
8-Pin Plastic DIP	-55°C to +125°C	SE532N
8-Pin Ceramic DIP	-55°C to +125°C	SE532FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage, V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation $T_A = 25°C$ (Still air)[1] FE package N package D package	 780 1160 780	 mW mW mW
	Output short-circuit to GND[5] V+ < 15 V_{DC} and $T_A = 25°C$	Continuous	
T_A	Operating ambient temperature range NE532/LM358 LM258 SA532/LM2904 SE532/LM158	 0 to +70 -25 to +85 -40 to +85 -55 to +125	 °C °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V+ = +5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358/2904			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$ $R_S = 0\Omega$, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7			7		µV/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$ Over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift	Over temp.		10			10		pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$ Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		45 40	150 300		45 40	250 500	nA nA
I_B	Drift	Over temp.		50			50		pA/°C
V_{CM}	Common-mode voltage range[3]	$V+ = 30V$ Over temp., $V+ = 30V$	0 0		V+ −1.5 V+ −2.0	0 0		V+ −1.5 V+ −2.0	V V
CMRR	Common-mode rejection ratio	$V+ = 30V$	70	85		65	70		dB
V_{OH}	Output voltage swing	$R_L \geq 20k\Omega$, $V+ = 30V$, over temp. $R_L \geq 10k\Omega$, $V+ = 30V$, over temp.	26 27	 28		26 27	 28		V V
V_{OL}	Output voltage swing	$R_L \geq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V+ = 30V$ $R_L = \infty$ on all amplifiers, over temp., $V+ = 30V$		0.5 0.6	1.0 1.2		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, V_{OUT} ±10V, $V+ = 15V$ (for large V_O swing) over temp.	50 25	100		25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	$R_S = 0\Omega$	65	100		65	100		dB
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		−120			−120		dB
I_{OUT}	Output current Source	$V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V+ = 15V_{DC}$	20	40		20	40		mA
		$V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V+ = 15V_{DC}$, over temp.	10	20		10	20		mA
	Sink	$V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, $V+ = 15V_{DC}$	10	20		10	20		mA
		$V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, $V+ = 15V_{DC}$, over temp.	5	8		5	8		mA
		$V_{IN+} = 0V$, $V_{IN-} = +1V_{DC}$, $V_O = 200mV$	12	50		12	50		µA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, V+ = +5V, unless otherwise specified.

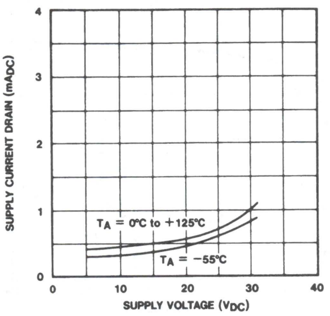
SYMBOL	PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358/2904			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{SC}	Short circuit current[5]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V
GBW	Unity gain bandwidth	$T_A = 25°C$		1			1		MHz
SR	Slew rate	$T_A = 25°C$		0.3			0.3		V/µs
V_{NOISE}	Input noise voltage	$T_A = 25°C$, f = 1kHz		40			40		nV/$\sqrt{Hz}$

NOTES:

1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ −1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to $+32V_{DC}$ without damage.

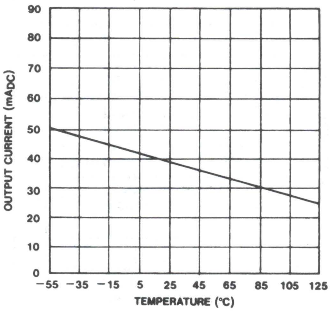
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



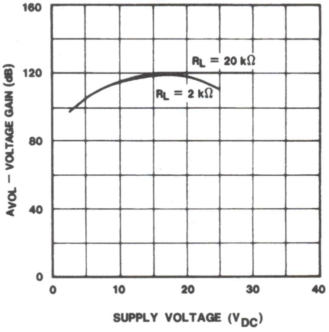
OP12810S

Current Limiting



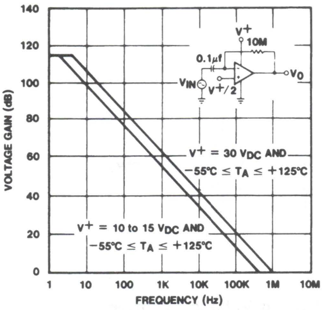
OP12820S

Voltage Gain



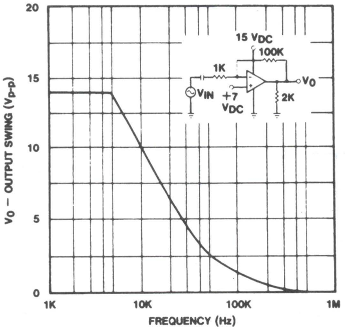
OP12831S

Open-Loop Frequency Response



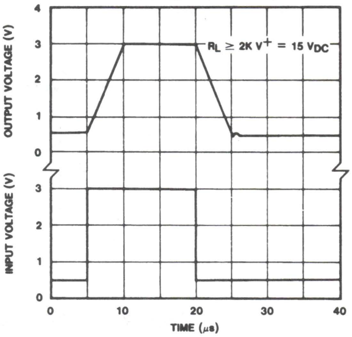
OP12840S

Large-Signal Frequency Response



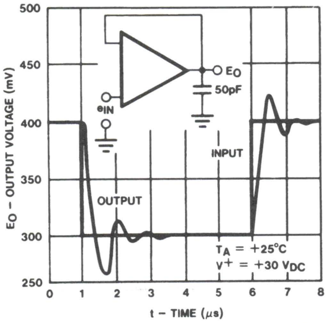
OP12850S

Voltage-Follower Pulse Response



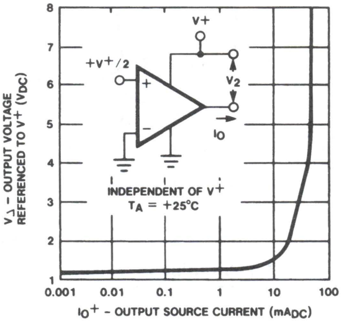
OP12860S

Voltage-Follower Pulse Response (Small-Signal)



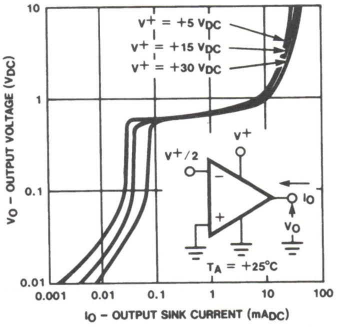
OP12870S

Output Characteristics Current Sourcing



OP12880S

Output Characteristics Current Sinki



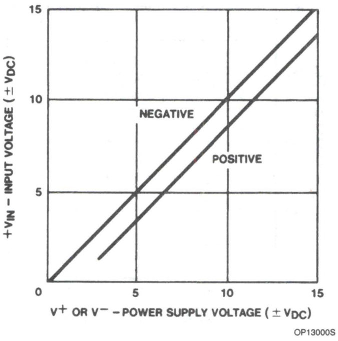
OP12890S

Low Power Dual Operational Amplifiers

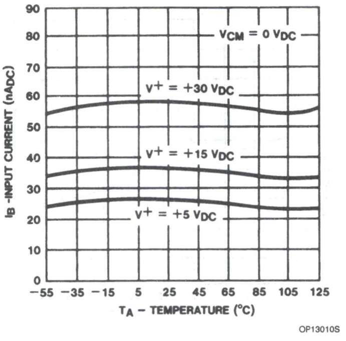
NE/SA/SE532/ LM158/258/358/2904

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

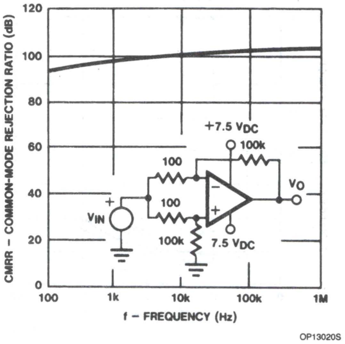
Input Voltage Range



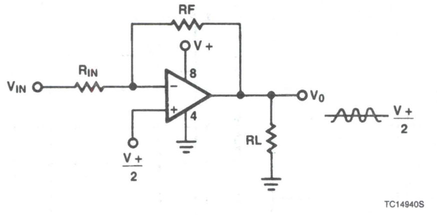
Input Current



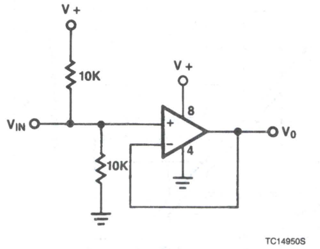
Common-Mode Rejection Ratio



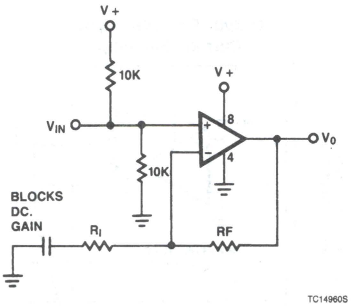
TYPICAL APPLICATIONS


RF
V+
RIN
VIN
8
4
VO
V+/2
RL
V+/2
TC14940S

Single Supply Inverting Amplifier


V+
10K
V+
VIN
8
10K
4
VO
TC14950S

Input Biasing Voltage Follower


V+
10K
V+
VIN
8
VO
10K
4
BLOCKS
DC.
GAIN
RI
RF
TC14960S

Non-Inverting Amplifier

NE/SE5535

Dual High Slew Rate Op Amp

Product Specification

Linear Products

DESCRIPTION

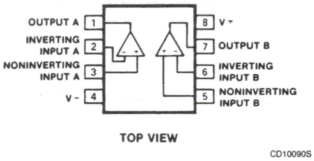
The NE/SE5535 is a new generation operational amplifier featuring high slew rates combined with improved input characteristics. The 5535 is a dual configuration. Internally compensated for unity gain, the SE5535 features a guaranteed unity gain slew rate of 10V/μs with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 747 and 1558.

FEATURES

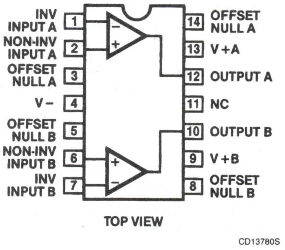
- **15V/μs unity gain slew rate**
- **Internal frequency compensation**
- **Low input offset voltage — 2mV**
- **Low input bias current 80nA max**
- **Short-circuit protected**
- **Large common-mode and differential voltage ranges**
- **Pin compatibility $\frac{5535}{747,1558}$**
- **Dual configuration**
- **Low noise current 0.15pA/$\sqrt{\text{Hz}}$ typ.**

PIN CONFIGURATION

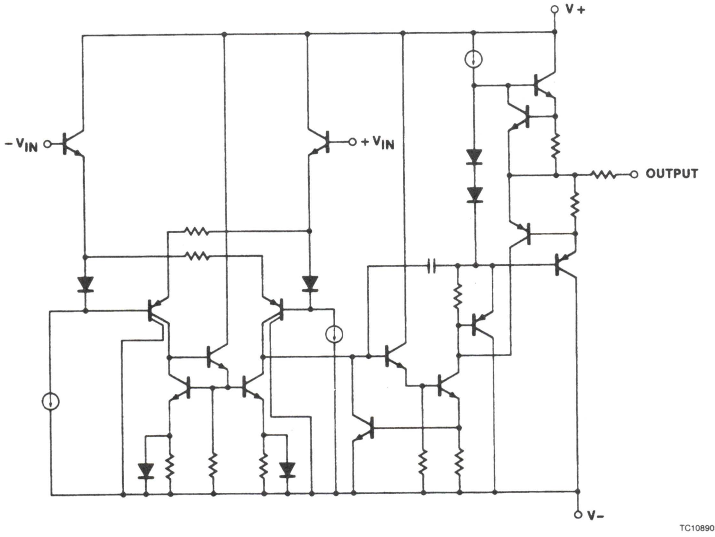
N Package


OUTPUT A
1
INVERTING INPUT A
2
NONINVERTING INPUT A
3
V-
4
NONINVERTING INPUT B
5
INVERTING INPUT B
6
OUTPUT B
7
V+
8
TOP VIEW
CD10090S

F Package


INV INPUT A
1
NON-INV INPUT A
2
OFFSET NULL A
3
V−
4
OFFSET NULL B
5
NON-INV INPUT B
6
INV INPUT B
7
OFFSET NULL B
8
V+B
9
OUTPUT B
10
NC
11
OUTPUT A
12
V+A
13
OFFSET NULL A
14
TOP VIEW
CD13780S

EQUIVALENT SCHEMATIC (One Amplifier)


V+
−VIN
+VIN
OUTPUT
V−
TC10890S

Dual High Slew Rate Op Amp NE/SE5535

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5535N
8-Pin Plastic DIP	-55°C to +125°C	SE5535N
14-Pin Cerdip	0 to +70°C	NE5535F
14-Pin Cerdip	-55 to +125°C	SE5535F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	SE5535	NE5535	UNIT
V_S	Supply voltage	±22	±18	V
P_D	Internal power dissipation[1] N package F package	 500 1000	 500 1000	 mW mW
V_{IN}	Differential input voltage	±30	±30	V
V_{IN}	Input voltage[2]	±15	±15	V
T_A	Operating temperature range	-55 to +125	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	300	°C
I_{SC}	Output short-circuit[3]	Indefinite	Indefinite	

NOTES:

1. Rating applies for thermal resistances junction to ambient of 100°C/W and 110°C/W for N and F packages, respectively. Maximum junction temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

Dual High Slew Rate Op Amp

NE/SE5535

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.*

SYMBOL	PARAMETER	TEST CONDITIONS	SE5535			NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		μV/°C
I_{OS}	Input offset current	Over temp.		5	20 40		15	40 80	nA nA
ΔI_{OS}	Input offset current	Over temp.		25			40		pA/°C
I_B	Input current	Over temp.		45	80 200		65	150 200	nA nA
ΔI_B	Input current	Over temp.		50			80		pA/°C
V_{CM}	Common-mode voltage range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$ $R_L = 2k\Omega$, $V_{OUT} = \pm 10V$, over temp.	50 25	500		50 25	500		V/mV V/mV
V_{OUT}	Output voltage	$R_L \geq 2k\Omega$, over temp. $R_L \geq 10k\Omega$, over temp.	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I_{CC}	Supply current	Per amplifier Per amplifier, over temp.		1.8 2	2.8 3.3		1.8 2	2.8	mA mA
P_D	Power dissipation	Per amplifier Per amplifier, over temp.		54 60	84 99		54 60	84	mW mW
I_{SC}	Output short-circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω

NOTE:

* Temperature range:
SE types $-55°C \leq T_A \leq 125°C$
NE types $0°C \leq T_A \leq 70°C$

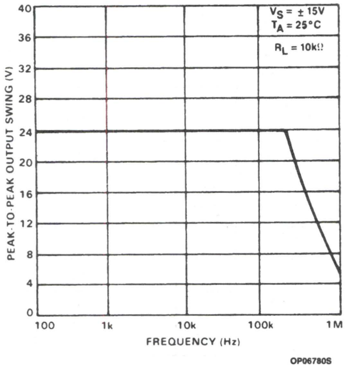
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5535			NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain/bandwidth product			1			1		MHz
	Transient response								
t_R	Small-signal rise time			0.25			0.25		μs
	Small-signal overshoot			6			6		%
t_S	Settling time	To 0.1%		3			3		μs
SR	Slew rate	$R_L \geq 10k\Omega$, unity gain, non-inverting	10	15		10	15		V/μs
	Input noise voltage	$f = 1kHz$, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$

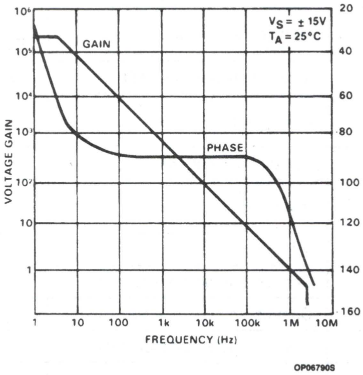
Dual High Slew Rate Op Amp NE/SE5535

TYPICAL PERFORMANCE CHARACTERISTICS

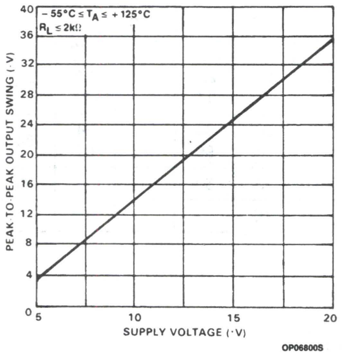
Output Voltage Swing as a Function of Frequency



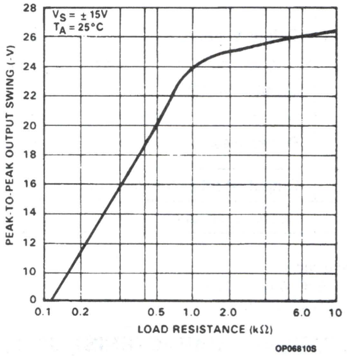
Open-Loop Voltage Gain as a Function of Frequency



Output Voltage Swing as a Function of Supply Voltage

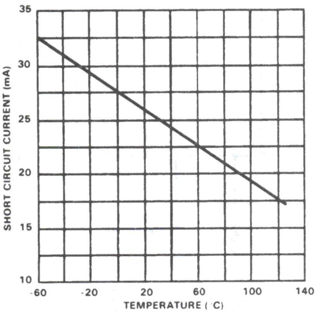


Output Voltage Swing as a Function of Load Resistance

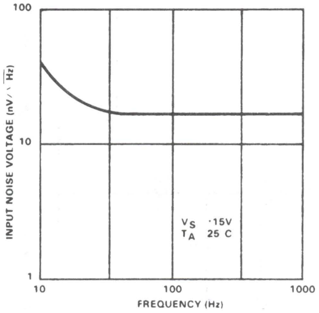


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

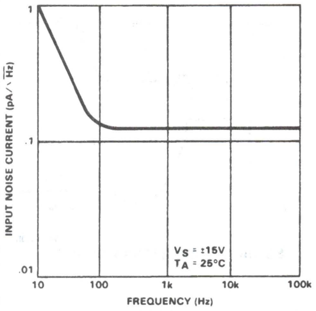
Output Short-Circuit Current as a Function of Ambient Temperature



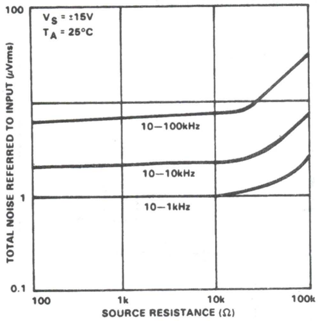
Input Noise Voltage as a Function of Frequency



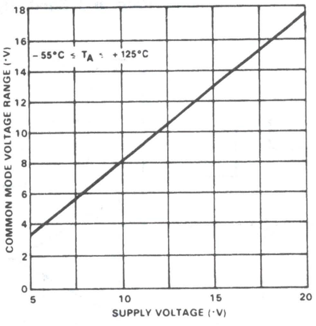
Input Noise Current as a Function of Frequency



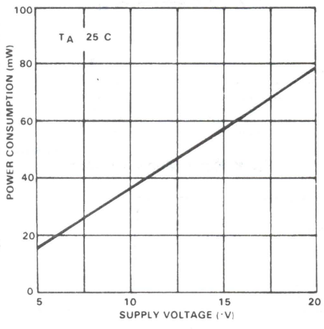
Broadband Noise for Various Bandwidths



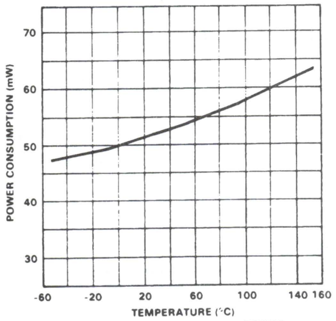
Input Common-Mode Voltage Range as a Function of Supply Voltage



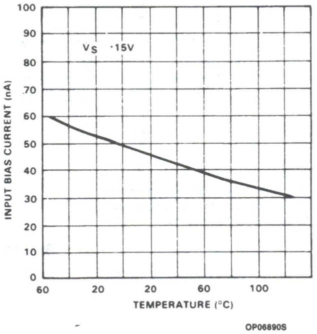
Power Consumption as a Function of Supply Voltage



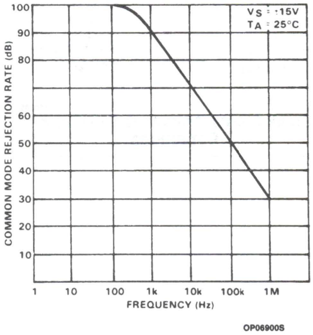
Power Consumption as a Function of Ambient Temperature



Input Bias Current as a Function of Ambient Temperature

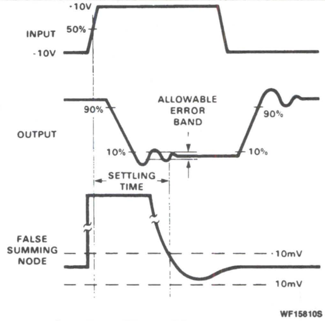


Common-Mode Rejection Ratio as a Function of Frequency

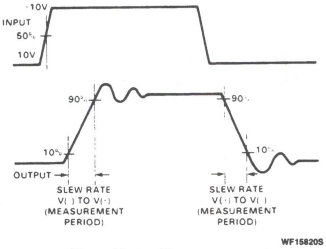


Dual High Slew Rate Op Amp NE/SE5535

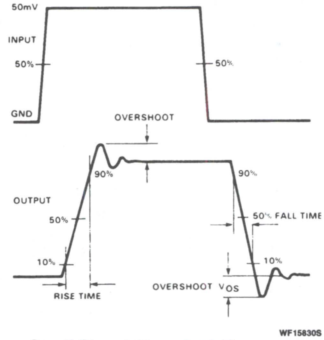
VOLTAGE WAVEFORMS


+10V
INPUT
50%
-10V
90%
ALLOWABLE
ERROR
BAND
90%
OUTPUT
10%
10%
SETTLING
TIME
FALSE
SUMMING
NODE
+10mV
10mV
WF15810S

Settling Time Measurement

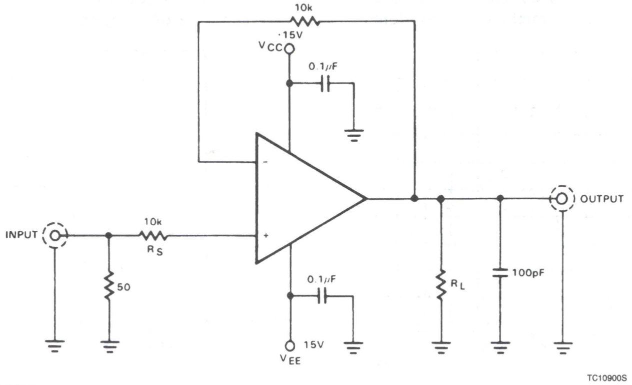

+10V
INPUT
50%
10V
90%
90%
10%
10%
OUTPUT
SLEW RATE
V( ) TO V(+)
(MEASUREMENT
PERIOD)
SLEW RATE
V(+) TO V( )
(MEASUREMENT
PERIOD)
WF15820S

Slew Rate Measurement


50mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT
50%
50% FALL TIME
10%
10%
RISE TIME
OVERSHOOT V_OS
WF15830S

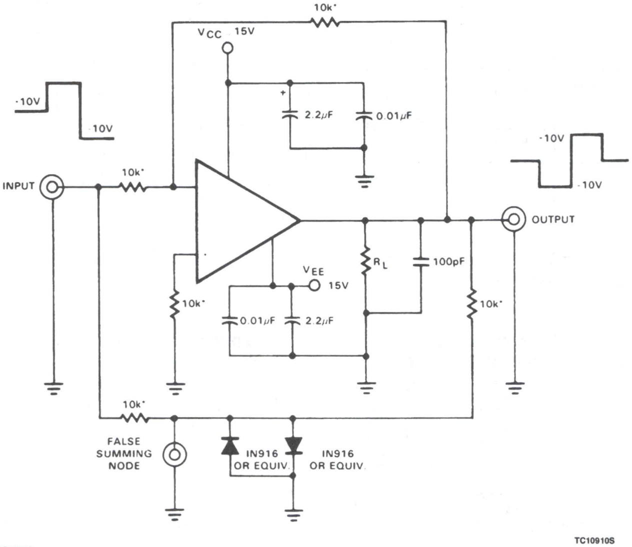
Small-Signal Transient Response Definitions

TEST CIRCUITS


10k
+15V
V_CC
0.1μF
-
+
OUTPUT
INPUT
10k
R_S
50
0.1μF
15V
V_EE
R_L
100pF
TC10900S

NOTES:
1. Pins not shown are not connected.
2. All resistor values are typical and in ohms.

Slew Rate and Small-Signal Transient Response

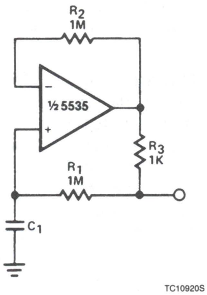

10k*
V_CC 15V
+
2.2μF
0.01μF
-10V
10V
-10V
10V
INPUT
10k*
OUTPUT
-
R_L
100pF
V_EE
15V
10k*
0.01μF
2.2μF
10k*
10k*
FALSE
SUMMING
NODE
IN916
OR EQUIV.
IN916
OR EQUIV.
TC10910S

NOTES:
1. Pins not shown are not connected.
2. All resistor values are typical and in ohms.
   *Match to within 0.01%.

Settling Time

INTRODUCTION

The NE5535 is a new generation monolithic op amp which features improved input characteristics. The device is compensated to unity gain and has a minimum guaranteed unity gain slew rate of 10Vμs. This is achieved by employing a clamped super beta input stage which has lower input bias current.



NOTE:
All resistor values are in ohms.

Figure 1. Capacitance Multiplier

APPLICATIONS

These improved parameters can be put to good use in applications such as sample and hold circuits which require low input current and in voltage-follower circuits which require high slew rates. The circuit that follows will yield maximum small-signal transient response and slew rate for the NE5535 at unity gain.

It is always good practice in designing a system to use dual tracking regulators to power the dual-supply op amps. This will guarantee the positive and negative supply voltage will be equal during power-up. With the NE5535, it is possible to degrade the input circuit characteristics by not applying the power supplies simultaneously. The NE5535 is capable of directly replacing the μA741 with higher input resistance which will improve such designs as active filters, sample and hold, as well as voltage-followers.

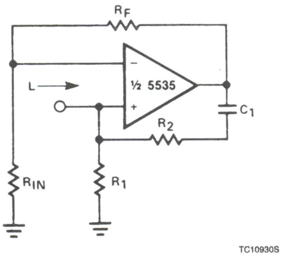
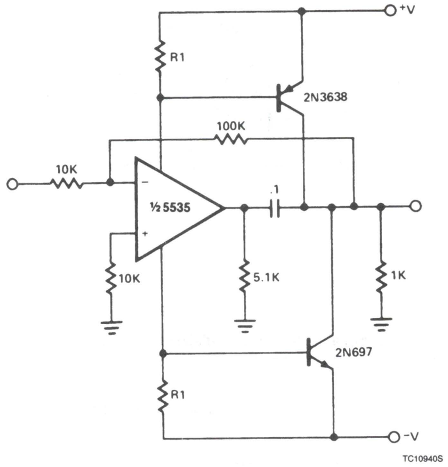


Figure 2. Virtual Inductor



NOTE:
All resistor values are in ohms.

Figure 3. Power Booster

The NE5535 can be used either with single or split power supplies.

Capacitance Multiplier

The circuit in Figure 1 can be used to simulate large capacitances using small value components. With the values shown and C = 10μF, an effective capacitance of 10,000μF was obtained. The Q available is limited by the effective series resistance. So R1 should be as large as practical.

Simulated Inductor

With a constant current excitation, the voltage dropped across an inductance increases with frequency. Thus, an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 2 yields such a response with the effective inductance being equal to:

$$L = R_1 R_2 C$$

The Q of this inductance depends upon R_1 being equal to R_2. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of instability at high frequencies. R_1 should therefore always be slightly smaller than R_2 to assure stable operation.

Power Amplifier

For most applications, the available power from op amps is sufficient. There are times when more power handling capability is necessary. A simple power booster capable of driving moderate loads is offered in Figure 3.

The circuit as shown uses an NE5535 device. Other amplifiers may be substituted only if R_1 values are changed because of the I_{CC} current required by the amplifier. R_1 should be calculated from the expression

$$R_1 = \frac{600\text{mV}}{I_{CC}}$$

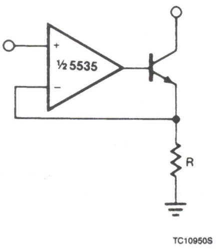
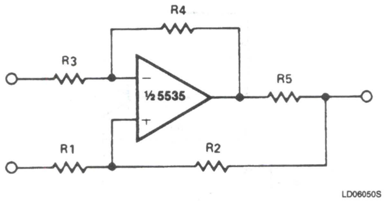


Figure 4. Voltage-to-Current Converter

Dual High Slew Rate Op Amp NE/SE5535



NOTES:

$\frac{R_2}{R_1}=\frac{R_4}{R_3}$

$I_{OUT}=\frac{V_{IN}\cdot R_2}{R_5\cdot R_1}$

Figure 5. Voltage-to-Current Converter

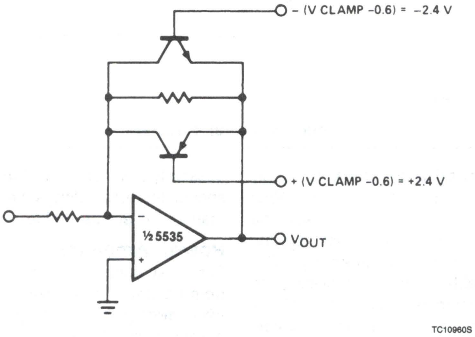
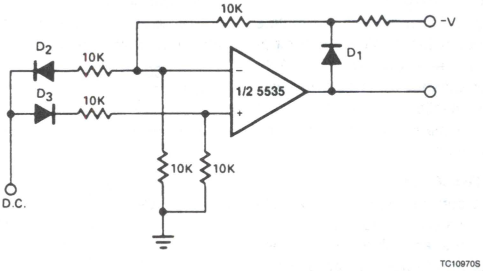


Figure 6. Active Clamp-Limiting Amplifier



NOTE:
All resistor values are in ohms.

Figure 7. Absolute Value Amplifier

Voltage-to-Current Converters

A simple voltage-to-current converter is shown in Figure 4. The current out is $I_{OUT} \cong V_{IN}/R$. For negative currents, a PNP can be used and, for better accuracy, a Darlington pair can be substituted for the transistor. With careful design, this circuit can be used to control currents of many amps. Unity gain compensation is necessary.

The circuit in Figure 5 has a different input and will produce either polarity of output current. The main disadvantages are the error current flowing in R_2 and the limited current available.

Active Clamp-Limiting Amplifier

The modified inverting amplifier in Figure 6 uses an active clamp to limit the output swing with precision. Allowance must be made for the V_{BE} of the transistors. The swing is limited by the base-emitter breakdown of the transistors. A simple circuit uses two back-to-back zener diodes across the feedback resistor, but tends to give less precise limiting and cannot be easily controlled.

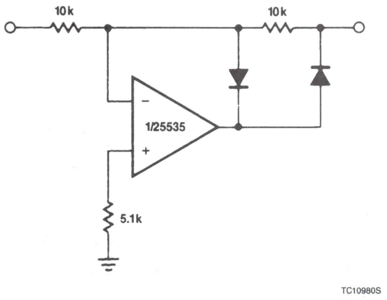
Absolute Value Amplifier

The circuit in Figure 7 generates a positive output voltage for either polarity of input. For positive signals, it acts as a noninverting amplifier and for negative signals, as an inverting amplifier. The accuracy is poor for input voltages under 1V, but for less stringent applications, it can be effective.

Half-Wave Rectifier

Figure 8 provides a circuit for accurate half-wave rectification of the incoming signal. For positive signals, the gain is 0; for negative signals, the gain is −1. By reversing both diodes, the polarity can be inverted. This circuit provides an accurate output, but the output impedance differs for the two input polarities and buffering may be needed. The output must slew through two diode drops when the input polarity reverses. The NE5535 device will work up to 10kHz with less than 5% distortion.

Dual High Slew Rate Op Amp NE/SE5535


10k
10k
1/25535
5.1k
TC10980S

NOTE:
All resistor values are in ohms.

Figure 8. Half-Wave Rectifier

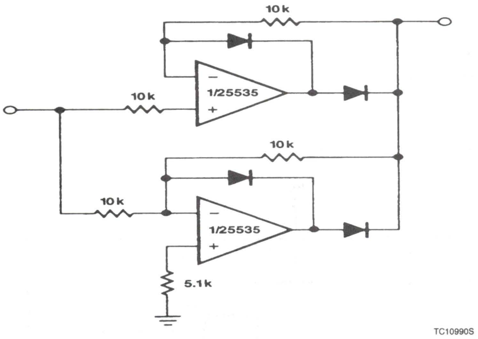
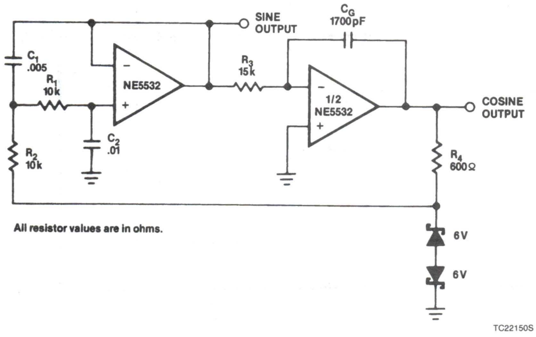

10k
1/25535
10k
10k
10k
1/25535
5.1k
TC10990S

Figure 9. Precision Full-Wave Rectifier


C1 .005
R1 10k
NE5532
C2 .01
R2 10k
SINE OUTPUT
CG 1700pF
R3 15k
1/2 NE5532
COSINE OUTPUT
R4 600Ω
All resistor values are in ohms.
6V
6V
TC22150S

NOTE:
All resistor values are in ohms.

Figure 10. Two-Phase Sine Wave Oscillator

Precision Full-Wave Rectifier

The circuit in Figure 9 provides accurate full-wave rectification. The output impedance is low for both input polarities, and the errors are small at all signal levels. Note that the output will not sink heavy currents, except a small amount through the 10kΩ resistors. Therefore, the load applied should be referenced to ground or a negative voltage. Reversal of all diode polarities will reverse the polarity of the output. Since the outputs of the amplifiers must slew through two diode drops when the input polarity changes, 741 type devices give 5% distortion at about 300Hz.

Two-Phase Sine Wave Oscillator

The circuit (refer to Figure 10) uses a 2-pole pass Butterworth, followed by a phase-shifting single-pole stage, fed back through a voltage limiter to achieve sine and cosine outputs. The values shown using the μA741 amplifiers give about 1.5% distortion at the sine output and about 3% distortion at the cosine output. By careful trimming of C_G and/or the limiting network, better distortion figures are possible. The component values shown give a frequency of oscillation of about 2kHz. The values can be readily selected for other frequencies. The NE5535 should be used at higher frequencies to reduce distortion due to slew limiting.

TCA520
Operational Amplifier

Product Specification

DESCRIPTION

The TCA520 is a bipolar integrated operational amplifier primarily intended for low-power, low-voltage applications and as a comparator in digital systems.

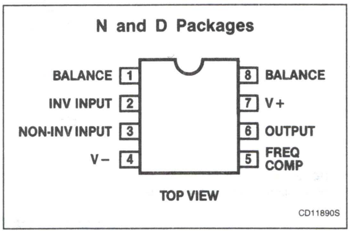
FEATURES

- Wide supply voltage range
- Low supply voltage operation
- Low power consumption
- Low input bias current
- Offset compensation facility
- Frequency compensation facility
- High slew rate
- Large output voltage swing
- TTL compatible output

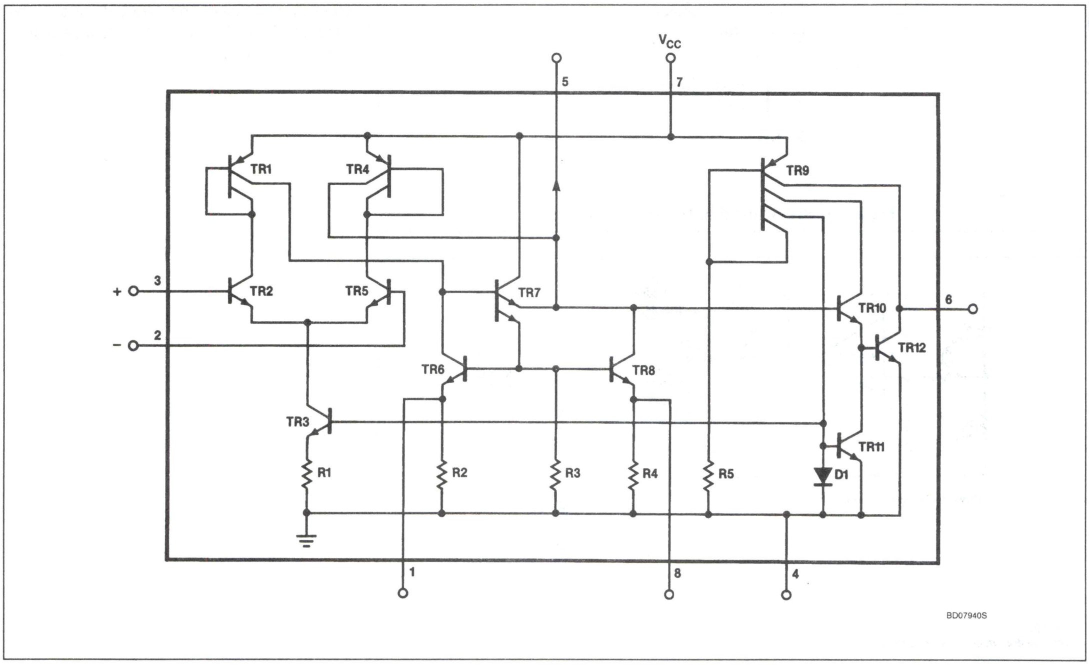
APPLICATIONS

- Integrator
- Differentiator
- Summing amplifier

PIN CONFIGURATION


N and D Packages
BALANCE 1
INV INPUT 2
NON-INV INPUT 3
V− 4
8 BALANCE
7 V+
6 OUTPUT
5 FREQ COMP
TOP VIEW
CD11890S

CIRCUIT DIAGRAM


V$_{CC}$
5
7
TR1
TR4
TR9
3
+
TR2
TR5
TR7
TR10
6
2
−
TR12
TR6
TR8
TR3
TR11
R1
R2
R3
R4
R5
D1
1
8
4
BD07940S

Operational Amplifier TCA520

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	−25°C to +85°C	TCA520BN
8-Pin Plastic SO (SOT-96A)	−25°C to +85°C	TCA520TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage, DC	22	V
V_I $-V_I$	Input voltage	V_{CC} 0	V V
$\pm V_{ID}$	Differential input voltage	7	V
P_{TOT}	Power dissipation at $T_A = 85°C$	200	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +85	°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$; $V- = 0V$; $T_A = 25°C$; R_L from Q to V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply V_{CC} (Pin 7)					
I_{CC}	Supply current, unloaded	0.5	0.8	1.2	mA
Inputs I+ and I−; Pins 3 and 2					
V_I	Input voltage	0.9		$V_{CC} - 0.5$	V
I_{BIAS}	Input bias current		60	250	nA
V_{IO}	Input offset voltage		1	6	mV
ΔV_{IO}	Variation with temperature		5		μV/K
I_{IO}	Input offset current		10	75	nA
CMRR	Common-mode rejection ratio	70	100		dB
$V_{N(RMS)}$	Input noise voltage at f = 1kHz		15		$nV/\sqrt{Hz}$
$I_{N(RMS)}$	Input noise current at f = 1kHz		0.4		$pA/\sqrt{Hz}$
Output Q (Pin 6)					
V_Q	Output voltage range at $R_L = 5k\Omega$	0.1		$V_{CC} - 0.1$	V
 $-I_{OH}$ I_{OL}	Output current HIGH at $V_Q = V_{CC} - 0.4V$ LOW at $V_Q = 0.4V$	 100 6	 200 12		 μA mA
A_{VD}	DC voltage amplification at $R_L = 5k\Omega$	10 000	15 000		
A_{VD}	AC voltage amplification at f = 1kHz; $C_{FC} = 100pF$		58		dB
 S_{VOAV} S_{VOAV}	Slew rate (average rate of change of the output voltage) at $R_L = 1k\Omega$ $C_{FC} = 0pF$ $C_{FC} = 100pF$		 25 500		 V/μs mV/μs

Operational Amplifier TCA520

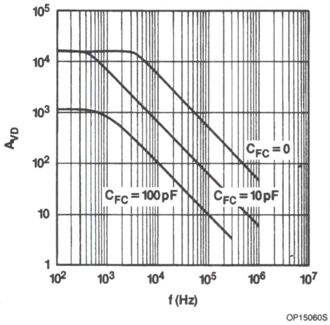


Figure 1. Typical Values of the Open-Loop Voltage Amplification as a Function of Frequency

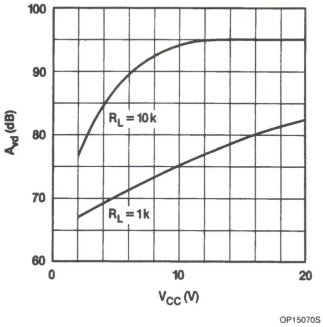


Figure 2. Typical Values of the Open-Loop Voltage Amplification as a Function of Supply Voltage

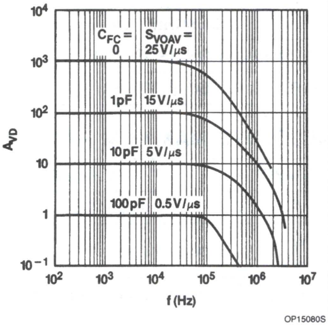


Figure 3. Typical Frequency Response and Slew Rate for Various Closed-Loop Gains

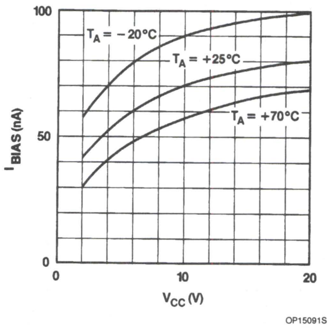


Figure 4.Typical Values of the Input Bias Current as a Function of Supply Voltage, With Ambient Temperature as a Parameter

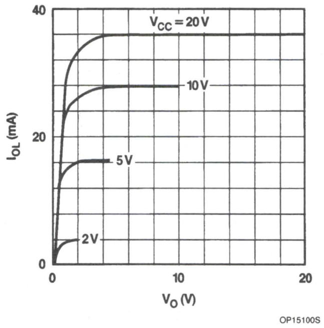


Figure 5. Output Current LOW as a Function of Output Voltage, With Supply Voltage as a Parameter

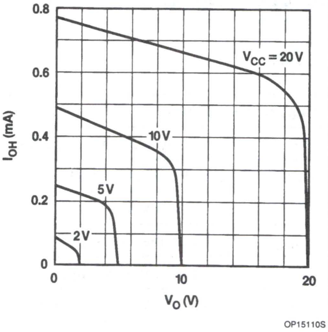


Figure 6. Output Current HIGH as a Function of Output Voltage, With Supply Voltage as a Parameter

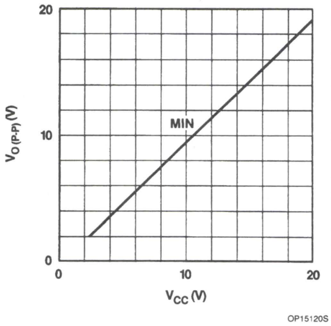


Figure 7. Minimum Values of the Output Voltage Swing as a Function of Supply Voltage for $R_L = 1k\Omega$

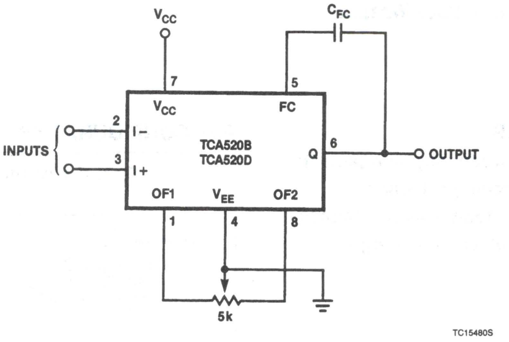

VCC
CFC
7
5
VCC
FC
2
I−
INPUTS
TCA520B
TCA520D
6
Q
OUTPUT
3
I+
OF1
VEE
OF2
1
4
8
5k
TC15480S

Figure 8. Typical Arrangement of the TCA520 With Frequency and Offset Compensation

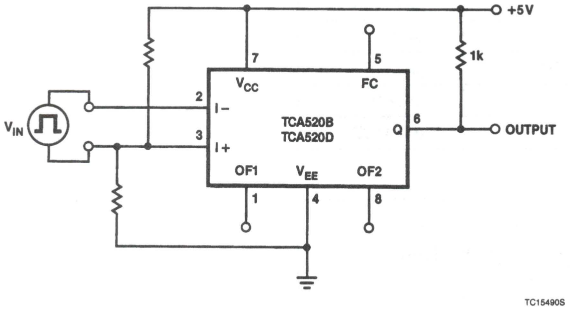

+5V
7
5
1k
VCC
FC
2
I−
VIN
TCA520B
TCA520D
Q
6
OUTPUT
3
I+
OF1
VEE
OF2
1
4
8
TC15490S

Figure 9. Typical Application of the TCA520 as a Comparator

Signetics

μA741/μA741C/SA741C
General Purpose Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

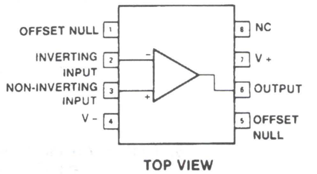
The μA741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit-protected and allows for nulling of offset voltage.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**

PIN CONFIGURATION

D, F, N Packages



OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V- 4
NC 8
V+ 7
OUTPUT 6
OFFSET NULL 5
-
+

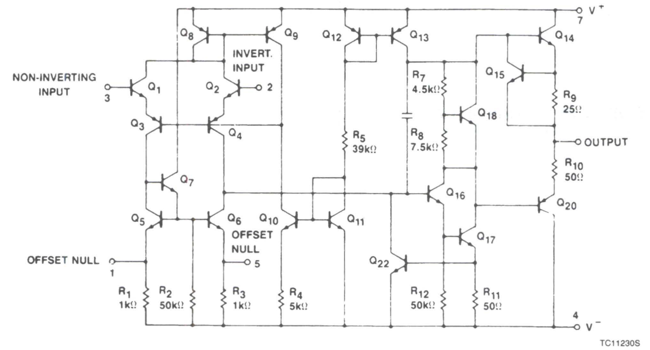
TOP VIEW

CD10181S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	-55°C to +125°C	μA741N
8-Pin Plastic DIP	0 to +70°C	μA741CN
8-Pin Plastic DIP	-40°C to +85°C	SA741CN
8-Pin Cerdip	-55°C to +125°C	μA741F
8-Pin Cerdip	0 to +70°C	μA741CF
8-Pin SO	0 to +70°C	μA741CD

EQUIVALENT SCHEMATIC



V+ 7
Q8
Q9
Q12
Q13
Q14
INVERT. INPUT
NON-INVERTING INPUT 3
Q1
Q2
2
R7 4.5kΩ
Q15
R9 25Ω
Q3
Q4
R5 39kΩ
R8 7.5kΩ
Q18
OUTPUT
R10 50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
OFFSET NULL 5
Q17
OFFSET NULL 1
Q22
R1 1kΩ
R2 50kΩ
R3 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
4 V-

TC11230S

General Purpose Operational Amplifier μA741/μA741C/SA741C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage		
	μA741C	±18	V
	μA741	±22	V
P_D	Internal power dissipation		
	D package	500	mW
	N package	1000	mW
	F package	1000	mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
I_{SC}	Output short-circuit duration	Continuous	
T_A	Operating temperature range		
	μA741C	0 to +70	°C
	SA741C	−40 to +85	°C
	μA741	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS (μA741, μA741C) $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10kΩ$		1.0	5.0		2.0	6.0	mV
		$R_S = 10kΩ$, over temp.		1.0	6.0			7.5	mV
$ΔV_{OS}/ΔT$				10			10		μV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		20	500				nA
$ΔI_{OS}/ΔT$				200			200		pA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
$ΔI_B/ΔT$				1			1		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10kΩ$	±12	±14		±12	±14		V
		$R_L = 2kΩ$, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2kΩ$, $V_O = ±10V$	50	200		20	200		V/mV
		$R_L = 2kΩ$, $V_O = ±10V$, over temp.	25			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Supply voltage rejection ratio	$R_S \leqslant 10kΩ$		10	150		10	150	μV/V
		$R_S \leqslant 10kΩ$, over temp.							μV/V
CMRR	Common-mode rejection ratio	Over temp.	70	90					dB
									dB
I_{CC}	Supply current	$T_A = +125°C$		1.4	2.8				mA
		$T_A = -55°C$		1.5	2.5		1.4	2.8	mA
				2.0	3.3				mA

DC ELECTRICAL CHARACTERISTICS (Continued) (μA741, μA741C) $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		MΩ
P_D	Power consumption			50	80		50	85	mW
		$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		45	100				mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current		10	25	60	10	25	60	mA

DC ELECTRICAL CHARACTERISTICS (SA741C) $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

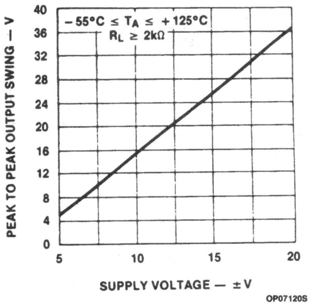
SYMBOL	PARAMETER	TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10kΩ$		2.0	6.0	mV
		$R_S = 10kΩ$, over temp.			7.5	mV
$ΔV_{OS}/ΔT$				10		μV/°C
I_{OS}	Offset current			20	200	nA
		Over temp.			500	nA
$ΔI_{OS}/ΔT$				200		pA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temp.			1500	nA
$ΔI_B/ΔT$				1		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10kΩ$	±12	±14		V
		$R_L = 2kΩ$, over temp.	±10	±13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2kΩ$, $V_O = ±10V$	20	200		V/mV
		$R_L = 2kΩ$, $V_O = ±10V$, over temp.	15			V/mV
	Offset voltage adjustment range			±30		mV
PSRR	Supply voltage rejection ratio	$R_S \leqslant 10kΩ$		10	150	μV/V
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		V
R_{IN}	Input resistance		0.3	2.0		MΩ
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

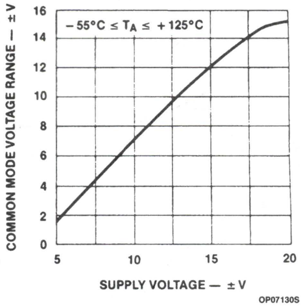
SYMBOL	PARAMETER	TEST CONDITIONS	μA741, μA741C			UNIT
			Min	Typ	Max	
C_{IN}	Parallel input capacitance	Open-loop, f = 20Hz		1.4		pF
	Unity gain crossover frequency	Open-loop		1.0		MHz
	Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2kΩ$, $C_L \leqslant 100pF$				
t_R	Rise time			0.3		μs
	Overshoot			5.0		%
SR	Slew rate	$C \leqslant 100pF$, $R_L \geqslant 2kΩ$, $V_{IN} = ±10V$		0.5		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

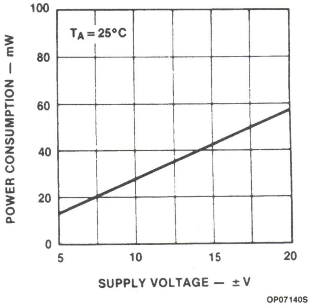
Output Voltage Swing as a Function of Supply Voltage



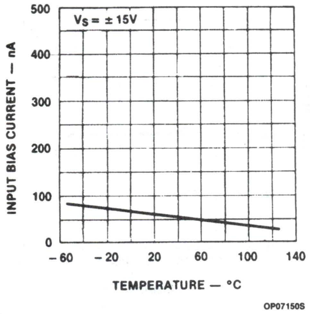
Input Common-Mode Voltage Range as a Function of Supply Voltage



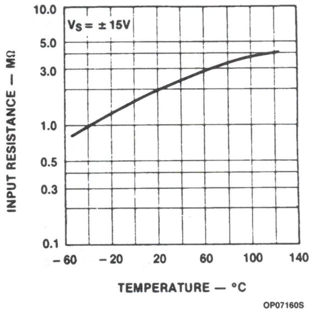
Power Consumption as a Function of Supply Voltage



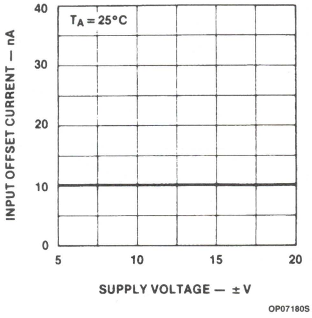
Input Bias Current as a Function of Ambient Temperature



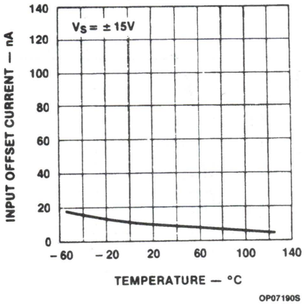
Input Resistance as a Function of Ambient Temperature



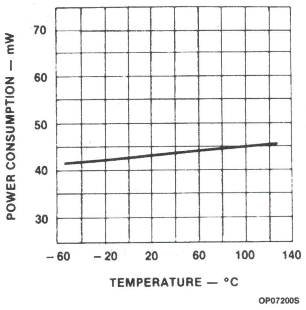
Input Offset Current as a Function of Supply Voltage



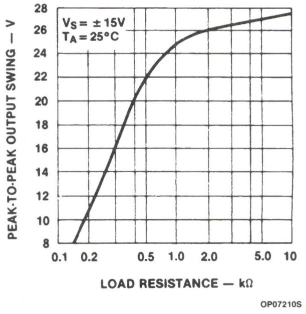
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

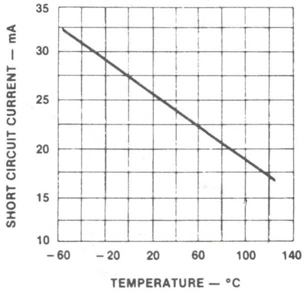


Output Voltage Swing as a Function of Load Resistance



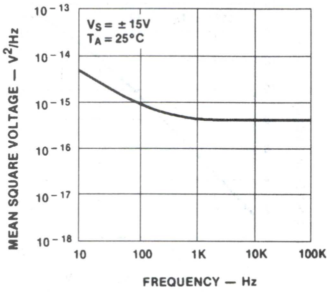
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Output Short-Circuit Current as a Function of Ambient Temperature



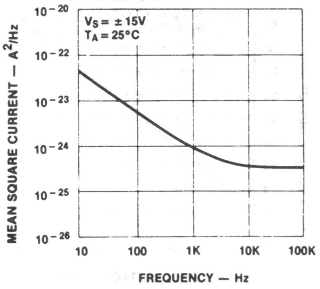
OP07220S

Input Noise Voltage as a Function of Frequency



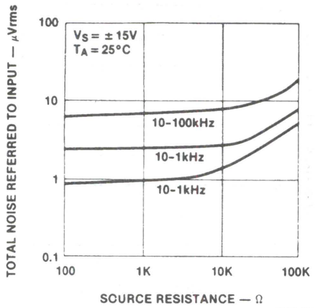
OP07230S

Input Noise Current as a Function of Frequency



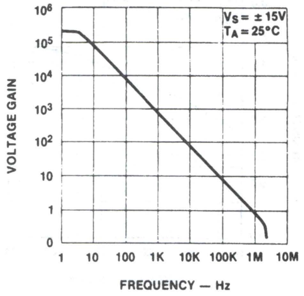
OP07240S

Broadband Noise for Various Bandwidths



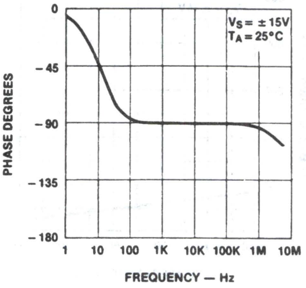
OP07250S

Open-Loop Voltage Gain as a Function of Frequency



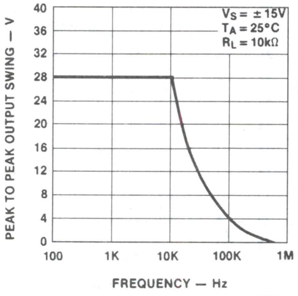
OP07260S

Open-Loop Phase Response as a Function of Frequency



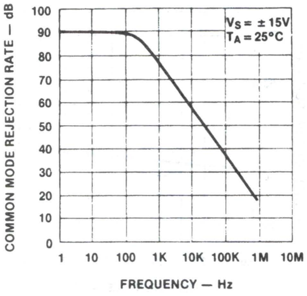
OP07270S

Output Voltage Swing as a Function of Frequency



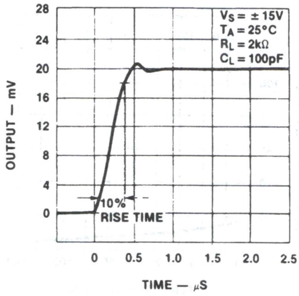
OP07280S

Common-Mode Rejection Ratio as a Function of Frequency



OP07290S

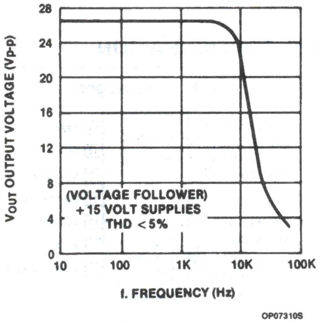
Transient Response



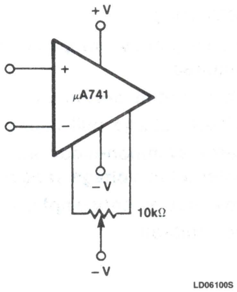
OP07300S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Power Bandwidth (Large Signal Swing vs Frequency)



Voltage Offset Null



Signetics

μA747/747C/SA747C
Dual Operational Amplifier

Product Specification

Linear Products

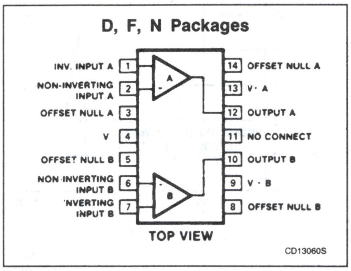
DESCRIPTION

The 747 is a pair of high-performance monolithic operational amplifiers constructed on a single silicon chip. High common-mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage-follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed-loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

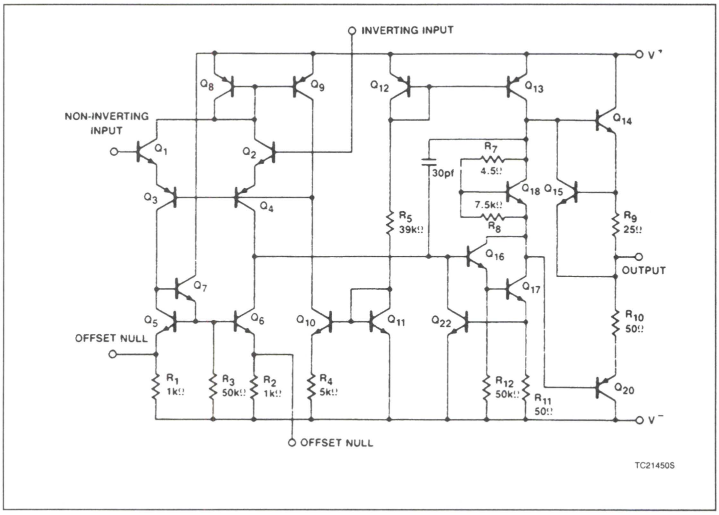
- **No frequency compensation required**
- **Short-circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**

PIN CONFIGURATION


D, F, N Packages

INV. INPUT A 1
NON-INVERTING INPUT A 2
OFFSET NULL A 3
V 4
OFFSET NULL B 5
NON-INVERTING INPUT B 6
'NVERTING INPUT B 7
8 OFFSET NULL B
9 V · B
10 OUTPUT B
11 NO CONNECT
12 OUTPUT A
13 V· A
14 OFFSET NULL A
A
B
TOP VIEW
CD13060S

EQUIVALENT SCHEMATIC


INVERTING INPUT
V+
NON-INVERTING INPUT
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q20
Q22
30pf
R7 4.5kΩ
7.5kΩ R8
R5 39kΩ
R9 25Ω
OUTPUT
R10 50Ω
OFFSET NULL
R1 1kΩ
R3 50kΩ
R2 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
V−
OFFSET NULL
TC21450S

Dual Operational Amplifier

μA747/747C/SA747C

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	−55°C to +125°C	μA747N
14-Pin Plastic DIP	0 to +70°C	μA747CN
14-Pin Plastic DIP	−45°C to +85°C	SA747CN
14-Pin Cerdip	−55°C to +125°C	μA747F
14-Pin Cerdip	0 to +70°C	μA747CF
14-Pin SO	0 to +70°C	μA747CD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage μA747 μA747C SA747C	 ±22 ±18 ±18	 V V V
P_D	Internal power dissipation D Package N, F Packages	 700 900	 mW mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage	±15	V
	Voltage between offset null and V−	±0.5	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range μA747 μA747C SA747C	 −55 to +125 0 to +70 −40 to +85	 °C °C °C
T_{SOLD}	Lead temperature (soldering, 10sec)	 300	 °C
I_{SC}	Output short-circuit duration	Indefinite	

DC ELECTRICAL CHARACTERISTICS (μA747, μ747C) $T_A = 25°C$, $V_{CC} = \pm15V$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA747			μA747C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leqslant 10k\Omega$		2.0	5.0		2.0	6.0	mV
		$R_S \leqslant 10k\Omega$, over temp.		3.0	6.0		3.0	7.5	mV
$\Delta V_{OS}/\Delta T$				10			10		μV/°C
I_{OS}	Offset current			20	200		20	200	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		85	500				nA
		Over temperature					7.0	300	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_{BIAS}	Input current			80	500		80	500	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
		Over temperature					30	800	nA
$\Delta I_B/\Delta T$				1			1		nA/°C
V_{OUT}	Output voltage swing	$R_L \geqslant 2k\Omega$, over temp.	±10	±13		±10	±13		V
		$R_L \geqslant 10k\Omega$, over temp.	±12	±14		±12	±14		V
I_{CC}	Supply current each side			1.7	2.8		1.7	2.8	mA
		$T_A = +125°C$		1.5	2.5				m
		$T_A = -55°C$		2.0	3.3				mA
		Over temperature					2.0	3.3	mA
P_d	Power consumption			50	85		50	85	mW
		$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		60	100				mW
		Over temperature					60	100	mW
C_{IN}	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		V
R_{OUT}	Output resistance			75			75		Ω
	Channel separation			120			120		dB
PSRR	Supply voltage rejection ratio	$R_S \leqslant 10k\Omega$, over temp.		30	150		30	150	μV/V
A_{VOL}	Large-signal voltage gain (DC)	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm10V$	50,000			25,000			V/V
		Over temperature	25,000			15,000			V/V
CMRR	Common-mode rejection ratio	$R_S \leqslant 10k\Omega$, $V_{CM} = \pm12V$ Over temperature	70			70			dB

DC ELECTRICAL CHARACTERISTICS (SA747C) $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA747C			UNIT
			Min	Typ	Max	
$V_{OS}\Delta V_{OS}/\Delta T$	Offset voltage	$R_S = 10\Omega$ $R \leqslant 10k\Omega$, over temperature		2.0 3.0 10	6.0 7.5	mV!n
$I_{OS}\Delta I_{OS}/\Delta T$	Offset current	$R_S = 10\Omega$		2.0 3.0 10	6.0 7.5	mV mV μC/°C
$I_{BIAS}\Delta I_B/\Delta T$	Input bias current	Over temperature		1	500 1500	nA nA pA/°C
V_{OUT}	Output voltage swing	$R_L \geqslant 2k\Omega$, over temperature $R_L \geqslant 10k\Omega$, over temperature	± 10 ± 12	± 13 ± 14		
I_{CC}	Supply current	Over temperature		1.7 2.0	2.8 3.3	mA mA
P_d	Power consumption	Over temperature		50 60	85 100	mW mW
C_{IN}	Input capacitance			1.4		pF
	Offset voltage adjustment range			± 15		V
R_{OUT}	Output resistance			75		Ω
	Channel separation			120		dB
PSRR	Supply voltage rejection ratio	$R_S \leqslant 10k\Omega$, over temperature		30	150	μV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm 10V$	25,000			V/V
CMRR	Common-mode rejection ratio	$R_S \leqslant 10k\Omega$, $V_{CM} = \pm 12V$ Over temperature	70			dB
I_{SC}	Output short-circuit current		10	25	60	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

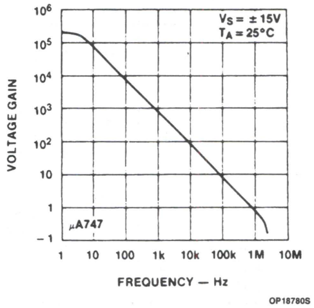
SYMBOL	PARAMETER	TEST CONDITIONS	μA747/μA747C/ SA747C			UNIT
			Min	Typ	Max	
t_R	Transient response Rise time Overshoot	$V_{IN} = 20mV$, $R_1 = 2k\Omega$, $C_1 < 100pF$ Unity gain $C_L \leqslant 100pF$ Unity gain $C_L \leqslant 100pF$		 0.3 5.0		 μs %
SR	Slew rate	$R_L > 2k\Omega$		0.5		V/μs

Dual Operational Amplifier

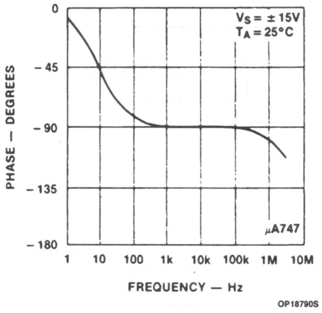
μA747/747C/SA747C

TYPICAL PERFORMANCE CHARACTERISTICS

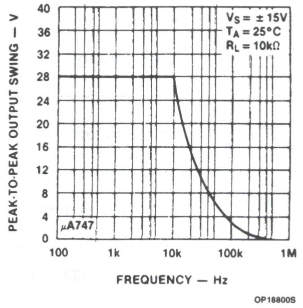
Open-Loop Voltage Gain as a Function of Frequency



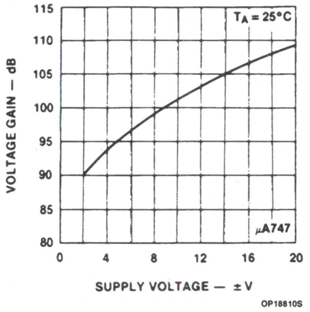
Open-Loop Phase Response as a Function of Frequency



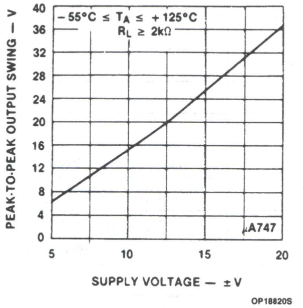
Output Voltage Swing as a Function of Frequency



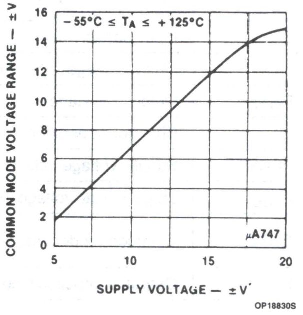
Open-Loop Voltage Gain as a Function of Supply Voltage



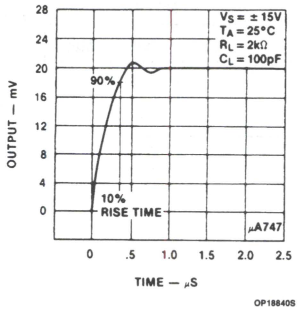
Output Voltage Swing as a Function of Supply Voltage



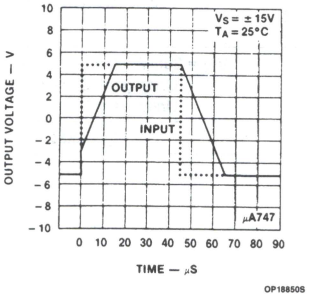
Input Common-Mode Voltage Range as a Function of Supply Voltage



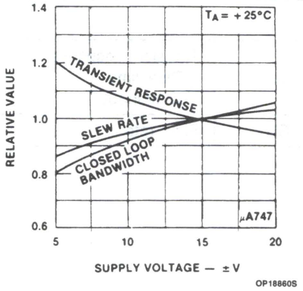
Transient Response



Voltage-Follower Large-Signal Pulse Response

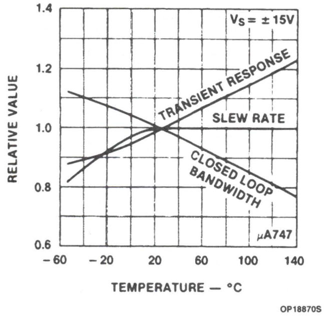


Frequency Characteristics as a Function of Supply Voltage

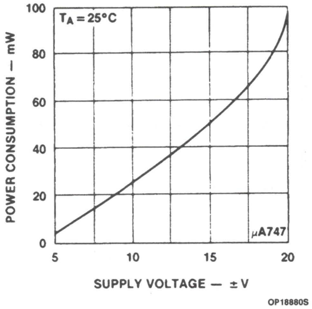


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

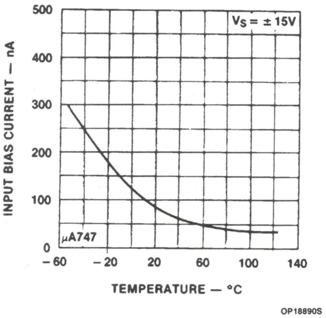
Frequency Characteristics as a Function of Ambient Temperature



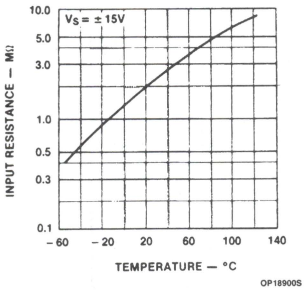
Power Consumption as a Function of Supply Voltage



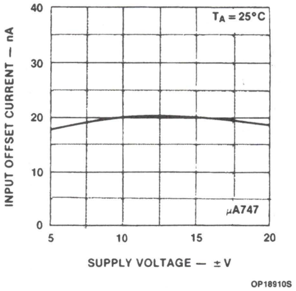
Input Bias Current as a Function of Ambient Temperature



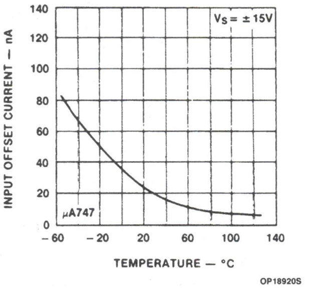
Input Resistance as a Function of Ambient Temperature



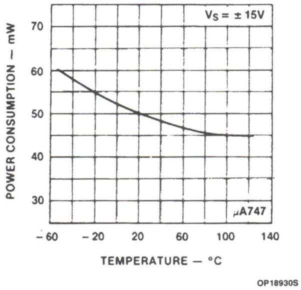
Input Offset Current as a Function of Supply Voltage



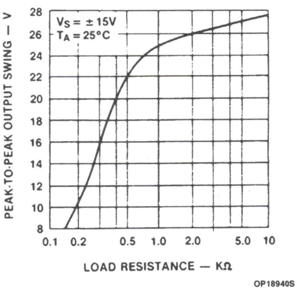
Input Offset Current as a Function of Ambient Temperature



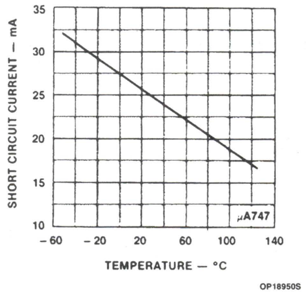
Power Consumption as a Function of Ambient Temperature



Output Voltage Swing as a Function of Load Resistance

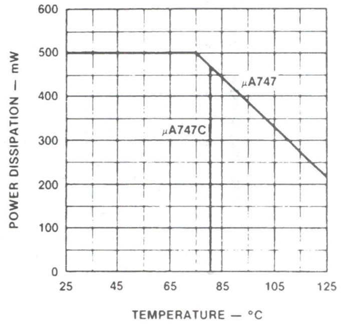


Output Short-Circuit Current as a Function of Ambient Temperature



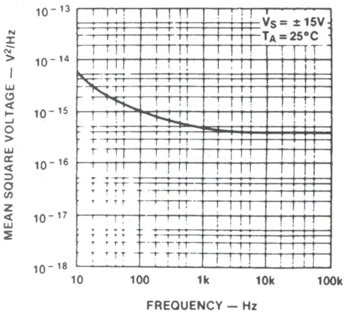
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Absolute Maximum Power Dissipation as a Function of Ambient Temperature



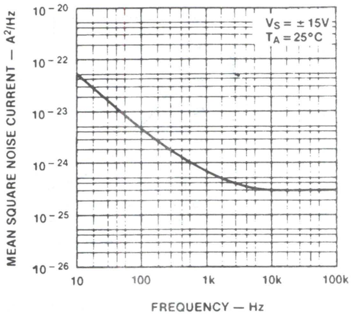
OP18960S

Input Noise Voltage as a Function of Frequency



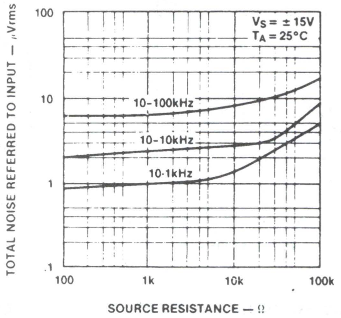
OP18970S

Input Noise Current as a Function of Frequency



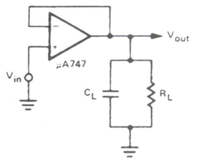
OP18980S

Broadband Noise for Various Bandwidths



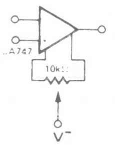
OP18990S

TEST CIRCUITS



TC21460S

Transient Response Test Circuit



TC21470S

Voltage Offset Null Circuit

Signetics

NE/SA5204
Wide-band High-Frequency Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The −3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

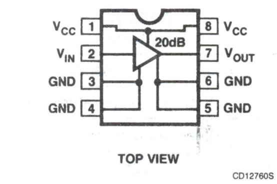
The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- **200MHz (min.), ±0.5dB bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-mount package available**
- **Cascadable**

PIN CONFIGURATION

N, D Packages



APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Networks**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5204N
	−40 to +85°C	SA5204N
8-Pin Plastic SO package	0 to +70°C	NE5204D
	−40 to +85°C	SA5204D

Wide-band High-Frequency Amplifier NE/SA5204

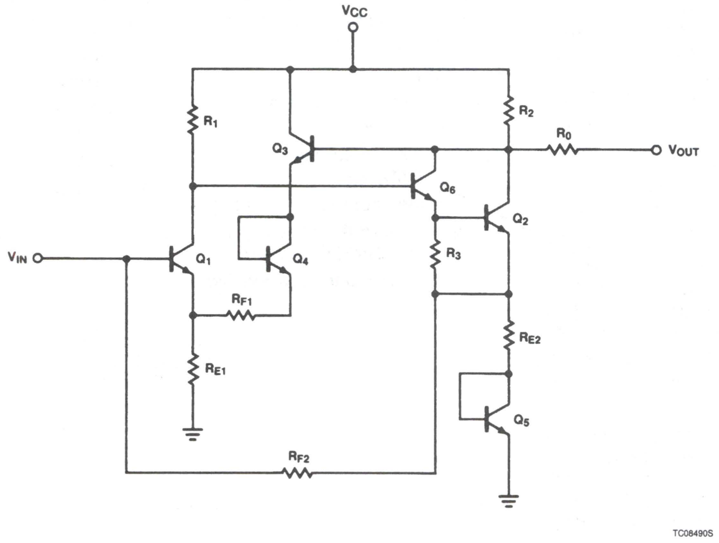
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	−40 to +85	°C
P_D	Maximum power dissipation[1, 2]		
	$T_A = 25°C$ (still-air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:

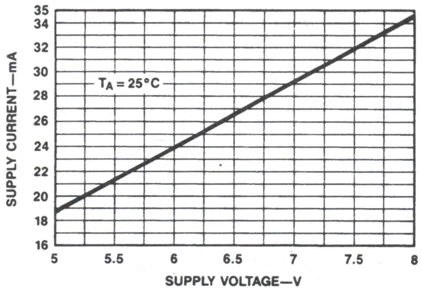
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



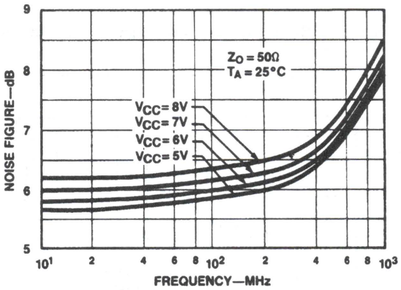
DC ELECTRICAL CHARACTERISTICS at $V_{CC} = 6V$, $Z_S = Z_L = Z_O = 50\Omega$ and $T_A = 25°C$, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f = 100MHz over temperature	16	19	22	dB
S11	Input return loss	f = 100MHz		25		dB
		DC −550MHz		12		dB
S22	Output return loss	f = 100MHz		27		dB
		DC −550MHz		12		dB
S12	Isolation	f = 100MHz		−25		dB
		DC −550MHz		−18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	−3dB	350	550		MHz
	Noise figure (75Ω)	f = 100MHz		4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0		dB
	Saturated output power	f = 100MHz		+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24		dBm



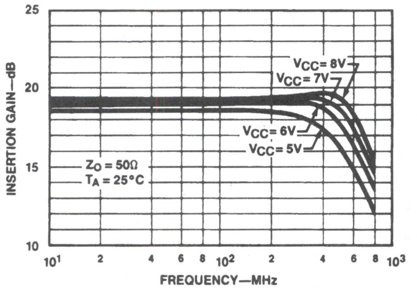
OP04640S

Figure 1. Supply Current vs Supply Voltage



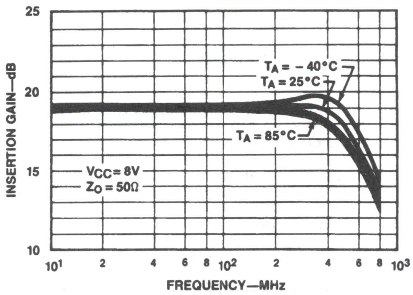
OP04650S

Figure 2. Noise Figure vs Frequency



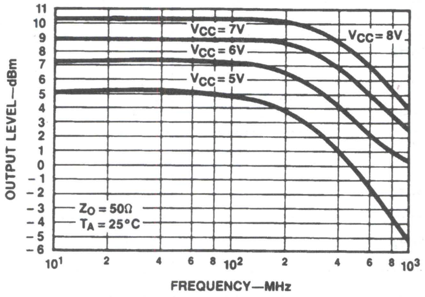
OP04660S

Figure 3. Insertion Gain vs Frequency (S_{21})



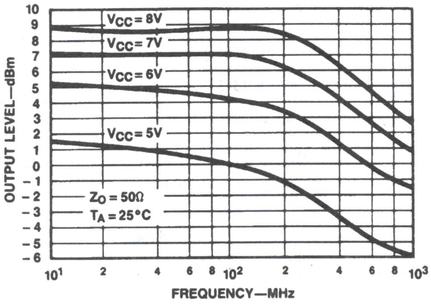
OP04671S

Figure 4. Insertion Gain vs Frequency (S_{21})



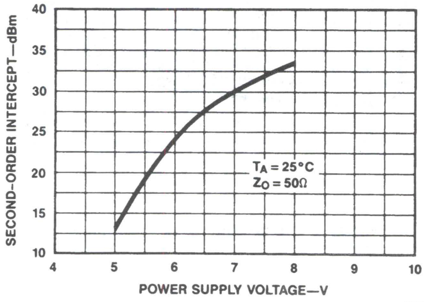
OP04680S

Figure 5. Saturated Output Power vs Frequency



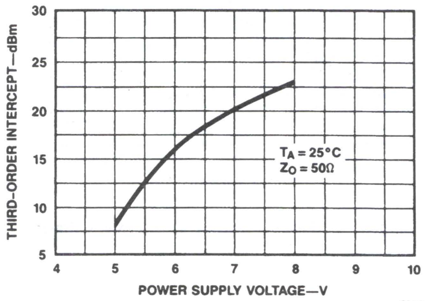
OP04690S

Figure 6. 1dB Gain Compression vs Frequency



OP04700S

Figure 7. Second-Order Output Intercept vs Supply Voltage



OP04710S

Figure 8. Third-Order Intercept vs Supply Voltage

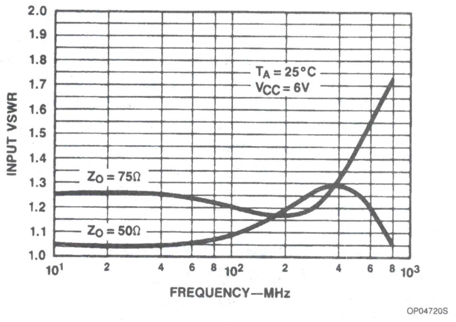


Figure 9. Input VSWR vs Frequency

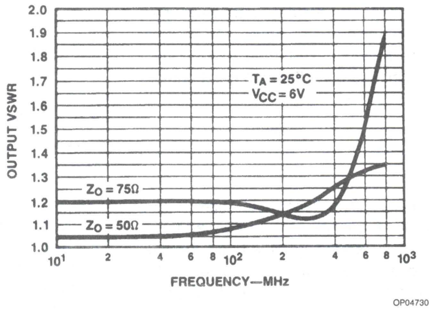


Figure 10. Output VSWR vs Frequency

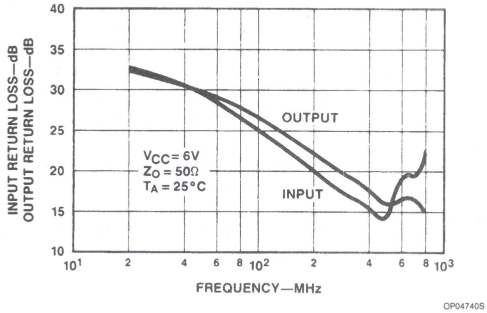


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

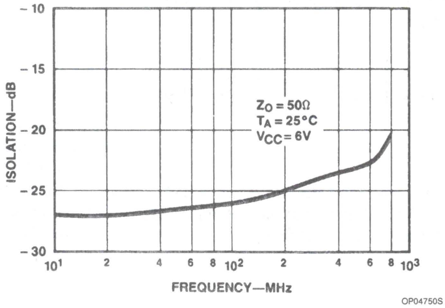


Figure 12. Isolation vs Frequency (S_{12})

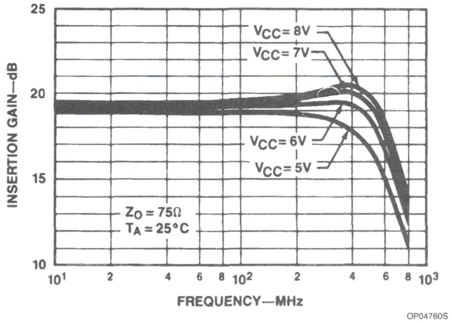


Figure 13. Insertion Gain vs Frequency (S_{21})

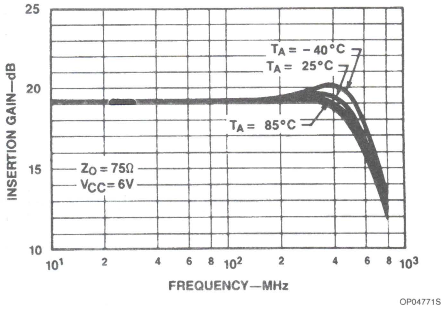


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0}\right\} \text{dB} \qquad (2)$$

where $I_{C1} = 5.5\text{mA}$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26\text{mV}$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\,R_{E1} \qquad (3)$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8\text{V}$, $I_{C1} = 5\text{mA}$ and $I_{C3} = 7\text{mA}$ (currents rated at $V_{CC} = 6\text{V}$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \qquad (4)$$

where $V_{CC} = 6\text{V}$, $R_2 = 225\Omega$, $I_{C2} = 7\text{mA}$ and $I_{C6} = 5\text{mA}$.

From here, it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

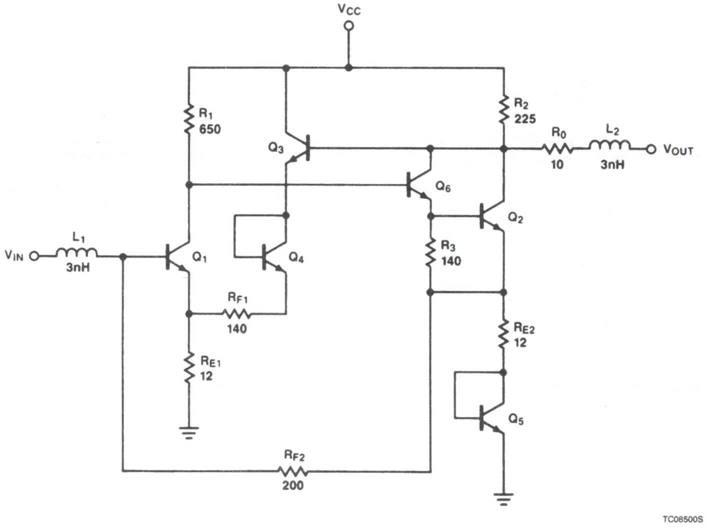


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

Both of the evaluation boards that will be discussed next do not have input and output capacitors because it is assumed the user will use AC-coupled test systems. Chip or foil capacitors can easily be inserted between the part and connector if the board trace is removed.

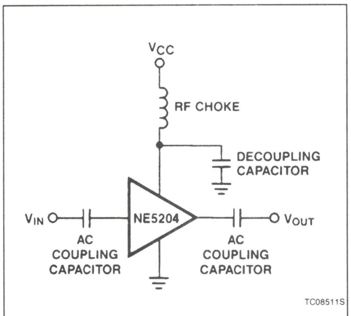
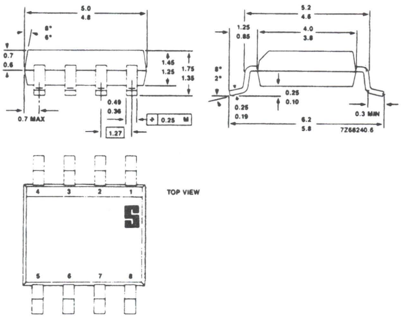
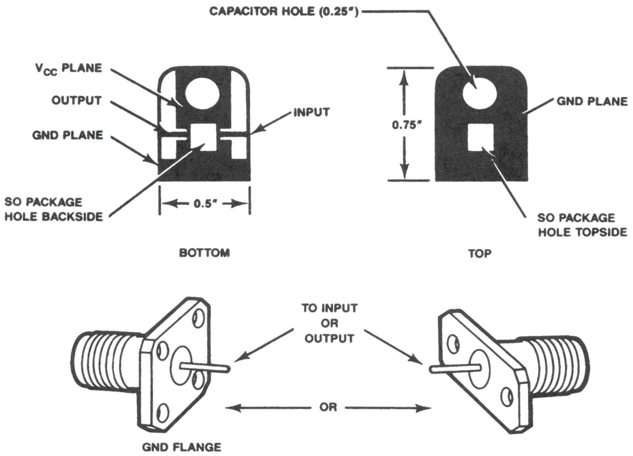

VCC
RF CHOKE
DECOUPLING CAPACITOR
VIN
NE5204
VOUT
AC COUPLING CAPACITOR
AC COUPLING CAPACITOR
TC08511S

Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)


5.0
4.8
8°
6°
0.7
0.6
1.45
1.25
1.75
1.35
0.49
0.36
0.7 MAX
0.25 M
1.27
5.2
4.6
1.25
0.85
4.0
3.8
8°
2°
0.25
0.10
0.25
0.19
6.2
5.8
0.3 MIN
7Z68240.6
4
3
2
1
TOP VIEW
5
6
7
8

PO00670S


CAPACITOR HOLE (0.25")
VCC PLANE
OUTPUT
GND PLANE
INPUT
SO PACKAGE HOLE BACKSIDE
0.5"
BOTTOM
0.75"
GND PLANE
SO PACKAGE HOLE TOPSIDE
TOP
TO INPUT OR OUTPUT
OR
GND FLANGE
SMA CONNECTOR

DF05890S

Figure 17. PC Board Layout for NE5204 Evaluation

50Ω EVALUATION BOARD

The evaluation board layout shown in Figure 17 produces excellent results. The board is to scale and is for the SO package. Both top and bottom are copper clad and the ground planes are bonded together through 50Ω SMA cable connectors. These are solder mounted on the sides of the board so that the signal traces line up straight to the connector signal pins.

Solid copper tubing is soldered through the flange holes between the two connectors for increased strength and grounding characteristics. Two- or four-hole flanges can be used. A flat, round decoupling capacitor is placed in the board's round hole and soldered between the bottom V_{CC} plane and the top side ground. The capacitor is as thin or thinner than the PC board thickness and has insulation around its side to isolate V_{CC} and ground. The square hole is for the SO package which is put in upside-down through the bottom of the board so that the leads are kept in position for soldering. Both holes are just slightly larger than the capacitor and IC to provide for a tight fit.

This board should be tested in a system with 50Ω input and output impedance for correct operation.

75Ω EVALUATION BOARD

Another evaluation board is shown in Figure 18. This system uses the same PC board as presented in Figure 17, but makes use of 75Ω female N-type connectors. The board is mounted in a nickel plated box* that is used to support the N-type connectors. This is an excellent way to test the part for cable TV applications. Again, the board should be tested in a system with 75Ω input- and output-impedance for correct operation.

NOTE:

*The box and connectors are available as a "MOD-PACK SYSTEM" from the ANZAC division of ADAMS-RUSSELL CO., INC., 80 Cambridge Street, Burlington, MA 01803.

SCATTERING PARAMETERS

The primary specifications for the NE5204 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

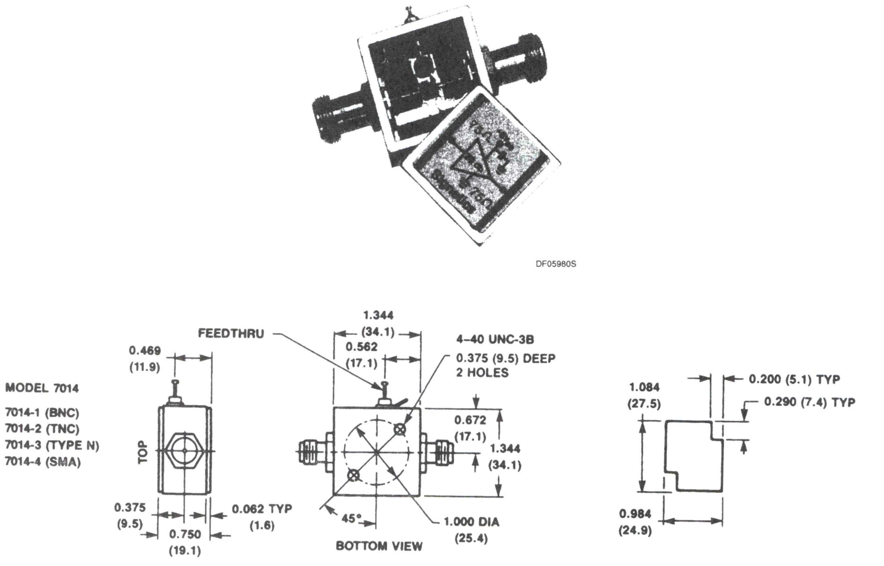
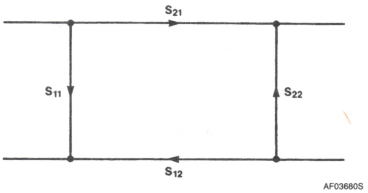

DF05980S
MODEL 7014
7014-1 (BNC)
7014-2 (TNC)
7014-3 (TYPE N)
7014-4 (SMA)
0.469
(11.9)
TOP
0.375
(9.5)
0.750
(19.1)
0.062 TYP
(1.6)
FEEDTHRU
1.344
(34.1)
0.562
(17.1)
4–40 UNC-3B
0.375 (9.5) DEEP
2 HOLES
0.672
(17.1)
1.344
(34.1)
45°
1.000 DIA
(25.4)
BOTTOM VIEW
1.084
(27.5)
0.200 (5.1) TYP
0.290 (7.4) TYP
0.984
(24.9)
AF03670S

Figure 18. 75Ω N-Type Connector System

Wide-band High-Frequency Amplifier NE/SA5204



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

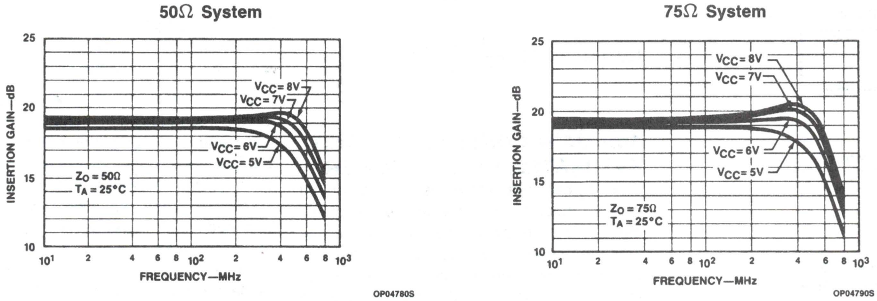
S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

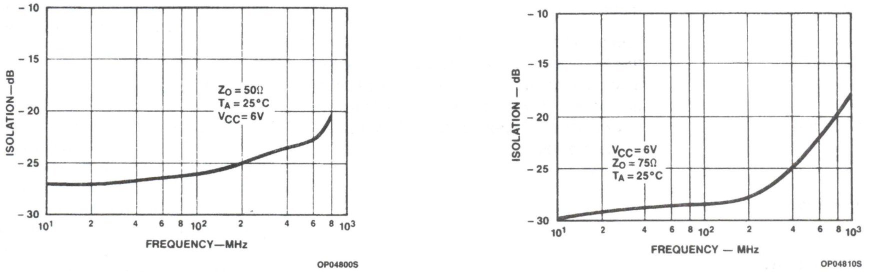
b.

Figure 19



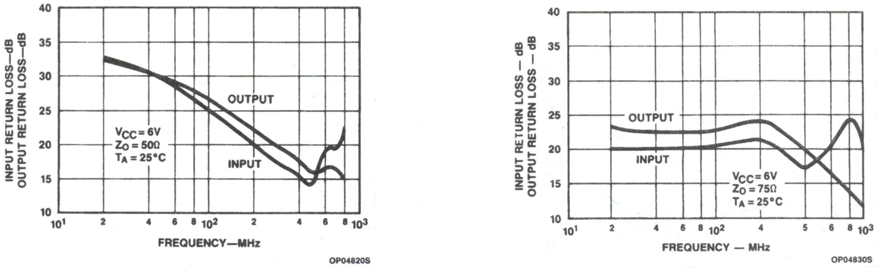
a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})



c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

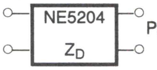
Figure 20

Actual S-parameter measurements, using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B), are shown in Figure 20. These were obtained with the device mounted in a PC board as described in Figures 17 and 18.

For 50Ω system measurements, SMA connectors were used. The 75Ω data was obtained using N-connectors.

Values for Figure 20 are measured and specified in the data sheet to ease adaptation and comparison of the NE5204 to other high-frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5204



$$P_{IN} = \frac{V_{IN}^2}{Z_D} \qquad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I = V_I^2$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE5204 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10\text{Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20\text{Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing-wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB
$S_{11}\text{dB} = 20\text{Log } |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB
$S_{22}\text{dB} = 20\text{Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to non-linearities in the amplifier, an indication of the point of transition between small-signal operation and the large-signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

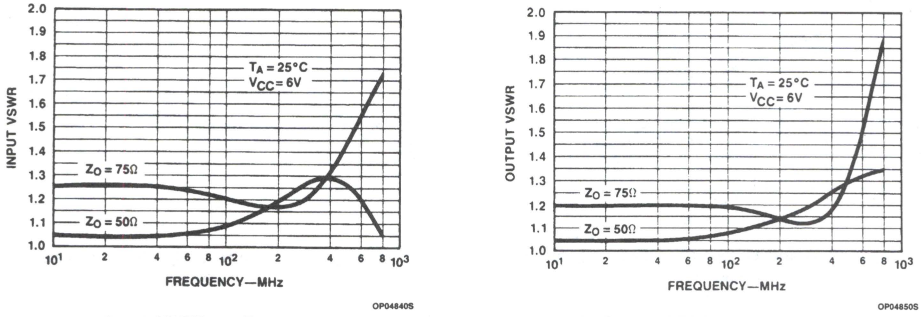
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second-order IMR is equal to the difference between the second-order intercept and the fundamental output level. The third-order IMR is equal to twice the difference between the third-order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second- and third-order output intercepts in dBm, and IMR_2 and IMR_3 are the second- and third- order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small-signal operat-



a. Input VSWR vs Frequency b. Output VSWR vs Frequency

Figure 21. Input/Output VSWR vs Frequency

ing range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point, the intermodulation products no longer follow the straight-line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select levels which are too low, because the test equipment may not be able to recover the signal from the noise. For the NE5204, an output level of −10.5dBm was chosen with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers*; by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985, published by John Wiley & Sons, Inc.

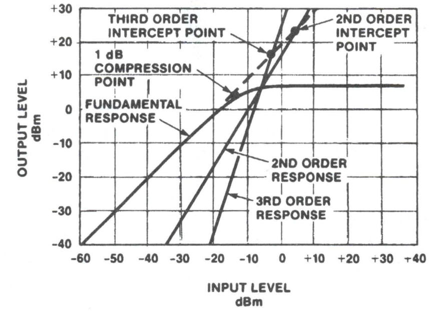


Figure 22

S-Parameter Techniques for Faster, More Accurate Network Design, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, HP App Note 154, 1972.

Signetics

NE/SA/SE5205
Wide-band High Frequency Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA/SE5205 is a High Frequency Amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the −3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 650MHz. The metal can and Cerdip package are hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

FEATURES

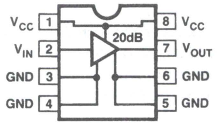
- **650MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to $50/75\Omega$ systems**
- **Surface mount package available**
- **Excellent performance in cable TV 75Ω systems**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

PIN CONFIGURATIONS

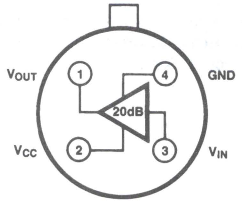
N, FE, D Packages



TOP VIEW

CD12760S

EC Package



CD09850S

NOTE:
Tab denotes Pin 1.

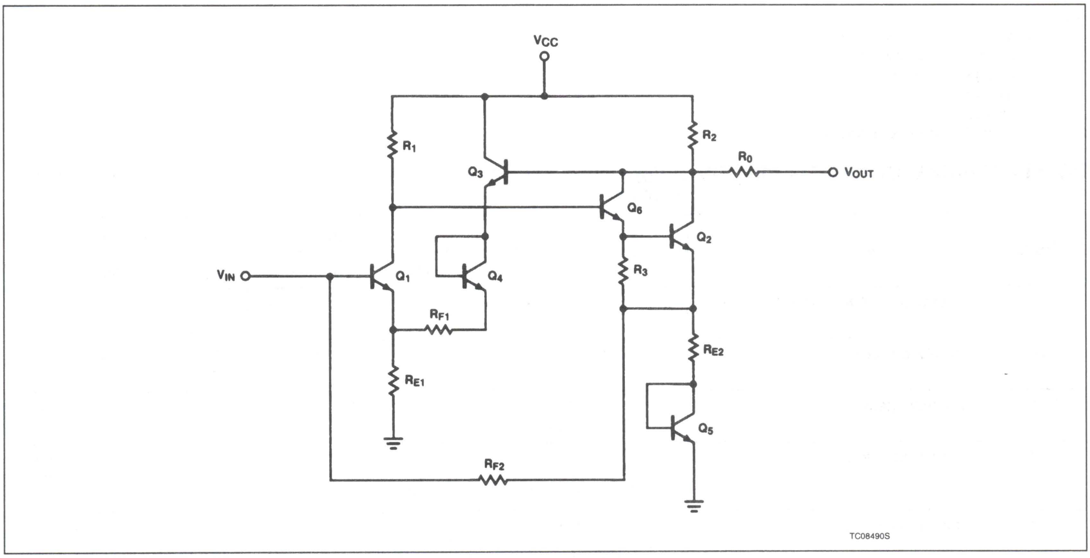
Wide-band High Frequency Amplifier

NE/SA/SE5205

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
8-Pin Metal can	0 to +70°C	NE5205EC
4-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	−40°C to +85°C	SA5205D
8-Pin Plastic DIP	−40°C to +85°C	SA5205N
8-Pin Cerdip	−40°C to +85°C	SA5205FE
8-Pin Cerdip	−55°C to +125°C	SE5205FE

EQUIVALENT SCHEMATIC


VCC
R1
R2
R0
Q3
VOUT
Q6
Q2
VIN
Q1
Q4
R3
RF1
RE2
RE1
Q5
RF2
TC08490S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade SE grade	 0 to +70 -40 to +85 -55 to +125	 °C °C °C
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1, 2] FE package N package D package EC package	 780 1160 780 1250	 mW mW mW mW

NOTES:

1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

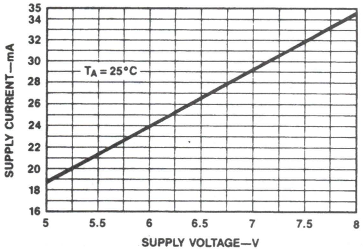
SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA/SE5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f = 100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f = 100MHz D, N, FE		25			25		dB
		DC – f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f = 100MHz EC package					24		dB
		DC – f_{MAX} EC				10			dB
S22	Output return loss	f = 100MHz D, N, FE		27			27		dB
		DC – f_{MAX}	12			12			dB
S22	Output return loss	f = 100MHz EC package					26		dB
		DC – F_{MAX}				10			dB
S12	Isolation	f = 100MHz		-25			-25		dB
		DC – f_{MAX}	-18			-18			dB

Wide-band High Frequency Amplifier

NE/SA/SE5205

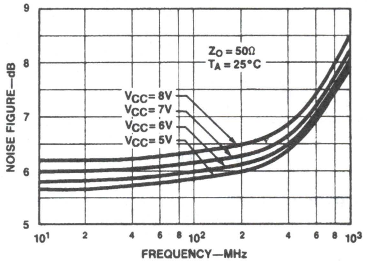
DC ELECTRICAL CHARACTERISTICS at $V_{CC} = 6V$, $Z_S = Z_L = Z_O = 50\Omega$ and $T_A = 25°C$, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA/SE5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth	±0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	−3dB D, N				550			MHz
f_{MAX}	Bandwidth	±0.5dB EC		300			500		MHz
f_{MAX}	Bandwidth	±0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	−3dB EC				600			MHz
f_{MAX}	Bandwidth	−3dB FE	400			400			MHz
	Noise figure (75Ω)	f = 100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0			6.0		dB
	Saturated output power	f = 100MHz		+7.0			+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24			+24		dBm



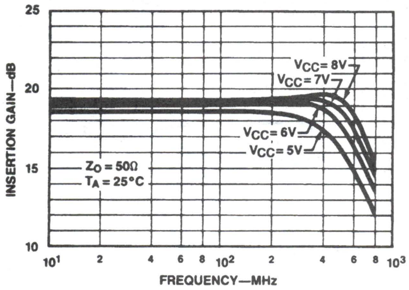
OP04640S

Figure 1. Supply Current vs Supply Voltage



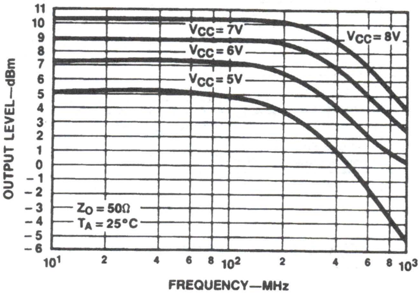
OP04650S

Figure 2. Noise Figure vs Frequency



OP04660S

Figure 3. Insertion Gain vs Frequency (S_{21})



OP04680S

Figure 4. Insertion Gain vs Frequency (S_{21})

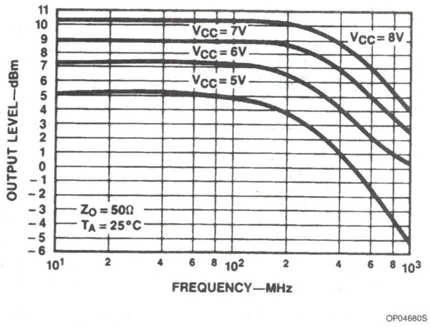


Figure 5. Saturated Output Power vs Frequency

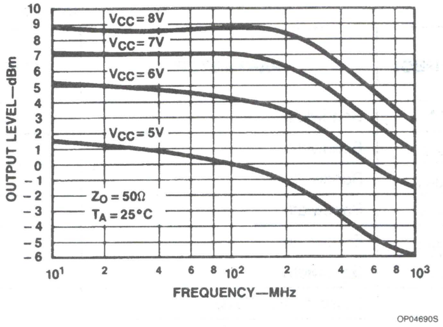


Figure 6. 1dB Gain Compression vs Frequency

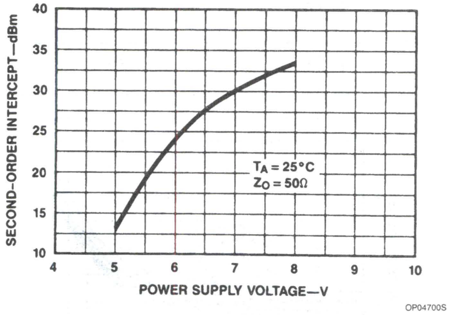


Figure 7. Second-Order Output Intercept vs Supply Voltage

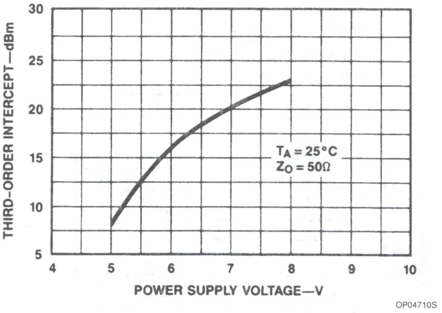


Figure 8. Third-Order Intercept vs Supply Voltage

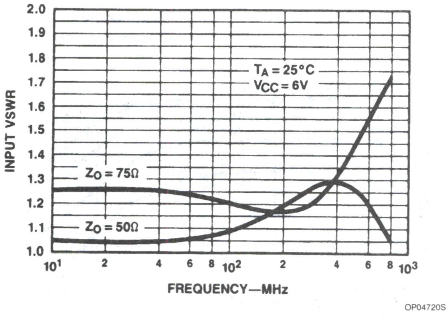


Figure 9. Input VSWR vs Frequency

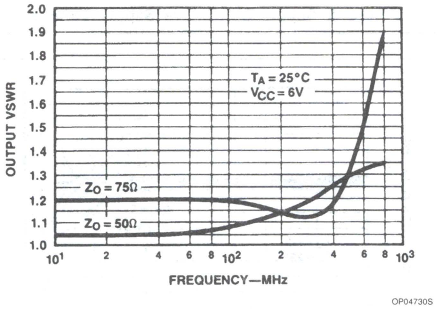


Figure 10. Output VSWR vs Frequency

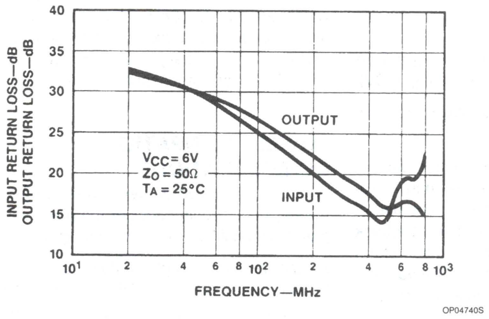


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

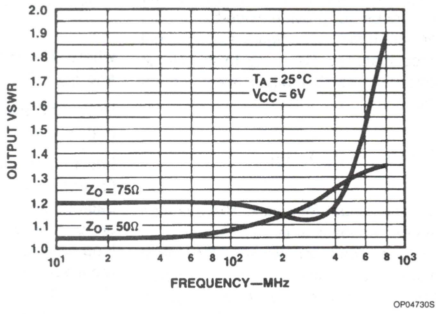


Figure 12. Isolation vs Frequency (S_{12})

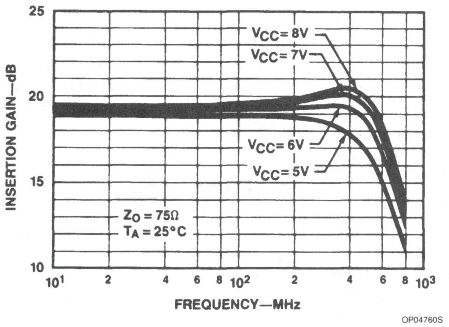


Figure 13. Insertion Gain vs Frequency (S_{21})

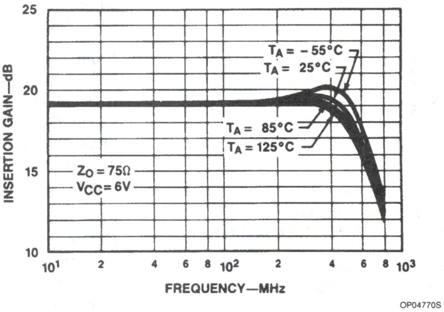


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}} \right]}{R_0} \right\} \text{dB} \qquad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\ R_{E1}$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \qquad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all

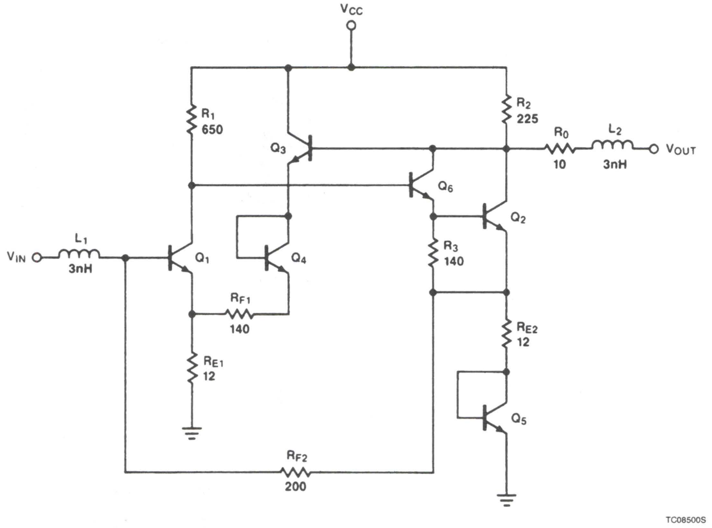


Figure 15. Schematic Diagram

GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

Both of the evaluation boards that will be discussed next do not have input and output capacitors because it is assumed the user will use AC coupled test systems. Chip or foil capacitors can easily be inserted between the part and connector if the board trace is removed.

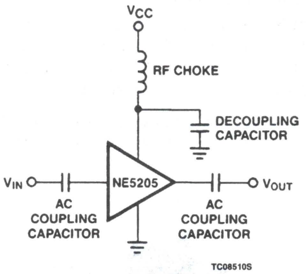
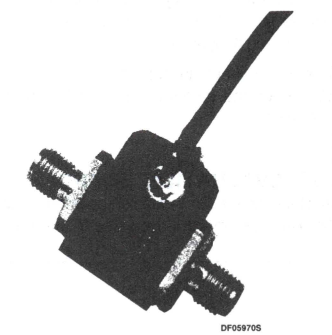
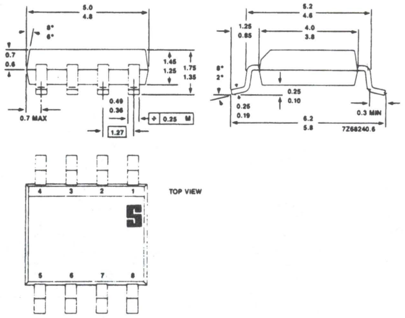

V_{CC}
RF CHOKE
DECOUPLING CAPACITOR
V_{IN}
NE5205
V_{OUT}
AC COUPLING CAPACITOR
AC COUPLING CAPACITOR
TC08510S

Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling



8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)


5.0
4.8
8°
6°
0.7
0.6
1.45
1.25
1.75
1.35
0.49
0.36
0.7 MAX
0.25 M
1.27
5.2
4.6
1.25
0.85
4.0
3.8
8°
2°
0.25
0.10
0.25
0.19
0.3 MIN
6.2
5.8
7Z68240.6
4
3
2
1
TOP VIEW
5
6
7
8

PO00670S

50Ω EVALUATION BOARD

The evaluation board layout shown in Figure 17 produces excellent results. The board is to scale and is for the SO package but can be used for the EC package as well. Both top and bottom are copper clad and the ground planes are bonded together through 50Ω SMA cable connectors. These are solder mounted on the sides of the board so that the signal traces line up straight to the connector signal pins.

Solid copper tubing is soldered through the flange holes between the two connectors for increased strength and grounding characteristics. Two or four hole flanges can be used. A flat round decoupling capacitor is placed in the board's round hole and soldered between the bottom V_{CC} plane and the top side ground. The capacitor is as thin or thinner than the PC board thickness and has insulation around its side to isolate V_{CC} and ground. The square hole is for the SO package which is put in upside down through the bottom of the board so that the leads are kept in

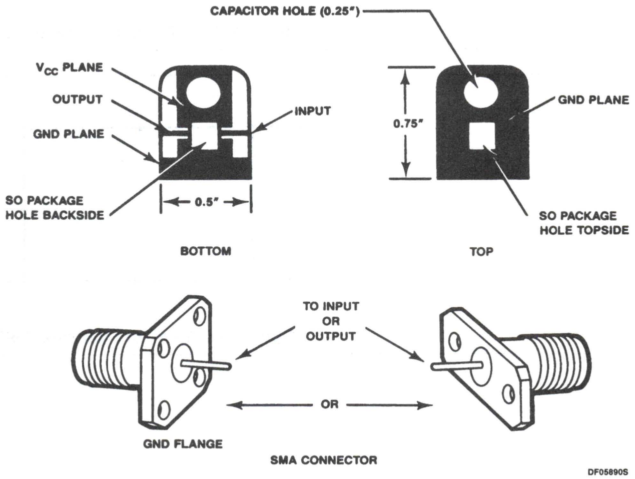

CAPACITOR HOLE (0.25″)
V_{CC} PLANE
OUTPUT
GND PLANE
INPUT
SO PACKAGE HOLE BACKSIDE
0.5″
BOTTOM
0.75″
GND PLANE
SO PACKAGE HOLE TOPSIDE
TOP
TO INPUT OR OUTPUT
OR
GND FLANGE
SMA CONNECTOR
DF05890S

Figure 17. BC Board Layout for NE/SA/SE5205 Evaluation

position for soldering. Both holes are just slightly larger than the capacitor and IC to provide for a tight fit.

This board should be tested in a system with 50Ω input and output impedance for correct operation.

75Ω EVALUATION BOARD

Another evaluation board is shown in Figure 18. This system uses the same PC board as presented in Figure 17, but makes use of 75Ω female N-type connectors. The board is mounted in a nickel plated box* that is used to support the N-type connectors. This is an excellent way to test the part for cable TV applications. Again, the board should be tested in a system with 75Ω input and output impedance for correct operation.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

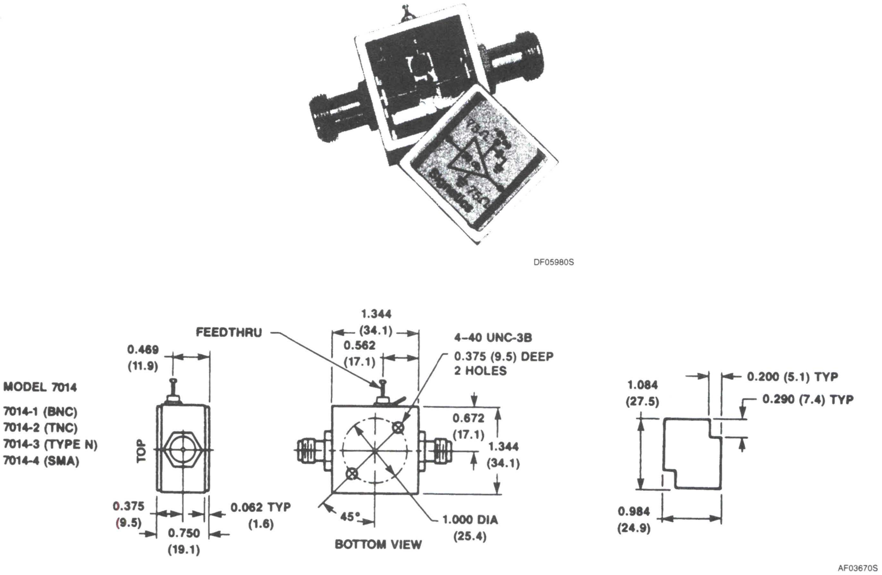

DF05980S
MODEL 7014
7014-1 (BNC)
7014-2 (TNC)
7014-3 (TYPE N)
7014-4 (SMA)
TOP
FEEDTHRU
0.469
(11.9)
0.375
(9.5)
0.750
(19.1)
0.062 TYP
(1.6)
1.344
(34.1)
0.562
(17.1)
4-40 UNC-3B
0.375 (9.5) DEEP
2 HOLES
0.672
(17.1)
1.344
(34.1)
45°
1.000 DIA
(25.4)
BOTTOM VIEW
1.084
(27.5)
0.200 (5.1) TYP
0.290 (7.4) TYP
0.984
(24.9)
AF03670S

Figure 18. 75Ω N-Type Connector System

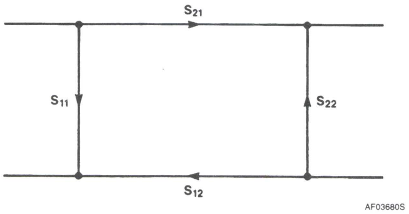

S21
S11
S22
S12
AF03680S

Figure 19a. Two-Port Network Defined

---

*The box and connectors are available as a "MOD-PACK SYSTEM" from the ANZAC division of ADAMS-RUSSELL CO., INC., 80 Cambridge Street, Burlington, MA 01803.

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

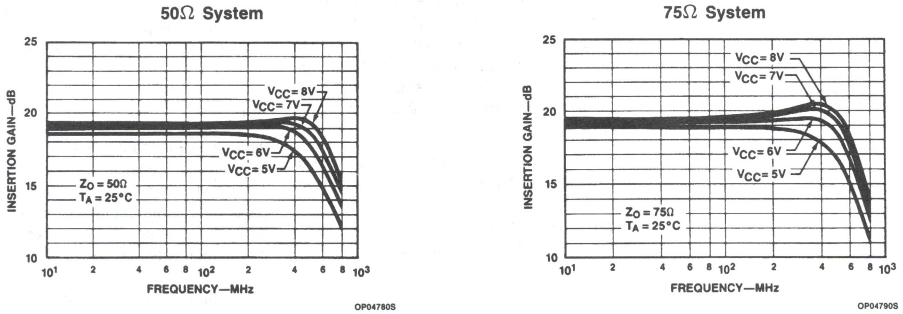
AF03690S

Figure 19b

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 20. These were obtained with the device mounted in a PC board as described in Figures 17 and 18.

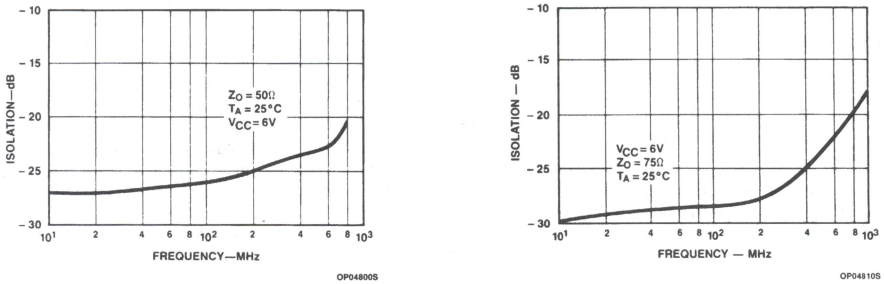
For 50Ω system measurements, SMA connectors were used. The 75Ω data was obtained using N-connectors.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high frequency amplifiers.



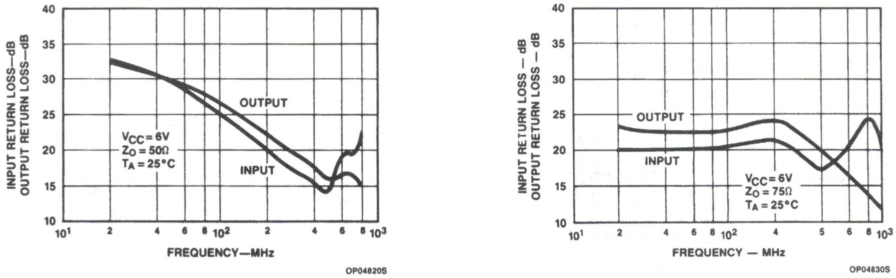
a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})



c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

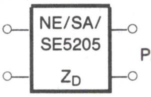
f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 20

Wide-band High Frequency Amplifier NE/SA/SE5205

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205



$$P_{IN} = \frac{V_{IN}^2}{Z_D} \qquad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$$

$$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$$

$$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB
$S_{11}\text{dB} = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB
$S_{22}\text{dB} = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

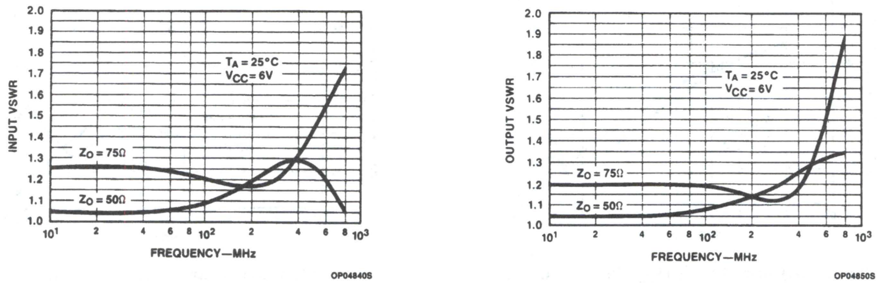
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency **b. Output VSWR vs Frequency**

Figure 21. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

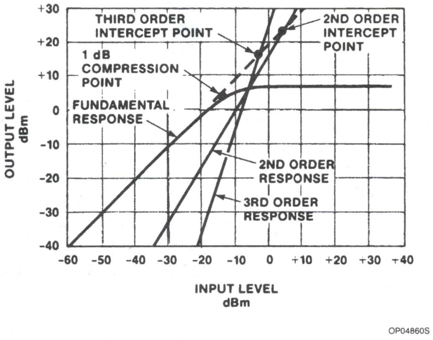


Figure 22

Signetics

NE/SA604
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The NE/SA604 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE/SA604 is available in a 16-lead dual in-line plastic and Cerdip packages and 16-lead SO (surface-mounted miniature package).

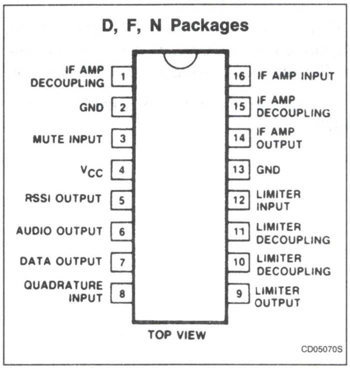
FEATURES

- **Low power consumption: 2.3mA typical**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.27μV into 50Ω matching network) for 12dB SINAD (Signal-to-Noise and Distortion ratio) at 455kHz**
- **SA604 meets cellular radio specifications**

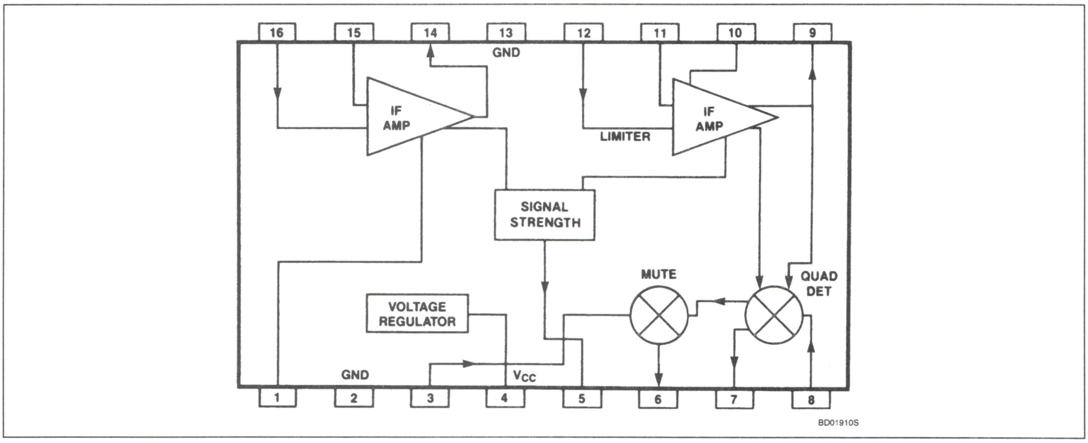
APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**

PIN CONFIGURATION


D, F, N Packages
IF AMP DECOUPLING 1
GND 2
MUTE INPUT 3
VCC 4
RSSI OUTPUT 5
AUDIO OUTPUT 6
DATA OUTPUT 7
QUADRATURE INPUT 8
16 IF AMP INPUT
15 IF AMP DECOUPLING
14 IF AMP OUTPUT
13 GND
12 LIMITER INPUT
11 LIMITER DECOUPLING
10 LIMITER DECOUPLING
9 LIMITER OUTPUT
TOP VIEW
CD05070S

BLOCK DIAGRAM


16
15
14
13
12
11
10
9
GND
IF AMP
LIMITER
IF AMP
SIGNAL STRENGTH
MUTE
QUAD DET
VOLTAGE REGULATOR
GND
VCC
1
2
3
4
5
6
7
8
BD01910S

Low Power FM IF System NE/SA604

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE604N
16-Pin Plastic SO	0 to +70°C	NE604D
16-Pin Cerdip	0 to +70°C	NE604F
16-Pin Plastic DIP	−40°C to +85°C	SA604N
16-Pin Cerdip	−40°C to +85°C	SA604F
16-Pin Plastic SO	−40°C to +85°C	SA604D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE604 SA604	 0 to +70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated.

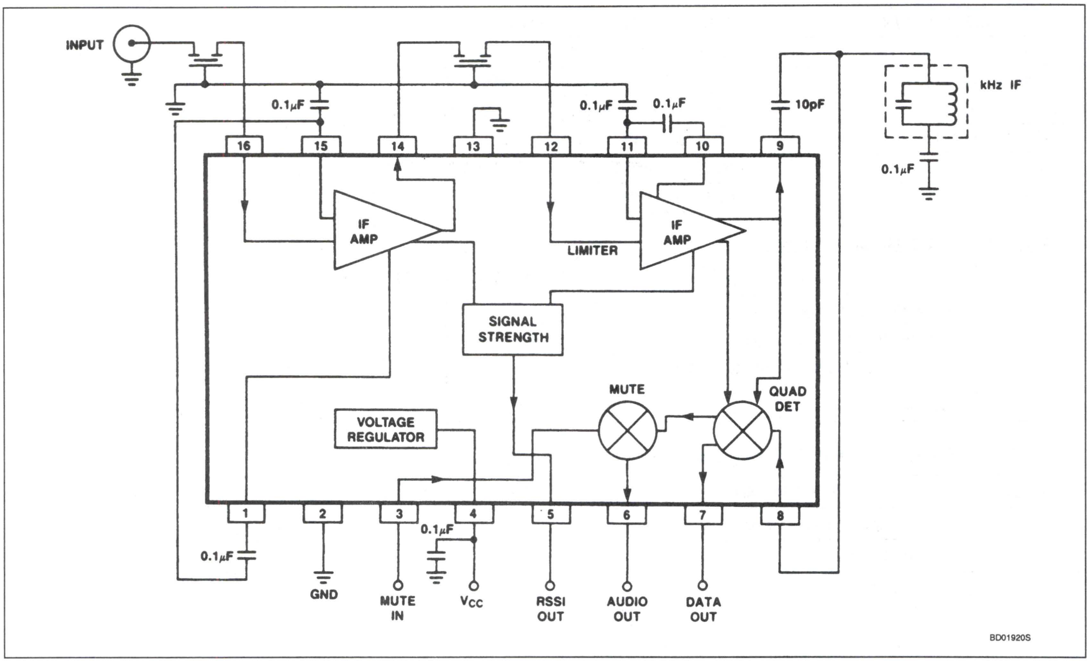
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain				2.7	mA
	Mute switch input threshold (on) (off)		 1.7 		 1.0	 V V

AC ELECTRICAL CHARACTERISTICS

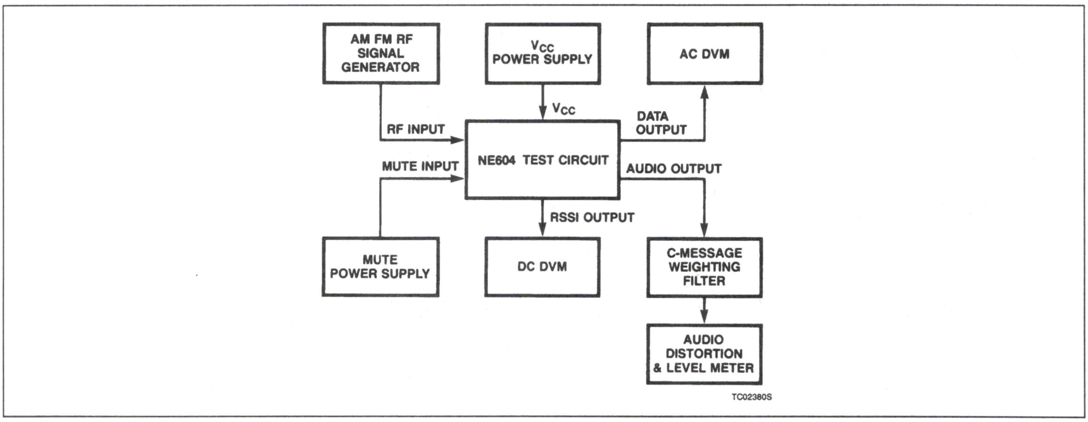
$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 455kHz; RF level = −47dBm; FM modulation = 1kHz with+8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

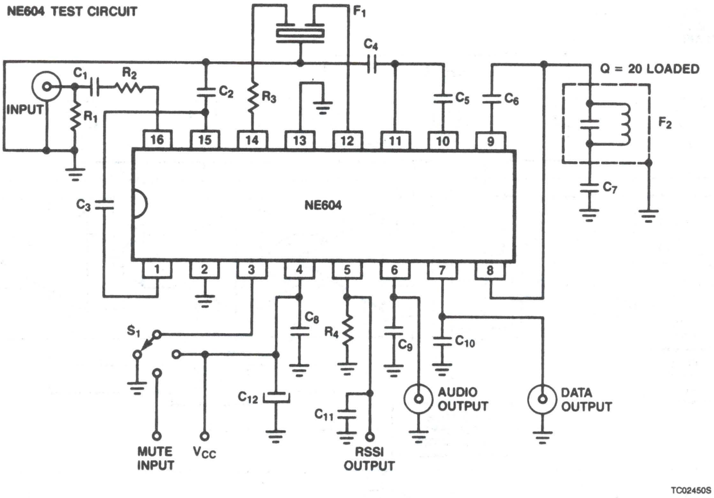
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input limiting − 3dB	Test at Pin 16			−90	dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level − 97dBm	12	15		dB
THD	Total harmonic distortion		−35			dB
S/N	Signal-to-noise ratio	No modulation for noise	70	75		dB
	RSSI output	$R_4 = 100k\Omega$ RF level = −97dBm RF level = −47dBm RF level = 3dBm	 0 2.0 4.0		 400 2.6 5.0	 mV V V
	RSSI range	$R_4 = 100k\Omega$ Pin 5		90		dB
	RSSI accuracy	$R_4 = 100k\Omega$ Pin 5		±1.5		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance		50			kΩ
	Muted audio output impedance			50		kΩ

TYPICAL APPLICATION


INPUT
0.1µF
0.1µF
0.1µF
10pF
kHz IF
0.1µF
16
15
14
13
12
11
10
9
IF AMP
LIMITER
IF AMP
SIGNAL STRENGTH
MUTE
QUAD DET
VOLTAGE REGULATOR
1
2
3
4
5
6
7
8
0.1µF
0.1µF
GND
MUTE IN
VCC
RSSI OUT
AUDIO OUT
DATA OUT
BD01920S

NE604 TEST SETUP


AM FM RF SIGNAL GENERATOR
VCC POWER SUPPLY
AC DVM
VCC
RF INPUT
DATA OUTPUT
NE604 TEST CIRCUIT
MUTE INPUT
AUDIO OUTPUT
RSSI OUTPUT
MUTE POWER SUPPLY
DC DVM
C-MESSAGE WEIGHTING FILTER
AUDIO DISTORTION & LEVEL METER
TC02380S



C1 10nF +80 − 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V Polyester
C3 100nF ± 10% 50V Polyester
C4 100nF ± 10% 50V Polyester
C5 100nF ± 10% 50V Polyester
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V Polyester
C8 100nF ± 10% 50V Polyester
C9 15nF ± 10% 50V Polyester
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8uF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film

Figure 1. NE604 Test Circuit and Parts List

DESCRIPTION OF OPERATION

The NE/SA604 is comprised of five subsystems for IF signal processing. These subsystems, two IF limiting amplifiers, quadrature detector, audio mute, and logarithmic signal strength, can be configured to satisfy many high-performance or low-power systems objectives. Internal temperature compensated bias regulation completes the circuitry. Taken together, the SA604 exceeds the demanding technical requirements for cellular radio.

Figure 2 shows the equivalent circuits of the NE/SA604.

Limiting Amplifiers

The NE/SA604 has two independent limiting IF amplifiers. The first has a gain of 30dB. The second has 60dB gain. Both have 1.5k nominal input impedance and 15MHz bandwidth. The output impedance of the first limiter is approximately 1kΩ. These impedances permit direct interface with popular ceramic filters such as the SFU455. On the surface, the 1k output of the first limiter would not seem correct. However, approximately 6dB insertion loss is required between limiter stages to optimize the linearity of the signal strength indicator. The impedance mismatch has little effect on passband. Use of an interstage filter reduces wide-band noise. A DC blocking capacitor or L/C filter can also be used.

As the signal frequency increases, the 90dB total gain can become a source of instability. Figure 3 shows the limiters as a closed-loop system with stray capacitance and the equivalent AC input impedance setting the loop gain.

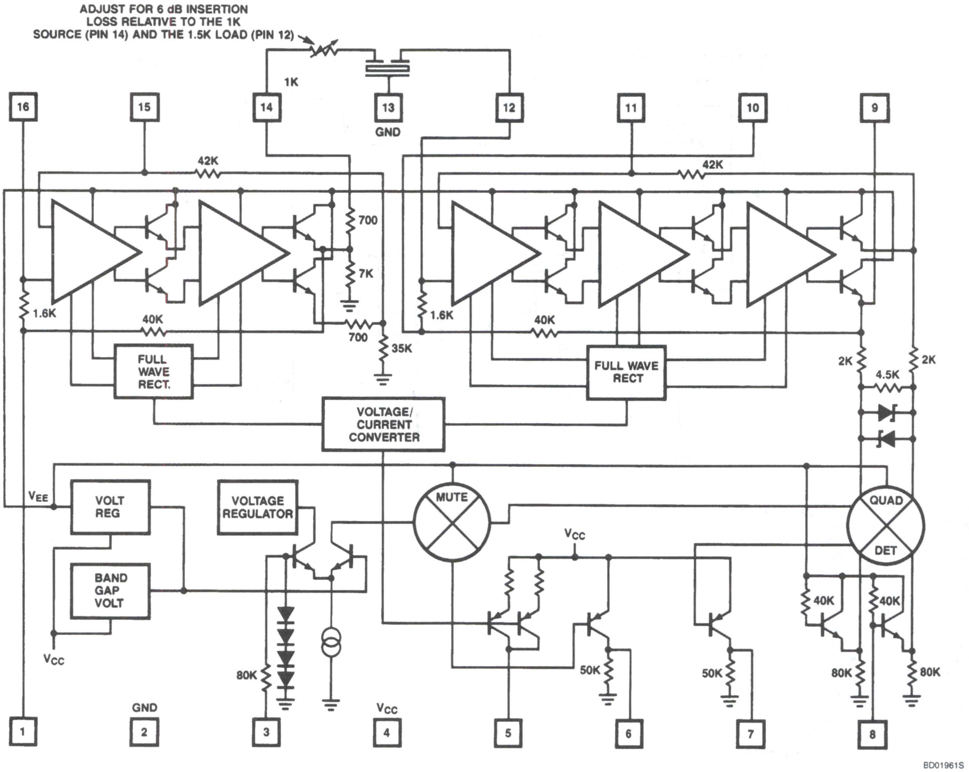

ADJUST FOR 6 dB INSERTION
LOSS RELATIVE TO THE 1K
SOURCE (PIN 14) AND THE 1.5K LOAD (PIN 12)
1K
16
15
14
13
GND
12
11
10
9
42K
42K
700
7K
1.6K
1.6K
40K
40K
700
35K
FULL WAVE RECT.
FULL WAVE RECT
VOLTAGE/ CURRENT CONVERTER
2K
2K
4.5K
VEE
VOLT REG
VOLTAGE REGULATOR
MUTE
QUAD DET
VCC
BAND GAP VOLT
VCC
80K
40K
40K
50K
50K
80K
80K
GND
VCC
1
2
3
4
5
6
7
8
BD01961S

Figure 2. Equivalent Circuit

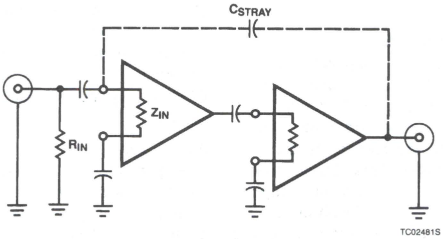
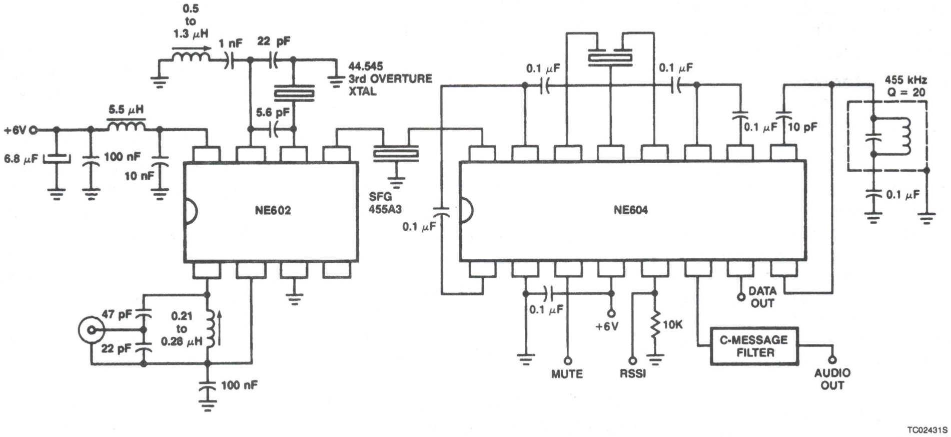

CSTRAY
ZIN
RIN
TC02481S

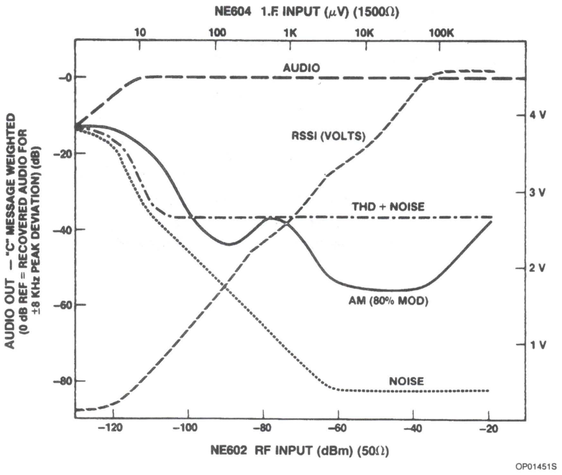
Figure 3. Considerations for Stability

The equivalent AC attenuation factor from the output to the input must be greater than 90dB or oscillation can occur. The input impedance of the device is nominally 1.5k. The stray layout capacitance is a frequency-dependent impedance so that as the frequency of operation or the value of stray capacitance increases, the output-to-input attenuation factor decreases. Keep stray capacitance low by using good RF layout technique. Sockets should be avoided above 455kHz.

Good RF layout is the proper way to avoid instability. However, if system constraints require, stability can be achieved by only using one of the limiting amplifiers, or by adding a resistance, R_{IN}, which will increase the attenuation factor.


0.5
to
1.3 μH
1 nF
22 pF
44.545
3rd OVERTURE
XTAL
5.6 pF
5.5 μH
+6V
6.8 μF
100 nF
10 nF
NE602
SFG
455A3
0.1 μF
NE604
0.1 μF
0.1 μF
0.1 μF
10 pF
455 kHz
Q = 20
0.1 μF
DATA
OUT
47 pF
0.21
to
0.28 μH
22 pF
100 nF
0.1 μF
+6V
10K
C-MESSAGE
FILTER
MUTE
RSSI
AUDIO
OUT
TC02431S

a. Cellular Radio Configuration



b. Cellular Circuit Performance

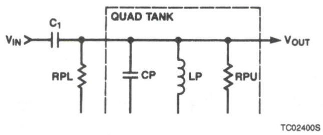
Figure 4

Adding an input resistor is an easy way to reduce the attenuation factor, but may make correct termination of interstage filters difficult or impossible. At 455kHz instability should not be a problem if reasonable RF layout is used.

Quadrature Detector

The detector of the NE604 is a four quadrant multiplier of the Gilbert cell type. It can be used for frequency or amplitude demodulation. Figure 4 indicates a typical quadrature FM configuration. Fully limited in-phase signal is applied to the multiplier internally. 90° phase shift is accomplished with the L/C tuned circuit connected directly to Pin 8 and capacitively to Pin 9. Because of the DC bias of the NE604, the phase shift network must be returned to ground through a low impedance capacitor. Recovered signal is continuously available at Pin 7 or on a switched basis at Pin 6.

The quadrature coil or crystal/ceramic discriminator affects three system parameters: bandwidth, linearity, and detected signal amplitude. Figure 6 shows three quadrature curves.



EQUATION

$$\frac{V_{OUT}}{V_{IN}} = \frac{j\omega C_1}{\frac{1}{RPL \| RPU}\left(1 + j2Q\frac{\Delta\omega}{\omega_0}\right) + j\omega C_1}$$

$Q = \omega_0 (RPL \| RPU)\, CP$

$\Delta\omega$ = PEAK DEVIATION

ω_0 = CENTER FREQUENCY

TC02390S

Figure 5. General Equations For Quadrature Coil

Table 1. System Parameters as Applied to Figure 4a

$\Delta\omega$	=	$2\pi * 8$kHz
ω_0	=	$2\pi * 455$kHz
CP	=	180pF
RPU	=	233K
RPL	=	40K
LP	=	644μH
Q	≈	20

Curve A has the most narrow bandwidth and high peak-to-peak output versus frequency deviation corresponding to a high Q network. Curve C is very low Q with good linearity and shows how very large deviations can be processed. Curve B shows how the quadrature network can cause non-linearity in the detected output. A loaded Q for the 455kHz quadrature coil of Figure 4 is 20. Using the test circuit of Figure 4 with an input of −47dBm, the recovered audio is typically 90mV$_{RMS}$ with −35dB distortion.

While the NE604 was designed principally for FM applications, the detector can be used for synchronous amplitude demodulation if the carrier is limited through the internal circuitry and AGC'd external to the device. The AGC'd signal is applied to Pin 8 instead of a quadrature signal. The signal strength indicator can control AGC. A low-pass filter on the output completes the demodulator. Figure 7 shows the equivalent circuit.

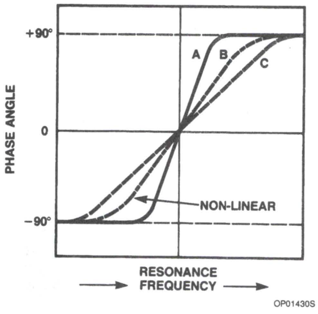


Figure 6. Quadrature

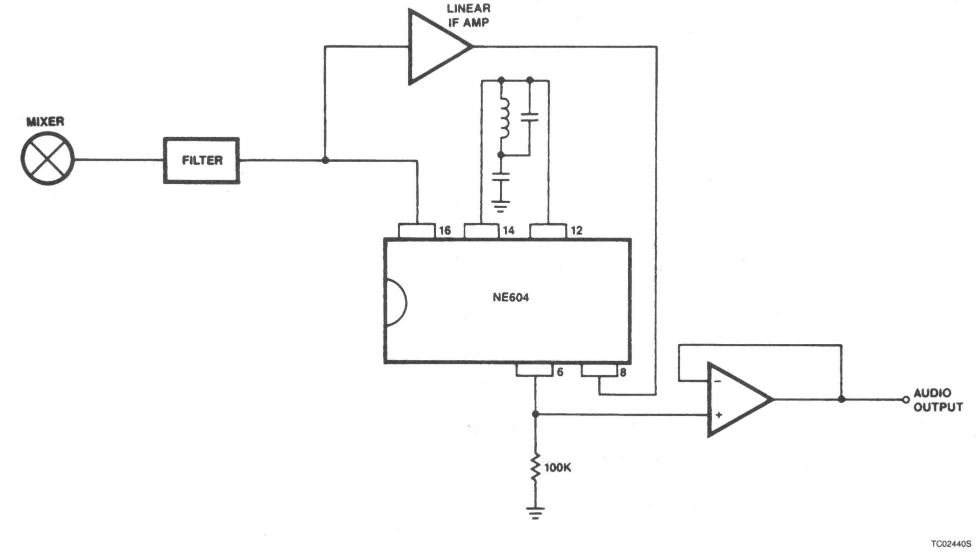

LINEAR
IF AMP
MIXER
FILTER
16
14
12
NE604
6
8
AUDIO
OUTPUT
100K
TC02440S

Figure 7. Synchronous AM Detection

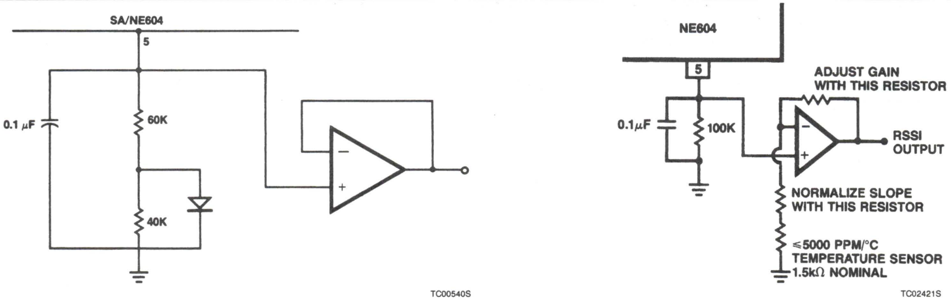
Audio Mute

An electronic switch permits muting or squelch of one of the demodulated outputs. The data (unmuted output) and audio (muted output) both have 50kΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (Pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

Signal Strength Indicator

The logarithmic signal strength indicator is a current source output with maximum source current of 50µA. The signal strength indicator's transfer function is approximately 10µA per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

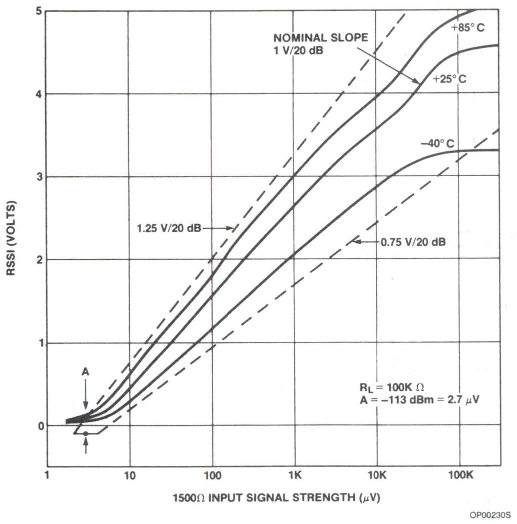
There is some temperature dependence to the signal strength output. Figure 8 shows the characteristic. Two suggested lead circuits are shown to improve linearity in critical applications. For cellular radio applications use of either technique and the SA604 device (−40°C to +85°C) will assure compliance with RSSI criteria.


SA/NE604
5
0.1 µF
60K
40K
TC00540S
NE604
5
ADJUST GAIN
WITH THIS RESISTOR
0.1µF
100K
RSSI
OUTPUT
NORMALIZE SLOPE
WITH THIS RESISTOR
≤5000 PPM/°C
TEMPERATURE SENSOR
1.5kΩ NOMINAL
TC02421S

a. Temperature-Compensated RSSI Circuits

b.

Figure 8. Signal Strength



c. RSSI vs Signal Strength Figure 8 (Continued)

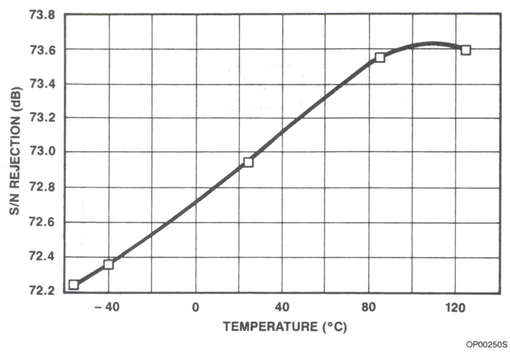


Figure 9. SA/NE604 Signal-To-Noise Ratio vs Temperature

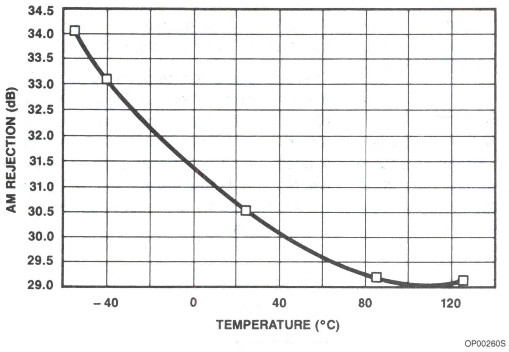


Figure 10. SA/NE604 AM Rejection vs Temperature

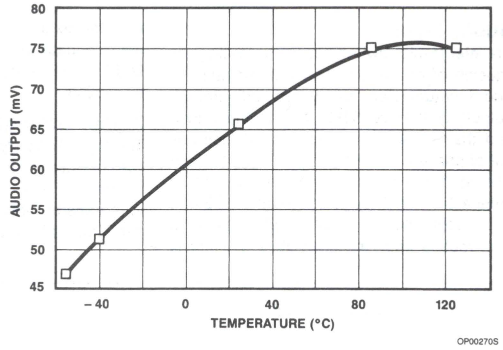


Figure 11. SA/NE604 Audio Output vs Temperature

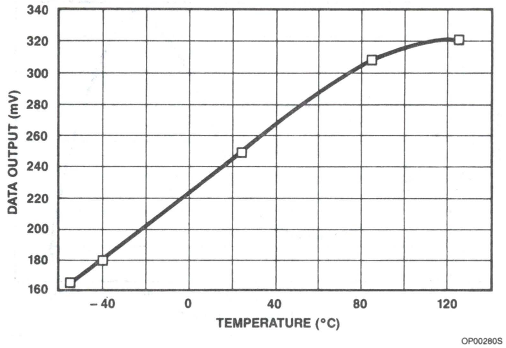


Figure 12. NE/SA604 Data Output vs Temperature

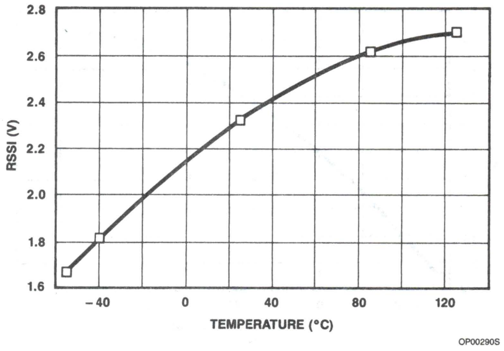


Figure 13. RSSI vs Temperature

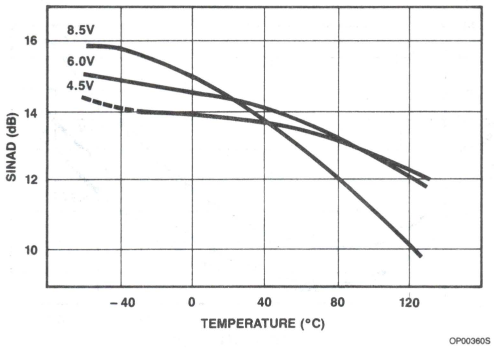


Figure 14. NE/SA604 SINAD vs Temperature and V_{CC}

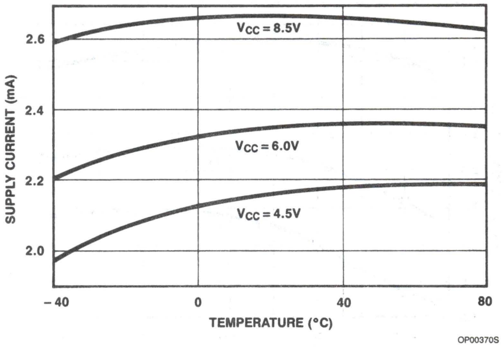


Figure 15. SA604 Supply Current vs Temperature

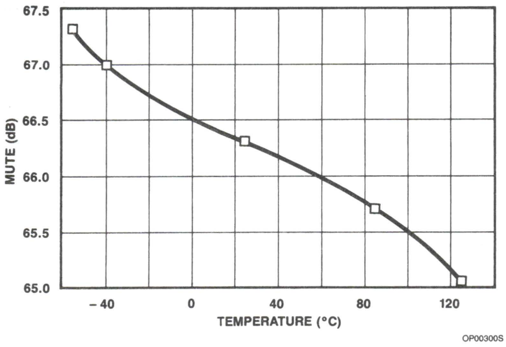


Figure 16. NE/SA604 Muting vs Temperature

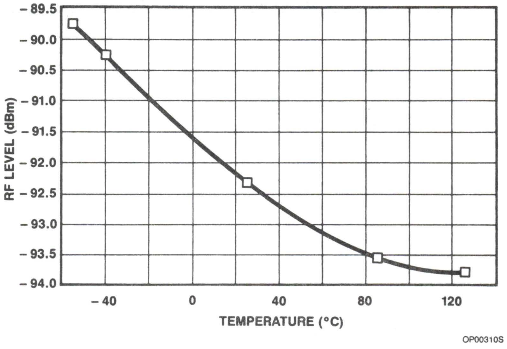


Figure 17. NE/SA604 Limiting RF Level vs Temperature

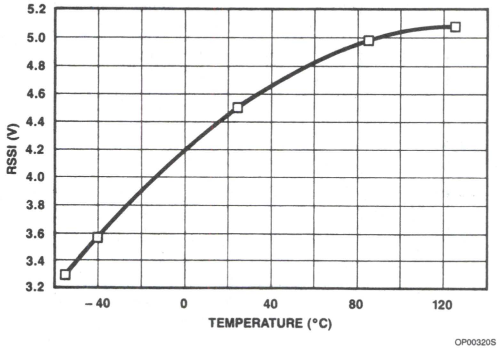


Figure 18. NE/SA604 Large-Signal Uncompensated RSSI Voltage vs Temperature

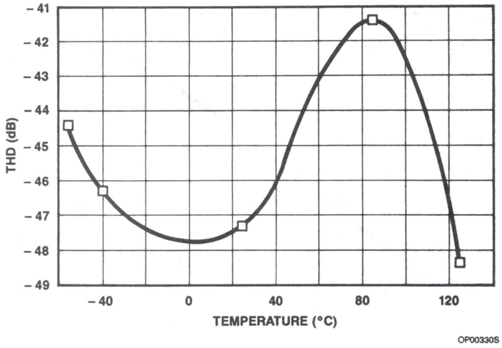


Figure 19. NE/SA604 Total Harmonic Distortion vs Temperature

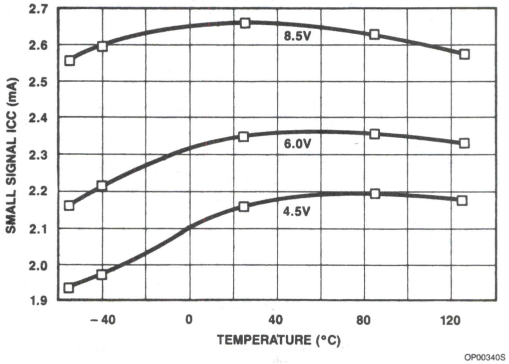


Figure 20. NE/SA604 Supply Current vs Temperature and Voltage

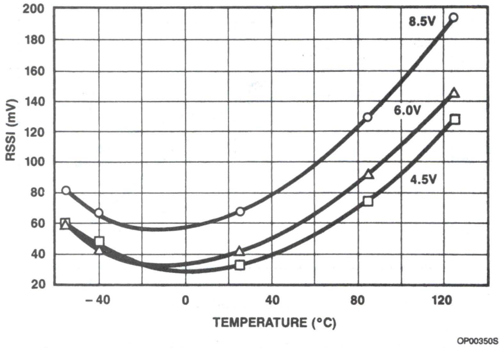


Figure 21. Small-Signal RSSI vs Temperature and Voltage

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Designing With the NE/SA604

Application Note

Linear Products

INTRODUCTION

The SA/NE604 represents a new standard of performance in low power FM IF integrated circuits. Originally designed for cellular radio applications, the 604 is also well suited to other radio frequency circuits where good performance and low power consumption are the important design considerations. When used with its companion double-balanced mixer, the SA/NE602, a low power system solution for the cellular radio and other RF applications is realized (Reference 1).

Figures 1 and 2 show the device pin-out and a functional diagram of the 604. The device provides an IF amplifier, quadrature detector, received signal strength indicator (RSSI), and mute circuit. Two detector outputs are provided for audio and data information with the audio output being controlled by the mute circuit.

CIRCUIT OVERVIEW

The IF amplifier consists of five differential stages with a total gain of about 90dB. Provision is made for an external inter-stage filter to reduce broadband noise and increase receiver selectivity. The differential input to the first IF section appears at Pins 15 and 16. One pin is usually AC-coupled to ground (Pin 15) with Pin 16 used as the "high" input. The first IF section has a typical gain of 40dB with its output appearing on Pin 14. Similar to the first IF section, the second section uses a differential input appearing at Pins 12 and 11, with Pin 11 usually AC-coupled to ground. The five stages are identical and any one may go into limiting, depending on the RF input level.

The interstage filter can be ceramic, crystal, or an LC circuit. RSSI tracking is optimized when the filter circuit loss is 6dB. The output impedance of both amplifier sections (Pins 14 and 9) is about 1kΩ. For convenience, an "L" pad circuit showing 6dB loss is shown in Figure 3. This circuit allows observation of the RSSI response without using a filter.

The quadrature detector multiplies two IF signals to produce the audio output. One of the IF signals is differentially phase shifted by an external quadrature tank or discriminator circuit connected between Pins 8 and 9 (Figure 4). The second IF signal is fed to the other detector input internally. Figure 5 shows the desired phase/frequency response of the quadrature-tuned circuit. A detailed mathematical explanation of detector operation can be found in Reference 2. The detected audio appears at the data terminal (Pin 7) and, via the mute circuit, at the audio (Pin 6) terminal.

The cellular radio specifications call for a logarithmic signal strength indicator accurate within 3dB over an 80dB dynamic range. The 604 meets this requirement with an effective technique. A sample current corresponding to the output of each IF stage is fed to a summing amplifier. The output of this amplifier provides a current source which is reflected by a current mirror. The current mirror output that appears on pin 5 provides the logarithmic RSSI information. It is usable over a 90dB dynamic range with 1.5dB accuracy. Typically, a 100kΩ resistor is used to convert the RSSI current to a voltage which is logarithmically proportional to the received signal strength.

PACKAGING

Both the SA/NE604 and its companion double balanced mixer, the SA/NE602, are available in either the plastic dual-in-line "DIP" or surface mounted "SO" packages. The NE prefix specifies a 0 to+70°C operating temperature range while SA specifies−40 to+85°C operation. The extensive temperature data presented in this application note pertain to both the SA and NE devices.

TYPICAL APPLICATIONS

Figure 6 is a simplified schematic diagram of the 604 which details the internal circuitry adjacent to the device's pins. This should help the designer match impedances to external circuitry. Figure 7 shows the schematic diagram of a typical test circuit using the 604 and 602.

The quadrature tuned circuit (F3) shifts the phase of the IF signal as shown in Figure 5. Low distortion demodulation is obtained if the IF signal deviation is restricted to the linear portion of the S-curve. There are three variables affecting quadrature linearity: circuit Q, deviation, and IF frequency. If the deviation is increased, the Q must be decreased for a given degree of linearity. The circuit Q will also affect the demodulated signal level. A higher Q will yield a higher audio output from the quadrature detector since the phase shift will be greater for a given deviation. The quadrature Q must be optimized for a given frequency deviation, IF frequency, and desired linearity. A loaded Q of about 20 is typical for narrow band FM applications using a 455kHz IF.

The supply voltage for the 602/604 pair can range from 4.5 to 8V. Optimum overall performance is realized at 6.0V for the device pair. Several operation parameters are plotted for supply voltage as well as temperature.

Quadrature detector linearity can be affected by temperature variations. LC circuit resonances will drift as the coil and capacitor values change with temperature. This effect becomes more critical with increased circuit Q. If wide temperature variations are expected, careful choice of circuit components can minimize this effect. Most inductors have positive temperature coefficients (increase of inductance with increase of temperature). If a negative coefficient capacitor is chosen to compensate the inductor, the resonant frequency will track over temperature.

Since a bipolar current source is used to provide the RSSI function, the current will change with temperature. An increase in temperature will result in an increase in RSSI indication (Figure 8, uncorrected response). The circuit shown in Figure 9 will "smooth" the response over temperature by dropping the load impedance presented to Pin 5 as temperature increases (Figure 8, corrected response).

All the major performance parameters of the 604 are shown in Figure 10. Figure 11 illustrates a typical test set-up for measuring many of the discussed parameters. Figures 12 to 25 provide a comprehensive guide to 604 performance over temperature and other variables.

USE AS A FIELD STRENGTH/ RF VOLTMETER

As stated earlier the RSSI function is usable over a 90dB dynamic range. This function taken alone can provide a useful RF voltmeter function. The circuit in Figure 26 can be used as a field strength or RF voltmeter application. A linear readout device can be calibrated directly in decibels or logarithmically for power, current, or volts.

USE AS AN AM SYNCHRONOUS DETECTOR

The 604 can also be used as an AM envelope detector. The IF signal is fed to both the 604, as in the FM application, and to an additional

Designing With the NE/SA604

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linear IF amplifier (Figure 27). The linear amplifier then feeds the quadrature detector which mixes with the AM limited carrier and demodulates the envelope. 1% THD is obtainable with this technique with a 90% AM modulated signal.

USE AS A PRODUCT DETECTOR

Figure 28 shows how the 604 can be used as a product detector for SSB or DSB. In this case the LO is applied to the 604 IF amplifier and an external linear IF amplifier is used for the SSB or DSB signal. The 604 quadrature detector then acts as the product detector. With the addition of a simple switching array, a single 604 can be used for FM, AM, or SSB detection in a communications receiver!

REFERENCES

1. Zavrel, R.: Signetics AN198 *Designing With the SA/NE 602*, December, 1984.

2. Hayward, W.: *Introduction to Radio Frequency Design*, 1982, Prentice-Hall.

Written by Bob Zavrel

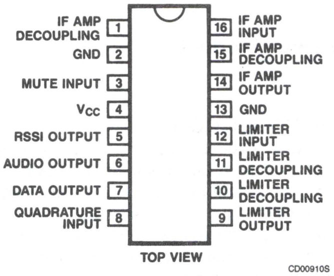

IF AMP DECOUPLING 1
GND 2
MUTE INPUT 3
V_{CC} 4
RSSI OUTPUT 5
AUDIO OUTPUT 6
DATA OUTPUT 7
QUADRATURE INPUT 8
16 IF AMP INPUT
15 IF AMP DECOUPLING
14 IF AMP OUTPUT
13 GND
12 LIMITER INPUT
11 LIMITER DECOUPLING
10 LIMITER DECOUPLING
9 LIMITER OUTPUT
TOP VIEW
CD00910S

Figure 1. Pin Configuration

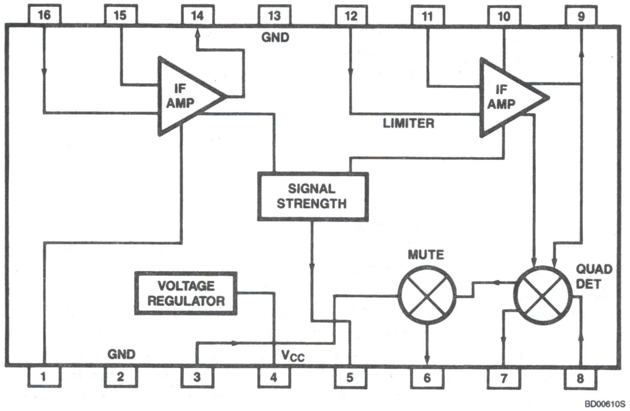
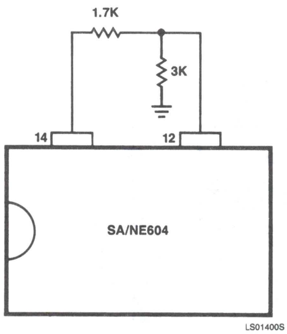
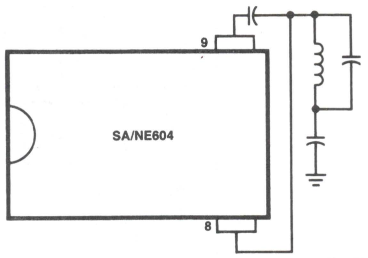

16
15
14
13
12
11
10
9
GND
IF AMP
LIMITER
IF AMP
SIGNAL STRENGTH
MUTE
QUAD DET
VOLTAGE REGULATOR
GND
V_{CC}
1
2
3
4
5
6
7
8
BD00610S

Figure 2. Block Diagram


1.7K
3K
14
12
SA/NE604

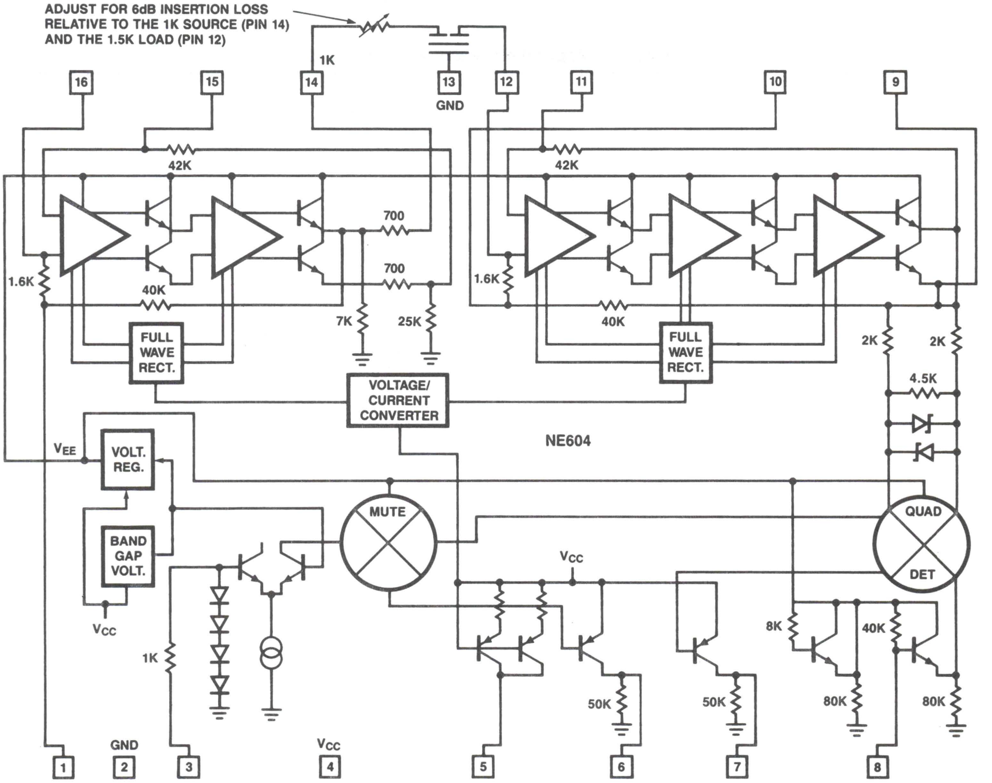
LS01400S

Figure 3. 6dB "L" Pad



LS01410S

Figure 4. Quadrature Network


ADJUST FOR 6dB INSERTION LOSS RELATIVE TO THE 1K SOURCE (PIN 14) AND THE 1.5K LOAD (PIN 12)

1K
16
15
14
13
GND
12
11
10
9
42K
42K
700
700
1.6K
40K
1.6K
40K
7K
25K
FULL WAVE RECT.
FULL WAVE RECT.
2K
2K
4.5K
VOLTAGE/ CURRENT CONVERTER
NE604
VEE
VOLT. REG.
BAND GAP VOLT.
VCC
MUTE
QUAD DET
VCC
1K
8K
40K
50K
50K
80K
80K
GND
VCC
1
2
3
4
5
6
7
8

TC00530S

Figure 5

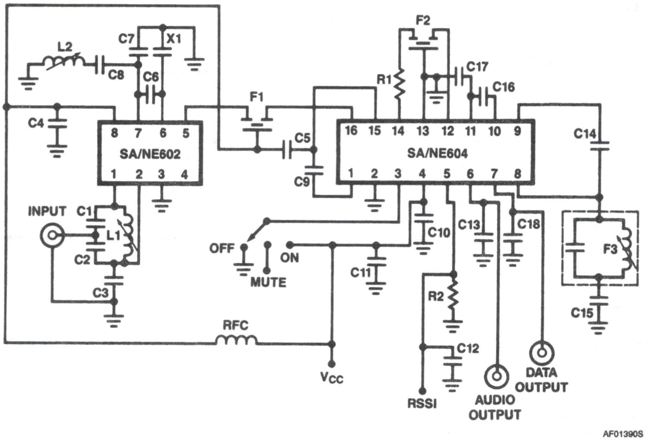

L2
C7
X1
C8
C6
F2
R1
C17
C16
F1
C4
8 7 6 5
SA/NE602
1 2 3 4
C5
16 15 14 13 12 11 10 9
SA/NE604
1 2 3 4 5 6 7 8
C9
C14
INPUT
C1
L1
C2
C3
OFF
ON
MUTE
C10
C13
C18
F3
C11
R2
C15
RFC
C12
VCC
RSSI
AUDIO OUTPUT
DATA OUTPUT
AF01390S

Figure 6. Application Demonstration Board

Designing With the NE/SA604

C1	47 pF ± 2%	100 V	N750 Ceramic
C2	220 pF ± 2%	100 V	N750 Ceramic
C3	0.1 µF ± 10%	50 V	Polyester
C4	10 nF ± 80% 20%	63 V	K10000 — 25X Ceramic
C5	0.1 µF ± 10%	50 V	Polyester
C6	5.6 pF ± 25%	100 V	NPO Ceramic
C7	22 pF ± 2%	100 V	N150 Ceramic
C8	1 nF ± 10%	100 V	K2000 — Y5P Ceramic
C9	0.1 µF ± 10%	50 V	Polyester
C10	0.1 µF ± 10%	50 V	Polyester
C11	6.8 µF ± 20%	25 V	Tantalum
C12	1 nF ± 10%	100 V	K2000 — Y5P Ceramic
C13	15 nF ± 10%	50 V	Polyester
C14	10 pF ± 2%	100 V	NPO Ceramic
C15	0.1 µF ± 10%	50 V	Polyester
C16	0.1 µF ± 10%	50 V	Polyester
C17	0.1 µF ± 10%	50 V	Polyester
C18	150 pF ± 2%	100 V	N1500 Ceramic
R1	1.5 K ± 5%	1/8 W	Carbon Composition
R2	100 K ± 1%	1/4 W	Metal Film
RFC	5.5 µH	RF Chocke J.W. Miller 542 — 4609	
L1	0.209 — 0.283 µH	Adjustable VHF Coil Miller 48A257MPC	
L2	0.5 — 1.3 µH	Adjustable Coil 1811 — 0036TW	
F1	455 kHz	Ceramic Filter Murata SFG 455A3	
F2			
F3	455 kHz	IF Filter Toko A2549	
X1	44.545 MHz	Third Overtone Crystal	

TB00440S

Figure 7. Application Test Board Parts

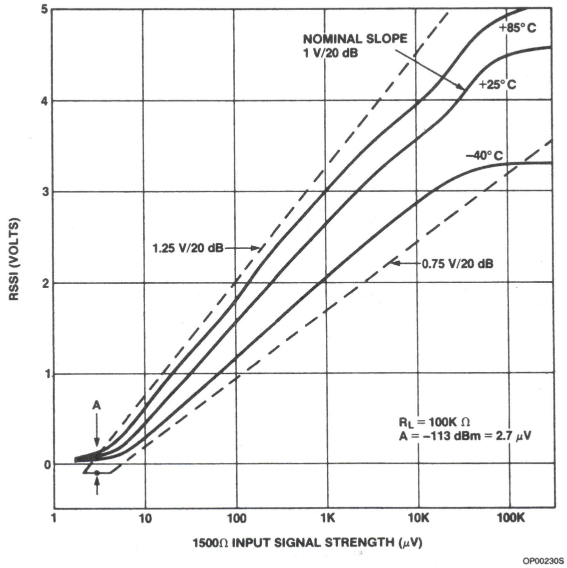


Figure 8. RSSI vs Signal Strength

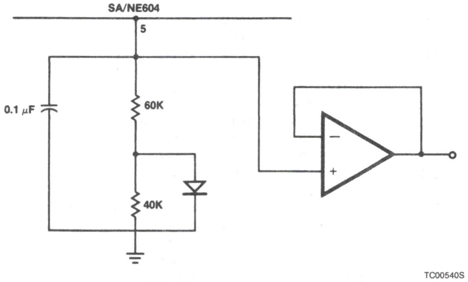

SA/NE604
5
0.1 μF
60K
40K
−
+
TC00540S

Figure 9. Temperature-Compensated RSSI Circuit

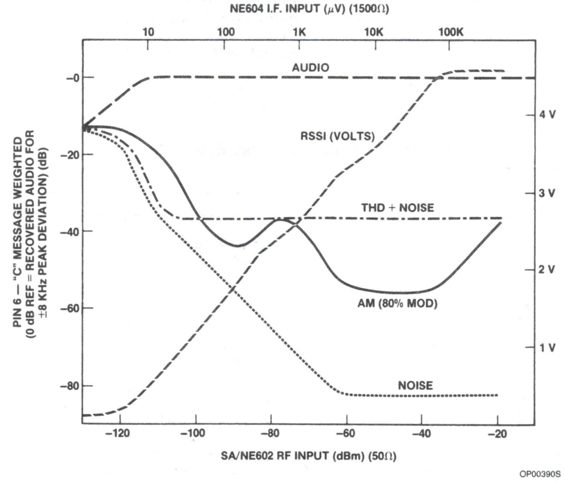


Figure 10. NE602/604 System Performance

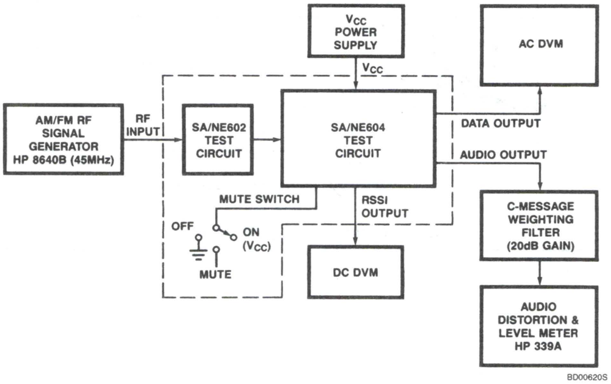

V_CC POWER SUPPLY
V_CC
AC DVM
AM/FM RF SIGNAL GENERATOR HP 8640B (45MHz)
RF INPUT
SA/NE602 TEST CIRCUIT
SA/NE604 TEST CIRCUIT
DATA OUTPUT
AUDIO OUTPUT
MUTE SWITCH
RSSI OUTPUT
OFF
ON (V_CC)
MUTE
DC DVM
C-MESSAGE WEIGHTING FILTER (20dB GAIN)
AUDIO DISTORTION & LEVEL METER HP 339A
BD00620S

Figure 11. NE/SA602/NE/SA604 Applications Board

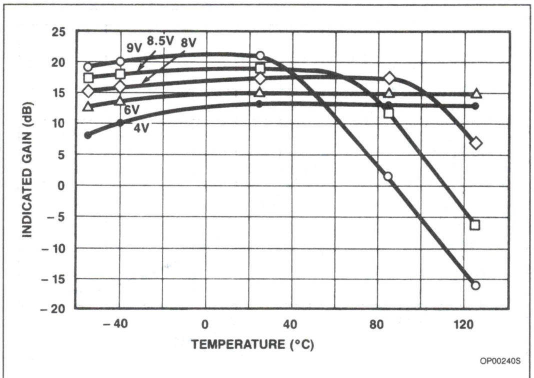


Figure 12. NE/SA604 Indicated Gain vs Temperature and Voltage

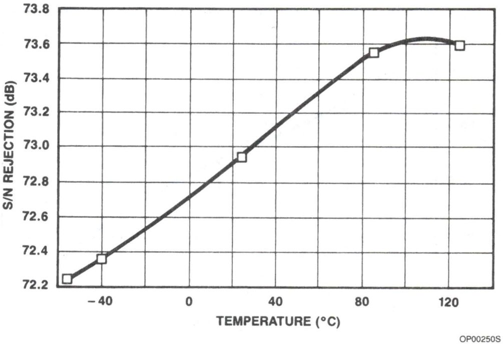


Figure 13. NE/SA604 Signal-To-Noise Ratio vs Temperature

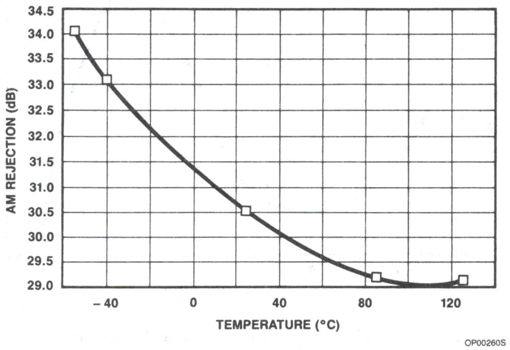


Figure 14. NE/SA604 AM Rejection vs Temperature

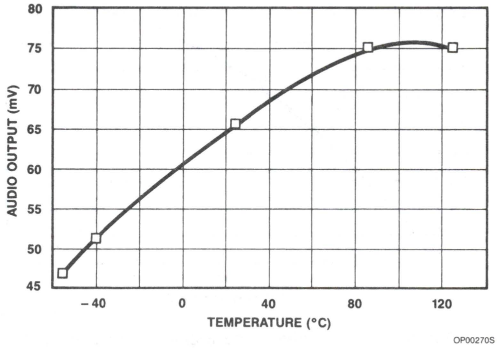


Figure 15. NE/SA604 Audio Output vs Temperature

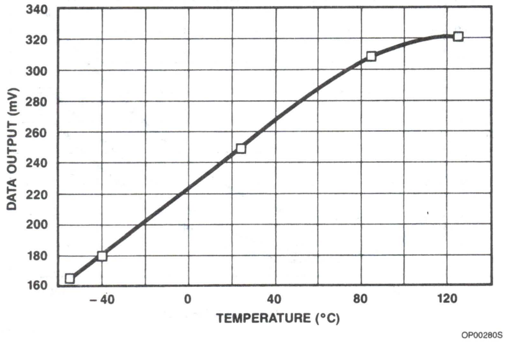


Figure 16. NE/SA604 Data Output vs Temperature

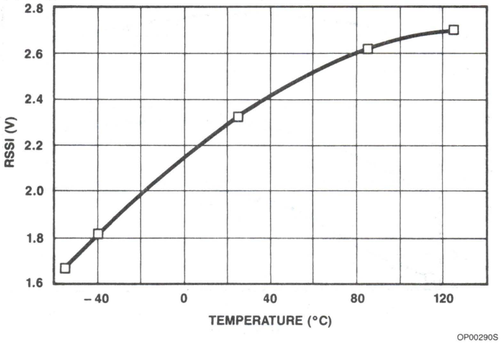


Figure 17. RSSI vs Temperature

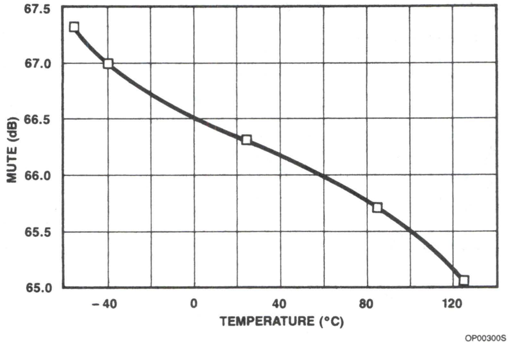


Figure 18. NE/SA604 Muting vs Temperature

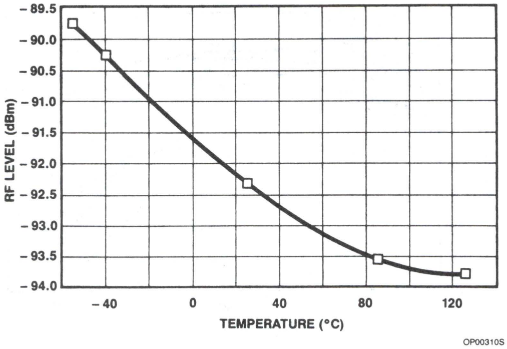


Figure 19. NE/SA604 Limiting RF Level vs Temperature

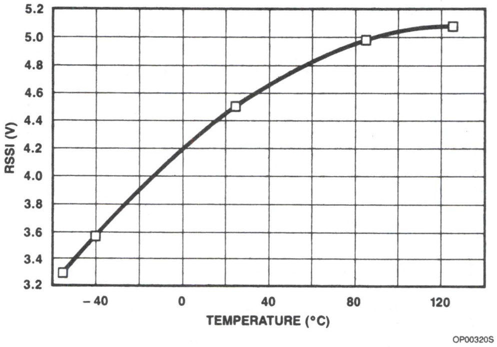


Figure 20. NE/SA604 Large Signal Uncompensated RSSI Voltage vs Temperature

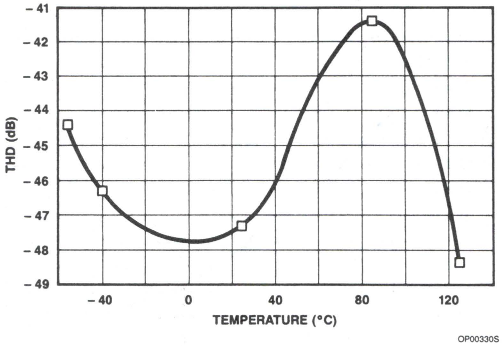


Figure 21. NE/SA604 Total Harmonic Distortion vs Temperature

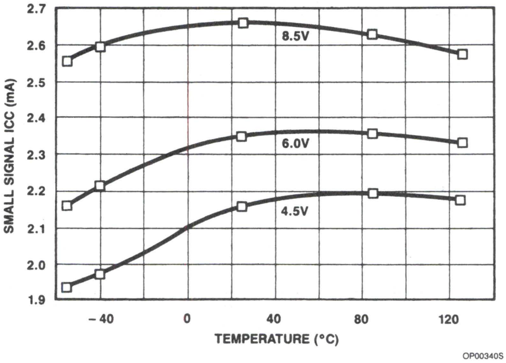


Figure 22. NE/SA604 Supply Current vs Temperature and Voltage

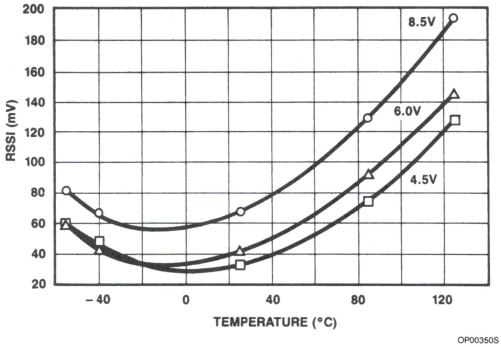


Figure 23. Small-Signal RSSI vs Temperature and Voltage

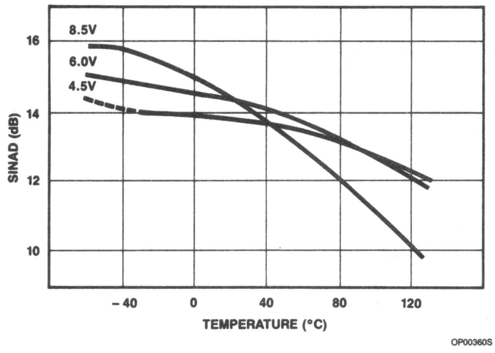


Figure 24. NE/SA604 SINAD vs Temperature and V_{CC}

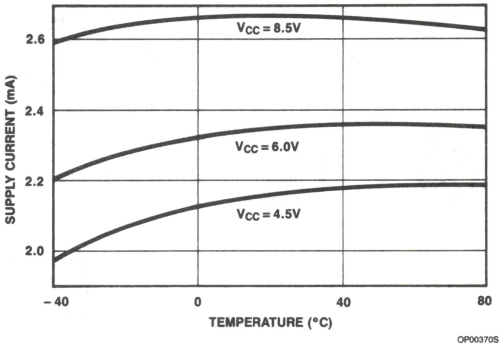


Figure 25. SA604 Supply Current vs Temperature

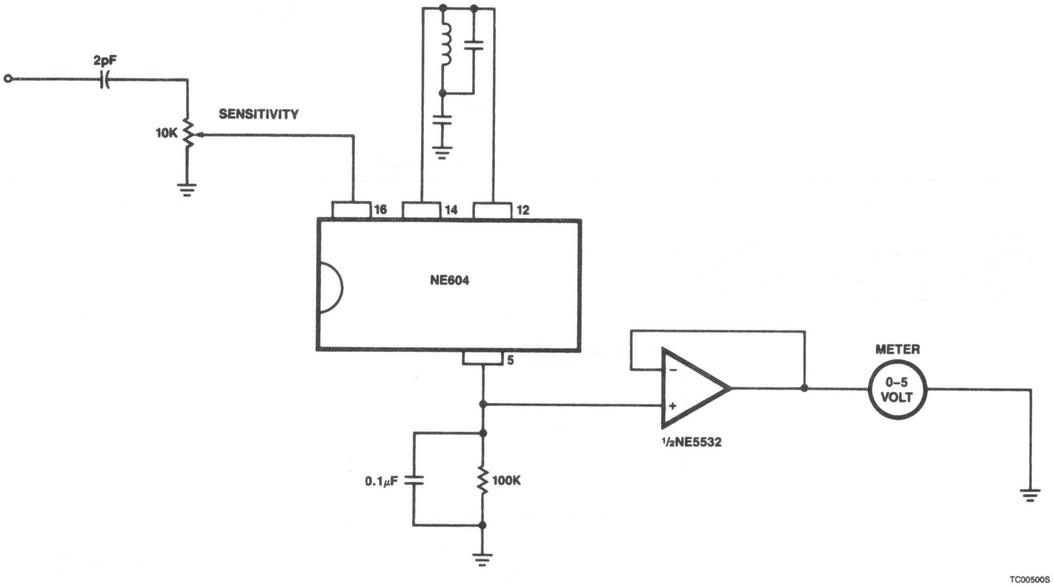

2pF
SENSITIVITY
10K
16
14
12
NE604
5
0.1μF
100K
½NE5532
METER
0–5
VOLT
TC00500S

Figure 26. Field Strength Meter

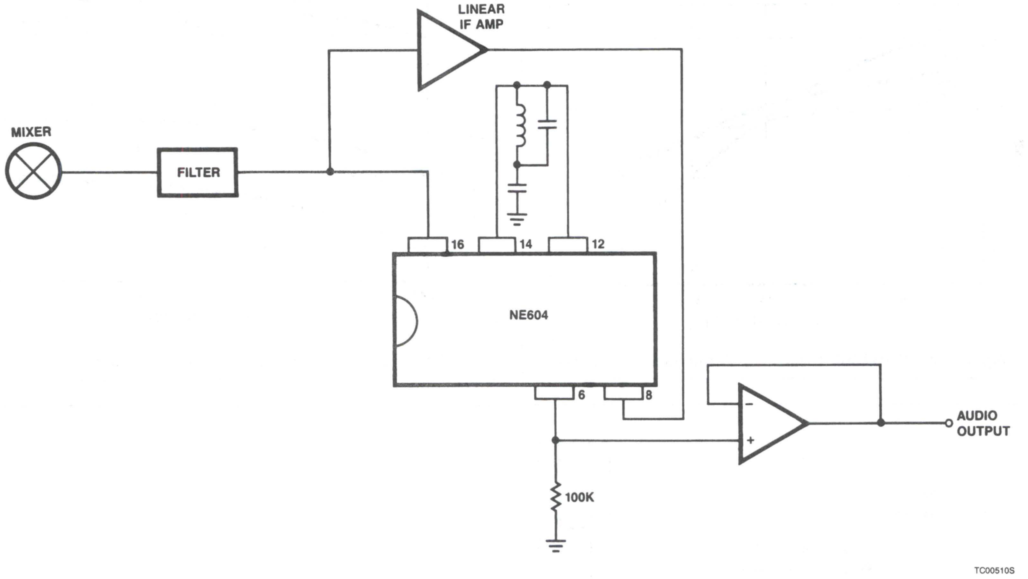

LINEAR
IF AMP
MIXER
FILTER
16
14
12
NE604
6
8
−
+
AUDIO
OUTPUT
100K
TC00510S

Figure 27. AM Synchronous Detector

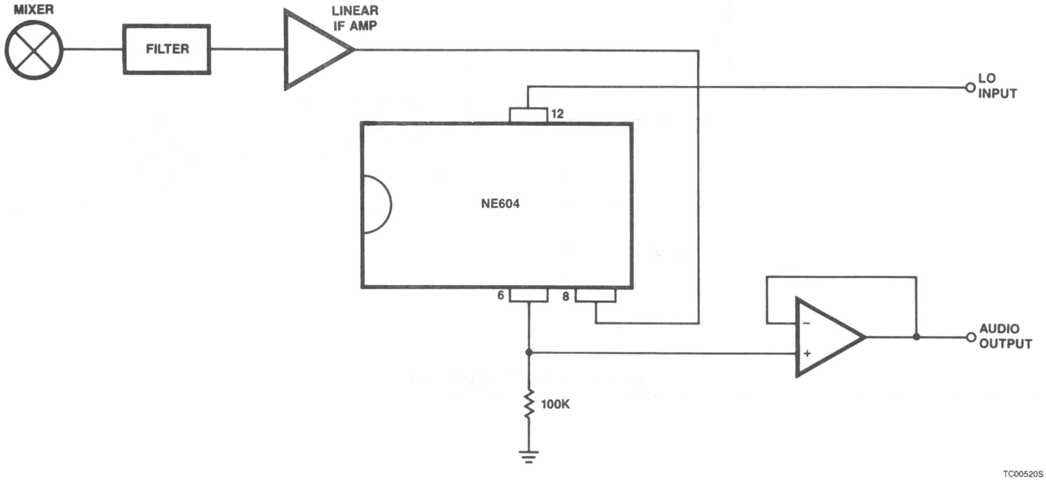

MIXER
FILTER
LINEAR
IF AMP
LO
INPUT
12
NE604
6
8
−
+
AUDIO
OUTPUT
100K
TC00520S

Figure 28. Product Detector

Signetics

AN1991
Audio Decibel Level Detector With Meter Driver

Application Note

Linear Products

Author: Robert J. Zavrel Jr.

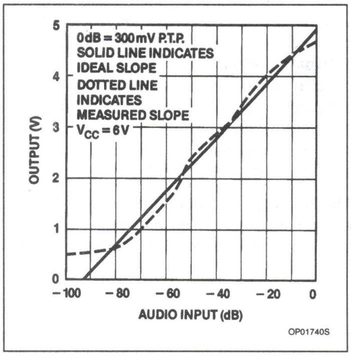
DESCRIPTION

Although the NE604 was designed as an RF device intended for the cellular radio market, it has features which permit other design configurations. One of these features is the Received Signal Strength Indicator (RSSI). In a cellular radio, this function is necessary for continuous monitoring of the received signal strength by the radio's microcomputer. This circuit provides a logarithmic response proportional to the input signal level. The NE604 can provide this logarithmic response over an 80dB range up to a 15MHz operating frequency. This paper describes a technique which optimizes this useful function within the audio band.

A sensitive audio level indicator circuit can be constructed using two integrated circuits: the NE604 and NE532. This circuit draws very little power (less than 5mA with a single 6V power supply) making it ideal for portable battery operated equipment. The small size and low-power consumption belie the 80dB dynamic range and 10.5μV sensitivity.

The RSSI function requires a DC output voltage which is proportional to the $\log_{10}$ of the input signal level. Thus a standard 0 – 5 voltmeter can be linearly calibrated in decibels over a single 80dB range. The entire circuit is composed of 9 capacitors and two resistors along with the two ICs. No tuning or calibration is required in a manufacturing setting.

The Audio Input vs Output Graph shows that the circuit is within 1.5dB tolerance over the 80dB range for audio frequencies from 100Hz to 10kHz. Higher audio levels can be measured by placing an attenuator ahead of the input capacitor. The input impedance is high (about 50k), so lower impedance terminations (50 or 600Ω) will not be affected by the input impedance. If very accurate tracking is required (< 0.5dB accuracy), a 40 or 50dB segment can be "selected". A range switch can then be added with appropriate attenuators if more than 40 or 50dB dynamic range is required.



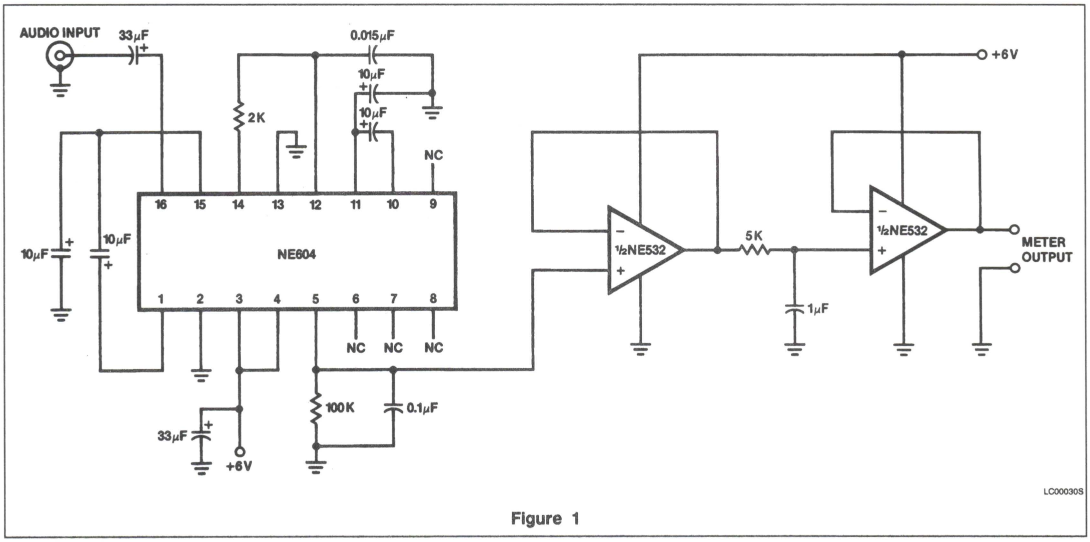


Figure 1

Audio Decibel Level Detector With Meter Driver

AN1991

There are two amplifier sections in the 604 with 2 and 3 stages in the first and second sections respectively. Each stage outputs a sample current to a summing circuit. The summing circuit has a current mirror which appears at Pin 5. This current is thus proportional to the $\log_{10}$ of the input audio signal. A voltage is dropped across the 100k resistor by the current, and a 0.1μF capacitor is used to bypass and filter the output signal. The 532 op amp is used as a buffer and meter driver, although a digital voltmeter could replace both the op amp and the meter shown. The rest of the capacitors are used for power supply and amplifier input bypassing.

The RC circuit between Pins 14 and 12 forms a low-pass filter which can be adjusted by changing the value of C1. Raising the capacitance will lower the cut-off frequency and also lower the zero signal output resting voltage (about 0.6V). Lowering the capacitance value will have the opposite effect with some reduction in dynamic range, but will raise the frequency response. The 2kΩ resistor value provides the near-ideal inter-stage loss for maximum RSSI linearity. C2 can also be changed. The trade-off here is between output damping and ripple. Most analog and digital metering methods will tend to cancel the effects of small or moderate ripple voltages through integration, but high ripple voltages should be avoided.

A second op amp is used with an optional second filter. This filter has the advantage of a low impedance signal source by virtue of the first op amp. Again, a trade-off exists between meter damping and ripple attenuation. If very low ripple and low damping are both required, a more complex active low-pass filter should be constructed.

Some applications of this circuit might include:

1. Portable acoustic analyzer
2. Microphone tester
3. Audio spectrum analyzer
4. VU meters
5. S-meter for direct conversion radio receiver
6. Audio dynamic range testers
7. Audio analyzers (THD, noise, separation, response, etc.)

NE614
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The NE614 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE614 is available in a 16-lead dual in-line plastic package and 16-lead SO (surface-mounted miniature package).

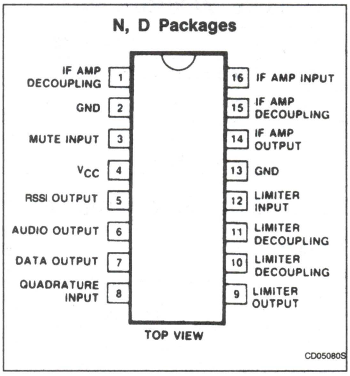
FEATURES

- **Low power consumption**
- **Logarithmic signal strength indicator**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity**

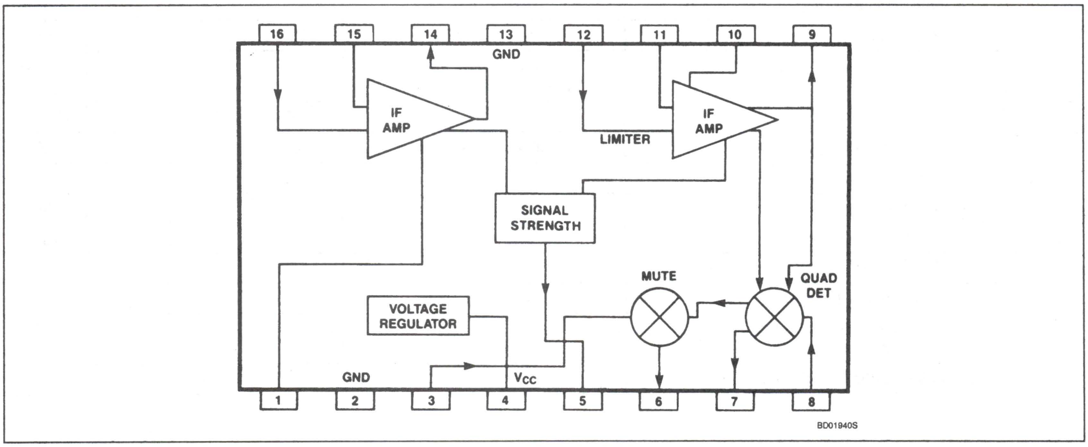
APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Cordless telephone**
- **Remote control**

PIN CONFIGURATION


N, D Packages
IF AMP DECOUPLING 1
GND 2
MUTE INPUT 3
VCC 4
RSSI OUTPUT 5
AUDIO OUTPUT 6
DATA OUTPUT 7
QUADRATURE INPUT 8
16 IF AMP INPUT
15 IF AMP DECOUPLING
14 IF AMP OUTPUT
13 GND
12 LIMITER INPUT
11 LIMITER DECOUPLING
10 LIMITER DECOUPLING
9 LIMITER OUTPUT
TOP VIEW
CD05080S

BLOCK DIAGRAM


16
15
14
13
12
11
10
9
GND
IF AMP
LIMITER
IF AMP
SIGNAL STRENGTH
MUTE
QUAD DET
VOLTAGE REGULATOR
GND
VCC
1
2
3
4
5
6
7
8
BD01940S

Low Power FM IF System NE614

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE614N
16-Pin Plastic SO	0 to +70°C	NE614D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE614	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain				3.0	mA
	Mute switch input threshold					
	(on)		1.7			V
	(off)				1.0	V

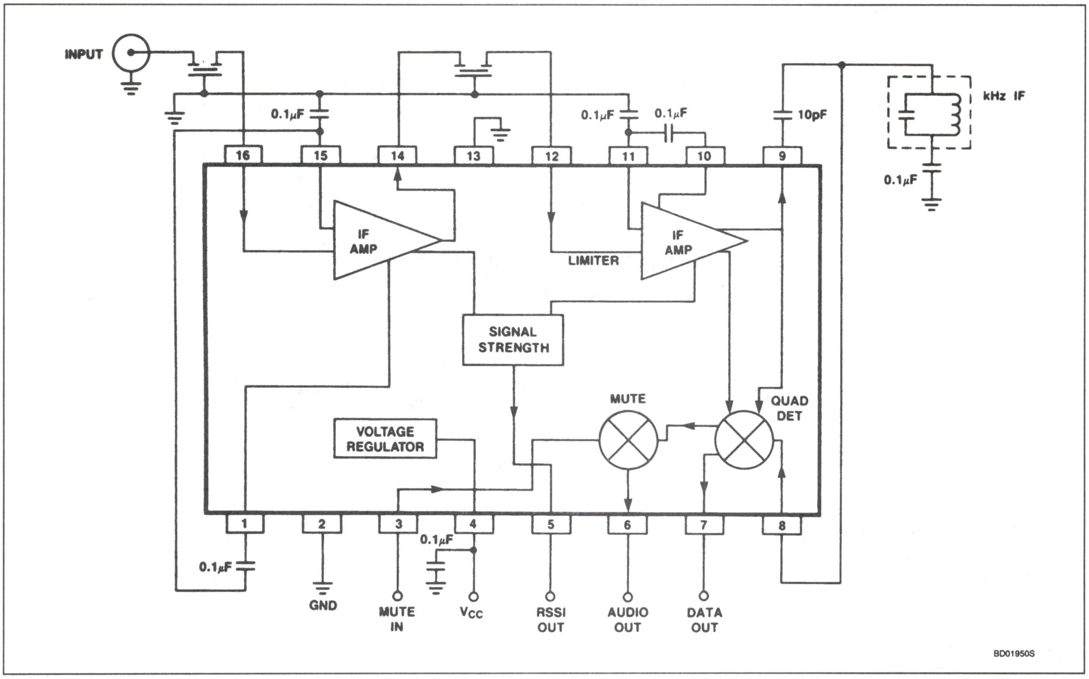
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 455kHz; RF level = -47dBm; FM modulation = 1kHz with +8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

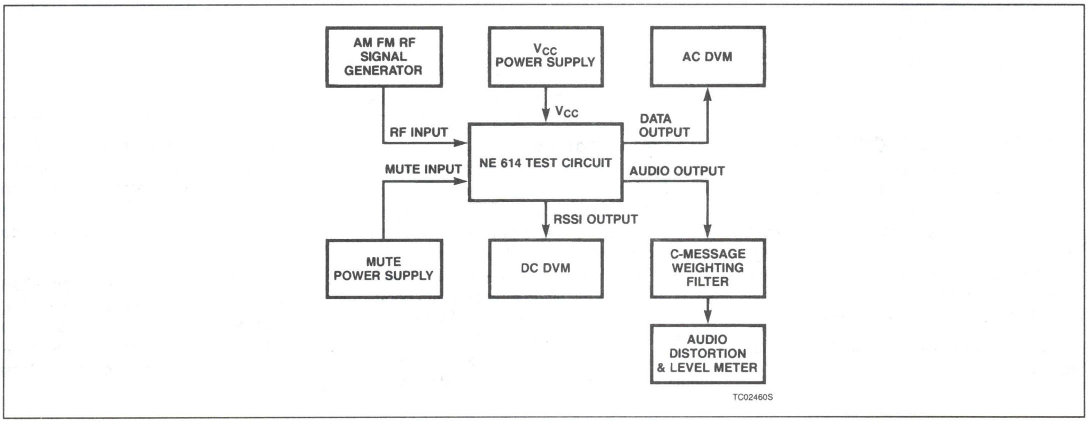
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input limiting - 3dB	Test at pin 16		-90	-80	dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level - 97dBm	8	12		dB
THD	Total harmonic distortion		-35			dB
S/N	Signal-to-noise ratio	No modulation		75		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance		50			kΩ
	Muted audio output impedance			50		kΩ

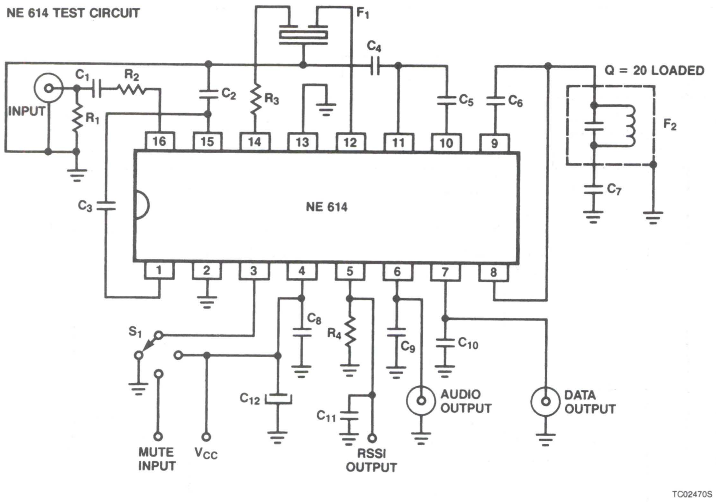
Low Power FM IF System NE614

TYPICAL APPLICATION


INPUT
0.1µF
0.1µF
0.1µF
10pF
kHz IF
0.1µF
16
15
14
13
12
11
10
9
IF AMP
LIMITER
IF AMP
SIGNAL STRENGTH
MUTE
QUAD DET
VOLTAGE REGULATOR
1
2
3
4
5
6
7
8
0.1µF
0.1µF
GND
MUTE IN
V$_{CC}$
RSSI OUT
AUDIO OUT
DATA OUT
BD01950S

TEST SETUP


AM FM RF SIGNAL GENERATOR
V$_{CC}$ POWER SUPPLY
AC DVM
V$_{CC}$
RF INPUT
DATA OUTPUT
NE 614 TEST CIRCUIT
MUTE INPUT
AUDIO OUTPUT
RSSI OUTPUT
MUTE POWER SUPPLY
DC DVM
C-MESSAGE WEIGHTING FILTER
AUDIO DISTORTION & LEVEL METER
TC02460S



NOTES:
C1 10nF +80−20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V Polyester
C3 100nF ± 10% 50V Polyester
C4 100nF ± 10% 50V Polyester
C5 100nF ± 10% 50V Polyester
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V Polyester
C8 100nF ± 10% 50V Polyester
C9 15nF ± 10% 50V Polyester
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8μF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film

Figure 1. NE614 Test Circuit and Parts List

DESCRIPTION OF OPERATION

The NE614 is comprised of five subsystems for IF signal processing. These subsystems, two IF limiting amplifiers, quadrature detector, audio mute, and logarithmic signal strength, can be configured to satisfy many high-performance or low power systems objectives. Internal temperature compensated bias regulation completes the circuitry.

Figure 2 shows the equivalent circuits of the NE614.

Limiting Amplifiers

The NE614 has two independent limiting IF amplifiers. The first has a typical gain of 30dB. The second typically has 60dB gain. Both have 1.5k nominal input impedance and 15MHz bandwidth. The output impedance of the first limiter is approximately 1kΩ. These impedances permit direct interface with popular ceramic filters such as the SFU455. On the surface, the 1k output of the first limiter would not seem correct. However, approximately 6dB insertion loss is required between limiter stages to optimize the linearity of the signal strength indicator. The impedance mismatch has little effect on passband. Use of an interstage filter reduces wide-band noise. A DC blocking capacitor or L/C filter can also be used.

As the signal frequency increases, the 90dB total gain can become a source of instability. Figure 3 shows the limiters as a closed-loop system with stray capacitance and the equivalent AC input impedance setting the loop gain.

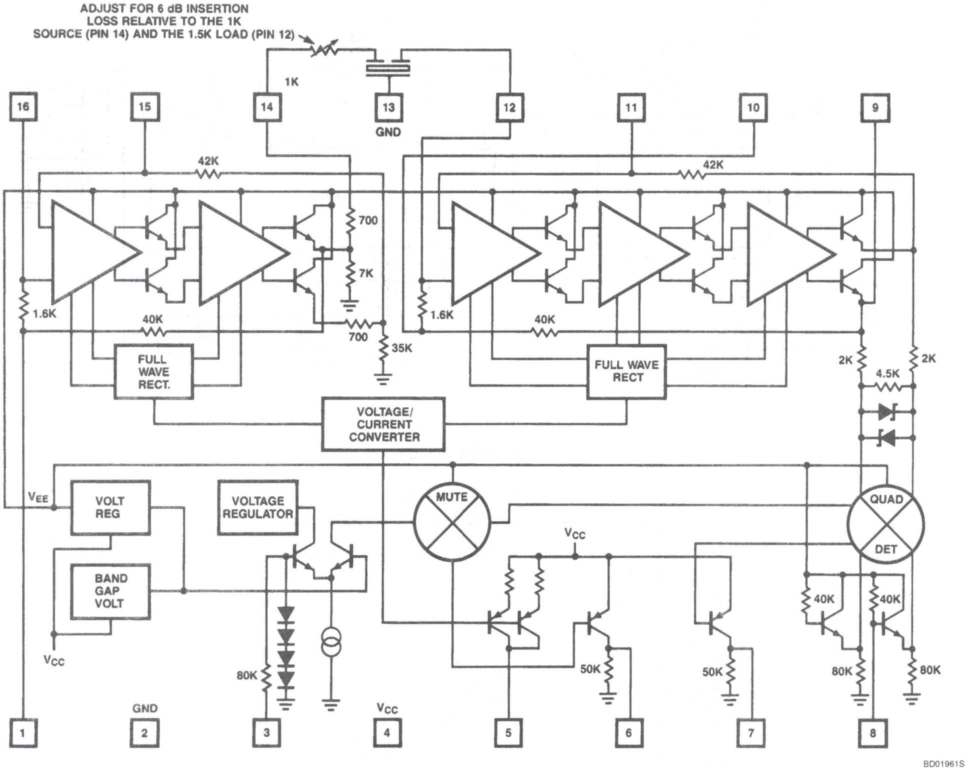

ADJUST FOR 6 dB INSERTION LOSS RELATIVE TO THE 1K SOURCE (PIN 14) AND THE 1.5K LOAD (PIN 12)
1K
16
15
14
13
GND
12
11
10
9
42K
42K
700
7K
1.6K
40K
700
35K
1.6K
40K
FULL WAVE RECT.
FULL WAVE RECT
2K
2K
4.5K
VOLTAGE/ CURRENT CONVERTER
V_{EE}
VOLT REG
VOLTAGE REGULATOR
MUTE
QUAD DET
V_{CC}
BAND GAP VOLT
V_{CC}
80K
40K
40K
50K
50K
80K
80K
GND
V_{CC}
1
2
3
4
5
6
7
8
BD01961S

Figure 2. Equivalent Circuit

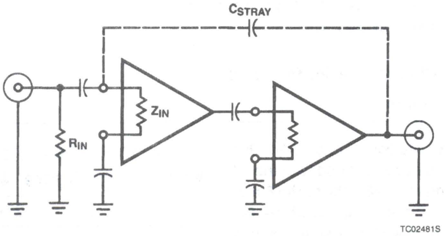
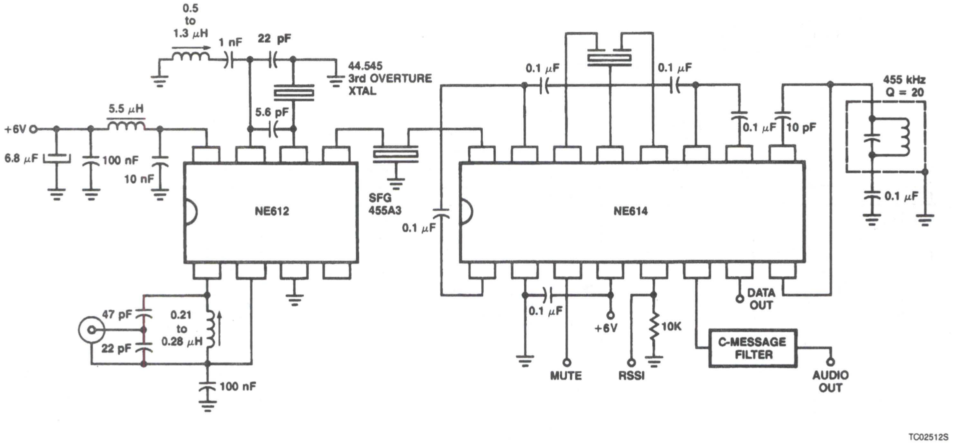

C_{STRAY}
Z_{IN}
R_{IN}
TC02481S

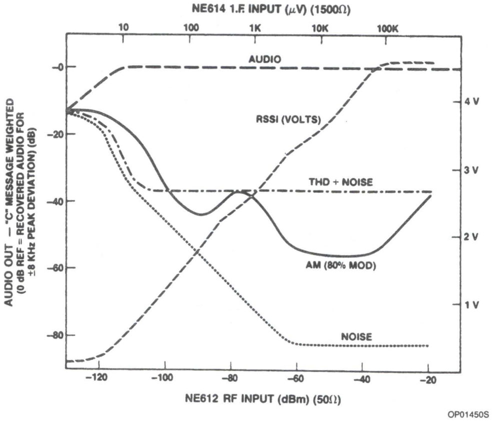
Figure 3. Considerations for Stability

The equivalent AC attenuation factor from the output to the input must be greater than 90dB or oscillation can occur. The input impedance of the device is nominally 1.5k. The stray layout capacitance is a frequency-dependent impedance so that as the frequency of operation or the value of stray capacitance increases, the output-to-input attenuation factor decreases. Keep stray capacitance low by using good RF layout technique. Sockets should be avoided above 455kHz.

Good RF layout is the proper way to avoid instability. However, if system constraints require, stability can be achieved by only using one of the limiting amplifiers, or by adding a resistance, R_{IN}, which will increase the attenuation factor.


0.5
to
1.3 μH
1 nF
22 pF
44.545
3rd OVERTURE
XTAL
5.6 pF
5.5 μH
+6V
6.8 μF
100 nF
10 nF
NE612
SFG
455A3
0.1 μF
0.1 μF
0.1 μF
455 kHz
Q = 20
0.1 μF
10 pF
0.1 μF
NE614
47 pF
0.21
to
0.28 μH
22 pF
100 nF
0.1 μF
+6V
10K
DATA
OUT
C-MESSAGE
FILTER
MUTE
RSSI
AUDIO
OUT
TC02512S

a. NE614 Application Circuit



b. Typical Application Circuit Performance

Figure 4

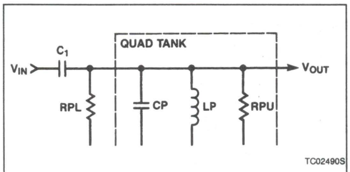
Adding an input resistor is an easy way to reduce the attenuation factor, but may make correct termination of interstage filters difficult or impossible. At 455kHz instability should not be a problem if reasonable RF layout is used. Figure 4a indicates a 455kHz circuit configuration which should serve as a reasonable starting point for many applications. This circuit is configured for 46/49MHz cordless telephone.

Quadrature Detector

The detector of the NE614 is a four quadrant multiplier of the Gilbert cell type. It can be used for frequency or amplitude demodulation. Figure 4b indicates a typical quadrature FM configuration. Fully limited in-phase signal is applied to the multiplier internally. 90° phase phase shift is accomplished with the L/C tuned circuit connected directly to Pin 8 and capacitively to Pin 9. Because of the DC bias of the NE614, the phase shift network must be returned to ground through a low impedance capacitor. Recovered signal is continuously available at Pin 7 or on a switched basis at Pin 6.

Table 1. System Parameters as Applied to Figure 4a

$\Delta\omega$	=	$2\pi*8$kHz
ω_0	=	$2\pi*455$kHz
CP	=	180pF
RPU	=	233K
RPL	=	40K
LP	=	644μH
Q	≈	20



EQUATION

$$\frac{V_{OUT}}{V_{IN}} = \frac{j\omega C_1}{\frac{1}{RPL\,|\,|\,RPU}\left(1 + j2Q\frac{\Delta\omega}{\omega_0}\right) + j\omega C_1}$$

$Q = \omega_0\,(RPL\,|\,|\,RPU)\,CP$

$\Delta\omega$ = PEAK DEVIATION

ω_0 = CENTER FREQUENCY

TC02500S

Figure 5. General Equations For Quadrature Coil

The quadrature coil or crystal/ceramic discriminator affects three system parameters: Bandwidth, linearity, and detected signal amplitude. Figure 6 shows three quadrature curves.

Curve A has the most narrow bandwidth and high peak-to-peak output versus frequency deviation corresponding to a high Q network. Curve C is very low Q with good linearity and shows how very large deviations can be processed. Curve B shows how the quadrature network can cause non-linearity in the detected output. A typical loaded Q for the 455kHz quadrature coil of Figure 4 is 20. Using the test circuit of Figure 4 with an input of −47dBm, the recovered audio is typically 90mV$_{RMS}$ with −35dB distortion.

While the NE614 was designed principally for FM applications, the detector can be used for synchronous amplitude demodulation if the carrier is limited through the internal circuitry and AGC'd external to the device. The AGC'd signal is applied to Pin 8 instead of a quadrature signal. The signal strength indicator can control AGC. A low-pass filter on the output completes the demodulator. Figure 7 shows the equivalent circuit.

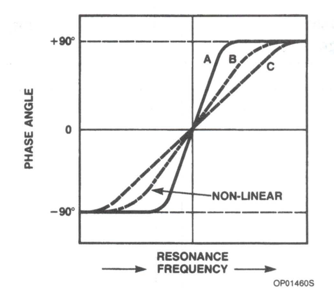


Figure 6. Quadrature

Audio Mute

An electronic switch permits muting or squelch of one of the demodulated outputs. The data (unmuted output) and audio (muted output) both have 50kΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (Pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

Signal Strength Indicator

The logarithmic signal strength indicator is a current source output with maximum source current of 50μA. The signal strength indicator's transfer function is approximately 10μA per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

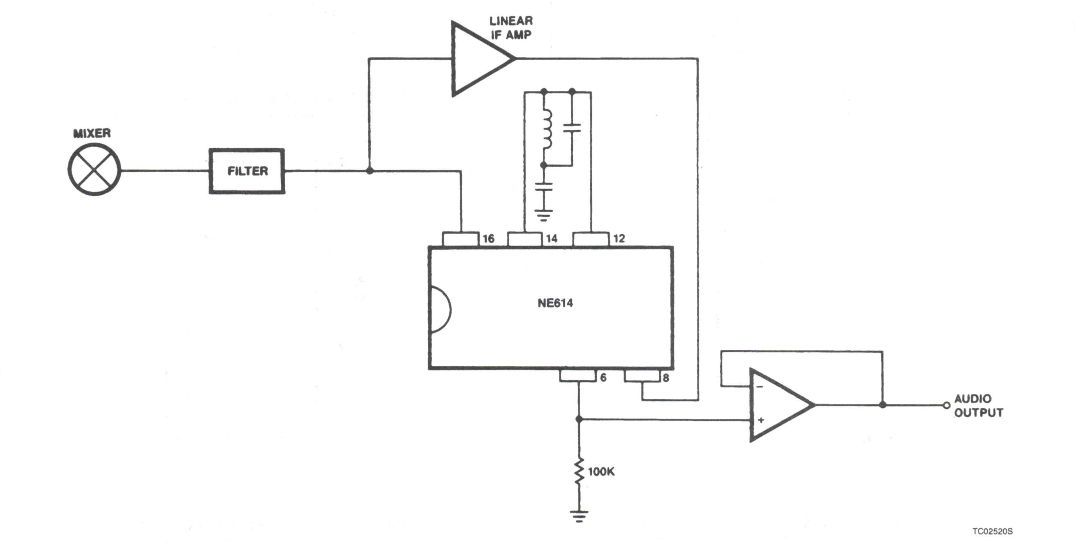


Figure 7. Synchronous AM Detection

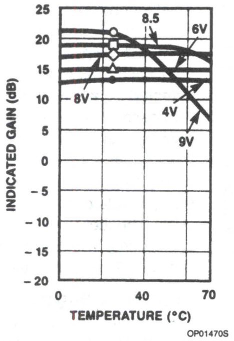


Figure 8. NE614 Indicated Gain vs Temperature and Voltage

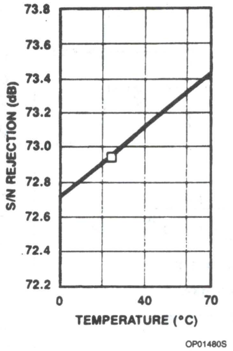


Figure 9. NE614 Signal-To-Noise Ratio vs Temperature

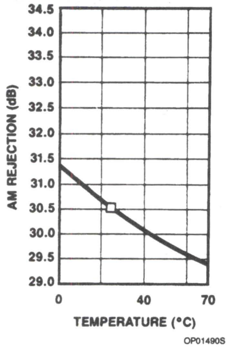


Figure 10. NE614 AM Rejection vs Temperature

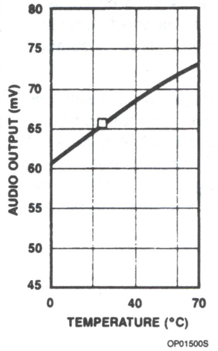


Figure 11. NE614 Audio Output vs Temperature

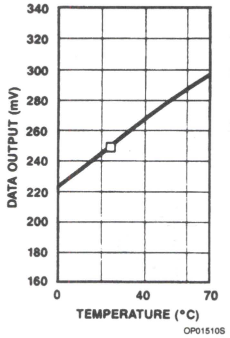


Figure 12. NE614 Data Output vs Temperature

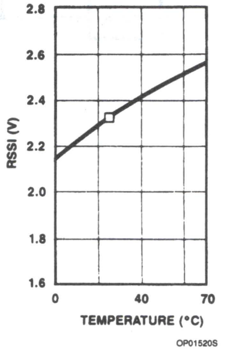


Figure 13. RSSI vs Temperature

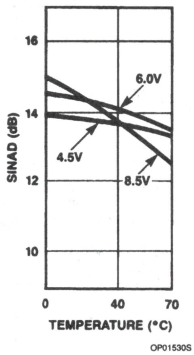


Figure 14. NE614 SINAD vs Temperature and V_{CC}

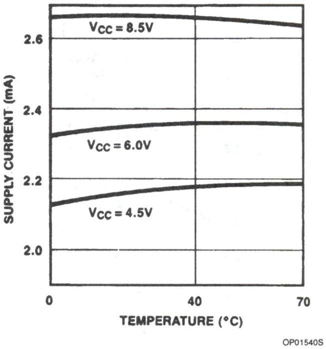


Figure 15. NE614 Supply Current vs Temperature

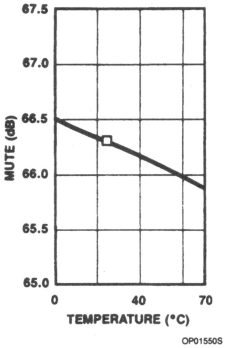


Figure 16. NE614 Muting vs Temperature

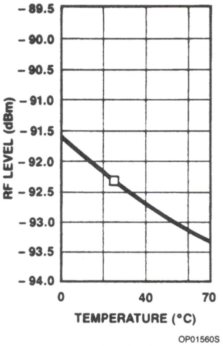


Figure 17. NE614 Limiting RF Level vs Temperature

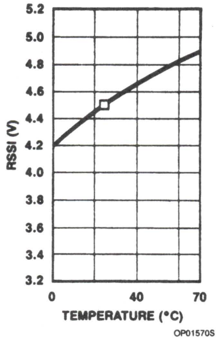


Figure 18. NE614 Large Signal Uncompensated RSSI Voltage vs Temperature

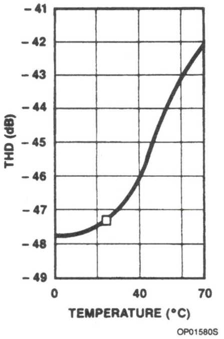


Figure 19. NE614 Total Harmonic Distortion vs Temperature

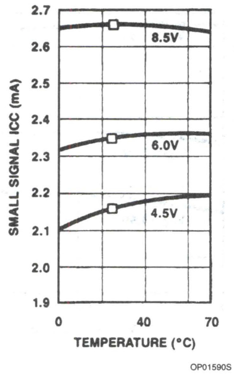


Figure 20. NE614 Supply Current vs Temperature and Voltage

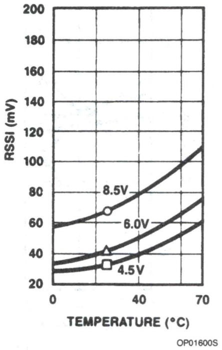


Figure 21. Small-Signal RSSI vs Temperature and Voltage

Signetics

NE/SE5539
Ultra-High Frequency Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

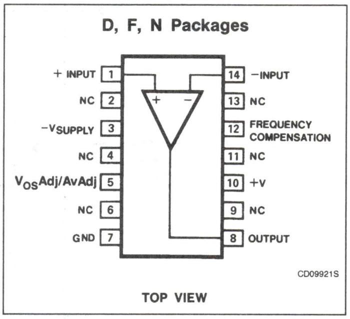
FEATURES

- **Gain bandwidth product: 1.2GHz at 17dB**
- **Slew rate: 600/Vμs**
- **Full power response: 48MHz**
- **A_{VOL}: 52dB typical**
- **350MHz unity gain**

APPLICATIONS

- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	−55°C to +125°C	SE5539N
14-Pin Cerdip	−55°C to +125°C	SE5539F

ABSOLUTE MAXIMUM RATINGS[1]

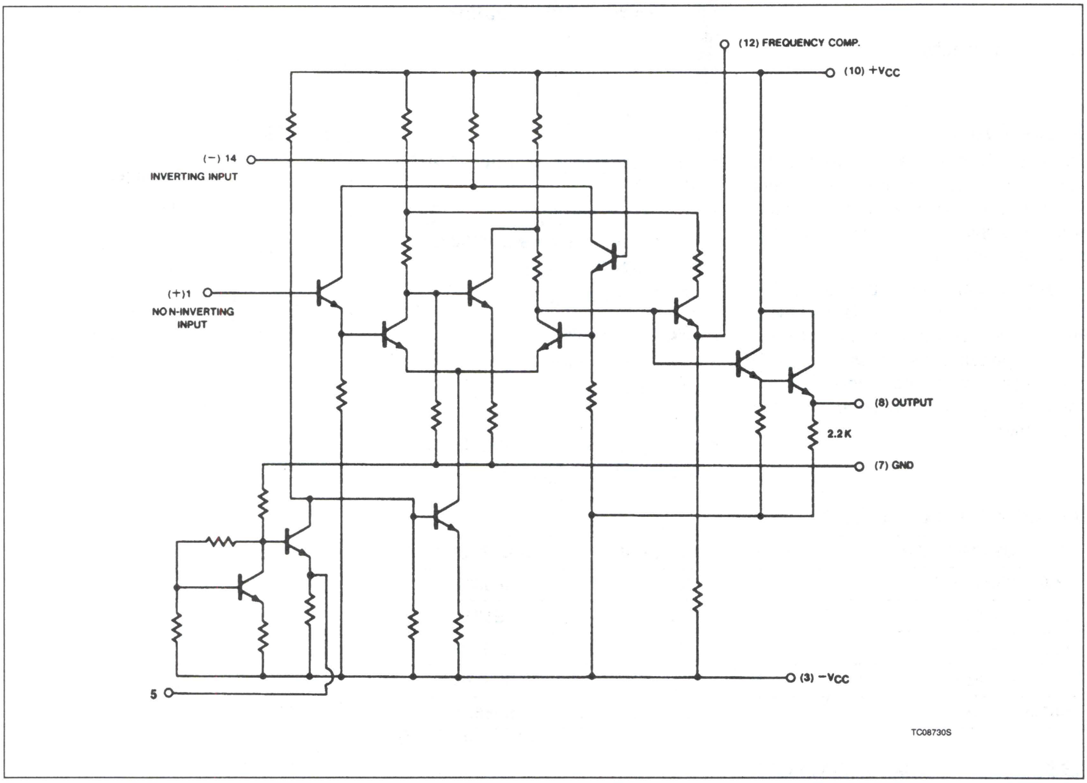
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range NE SE	 0 to 70 −55 to +125	 °C °C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTE:

1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.

Ultra-High Frequency Operational Amplifier NE/SE5539

EQUIVALENT CIRCUIT


(12) FREQUENCY COMP.
(10) $+V_{CC}$
(−) 14
INVERTING INPUT
(+)1
NON-INVERTING INPUT
(8) OUTPUT
2.2K
(7) GND
(3) $-V_{CC}$
5
TC08730S

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, V_{CM} ± 1.7V		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

Ultra-High Frequency Operational Amplifier

NE/SE5539

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				−Swing	−1.5	−2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_0 = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_0 = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV/V
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_0 = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_0 = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				−Swing	−1.1	−1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				−Swing	−1.4	−1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_0 = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega^1$		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega^1$		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega^1$		600			600		V/µs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega^1$		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega^1$		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega^1$		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$		4			4		$nV/\sqrt{Hz}$

NOTE:
1. External compensation.

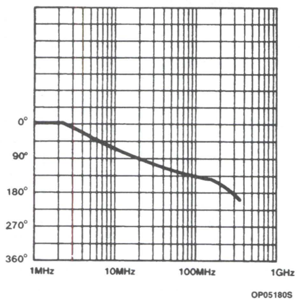
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2^1$		120		MHz
t_S	Settling time	$A_{CL} = 2^1$		23		ns
SR	Slew rate	$A_{CL} = 2^1$		330		V/µs
t_{PD}	Propagation delay	$A_{CL} = 2^1$		4.5		ns
	Full power response	$A_{CL} = 2^1$		20		MHz

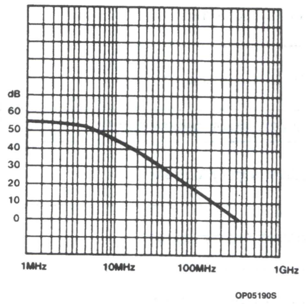
NOTE:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

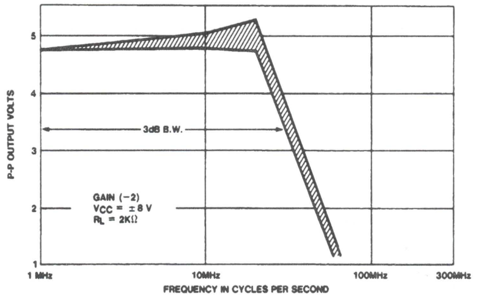


NE5539 Open-Loop Gain



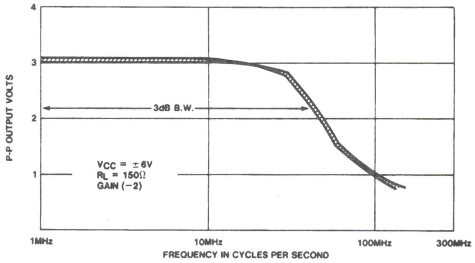
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



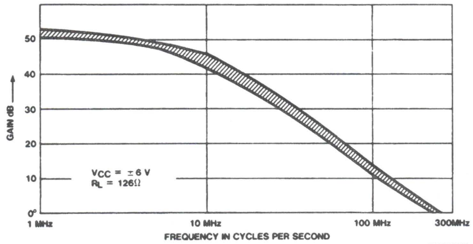
OP05200S

Power Bandwidth (NE)



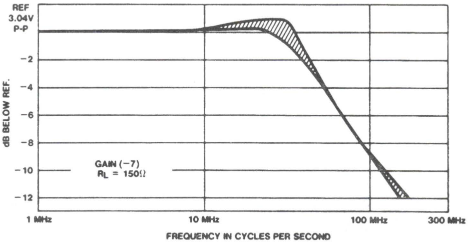
OP05210S

SE5539 Open-Loop Gain vs Frequency



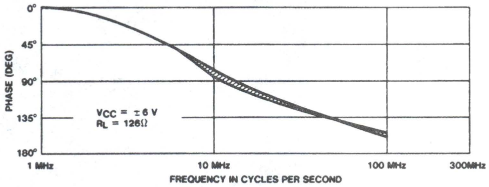
OP05220S

Power Bandwidth

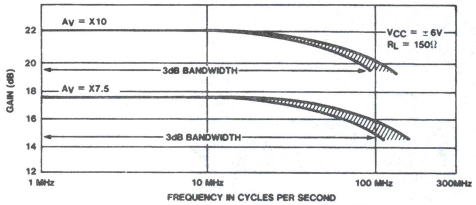


OP05230S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05250S

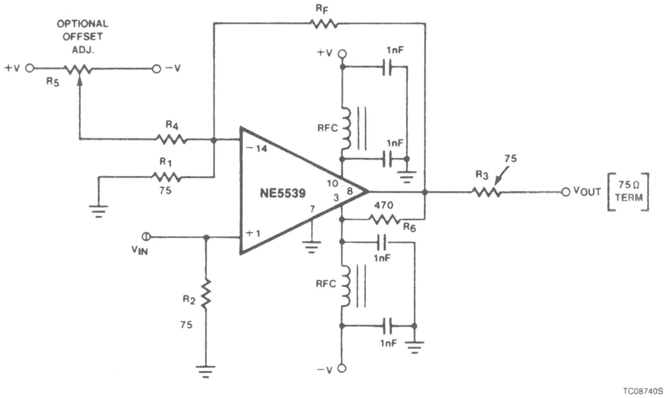
NOTE

▨ Indicates typical distribution −55°C ≤ T_A ≤ 125°C

OP05240S

CIRCUIT LAYOUT CONSIDERATIONS

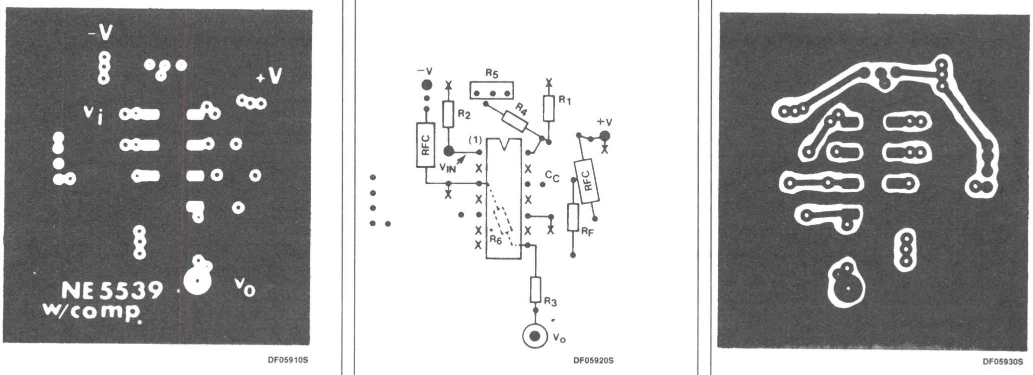
As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed cirucit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.


OPTIONAL
OFFSET
ADJ.
+V
R5
-V
RF
+V
1nF
RFC
1nF
R4
R1
75
-14
NE5539
10
3
8
7
+1
VIN
470
R6
1nF
RFC
R2
75
1nF
-V
R3
75
VOUT
75Ω TERM
TC08740S

NOTE:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON

NOTE:
R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

NOTE:
RFC 3T # 26 BUSSWIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)


-V
+V
Vi
NE 5539
w/comp.
Vo
DF05910S
-V
R5
R2
R4
R1
+V
RFC
(1)
VIN
X
CC
RFC
RF
R6
R3
Vo
DF05920S
DF05930S

Top Plane Copper[1] (Component Side)

Component Side (Component Layout)

Bottom Plane Copper[1]

NOTES:
(X) indicates ground connection to top plane.
*R_6 is on bottom side.

NOTE:
Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

Ultra-High Frequency Operational Amplifier NE/SE5539

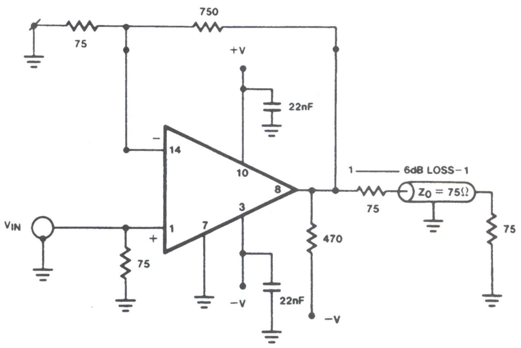
NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

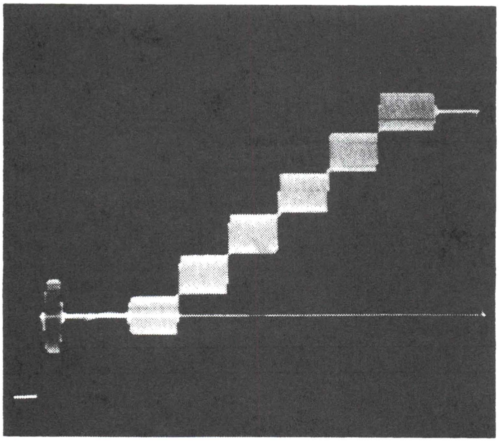
NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.



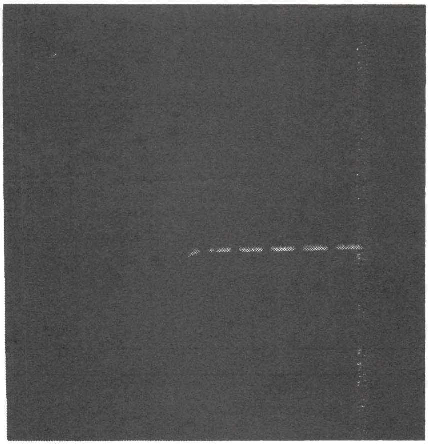
TCC8750S

Figure 2. NE5539 Video Amplifier



DF05940S

Figure 3. Input Signal



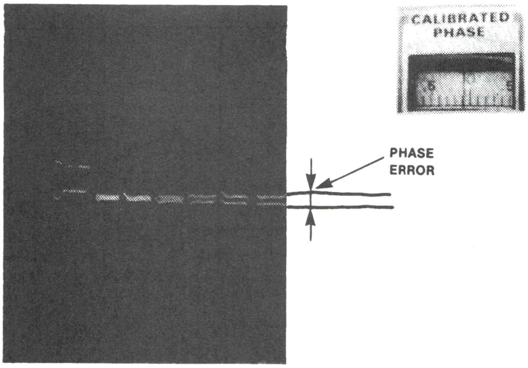
DF05950S

Figure 4. Differential Gain < 0.5%

NOTE:

1. Instruments used for these measurements were Tektronix, 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

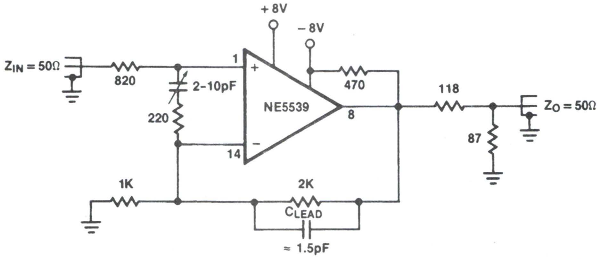
Ultra-High Frequency Operational Amplifier NE/SE5539


CALIBRATED
PHASE
PHASE
ERROR

DF05960S

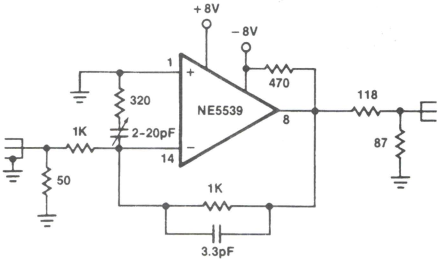
Figure 5. Differential Phase +0.1°

APPLICATIONS


+8V
−8V
Z_IN = 50Ω
820
1
+
2-10pF
220
14
−
NE5539
8
470
118
87
Z_O = 50Ω
1K
2K
C_LEAD
≈ 1.5pF

TC08760S

Figure 6. Non-Inverting Follower


+8V
−8V
1
+
320
2-20pF
1K
14
−
50
NE5539
8
470
118
87
1K
3.3pF

TC08770S

Figure 7. Inverting Follower

Signetics

Linear Products

AN140
Compensation Techniques for Use With the SE/NE5539

Application Note

NE5539 DESCRIPTION

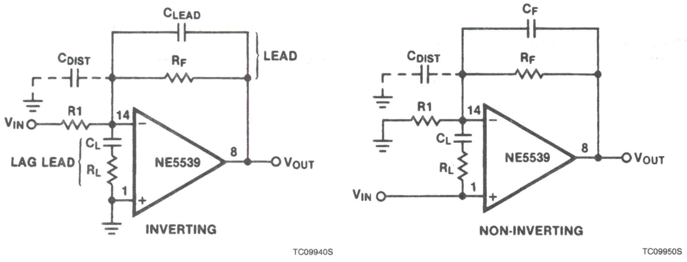
The Signetics SE/NE5539 ultra-high frequency operational amplifier is one of the fastest monolithic amplifiers made today. With a unity gain bandwidth of 350MHz and a slew rate of 600V/μs, it is second to none. Therefore, it is understandable that to attain this speed, standard internal compensation would have to be left out of its design. As a consequence, the op amp is not unconditionally stable for all closed-loop gains and must be externally compensated for gains below 17dB. Properly done, compensation need not limit slew rate. The following will explain how to use the methods available with the SE/NE5539.

LEAD AND LAG-LEAD COMPENSATION

A useful method for compensating the device for closed-loop gains below seven is to use lag-lead and lead networks as shown in Figure 1. The lead network is primarily concerned with compensating for loss of phase margin caused by distributed board capacitance and input capacitance, while lag-lead is mainly for optimizing transient response. Lead compensation modifies the feedback network and adds a zero to the overall transfer function. This increases the phase, but does not greatly change the gain magnitude. This zero improves the phase margin.

To determine components, it can be shown that the optimal conditions for amplifier stability occur when:

$$(R1)(C_{DIST}) = (R_F)(C_{LEAD}) \qquad (1)$$



NOTES:
$C_L = C_{LAG}$
$R_L = R_{LAG}$

Figure 1. Standard Lag-Lead Compensation

However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed-loop amplifier will be reduced. Based on using a double-sided copper-clad printed circuit board with a distributed capacitance of 3.5pF and a unity gain configuration, C_{LEAD} would be 3.5pF. Another way of stating the relationship between the distributed capacitance closed-loop gain and the lead compensation capacitor is:

$$C_{LEAD} = C_{DIST}\frac{R1}{R_F} \qquad (2)$$

When bandwidth is of primary concern, the lead compensation will usually be adequate. For closed-loop gains less than seven, lag-lead compensation is necessary for stability.

If transient response is also a factor in design, a lag-lead compensation network may be necessary (Reference Figure 1). For practical applications, the following equations can be used to determine proper lag-lead components:

$$\frac{R_F}{R1/R_{LAG}} \geqslant 7 \qquad (4)$$

Therefore,

$$R_{LAG} \leqslant \frac{R_F}{7 - R_F/R1} \qquad (5)$$

Using the above equation will insure a closed-loop gain of seven above the network break frequency. C_{LAG} may now be approximated using:

$$W_{LAG} \cong \frac{2\pi(GBW)}{10}\ \text{Rad/Sec} \qquad (6)$$

$$W_{LAG} = \frac{\pi(GBW)}{5}\ \text{Rad/Sec} \qquad (7)$$

where

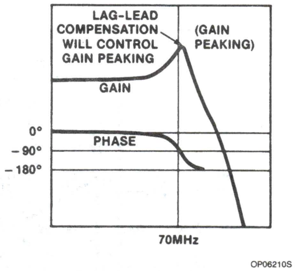
$$W_{LAG} = \frac{1}{(R_{LAG})(C_{LAG})} \qquad (8)$$

therefore,

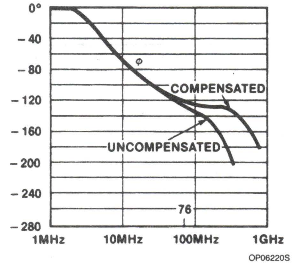
$$\frac{\pi(GBW)}{5} = \frac{1}{(R_{LAG})(C_{LAG})} \qquad (9)$$

and

$$C_{LAG} = \frac{5}{\pi R_{LAG}(GBW)} \qquad (10)$$



a. Closed-Loop Inverting Gain of Seven Gain-Phase Response (Uncompensated)



b. Open-Loop Phase

Figure 2

Compensation Techniques for Use With the SE/NE5539 AN140

This method adds a pole and zero to the transfer function of the device, causing the actual open-loop gain and phase curve to be reshaped, thus creating a progressive improvement above the critical frequency where phase changes rapidly. (Near 70MHz, see Figures 2a and 2b.) But also, the lag-lead network can be adjusted to optimize gain peaking for transient responses. Therefore, rise time, overshoot, and settling time can be changed for various closed-loop gains. The result of using this technique is shown for a pulse amplifier in Figure 3.

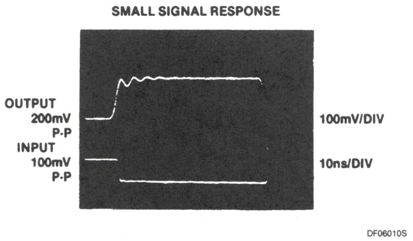


Figure 3. Compensated Pulse Response

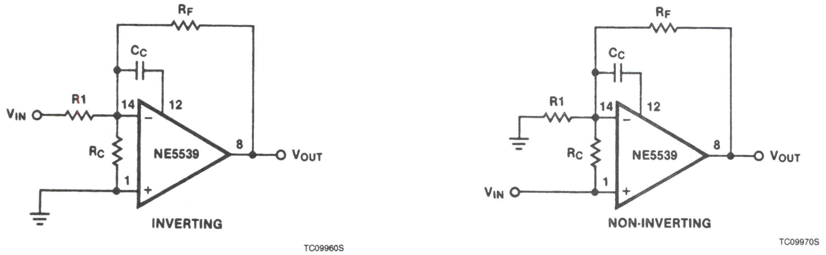

RF
CC
VIN
R1
14
12
RC
NE5539
8
VOUT
1
INVERTING
TC09960S
RF
CC
R1
14
12
RC
NE5539
8
VOUT
VIN
1
NON-INVERTING
TC09970S

Figure 4. Pin 12 Compensation

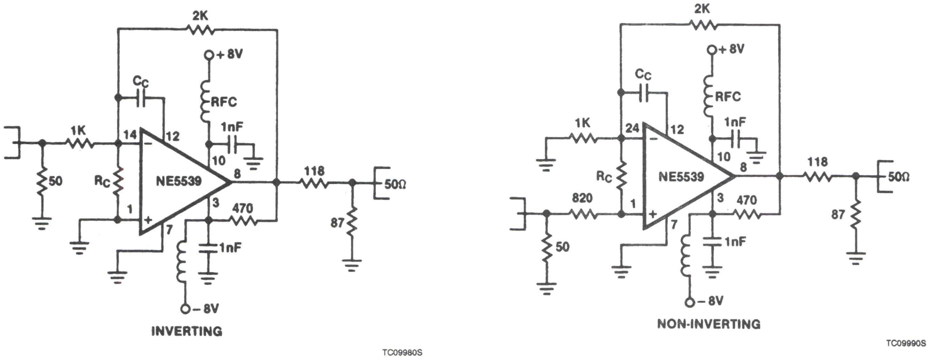
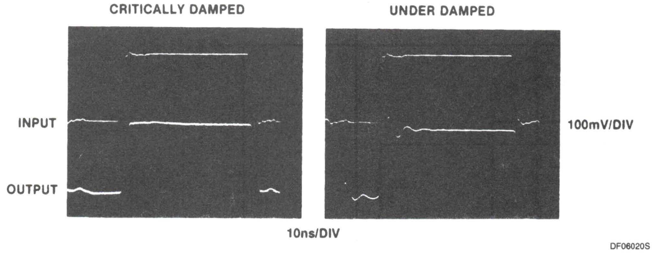

2K
+8V
CC
RFC
1K
14
12
1nF
10
8
50
RC
NE5539
118
50Ω
1
3
470
87
7
1nF
-8V
INVERTING
TC09980S
2K
+8V
CC
RFC
1K
24
12
1nF
10
8
RC
NE5539
118
50Ω
820
1
3
470
87
7
1nF
50
-8V
NON-INVERTING
TC09990S

Figure 5. Pulse Response Test Circuits



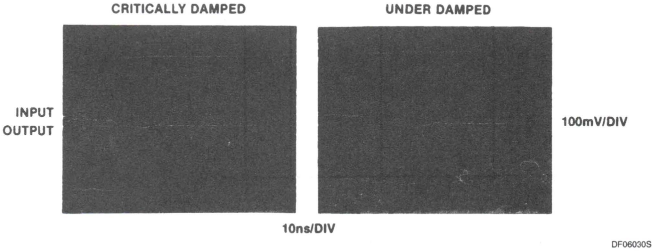
RISE TIME – 2.4ns
$R_C = 118\Omega$ — $C_C = 4.6pF$
PROPAGATION DELAY = 2.3ns

(a)

RISE TIME – 2.1ns
$R_C = 200$ — $C_C = 5.4pF$
PROPAGATION DELAY = 2.3ns

(b)

Figure 6. Small Signal Response — Non-Inverting



RISE TIME – 5.3ns
$R_C = 226\Omega$ — $C_C = 2.3pF$
PROPAGATION DELAY = 5.1ns

(a)

RISE TIME – 3.3ns
$R_C = 460$ — $C_C = 2.0pF$
PROPAGATION DELAY = 4.5ns

(b)

Figure 7. Small Signal Response — Inverting

USING PIN 12 COMPENSATION

An alternate method of external compensation is obtained by use of the SE/NE5539 frequency compensation pin. The circuits in Figure 4 show the correct way to use this pin. As can be seen, this method saves the use of one capacitor as compared to standard lag-lead and lead compensation as shown in Figure 1.

But, most importantly, both methods are equally effective; i.e., a good wide-band amplifier below 17dB, with control over ringing and overshoot. For example, inverting and non-inverting amplifier circuits using Pin 12 are shown in Figure 5. The corresponding pulse response for each circuit is shown in Figures 6 and 7 for the network values recommended. As shown by the response photos, the overshoot and settling time can be controlled by adjusting R_C and C_C. In damping the overshoot, rise time is slightly decreased. Also, the non-inverting configuration (Figure 6) gives a very fast response time compared to the inverting mode.

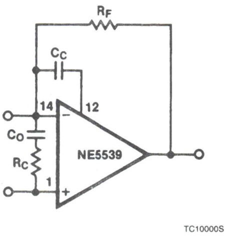


Figure 8. C_O Will Reduce Output Offset and Noise

If it is important to reduce output offset voltage and noise, an additional capacitor, C_O, can be added in series with the resistor (R_C) across the inputs. This should be a large value to block DC but not affect the benefits of the compensation components at high frequencies. A value of 0.01μF as shown in Figure 8 is sufficient.

INTERNAL CHARACTERISTICS OF THE SE/NE5539

In order to better understand the compensation procedure, a detailed discussion of the amplifier follows.

The complete amplifier schematic is shown in Figure 9. To clarify the effect of the compensation pin, the schematic is split into five main parts as shown in Figure 10.

Each segment in Figure 10 is defined as follows: starting from the non-inverting input, Section A_1 is the amplification from the input to the base of transistor Q_4. A_2 is from the base of Q_4 to the summation point at the collector of Q_3. Furthermore, A_3 represents the gain from the non-inverting input to the summation point via the common emitter side of Q_2 and Q_3. Finally, B_F is the feedback factor of the positive feedback loop from the collector of Q_3 to the base of Q_4.

From Figure 10, it can be seen that the total gain (A_T) is:

$$A_T = \frac{A_1A_2}{1-(B_FA_2)} + A_3(1 + B_FA_2)$$

Each term in this equation plays a role at different frequencies to determine the total transfer function of the device. Of particular importance is the pole in A_3 (near 340MHz) which causes a roll-off of 12dB/octave and loss of phase margin just before unity gain. This can be seen in the Bode plot in Figure 11a. To overcome this pole, a capacitor and resistor are connected as shown in Figures 12a and 12b. The compensation pin is connected to the emitter of Q_5, which is in an emitter-follower configuration. Therefore, a reactance connected to Pin 12 acts essentially as if it were connected at the base of Q_5. Since the capacitor is connected here, it is now a component of B_F and a zero is added to the transfer function. The resistor across the input pins controls overall gain and causes A_T to cross 0dB at a lower frequency; the capacitor in the feedback loop controls phase shift and gain peaking.

To further explain, Bode plots of open-loop response using varying capacitor values and corresponding pulse responses are shown in Figures 13a through 13f. The changes in gain and phase can readily be seen, as is the effect on bandwidth.

Compensation Techniques for Use With the SE/NE5539

AN140

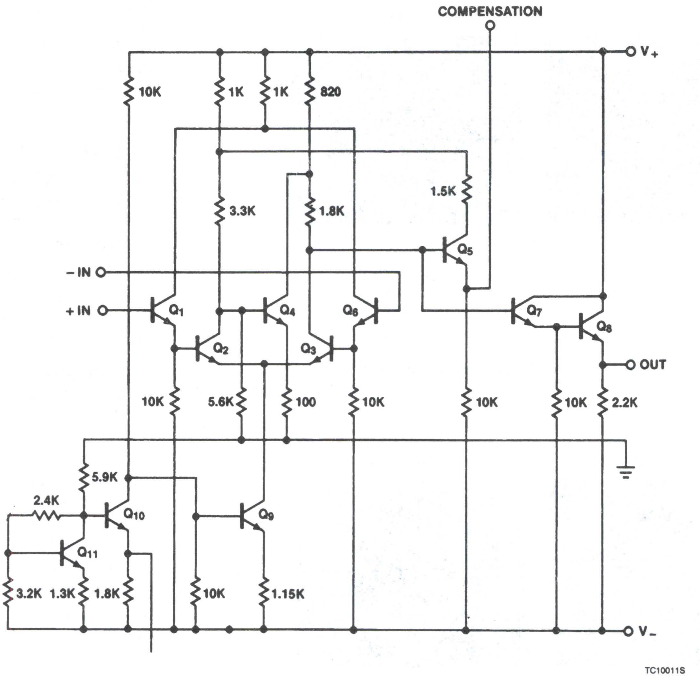

COMPENSATION
V+
10K
1K
1K
820
1.5K
3.3K
1.8K
Q5
−IN
+IN
Q1
Q4
Q6
Q7
Q8
Q2
Q3
OUT
10K
5.6K
100
10K
10K
10K
2.2K
5.9K
2.4K
Q10
Q9
Q11
3.2K
1.3K
1.8K
10K
1.15K
V−
TC10011S

Figure 9. Complete Schematic of SE/NE5539

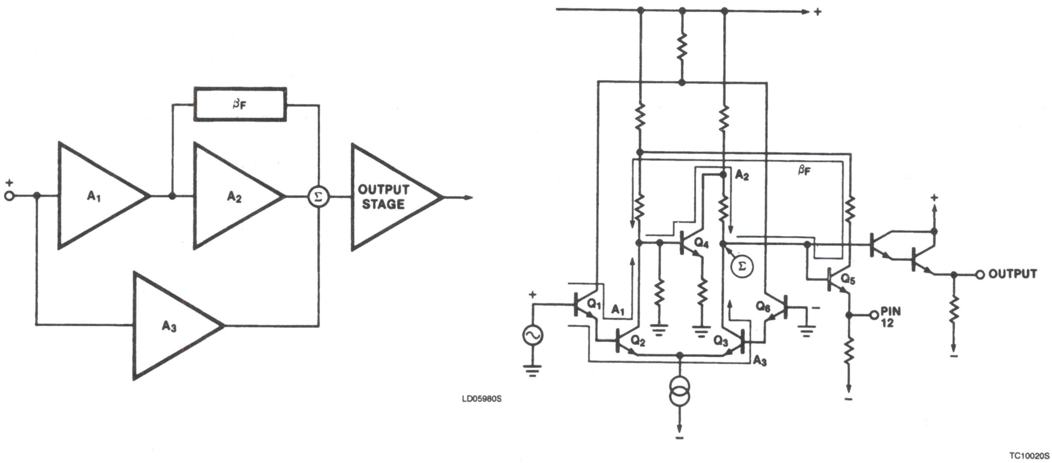
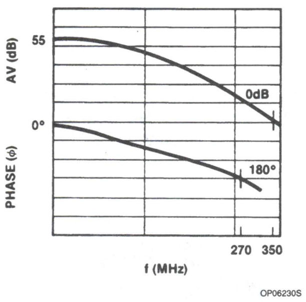

βF
+
A1
A2
Σ
OUTPUT STAGE
A3
LD05980S
+
A2
βF
+
Q4
Σ
Q5
OUTPUT
+
Q1
A1
Q6
−
PIN 12
Q2
Q3
A3
−
−
−
TC10020S

Figure 10. Internal Sections

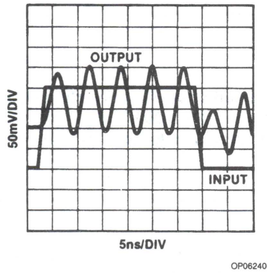
Compensation Techniques for Use With the SE/NE5539 AN140

COMPUTER ANALYSIS

The open-loop and pulse response plots were generated using an IBM 370 computer and SPICE, a general-purpose circuit simulation program. Each transistor in the part is mathematically modeled after actual device parameters, which were measured in the laboratory. These models are then combined with the resistors and voltage sources through node numbers so that the computer knows where each is connected.



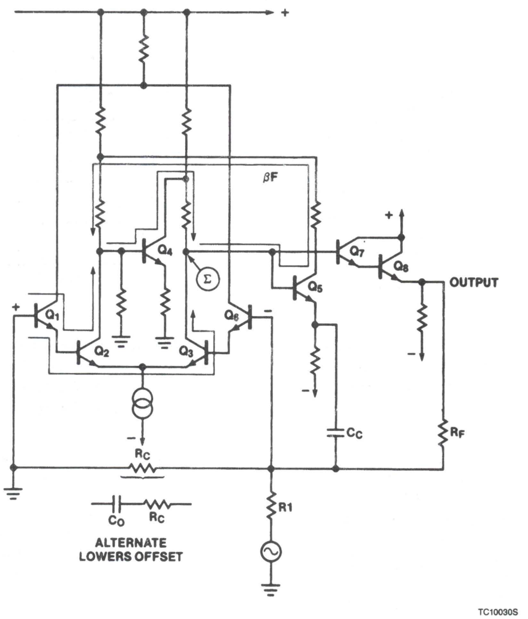
a. Open-Loop Gain — No Compensation (Computer Simulation)



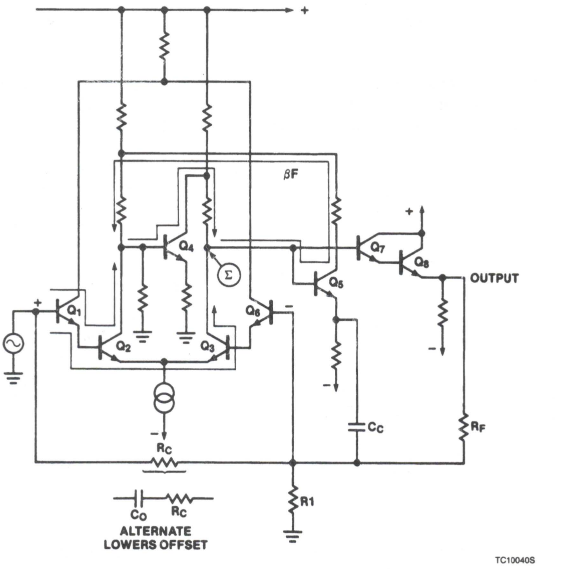
b. Closed-Loop Non-Inverting Response — No Compensation (Computer Simulation — Oscillation is Evident)

Figure 11

To indicate the accuracy of this system, the actual open-loop gain is compared to the computer plots in Figures 14 and 15. The real payoff for this system is that once a credible simulation is achieved, any outside circuit can be modeled around the op amp. This would be used to check for feasibility before breadboarding in the lab. The internal circuit can be treated like a black box and the outside circuit program altered to whatever application the user would like to examine.


+
βF
+
Q4
Q7
Q8
Σ
Q5
OUTPUT
+
Q1
Q6
−
Q2
Q3
−
−
Cc
RF
−
Rc
R1
Co
Rc
ALTERNATE LOWERS OFFSET
TC10030S

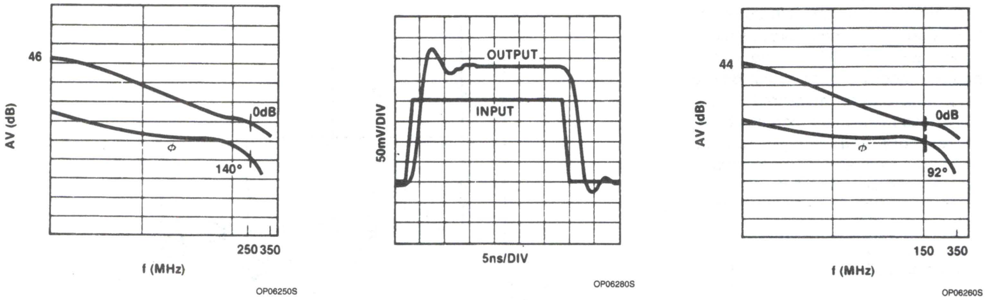
a. Pin 12 Compensation Showing Internal Connections — Inverting


+
βF
+
Q4
Q7
Q8
Σ
Q5
OUTPUT
+
Q1
Q6
−
Q2
Q3
−
−
Cc
RF
−
Rc
R1
Co
Rc
ALTERNATE LOWERS OFFSET
TC10040S

b. Pin 12 Compensation Showing Internal Connections — Non-Inverting

Figure 12

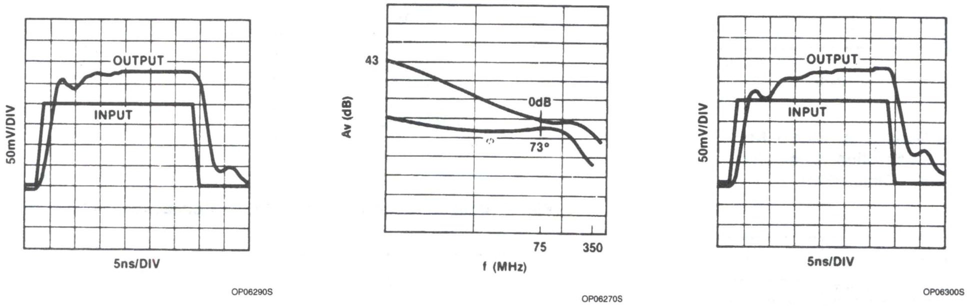
Compensation Techniques for Use With the SE/NE5539 AN140



a. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 1pF$, (Computer Simulation)

b. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 1pF$, $A_V = 3$ (Computer Simulation — Underdamped)

c. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 2pF$ (Computer Simulation)



d. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 2pF$, $A_V = 3$ (Computer Simulation — Critically-Damped)

e. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 3pF$, (Computer Simulation)

f. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 3pF$, $A_V = 3$ (Computer Simulation — Overdamped)

Figure 13

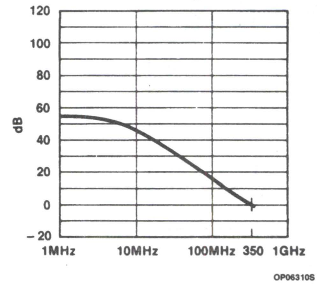


Figure 14. Actual Open-Loop Gain Measured in Lab

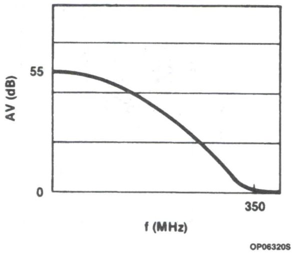


Figure 15. Computer-Generated Open-Loop Gain

1. J. Millman and C. C. Halkias: *Integrated Electronics: Analog and Digital Circuits and Systems,* McGraw-Hill Book Company, New York, 1972.

2. A. Vladimirescu, Kaihe Zhang, A. R. Newton, D. O. Peterson, A. Sanquiovanni-Vincentelli: "Spice Version 2G," University of California, Berkeley, California, August 10, 1981.

3. Signetics: *Analog Data Manual 1983,* Signetics Corporation, Sunnyvale, California 1983.

Signetics

NE5592
Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

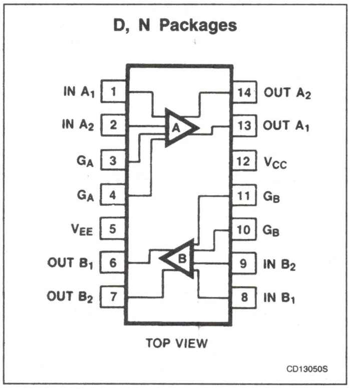
FEATURES

- **120MHz bandwidth**
- **Adjustable gain from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

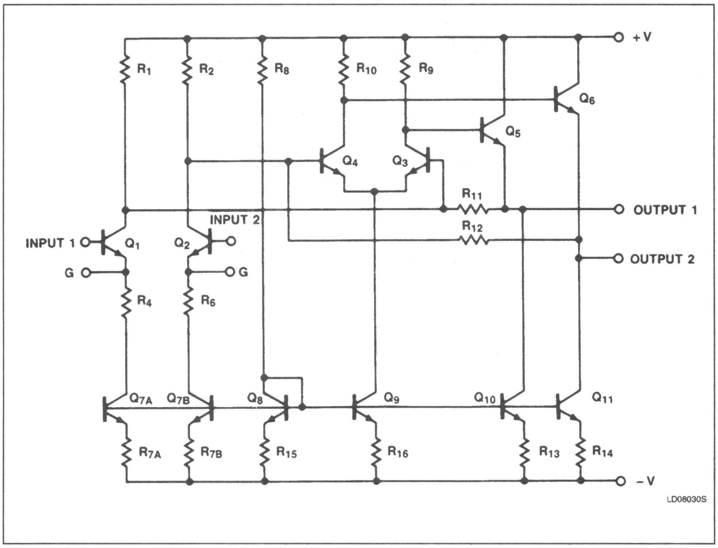
PIN CONFIGURATION


D, N Packages
IN A1 1
IN A2 2
GA 3
GA 4
VEE 5
OUT B1 6
OUT B2 7
8 IN B1
9 IN B2
10 GB
11 GB
12 VCC
13 OUT A1
14 OUT A2
A
B
TOP VIEW
CD13050S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT


+V
R1
R2
R8
R10
R9
Q6
Q5
Q4
Q3
R11
R12
OUTPUT 1
OUTPUT 2
INPUT 2
INPUT 1
Q1
Q2
G
G
R4
R6
Q7A
Q7B
Q8
Q9
Q10
Q11
R7A
R7B
R15
R16
R13
R14
-V
LD08030S

Video Amplifier NE5592

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P\text{-}P}$	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	μA
I_{BIAS}	Input bias current			5	20	μA
	Input noise voltage	BW 1kHz to 10MHz		4		$nV/\sqrt{Hz}$
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $V_{CM} \pm 1V$, $f = 5MHz$	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50	85		dB
	Channel separation	$V_{OUT} = 1V_{P\text{-}P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$	65	75		dB
V_{OS}	Output offset voltage gain select pins open	$R_L = \infty$ $R_L = \infty$		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$		35	44	mA

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $R_S = \phi$	55			dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50			dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$		75		dB
V_{OS}	Output offset voltage					
	gain select pins connected together	$R_L = \infty$			1.5	V
	gain select pins open	$R_L = \infty$			1.0	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	2.8			V
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$			47	mA

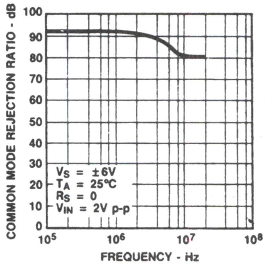
AC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage $V_S = \pm 6.0V$. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	$V_{OUT} = 1V_{P-P}$		25	20	MHz
t_R	Rise time			15		ns
t_{PD}	Propagation delay	$V_{OUT} = 1V_{P-P}$		7.5	12	ns

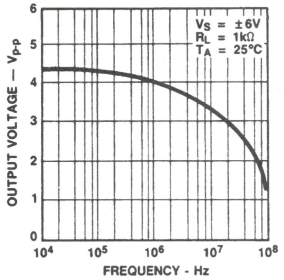
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



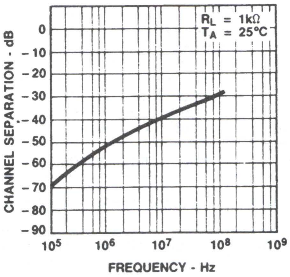
OP18580S

Output Voltage Swing as a Function of Frequency



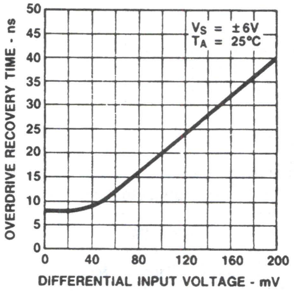
OP18590S

Channel Separation as a Function of Frequency



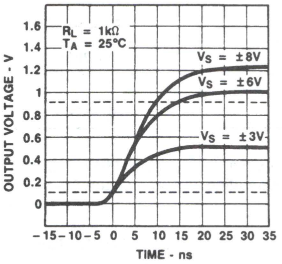
OP18600S

Differential Overdrive Recovery Time



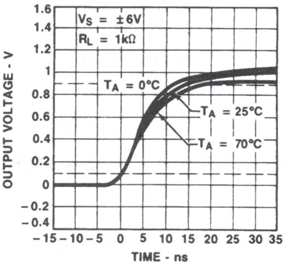
OP18610S

Pulse Response as a Function of Supply Voltage



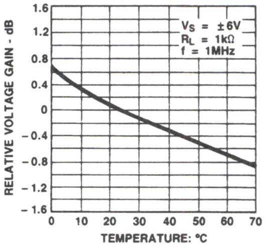
OP18620S

Pulse Response as a Function of Temperature



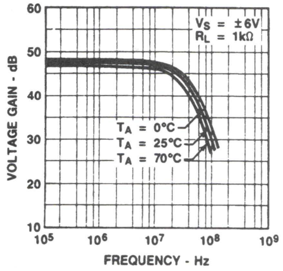
OP18630S

Voltage Gain as a Function of Temperature



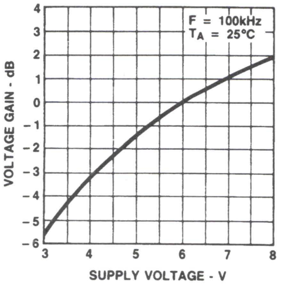
OP18640S

Gain vs Frequency as a Function of Temperature



OP18650S

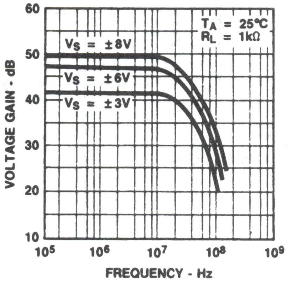
Voltage Gain as a Function of Supply Voltage



OP18660S

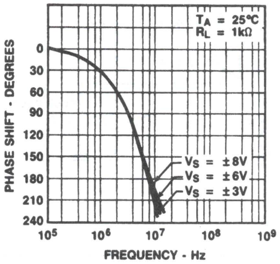
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



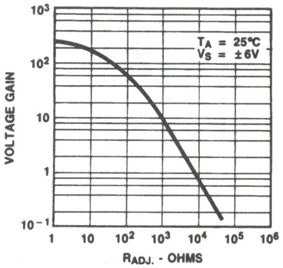
OP18670S

Phase vs Frequency as a Function of Supply Voltage



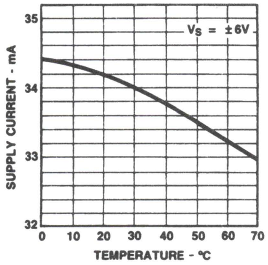
OP18680S

Voltage Gain as a Function of R_{ADJ}



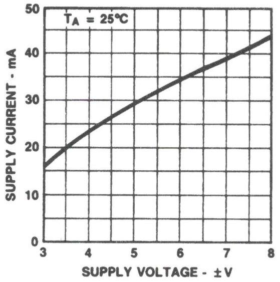
OP18690S

Supply Current as a Function of Temperature



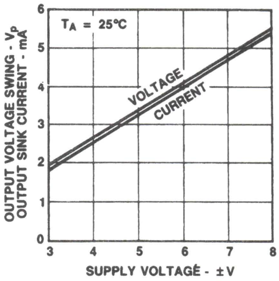
OP18700S

Supply Current as a Function of Supply Voltage



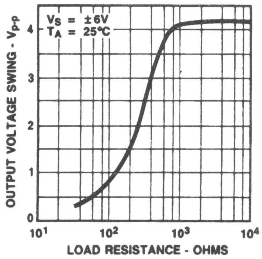
OP18710S

Output Voltage Swing and Sink Current as a Function of Supply Voltage



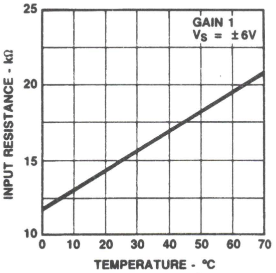
OP18720S

Output Voltage Swing as a Function of Load Resistance



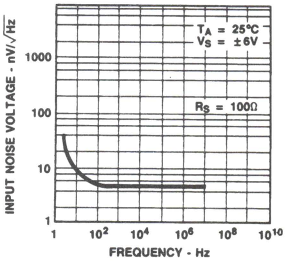
OP18730S

Input Resistance as a Function of Temperature



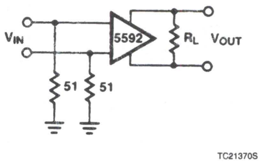
OP18740S

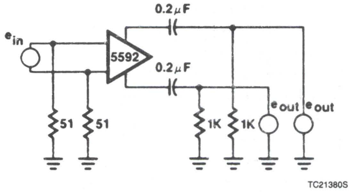
Input Noise Voltage as a Function of Frequency

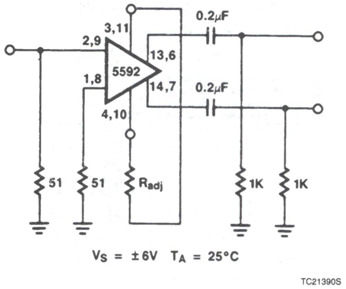


OP18750S

TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.


VIN
5592
RL
VOUT
51
51
TC21370S


ein
5592
0.2μF
0.2μF
51
51
1K
1K
eout
eout
TC21380S


3,11
2,9
1,8
5592
13,6
14,7
4,10
0.2μF
0.2μF
51
51
Radj
1K
1K
VS = ±6V TA = 25°C
TC21390S

Signetics

NE/SE592
Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

FEATURES

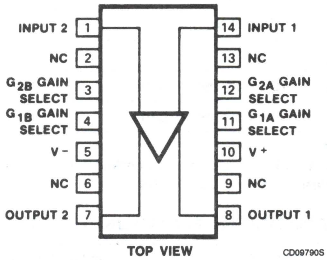
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

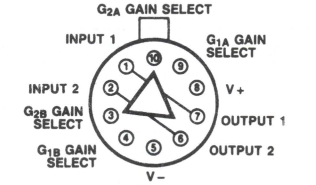
- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATIONS

D, F, N Packages


INPUT 2 1
NC 2
G2B GAIN SELECT 3
G1B GAIN SELECT 4
V− 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G2A GAIN SELECT
11 G1A GAIN SELECT
10 V+
9 NC
8 OUTPUT 1
TOP VIEW
CD09790S

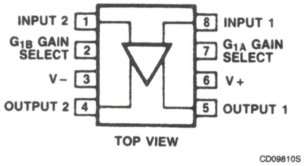
H Package*


G2A GAIN SELECT
INPUT 1
G1A GAIN SELECT
INPUT 2
V+
G2B GAIN SELECT
OUTPUT 1
G1B GAIN SELECT
OUTPUT 2
V−
1
2
3
4
5
6
7
8
9
10

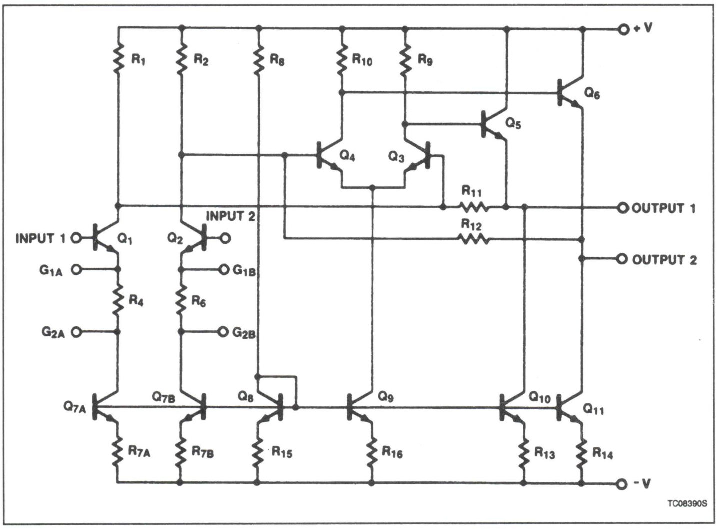
CD09800S

NOTES:
Pin 5 connected to case.
*Metal cans (H) not recommended for new designs.

D, F, N, Packages


INPUT 2 1
G1B GAIN SELECT 2
V− 3
OUTPUT 2 4
8 INPUT 1
7 G1A GAIN SELECT
6 V+
5 OUTPUT 1
TOP VIEW
CD09810S

EQUIVALENT CIRCUIT


+V
R1
R2
R8
R10
R9
Q6
Q5
Q4
Q3
R11
OUTPUT 1
R12
OUTPUT 2
INPUT 1
Q1
Q2
INPUT 2
G1A
G1B
R4
R6
G2A
G2B
Q7A
Q7B
Q8
Q9
Q10
Q11
R7A
R7B
R15
R16
R13
R14
−V
TC08390S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	−55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic Dip	0 to +70°C	NE592N8
8-Pin Cerdip	−55°C to +125°C	SE592F8
8-Pin SO	0 to +70°C	NE592D8
10-Lead metal can	0 to +70°C	NE592H
10-Lead metal can	−55°C to +125°C	SE592H

NOTE:
Also N8, N14, D8 and D14 package parts available in "High" gain version by adding "H" before package designation, as: NE592HD8.

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range SE592 NE592	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250	400	600	300	400	500	V/V
	Gain 2[2, 4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		kΩ
	Gain 2[2, 4]		10	30		20	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	60	86		60	86		dB
	Gain 2[4]	$V_{CM} \pm 1V$, $f = 5MHz$		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.0	V
	Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES:

1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leqslant T_A \leqslant 70°C$ for NE592; $-55°C \leqslant T_A \leqslant 125°C$ for SE592, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250		600	200		600	V/V
	Gain 2[2, 4]		80		120	80		120	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 2[2, 4]		8.0			8.0			kΩ
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	50			50			dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.2	V
	Gain 3[3]	$R_L = \infty$			1.0			1.0	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	2.8			2.5			V
I_{CC}	Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

AC ELECTRICAL CHARACTERISTICS

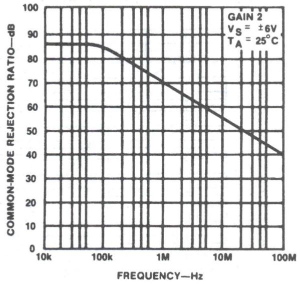
$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth								
	Gain 1[1]			40			40		MHz
	Gain 2[2, 4]			90			90		MHz
t_R	Rise time								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		10.5			10.5		ns
	Gain 2[2, 4]			4.5	12		4.5	10	ns
t_{PD}	Propagation delay								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		7.5			7.5		ns
	Gain 2[2, 4]			6.0	10		6.0	10	ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

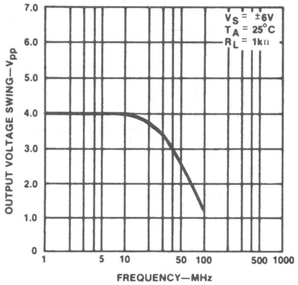
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



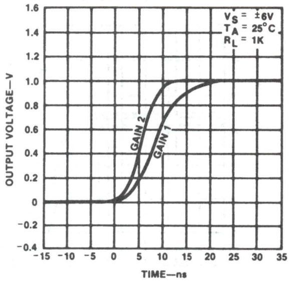
OP04421S

Output Voltage Swing As a Function of Frequency



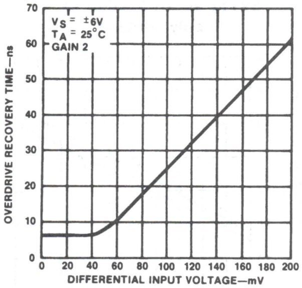
OP04430S

Pulse Response



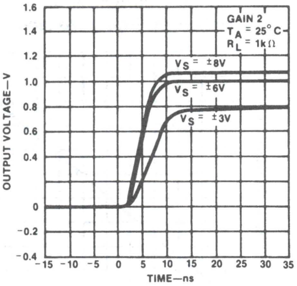
OP04440S

Differential Overdrive Recovery Time



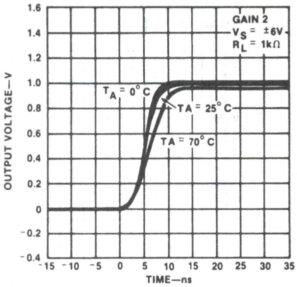
OP04450S

Pulse Response as a Function of Supply Voltage



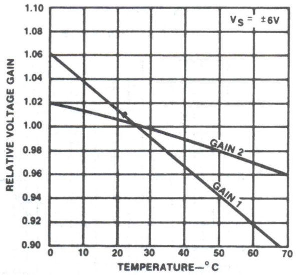
OP04460S

Pulse Response as a Function of Temperature



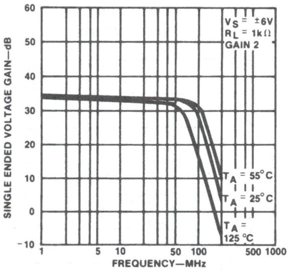
OP04470S

Voltage Gain as a Function of Temperature



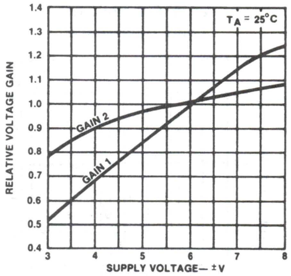
OP04480S

Gain vs Frequency as a Function of Temperature



OP04490S

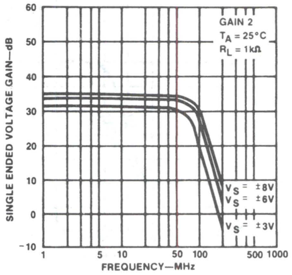
Voltage Gain as a Function of Supply Voltage



OP04500S

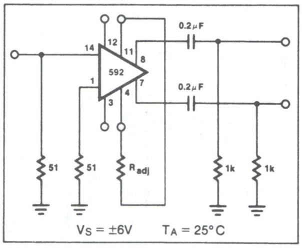
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



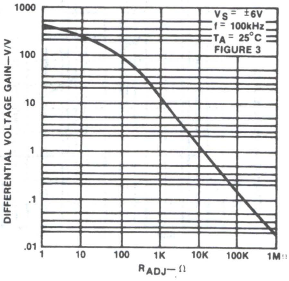
OP04510S

Voltage Gain Adjust Circuit



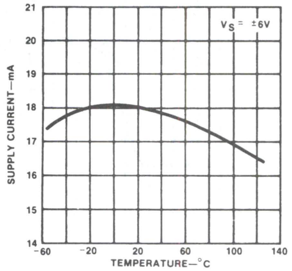
OP04521S

Voltage Gain as a Function of RADJ (Figure 3)



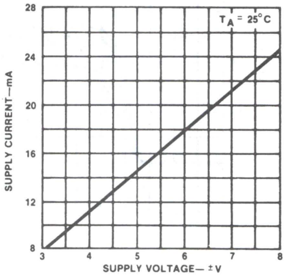
OP04530S

Supply Current as a Function of Temperature



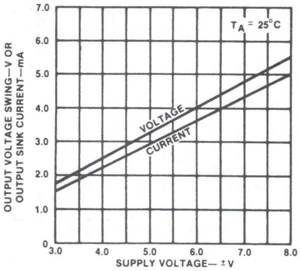
OP04540S

Supply Current as a Function of Supply Voltage



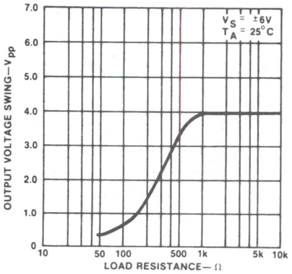
OP04550S

Output Voltage and Current Swing as a Function of Supply Voltage



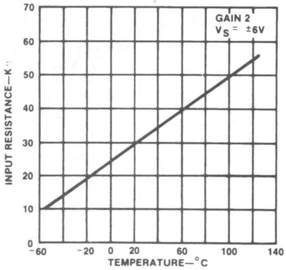
OP04560S

Output Voltage Swing as a Function of Load Resistance



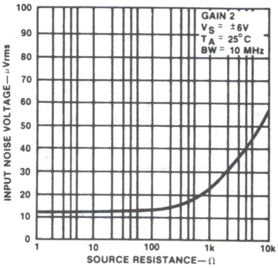
OP04570S

Input Resistance as a Function of Temperature



OP04580S

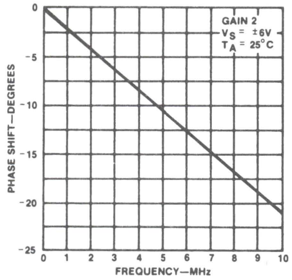
Input Noise Voltage as a Function of Source Resistance



OP04590S

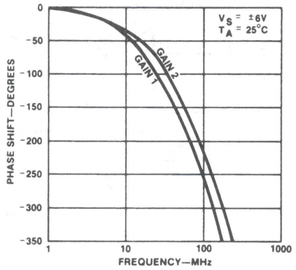
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Phase Shift as a Function of Frequency



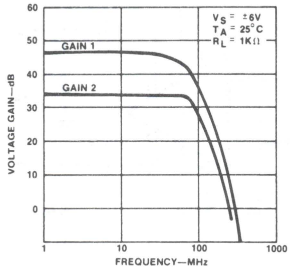
OP04600S

Phase Shift as a Function of Frequency



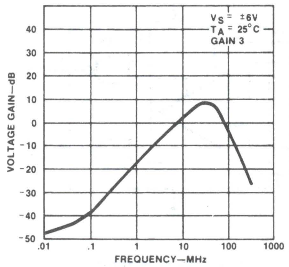
OP04610S

Voltage Gain as a Function of Frequency



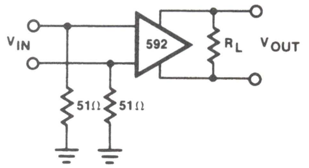
OP04620S

Voltage Gain as a Function of Frequency (All Gain Select Pins Open)

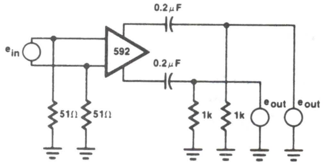


OP04630S

TEST CIRCUITS T_A = 25°C, unless otherwise specified.

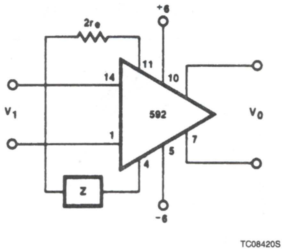

V_{IN}
592
R_L
V_{OUT}
51Ω
51Ω

TC08400S


0.2μF
592
0.2μF
e_{in}
51Ω
51Ω
1k
1k
e_{out}
e_{out}

TC08410S

TYPICAL APPLICATIONS



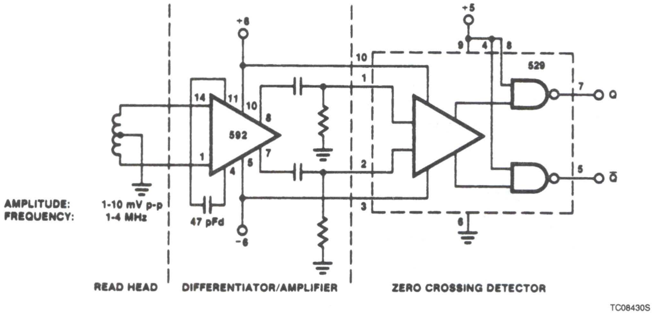
+6
2r_e
11
10
14
V_1
592
V_0
1
7
5
4
Z
-6
TC08420S

NOTE:

$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

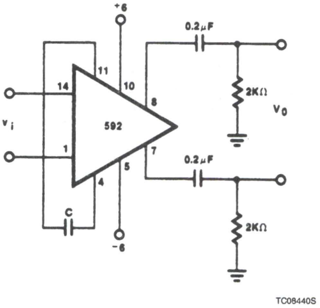
$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Basic Configuration



+6
+5
592
529
14
11
10
8
1
7
4
5
10
1
2
3
9
4
8
7
5
6
Q
Q̄
AMPLITUDE:
FREQUENCY:
1-10 mV p-p
1-4 MHz
47 pFd
-6
READ HEAD
DIFFERENTIATOR/AMPLIFIER
ZERO CROSSING DETECTOR
TC08430S

Disc/Tape Phase-Modulated Readback Systems



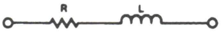
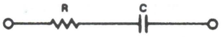
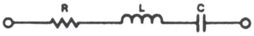
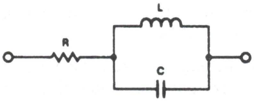
+6
0.2μF
14
11
10
8
2KΩ
V_i
592
V_0
1
7
5
4
0.2μF
C
2KΩ
-6
TC08440S

NOTE:
For frequency $F_1 << 1/2\pi(32)C$

$$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation With High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

TC08422S

NOTE:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

Signetics

Linear Products

AN141
Using the NE/SE592 Video Amplifier

Application Note

VIDEO AMPLIFIER PRODUCTS

NE/SE592 Video Amplifier

The 592 is a two-stage differential output, wide-band video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins $G_{1A}-G_{1B}$ and $G_{2A}-G_{2B}$, respectively. As shown by Figure 1, the emitter circuits of the differential pair return through independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus, the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400V/V. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single-ended gains are one-half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer, the input bias current required by the 592 may be passed directly through the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a DC path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output DC offset, they should be small — ideally 0Ω. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V − 1.0V = 0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.
4. The maximum input resistor size is:

$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}} \qquad (1)$$

$$= \frac{0.005\text{V}}{5\mu\text{A}}$$

$$= 1.00\text{k}\Omega$$

Of paramount importance during the design of the NE592 device was bandwidth. In a monolithic device, this precludes the use of PNP transistors and standard level-shifting techniques used in lower frequency devices. Thus, without the aid of level shifting, the output common-mode voltage present on the NE592 is typically 2.9V. Most applications, therefore, require capacitive coupling to the load. An exception to the rule is a differential amplifier with an input common-mode range greater than +2.9V as shown in Figure 2. In this circuit, the NE592 drives a NE511B transistor array connected as a differential cascode amplifier. This amplifier is capable of differential output voltages of $48V_{P\text{-}P}$ with a 3dB bandwidth of approximately 10MHz (depending on the capacitive load). For optimum operation, R1 is set for a no-signal level of +18V. The emitter resistors, R_E, were selected to give the cascode amplifier a differential gain of 10. The gain of the composite amplifier is adjusted at the gain selected point of the NE592.

Filters

As mentioned earlier, the emitter circuit of the NE592 includes two current sources.

Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 3, the overall gain at low frequencies is a negative 48dB.

Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB, or unity.

Referring to Figure 4, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA, causing the quantity of 2 r_e to be approximately 32Ω. Overall device gain is thus given by

$$\frac{V_O(s)}{V_{IN}(s)} = \frac{1.4 \times 10^4}{Z_{(S)} + 32} \qquad (2)$$

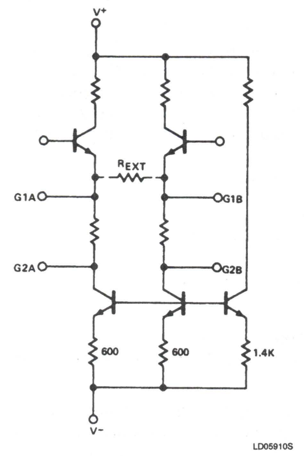
where $Z_{(S)}$ can be resistance or a reactive impedance. Table 2 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 2 is the gain calculation to determine the voltage gain as a function of frequency.

Table 1. Video Amplifier Comparison File

PARAMETER	NE/SE592	733
Bandwidth (MHz)	120	120
Gain	0,100,400	10,100,400
R_{IN} (k)	4 – 30	4 – 250
V_{P-P} (Vs)	4.0	4.0

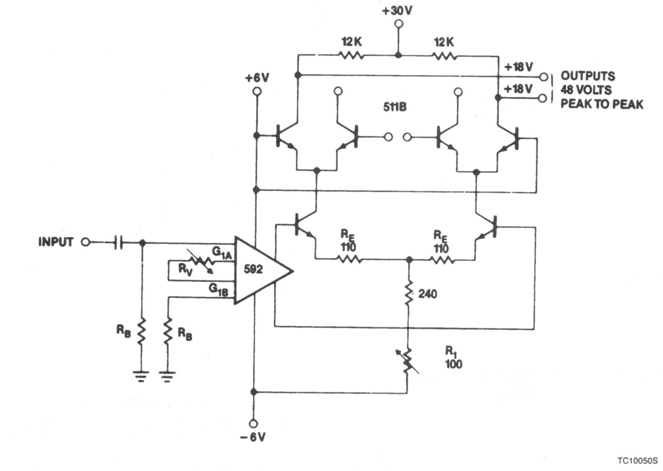
Using the NE/SE592 Video Amplifier

AN141



NOTE:
All resistor values are in ohms.

Figure 1. 592 Input Structure



NOTE:
All resistor values are in ohms.

Figure 2. Video Amplifier With High Level Differential Output

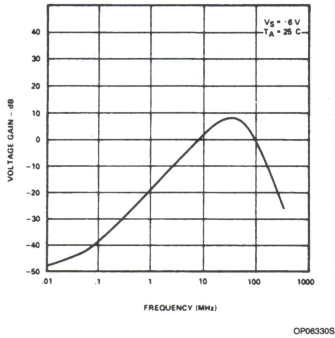
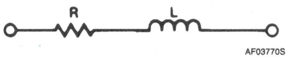
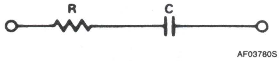
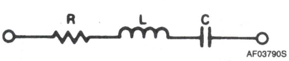
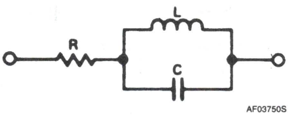


Figure 3. Voltage Gain as a Function of Frequency (All Gain Select Pins Open)

Table 2. Filter Networks

Z NETWORK	FILTER TYPE	$\frac{V_O(s)}{V_1(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE: In the networks above, the R value used is assumed to include 2 r_e, or approximately 32Ω.

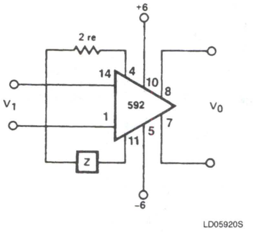
Differentiation

With the addition of a capacitor across the gain select terminals, the NE592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common-mode rejection for proper operation. Figure 5 shows a differential amplifier configuration with transfer function.

Disc File Decoding

In recovering data from disc or drum files, several steps must be taken to precondition the linear data. The NE592 video amplifier, coupled with the 8T20 bidirectional one-shot, provides all the signal conditioning necessary for phase-encoded data.

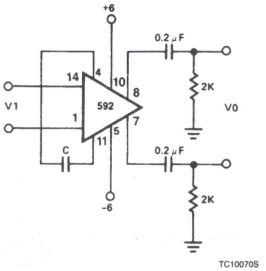
When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV_{P-P} to 3mV_{P-P} for oxide coated disc files and 1 to 20mV_{P-P} for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.


+6
2 re
14
4
10
8
V1
592
Vo
1
5
7
11
Z
-6
LD05920S

NOTE:

$$\frac{V_0(s)}{V_1(s)} = \frac{1.4 \times 10^4}{Z(s) + 2re} = \frac{1.4 \times 10^4}{Z(s) + 32}$$

Figure 4. Basic Gain Configuration for NE592, N14


+6
0.2 μF
14
4
10
8
2K
V1
592
V0
1
5
7
11
C
0.2 μF
-6
2K
TC10070S

NOTES:

For frequency $F_1 << 1/2\pi(32)C$

$V_0 \cong 1.4 \times 10^4 C \frac{d_{vi}}{dT}$

All resistor values are in ohms.

Figure 5. Differential With High Common-Mode Noise Rejection

The classical approach to peak time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the preconditioning described above is shown in Figure 6. Readback data is applied directly to the input of the first NE592. This amplifier functions as a wide-band AC-coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common-mode rejection ratio of the amplifier is preserved. DC components are also rejected because the NE592 has no gain at DC due to the capacitance across the gain select terminals.

The output of the first stage amplifier is routed to a linear phase shift low-pass filter. The filter is a single-stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$$L = {}^{2R}\!/_{\omega_C}$$

where
R = characteristic impedance (Ω)

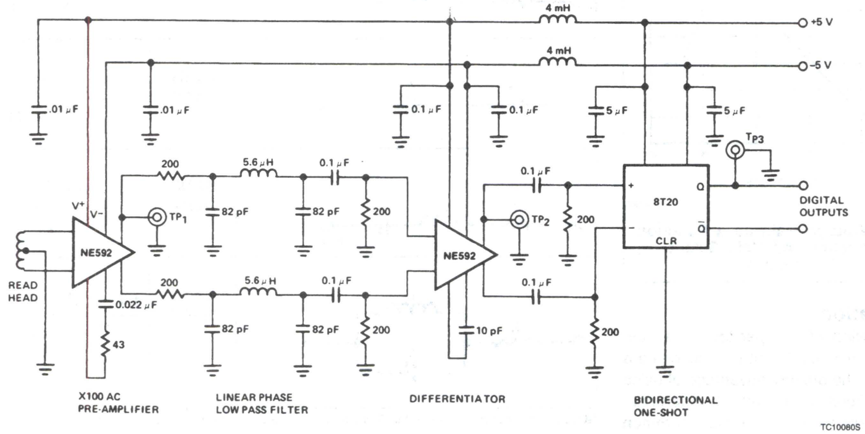
$$C = {}^{1}\!/_{\omega_C}$$

where
ω_C = cut-off frequency (radians/sec)

The second NE592 is utilized as a low noise differentiator/amplifier stage. The NE592 is excellent in this application because it allows differentiation with excellent common-mode noise rejection.

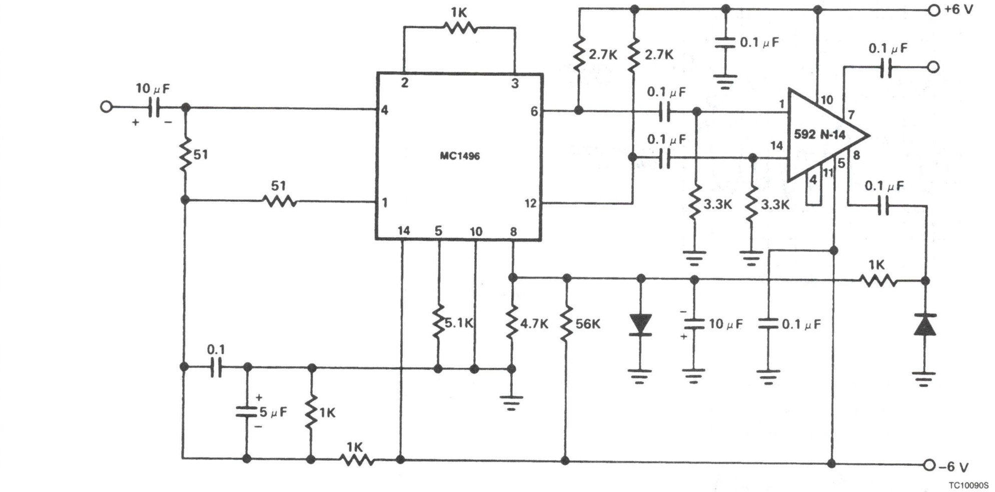
The output of the differentiator/amplifier is connected to the 8T20 bidirectional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 6 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 8.


4 mH
+5 V
4 mH
-5 V
.01 μF
.01 μF
0.1 μF
0.1 μF
5 μF
5 μF
TP3
200
5.6 μH
0.1 μF
0.1 μF
V+
V-
TP1
82 pF
82 pF
200
TP2
200
8T20
Q
Q̄
CLR
DIGITAL OUTPUTS
NE592
NE592
READ HEAD
200
5.6 μH
0.1 μF
0.1 μF
0.022 μF
82 pF
82 pF
200
10 pF
200
43
X100 AC PRE-AMPLIFIER
LINEAR PHASE LOW PASS FILTER
DIFFERENTIATOR
BIDIRECTIONAL ONE-SHOT
TC10080S

NOTE:
All resistor values are in ohms

Figure 6. 5MHz Phase-Encoded Data Read Circuitry


1K
2.7K
2.7K
0.1 μF
+6 V
0.1 μF
10 μF
+
−
2
3
4
6
0.1 μF
1
10
7
592 N-14
14
8
0.1 μF
51
MC1496
51
1
12
4
11
5
0.1 μF
3.3K
3.3K
14
5
10
8
1K
5.1K
4.7K
56K
10 μF
0.1 μF
0.1
5 μF
1K
1K
−6 V
TC10090S

NOTE:
All resistor values are in ohms

Figure 7. Wide-Band AGC Amplifier

Automatic Gain Control

The NE592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system.

The signal is fed to the signal input of the MC1496 and RC-coupled to the NE592. Unbalancing the carrier input of the MC1496 causes the signal to pass through unattenuated. Rectifying and filtering one of the NE592 outputs produces a DC signal which is proportional to the AC signal amplitude. After filtering; this control signal is applied to the MC1496 causing its gain to change.

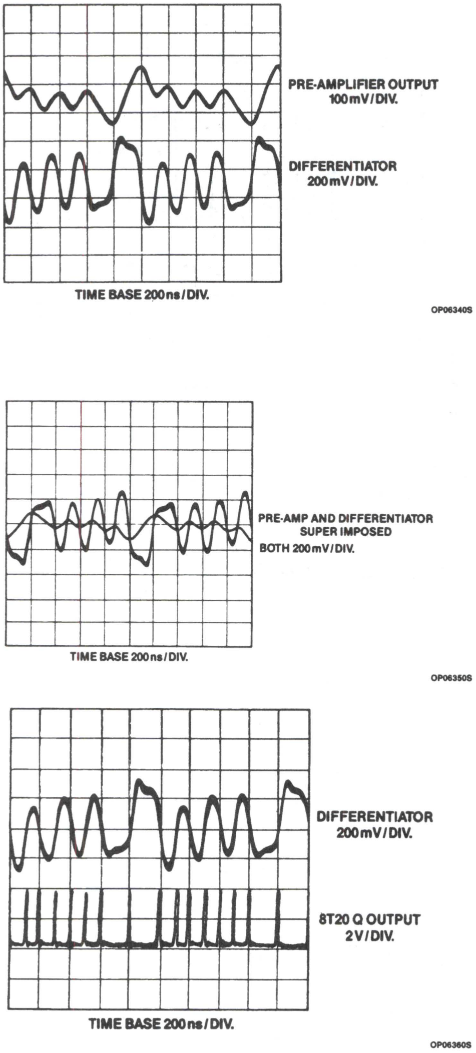


Figure 8. Test Results of Disc File Decoder Circuit

Signetics

μA733/733C
Differential Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

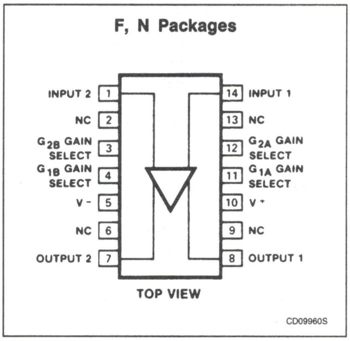
FEATURES

- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10, 100, and 400**
- **No frequency compensation required**
- **MIL-STD-883A, B, C available**

APPLICATIONS

- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memories**
- **Video recorder systems**

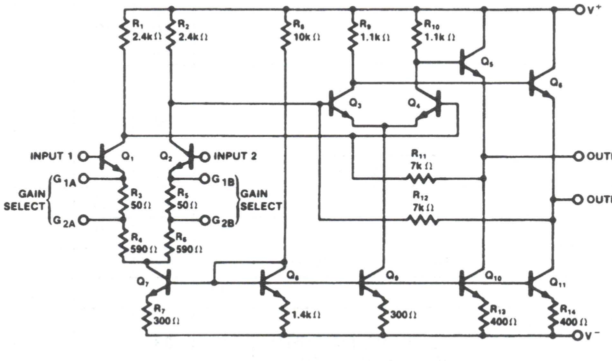
PIN CONFIGURATION


F, N Packages
INPUT 2 1
NC 2
G2B GAIN SELECT 3
G1B GAIN SELECT 4
V- 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G2A GAIN SELECT
11 G1A GAIN SELECT
10 V+
9 NC
8 OUTPUT 1
TOP VIEW
CD09960S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
14-Pin Ceramic DIP	−55°C to +125°C	μA733F
14-Pin Plastic DIP	−55°C to +125°C	μA733N
14-Pin Plastic DIP	0 to +70°C	μA733CN
14-Pin Ceramic DIP	0 to +70°C	μA733CF

CIRCUIT SCHEMATIC


V+
R1 2.4kΩ
R2 2.4kΩ
R8 10kΩ
R9 1.1kΩ
R10 1.1kΩ
Q5
Q6
Q3
Q4
INPUT 1
Q1
Q2
INPUT 2
R11 7kΩ
OUTPUT 1
GAIN SELECT
G1A
G2A
R3 50Ω
R4 590Ω
R5 50Ω
R6 590Ω
G1B
G2B
GAIN SELECT
R12 7kΩ
OUTPUT 2
Q7
Q8
Q9
Q10
Q11
R7 300Ω
1.4kΩ
300Ω
R13 400Ω
R14 400Ω
V−
TC08980S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range μA733C μA733	 0 to +70 -55 to +125	 °C °C
P_{MAX}	Maximum power dissipation[1] 25°C ambient temperature (still-air) F package N package	 1190 1420	 mW mW

NOTE:

1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C.

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain Gain 1[2] Gain 2[2] Gain 3[3]	$R_l = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	 250 80 8	 400 100 10	 600 120 12	 300 90 9	 400 100 10	 500 110 11	 V/V V/V V/V
BW	Bandwidth Gain 1[1] Gain 2[2] Gain 3[3]			 40 90 120			 40 90 120		 MHz MHz MHz
t_R	Rise time Gain 1[1] Gain 2[2] Gain 3[3]	$V_{OUT} = 1V_{P-P}$		 10.5 4.5 2.5	 12 		 10.5 4.5 2.5	 10 	 ns ns ns
t_{PD}	Propagation delay Gain 1[1] Gain 2[2] Gain 3[3]	$V_{OUT} = 1V_{P-P}$		 7.5 6.0 3.6	 10 		 7.5 6.0 3.6	 10 	 ns ns ns
R_{IN}	Input resistance Gain 1[2] Gain 2[2] Gain 3[3]		 10 	 4.0 30 250		 20 	 4.0 30 250		 kΩ kΩ kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW = 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2 Gain 2	 $V_{CM} = \pm 1V$, $f \leqslant 100kHz$ $V_{CM} = \pm 1V$, $f = 5MHz$	 60 	 86 60		 60 	 86 60		 dB dB
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB

Differential Video Amplifier

µA733/733C

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$.

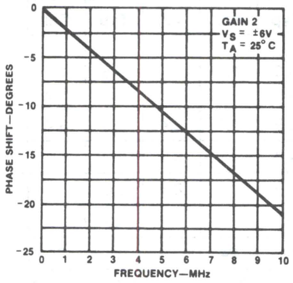
SYMBOL	PARAMETER	TEST CONDITIONS	µA733C			µA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$		 0.6 0.35	 1.5 1.5		 0.6 0.35	 1.5 1.0	 V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			**$0°C \leq T_A \leq 70°C$**			**$-55°C \leq T_A \leq 125°C$**			
	Differential voltage gain Gain 1[1] Gain 2[2] Gain[3]	$R_l = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	 250 80 8		 600 120 12	 200 80 8		 600 120 12	 V/V V/V V/V
R_{IN}	Input resistance Gain 2[2]		 8			 8			 kΩ
I_{OS}	Input offset current				6			5	µA
I_{BIAS}	Input bias current				40			40	µA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2	 $V_{CM} = \pm V$, $F \leq 100kHz$		 50			 50		 dB
SVRR	Supply voltage rejection ratio Gain 2	 $\Delta V_S = \pm 0.5V$	 50			 50			 dB
V_{OS}	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$			 1.5 1.5			 1.5 1.2	 V V
V_{DIFF}	Output voltage swing, differential	$R_L = 2k\Omega$	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

NOTES:

1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

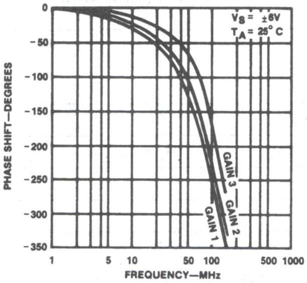
TYPICAL PERFORMANCE CHARACTERISTICS

Phase Shift as a Function of Frequency



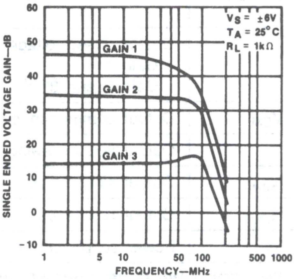
OP05620S

Phase Shift as a Function of Frequency



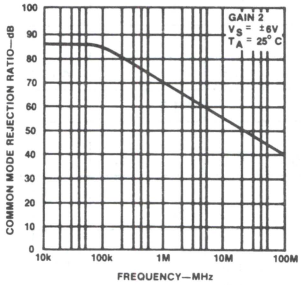
OP05630S

Voltage Gain as a Function of Frequency



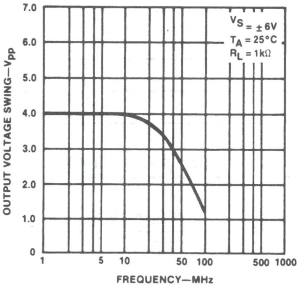
OP05640S

Common Mode Rejection Ratio as a Function of Frequency



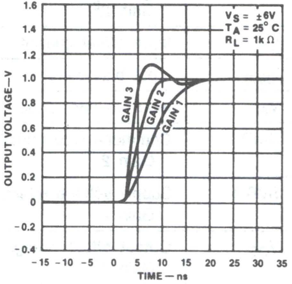
OP05650S

Output Voltage Swing as a Function of Frequency



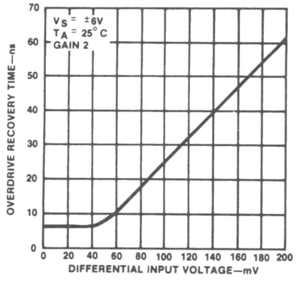
OP05660S

Pulse Response



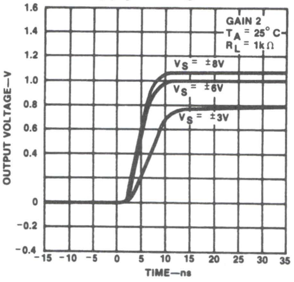
OP05670S

Differential Overdrive Recovery Time



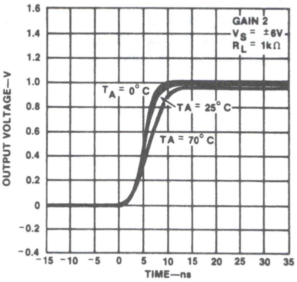
OP05680S

Pulse Response as a Function of Supply Voltage



OP05690S

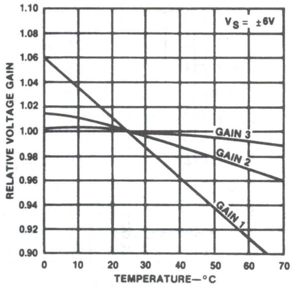
Pulse Response as a Function Of Temperature



OP05700S

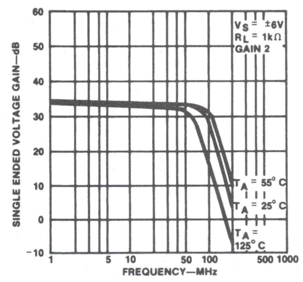
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Voltage Gain as a Function of Temperature



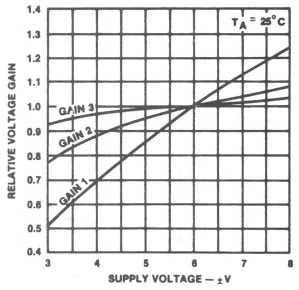
OP05710S

Gain vs Frequency as a Function of Temperature



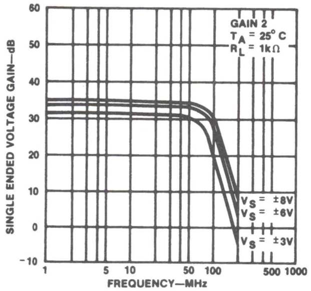
OP05720S

Voltage Gain as a Function of Supply Voltage



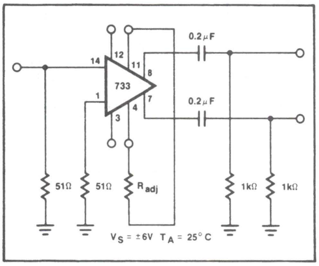
OP05730S

Gain vs Frequency as a Function of Supply Voltage



OP05740S

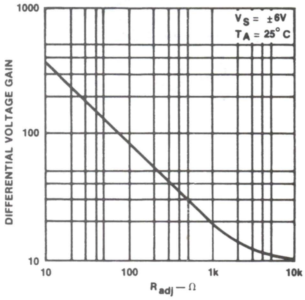
Voltage Gain Adjust Circuit



(Pin numbers apply to K Package)

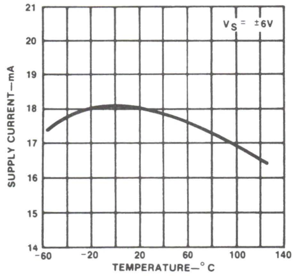
OP05750S

Voltage Gain as a Function of RADJ (Figure 3)



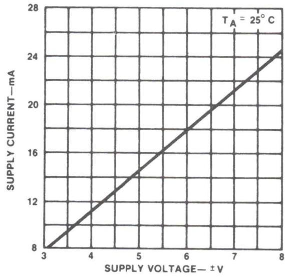
OP05760S

Supply Current as a Function of Temperature



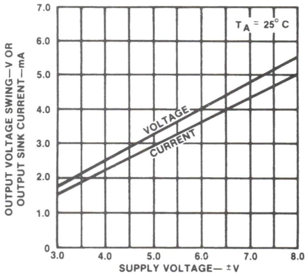
OP05770S

Supply Current as a Function of Supply Voltage



OP05780S

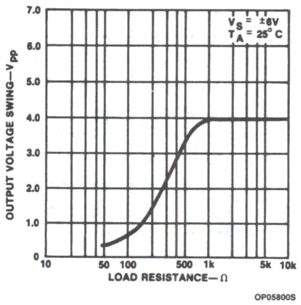
Output Voltage and Current Swing as a Function of Supply Voltage



OP05790S

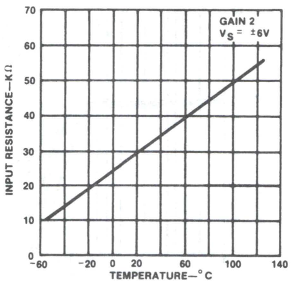
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Output Voltage Swing as a Function of Load Resistance



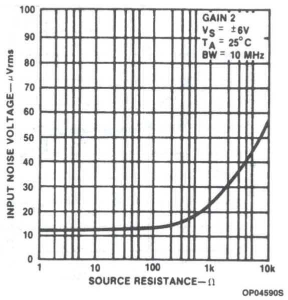
OP05800S

Input Resistance as a Function of Temperature



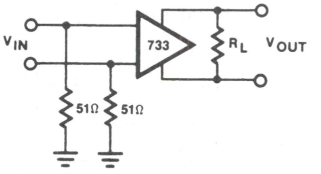
OP05810S

Input Noise Voltage as a Function of Source Resistance

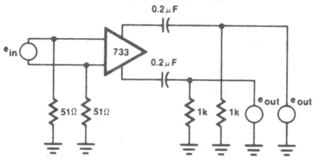


OP04590S

TEST CIRCUITS T_A = 25°C, unless otherwise specified.


VIN
733
RL
VOUT
51Ω
51Ω

TC08990S


0.2μF
0.2μF
ein
733
51Ω
51Ω
1k
1k
eout
eout

TC09000S

Signetics

NE5517/5517A
Dual Operational Transconductance Amplifier

Preliminary Specification

Linear Products

DESCRIPTION

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

Constant impedance buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistor and a biasing network which changes bias current in dependence of I_{ABC}.

Therefore, changes of output offset voltages are almost eliminated. This is an advantage of the NE5517 compared to LM13600. With the LM13600, a burst in the bias current I_{ABC} guides to an audible offset voltage change at the output. With the constant impedance buffers of the NE5517 this effect can be avoided and makes this circuit preferable for high quality audio applications.

FEATURES

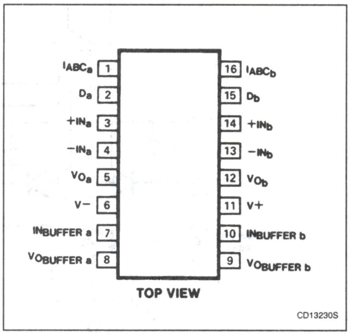
- **Constant impedance buffers**
- **ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change**
- **Pin compatible with LM13600**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **High output signal-to-noise ratio**

APPLICATIONS

- **Multiplexers**
- **Timers**
- **Electronic music synthesizers**
- **Dolby^{TM} HX Systems**
- **Current-controlled amplifiers, filters**
- **Current-controlled oscillators, impedances**

Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

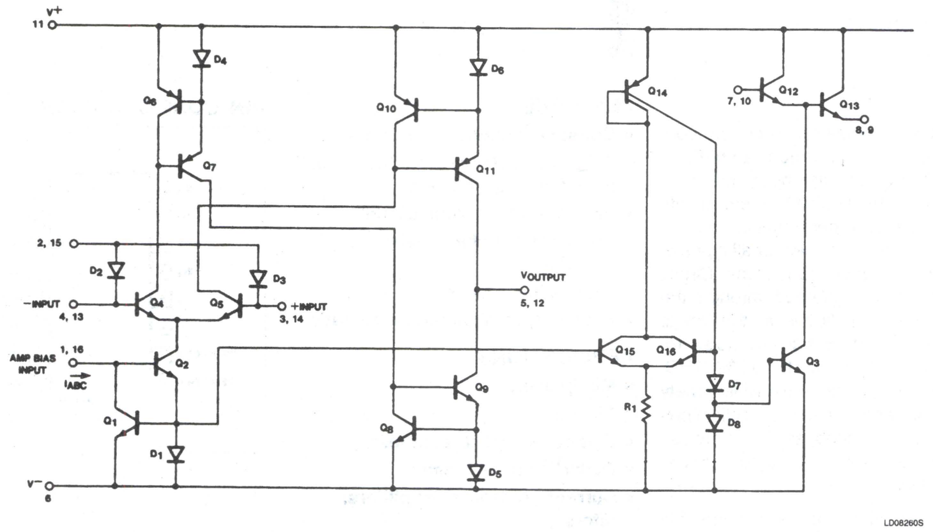
PIN CONFIGURATION



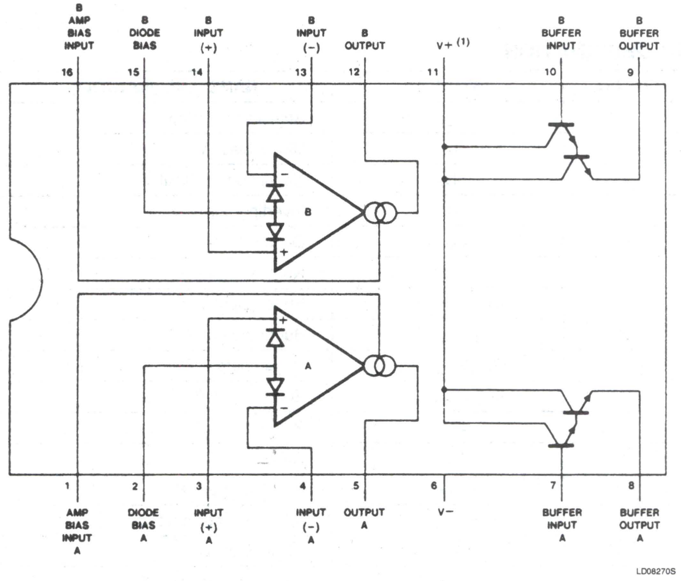
PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	V_{oa}	Output A
6	V−	Negative supply
7	$IN_{BUFFER\ (A)}$	Buffer input A
8	$VO_{BUFFER\ (A)}$	Buffer output A
9	$VO_{BUFFER\ (B)}$	Buffer output B
10	$IN_{BUFFER\ (B)}$	Buffer input B
11	V+	Positive supply
12	V_{OB}	Output B
13	$-IN_B$	Inverting input B
14	$+IN_B$	Non-inverting input B
15	D_B	Diode Bias B
16	I_{ABCB}	Amplifier bias input B

CIRCUIT SCHEMATIC


V+
11
D4
Q6
Q7
D6
Q10
Q11
Q14
Q12
Q13
7, 10
8, 9
2, 15
D2
D3
−INPUT
4, 13
Q4
Q5
+INPUT
3, 14
VOUTPUT
5, 12
AMP BIAS INPUT
1, 16
IABC
Q2
Q15
Q16
Q3
D7
D8
R1
Q9
Q8
Q1
D1
D5
V−
6
LD08260S

CONNECTION DIAGRAM


B AMP BIAS INPUT
B DIODE BIAS
B INPUT (+)
B INPUT (−)
B OUTPUT
V+ (1)
B BUFFER INPUT
B BUFFER OUTPUT
16
15
14
13
12
11
10
9
B
A
1
2
3
4
5
6
7
8
AMP BIAS INPUT A
DIODE BIAS A
INPUT (+) A
INPUT (−) A
OUTPUT A
V−
BUFFER INPUT A
BUFFER OUTPUT A
LD08270S

NOTE:
1. V_+ of output buffers and amplifiers are internally connected.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE5517N
16-Pin Plastic DIP	0 to +70°C	NE5517AN
16-Pin SOL DIP	0 to +70°C	NE5517D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage[1]		
	NE5517	36 V_{DC} or ±18	V
	NE5517A	44 V_{DC} or ±22	V
P_D	Power dissipation, $T_A = 25°C$[2]		
	NE5517N, NE5517AN	570	mW
V_{IN}	Differential input voltage	±5	V
I_D	Diode bias current	2	mA
I_{ABC}	Amplifier bias current	2	mA
I_{SC}	Output short-circuit duration	Indefinite	
I_{OUT}	Buffer output current[3]	20	mA
T_A	Operating temperature range		
	NE5517N, NE5517AN	0°C to +70	°C
V_{DC}	DC input voltage	$+V_S$ to $-V_S$	
T_{STG}	Storage temperature range	−65°C to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.

DC ELECTRICAL CHARACTERISTICS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage			0.4	5		0.4	2	mV
		Over temperature range						5	mV
		I_{ABC} 5μA		0.3	5		0.3	2	mV
	$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage		7			7		μV/°C
	V_{OS} including diodes	Diode bias current (I_D) = 500μA		0.5	5		0.5	2	mV
V_{OS}	Input offset change	$5\mu A \leqslant I_{ABC} \leqslant 500\mu A$		0.1			0.1	3	mV
I_{OS}	Input offset current			0.1	0.6		0.1	0.6	μA
	$\Delta I_{OS}/\Delta T$	Avg. TC of input offset current		0.001			0.001		μA/°C
I_{BIAS}	Input bias current	Over temperature range		0.4 1	5 8		0.4 1	5 7	μA μA
	$\Delta I_B/\Delta T$	Avg. TC of input current		0.01			0.01		μA/°C

DC ELECTRICAL CHARACTERISTICS[1] (Continued)

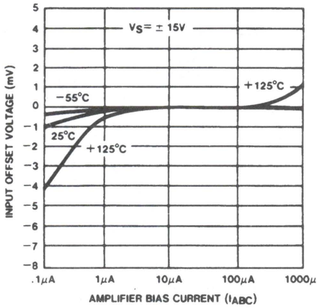
SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
g_M	Forward transconductance	Over temperature range	6700 5400	9600	13000	7700 4000	9600	12000	μmho μmho
	g_M tracking			0.3			0.3		dB
I_{OUT}	Peak output current	$R_L = 0$, $I_{ABC} = 5\mu A$		5		3	5	7	μA
		$R_L = 0$, $I_{ABC} = 500\mu A$	350	500	650	350	500	650	μA
		$R_L = 0$,	300			300			μA
V_{OUT}	Peak output voltage								
	Positive	$R_L = \infty$, $5\mu A \leqslant I_{ABC} \leqslant 500\mu A$	+12	+14.2		+12	+14.2		V
	Negative	$R_L = \infty$, $5\mu A \leqslant I_{ABC} \leqslant 500\mu A$	−12	−14.4		−12	−14.4		V
I_S	Supply current	$I_{ABC} = 500\mu A$, both channels		2.6	4		2.6	4	mA
	V_{OS} sensitivity								
	Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
	Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR	Common-mode rejection ration		80	110		80	110		dB
	Common-mode range		±12	±13.5		±12	±13.5		V
	Crosstalk	Referred to input[2] $20Hz < f < 20kHz$		100			100		dB
I_{IN}	Differential input current	$I_{ABC} = 0$, input = ±4V		0.02	100		0.02	10	nA
	Leakage current	$I_{ABC} = 0$ (Refer to test circuit)		0.2	100		0.2	5	nA
R_{IN}	Input resistance		10	26		10	26		kΩ
B_W	Open-loop bandwidth			2			2		MHz
SR	Slew rate	Unity gain compensated		50			50		V/μs
IN_{BUFFER}	Buff. input current	5		0.4	5		0.4	5	μA
VO_{BUFFER}	Peak buffer output voltage	5	10			10			V
	ΔV_{BE} of buffer	Refer to Buffer V_{BE} test[3] circuit		0.5	5		0.5	5	mV

NOTES:

1. These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
2. These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\mu A$, $R_{OUT} = 5k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
3. $V_S = \pm 15$, $R_{OUT} = 5k\Omega$ connected from Buffer output to $-V_S$ and $5\mu A \leqslant I_{ABC} \leqslant 500\mu A$.

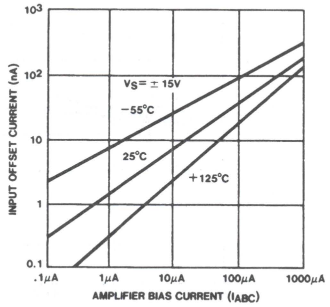
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage



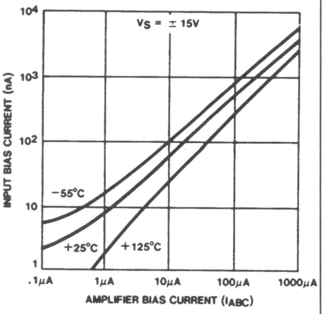
OP19330S

Input Offset Current



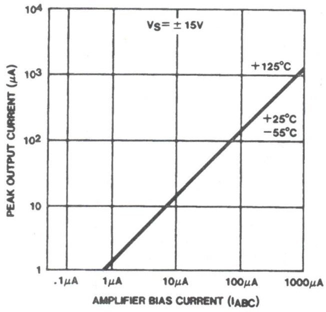
OP19340S

Input Bias Current



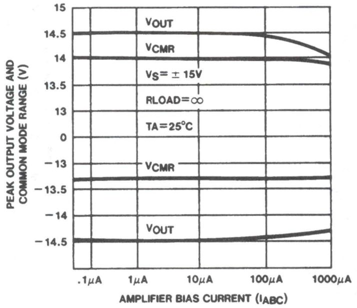
OP1935

Peak Output Current



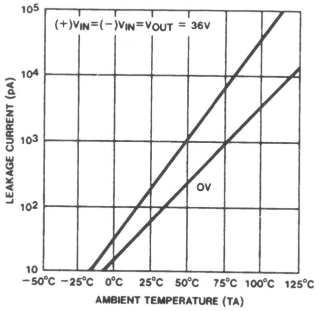
OP19360S

Peak Output Voltage and Common-Mode Range



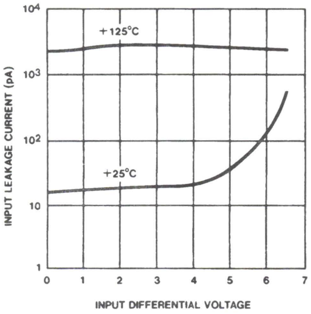
OP19370S

Leakage Current



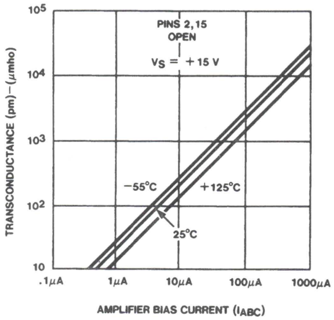
OP19380

Input Leakage



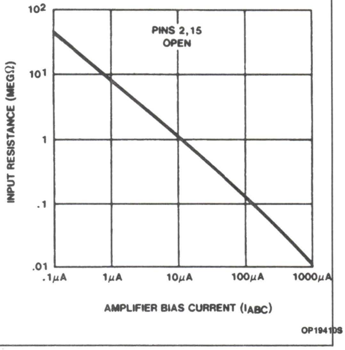
OP19390S

Transconductance



OP19400S

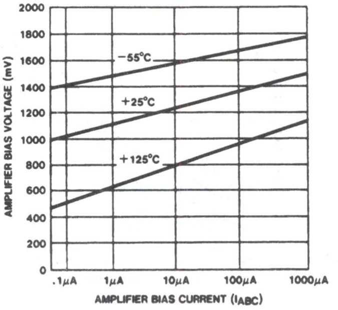
Input Resistance



OP1941

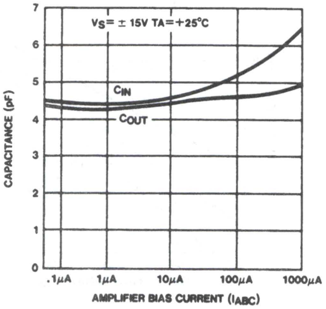
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Amplifier Bias Voltage vs Amplifier Bias Current



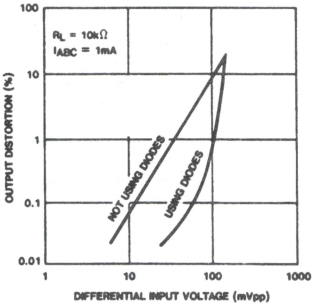
OP19420S

Input and Output Capacitance



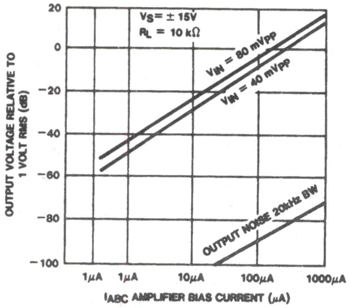
OP19430S

Distortion vs Differential Input Voltage



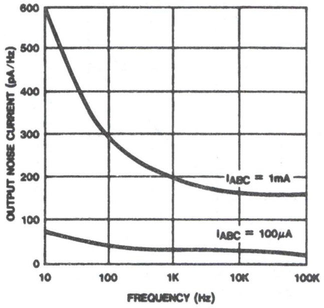
OP194

Voltage vs Amplifier Bias Current



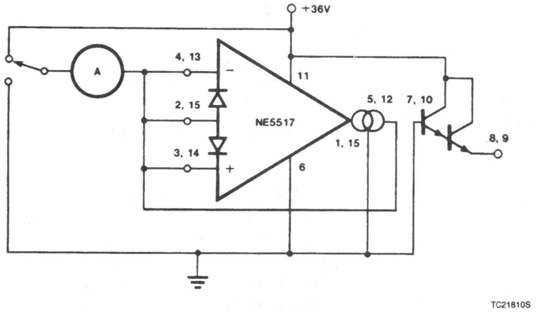
OP19460S

Output Noise vs Frequency

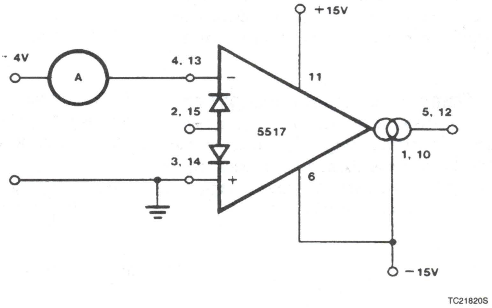


O19460S

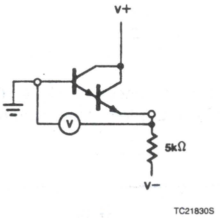
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)


+36V
A
4, 13
2, 15
3, 14
NE5517
11
5, 12
7, 10
1, 15
6
8, 9
TC21810S

Leakage Current Test Circuit

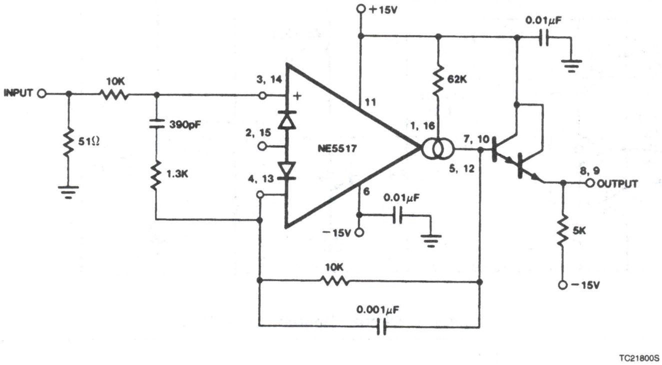

+15V
- 4V
A
4, 13
2, 15
3, 14
5517
11
6
5, 12
1, 10
−15V
TC21820S

Differential Input Current Test Circuit


V+
V
5kΩ
V−
TC21830S

Buffer V_{BE} Test Circuit

APPLICATIONS


+15V
0.01μF
INPUT
10K
51Ω
390pF
1.3K
3, 14
2, 15
4, 13
NE5517
11
62K
1, 16
7, 10
5, 12
6
0.01μF
−15V
8, 9
OUTPUT
5K
−15V
10K
0.001μF
TC21800S

Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 1.

1. Transconductance Amplifier

The transistor pair, Q_4 and Q_5, forms a transconductance stage. The ratio of their collector currents (I_4 and I_5, respectively) is defined by the differential input voltage, V_{IN}, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \tag{1}$$

Where V_{IN} is the difference of the two input voltages

$KT \cong 26mV$ at room temperature (300°K).

Transistors Q_1, Q_2 and diode D_1 form a current mirror which focuses the sum of current I_4 and I_5 to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \tag{2}$$

If V_{IN} is small, the ratio of I_5 and I_4 will approach to unity and the Taylor series of In function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \tag{3}$$

and $I_4 \approx I_5 \approx \frac{1}{2} I_B$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{\frac{1}{2} I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN}$$

$$I_5 - I_4 = V_{IN} \frac{(I_B q)}{2KT} \tag{4}$$

The remaining transistors (Q_6 to Q_{11}) and diodes (D_4 to D_6) form three current mirrors that produce an output current equal to I_5 minus I_4. Thus:

$$V_{IN} \left\{ I_B \frac{q}{2KT} \right\} = I_O \tag{5}$$

The term $\frac{(I_B q)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

2. Linearizing Diodes

For V_{IN} greater than a few millivolts, equation 3 becomes invalid and the transconductance increases nonlinearly. Figure 2 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S. Since

$I_4 + I_5 = I_B$ and $I_5 - I_4 = I_O$, that is:

$I_4 = \frac{1}{2}(I_B - I_O)$, $I_5 = \frac{1}{2}(I_B + I_O)$

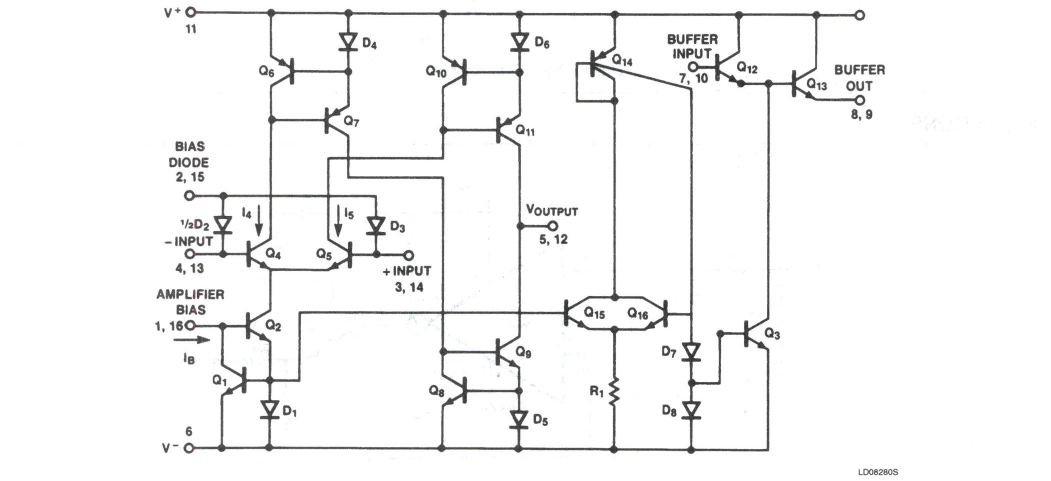


Figure 1. Circuit Diagram of NE5517

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q}\ \ln \frac{\frac{I_D}{2}+I_S}{\frac{I_D}{2}-I_s} = \frac{KT}{q}\ \ln \frac{\frac{1}{2}(I_B+I_0)}{\frac{1}{2}(I_B-I_0)}$$

$$I_0 = I_S\frac{(2^{I}B)}{I_D} \quad \text{for} \quad |I_S| < \frac{I_D}{2} \qquad (6)$$

The only limitation is that the signal current should not exceed ½ I_D.

3. Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14}, Q_{15}, Q_{16}, D_7, D_8, and R_1) suits the need.

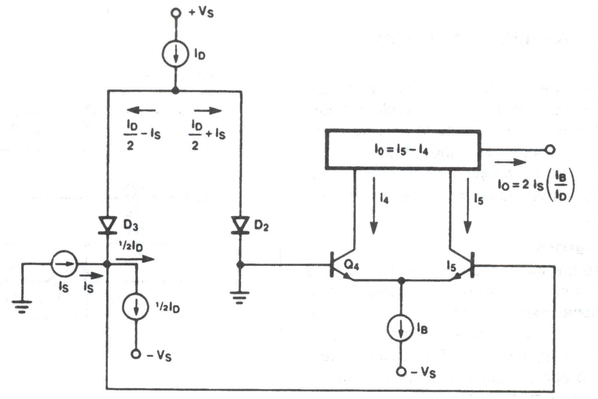


Figure 2. Linearizing Diode

APPLICATIONS

Voltage-Controlled Amplifier

The voltage divider R_2, R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \times \frac{R_3}{R_2+R_3} \times g_M;$$

$$V_{OUT} = I_{OUT} \times R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2+R_3}\ g_M\ R_L;$$

$$\boxed{A = \frac{R_3}{R_2+R_3} \times g_M \times R_L}$$

(3) $g_M = 19.2\ I_{ABC}$

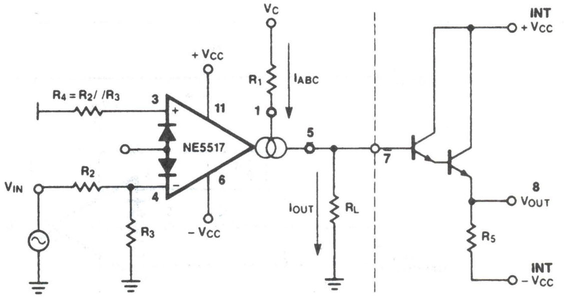
(g_M in ms for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2V is the voltage across two base-emitter baths in the current mirrors. This



TYPICAL VALUES: $R_1 = 47K$
$R_2 = 10K$
$R_3 = 200\Omega$
$R_4 = 200\Omega$
$R_1 = 100K$
$R_5 = 47K$

Figure 3

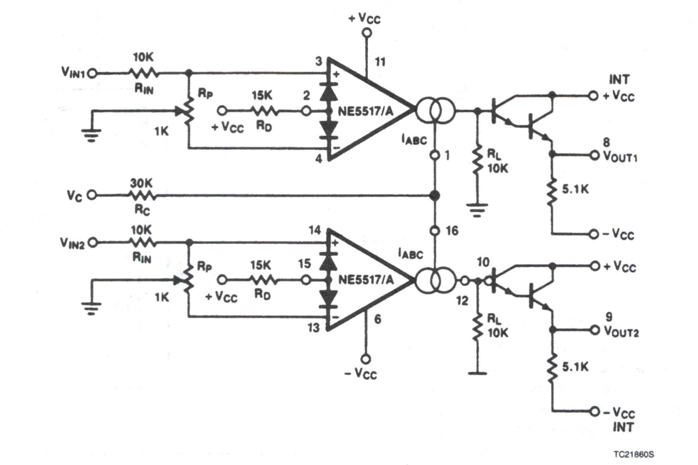
circuit is the base for many applications of the NE5517.

Stereo Amplifier With Gain Control

Figure 4 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3dB is easy to achieve. With the potentiometer, R_P, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 5.1kΩ resistors.

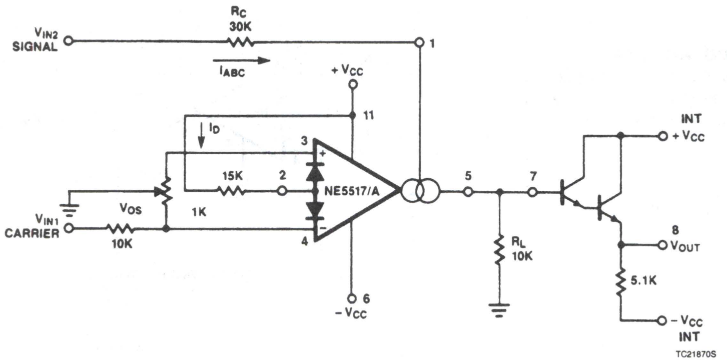
Modulators

Because the transconductance of an OTA is directly proportional to I_{ABC}, the amplification of a signal can be controlled easily. The output current is the product from transconductance × input voltage. The circuit is effective up to approximately 200kHz. Modulation of 99% is easy to achieve.



+Vcc
VIN1
10K
RIN
RP
15K
+Vcc
RD
1K
NE5517/A
IABC
RL
10K
INT
+Vcc
8
VOUT1
5.1K
-Vcc
VC
30K
RC
VIN2
10K
RIN
RP
15K
+Vcc
RD
1K
NE5517/A
IABC
RL
10K
+Vcc
9
VOUT2
5.1K
-Vcc
INT
-Vcc
1
2
3
4
6
10
11
12
13
14
15
16
TC21860S

Figure 4. Gain-Controlled Stereo Amplifier



VIN2
SIGNAL
RC
30K
IABC
+Vcc
ID
15K
1K
VOS
VIN1
CARRIER
10K
NE5517/A
1
2
3
4
5
6
7
11
-Vcc
RL
10K
INT
+Vcc
8
VOUT
5.1K
-Vcc
INT
TC21870S

Figure 5. Amplitude Modulator

Voltage-Controlled Resistors (VCR)

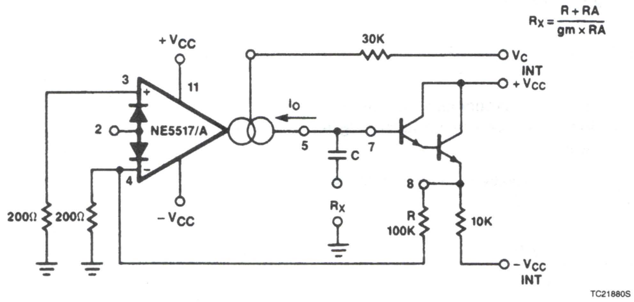
This principle is based on the capability of an OTA to vary a current proportional to a controlled voltage, according to a resistor. The circuit takes advantage of the possibility to control a resistor via g_M.

Voltage-Controlled Filters

Voltage-controlled filters can be realized extremely easily with the help of an OTA.

Figure 8 shows the circuit for a low-pass filter. Below the corner frequency the circuit has an amplification of 0dB. Above the corner frequency the attenuation drops by 6dB/octave.

The high-pass filter is built in a similar manner, except the input is coupled via capacitor.



RX = (R + RA)/(gm × RA)
+Vcc
30K
VC
INT
+Vcc
NE5517/A
IO
C
RX
R
100K
10K
-Vcc
INT
200Ω
200Ω
-Vcc
2
3
4
5
7
8
11
TC21880S

Figure 6. VCR

Voltage-Controlled Oscillators

Figure 12 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2Hz to 200kHz is possible by varying I_{ABC} from 1mA to 10μA.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 13.

Programmable Amplifier

The intention of the following application is to show how the NE5517 works in connection with a DAC. Almost all applications described above can be made digitally-programmable (μP-compatible) in this way.

In the application of Figure 14, the NE5118 is used — an 8-bit DAC with current output — its input register making this device fully μP-compatible.

The circuitry of Figure 14 consists of three functional blocks: the NE5118 which generates a control current equivalent to the applied data byte, a current mirror, and the NE5517.

The amplification is given by the following equation:

$$A = \frac{DW\ (10)}{256} \times \frac{I_{DAC\ MAX}}{2 \times V_T} \times R_L$$

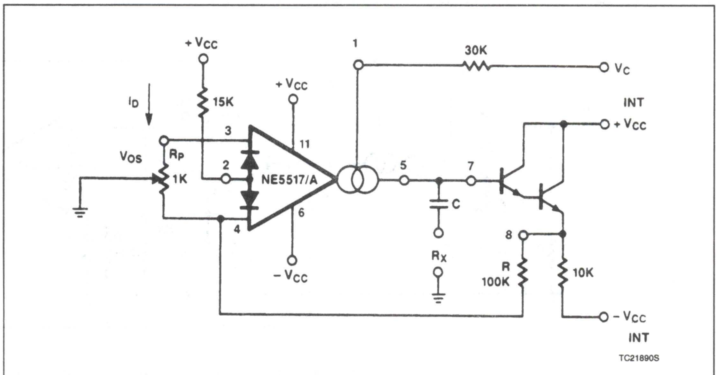
DW (10)	= Data word decimal
$I_{DAC\ MAX}$	= Maximum DAC output current (here −1mA)
R_L	= Load resistance

The equation is only valid for the amplification of the signal directly applied to the OTA. To get the gain overall, A must be multiplied with the input attenuation factor.

APPLICATION HINTS

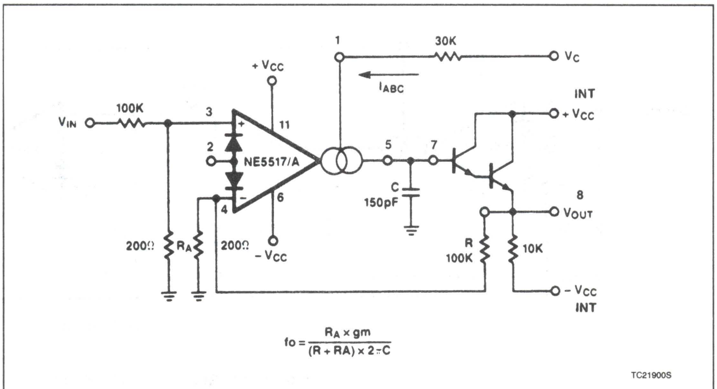
To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to −2mA. In this application, however, the current range is set through R_{REF} (10kΩ) to 0 to −1mA.

$$I_{DAC\ MAX} = 2 \times \frac{V_{REF}}{R_{REF}} = 2 \times \frac{5V}{10k} = 1mA$$



+Vcc
1
30K
Vc
+Vcc
ID
15K
INT
+Vcc
3
11
VOS
RP
1K
2
NE5517/A
5
7
C
6
4
8
RX
R
100K
10K
−Vcc
−Vcc
INT
TC21890S

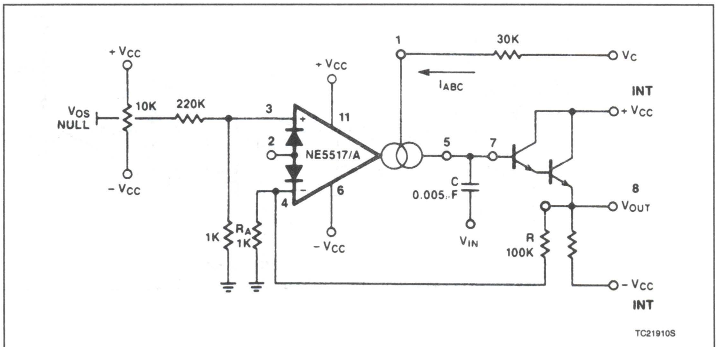
Figure 7. VCR With Linearizing Diodes



1
30K
Vc
+Vcc
IABC
INT
VIN
100K
3
11
+Vcc
2
NE5517/A
5
7
C
150pF
8
VOUT
4
6
200Ω
RA
200Ω
−Vcc
R
100K
10K
−Vcc
INT
TC21900S

$$fo = \frac{R_A \times gm}{(R + RA) \times 2\pi C}$$

Figure 8. Voltage-Controlled Low-Pass Filter



+Vcc
1
30K
Vc
+Vcc
IABC
INT
+Vcc
VOS
NULL
10K
220K
3
11
2
NE5517/A
5
7
−Vcc
C
0.005μF
8
VOUT
4
6
1K
RA
1K
−Vcc
VIN
R
100K
−Vcc
INT
TC21910S

Figure 9. Voltage-Controlled High-Pass Filter

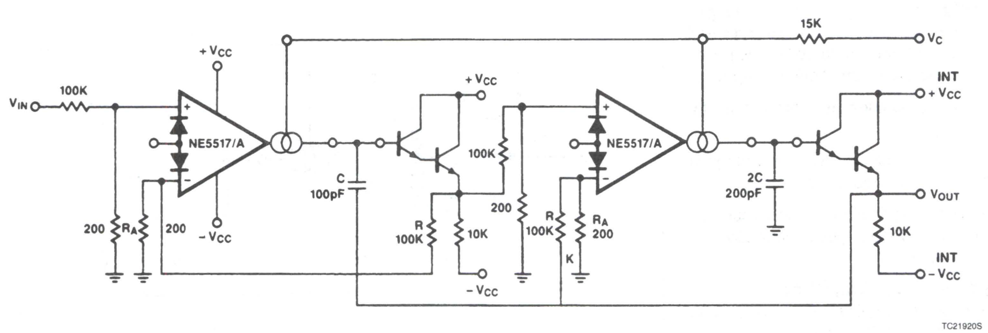

VIN
100K
+VCC
NE5517/A
200
RA
200
-VCC
C
100pF
+VCC
100K
R
100K
10K
-VCC
200
R
100K
RA
200
K
NE5517/A
15K
VC
2C
200pF
INT
+VCC
VOUT
10K
INT
-VCC
TC21920S

Figure 10. Butterworth Filter — 2nd Order

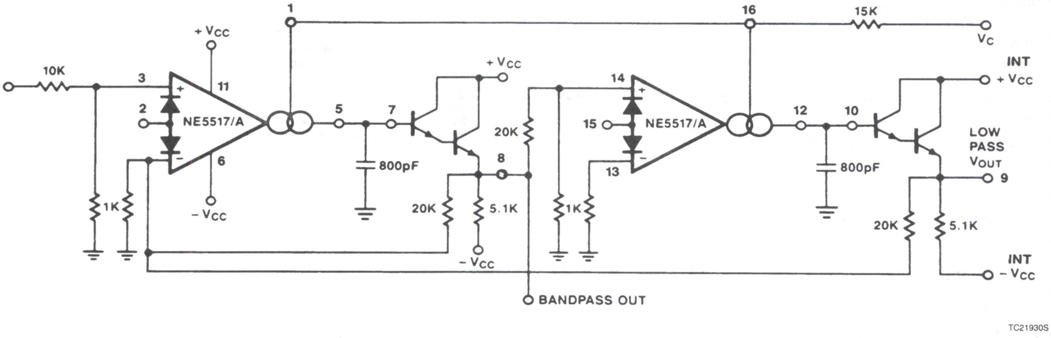

10K
3
2
+VCC
11
NE5517/A
6
-VCC
1K
1
5
7
800pF
+VCC
8
20K
20K
5.1K
-VCC
BANDPASS OUT
14
15
NE5517/A
13
1K
16
15K
VC
12
10
800pF
INT
+VCC
LOW
PASS
VOUT
9
20K
5.1K
INT
-VCC
TC21930S

Figure 11. State Variable Filter

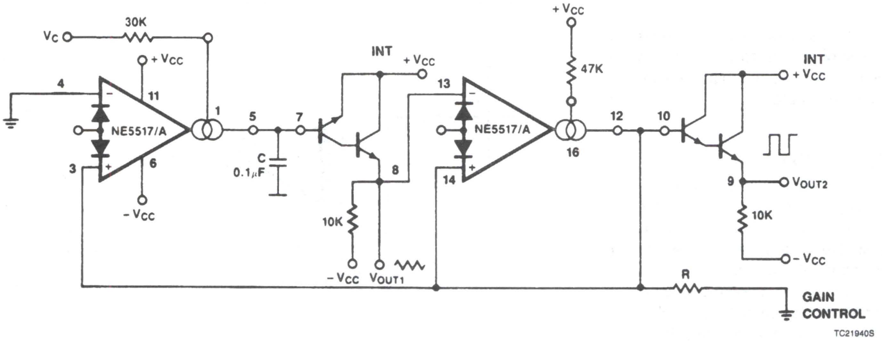
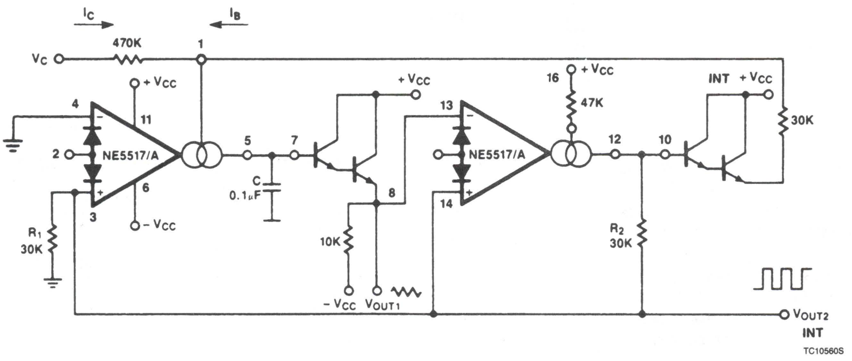

VC
30K
+VCC
4
11
NE5517/A
3
6
-VCC
1
5
7
C
0.1μF
INT
+VCC
8
10K
-VCC
VOUT1
13
NE5517/A
14
+VCC
47K
16
12
10
INT
+VCC
9
VOUT2
10K
-VCC
R
GAIN
CONTROL
TC21940S

Figure 12. Triangle-Square Wave Generator (VCO)

Dual Operational Transconductance Amplifier NE5517/5517A

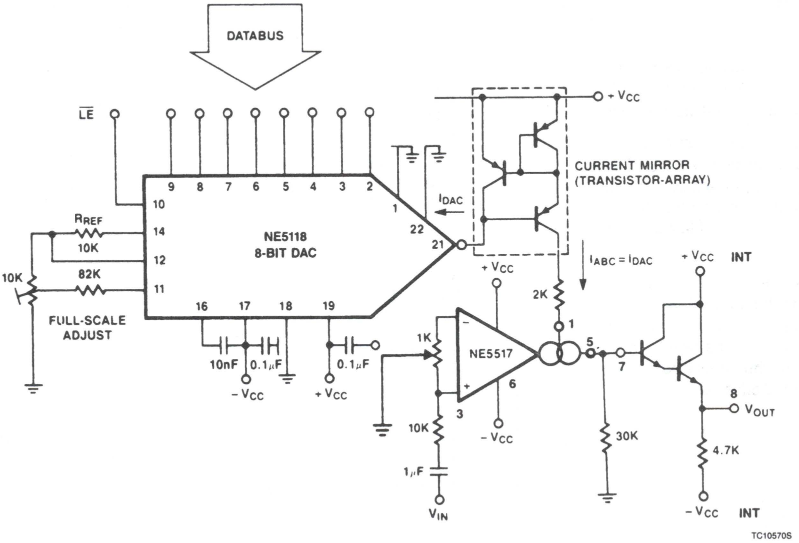


I_C
I_B
V_C
470K
1
+V_{CC}
4
11
2
NE5517/A
6
3
−V_{CC}
R_1
30K
5
7
C
0.1µF
+V_{CC}
8
10K
−V_{CC}
V_{OUT1}
13
14
NE5517/A
16
+V_{CC}
47K
12
10
INT +V_{CC}
30K
R_2
30K
V_{OUT2}
INT
TC10560S

NOTE:

$$V_{PK} = \frac{(V_S - 0.8)\,R_1}{R_1 + R_2} \quad T_H = \frac{2V_{PK} \times C}{I_B} \quad T_L = \frac{2V_{PK} \times C}{I_C} \quad f_{OSC} \frac{I_C}{2V_{PK} \times C} \quad I_C << I_B$$

Figure 13. Sawtooth Pulse VCO



DATABUS
$\overline{LE}$
9
8
7
6
5
4
3
2
10
1
22
21
14
12
11
NE5118
8-BIT DAC
16
17
18
19
R_{REF}
10K
82K
10K
FULL-SCALE ADJUST
10nF
0.1µF
−V_{CC}
0.1µF
+V_{CC}
I_{DAC}
+V_{CC}
CURRENT MIRROR (TRANSISTOR-ARRAY)
$I_{ABC} = I_{DAC}$
+V_{CC}
2K
1K
NE5517
1
5
7
6
3
−V_{CC}
10K
1µF
V_{IN}
30K
+V_{CC} INT
8
V_{OUT}
4.7K
−V_{CC} INT
TC10570S

Figure 14. Digital Programmable Amplifier

Signetics

Linear Products

AN145
NE5517/A Transconductance Amplifier Applications

Application Note

DESCRIPTION

The Signetics NE5517 is a truly versatile dual operational transconductance amplifier. In plain language, it is a voltage-to-current converter governed by the transconductance g_m, which is equivalent to I_{OUT}/V_{IN}. The g_m is increased or decreased linearly by varying the amplifier bias current (I_{ABC}) through an external pin (see Figure 1). From the proper use of the I_{ABC} pin, many control circuits can be realized.

For more insight into the way the part operates, the transconductance can be thought of as gain and is governed by the following equation:

$$g_M = \frac{I_{OUT}}{V_{IN}} = \frac{I_{ABCq}}{2KT} \qquad (1)$$

where the transconductance is dependent on the constant KT/q (which is 26mV at 25°C), and I_{ABC} (which is controlled by the user).

To make the device more universal and adaptable for many functions, two impedance buffers for voltage output applications are also included with the amps so that the part can be used as a programmable operational amplifier.

Linearizing diodes provide another useful option. These should be applied when large input voltages or wide temperature variations are encountered. To show the significance of the diodes, compare the difference between Equation 1 without diodes and Equation 2 with diodes:

$$\frac{I_{OUT}}{V_{IN}} = \frac{2\,I_{ABC}}{R_{IN}\,I_D} \qquad (2)$$

for I_{IN} greater than $\frac{I_D}{2}$

Here, it can be seen that the transconductance is not temperature dependent. R_{IN} is the signal input resistance and I_{IN} is the signal current. I_{IN} must not exceed half the diode current (I_D, nominally 1mA). The diode current is set by a resistor tied to $+V_{CC}$. A graph showing the output distortion improvement versus differential input voltage when using the diodes is shown in Figure 2.

An advantage that the NE5517 has over similar devices is a special biasing network between the amplifier and output impedance buffers. This network eliminates output offset current changes with a sudden change in the

PIN NO	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	I_{OS}	Output A
6	V−	Negative supply
7	$IN_{BUFFER\ (a)}$	Buffer input A
8	$VO_{Buffer\ (a)}$	Buffer output A
9	$VO_{Buffer\ (b)}$	Buffer output B
10	$IN_{Buffer\ (b)}$	Buffer input B
11	V+	Positive supply
12	I_{ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

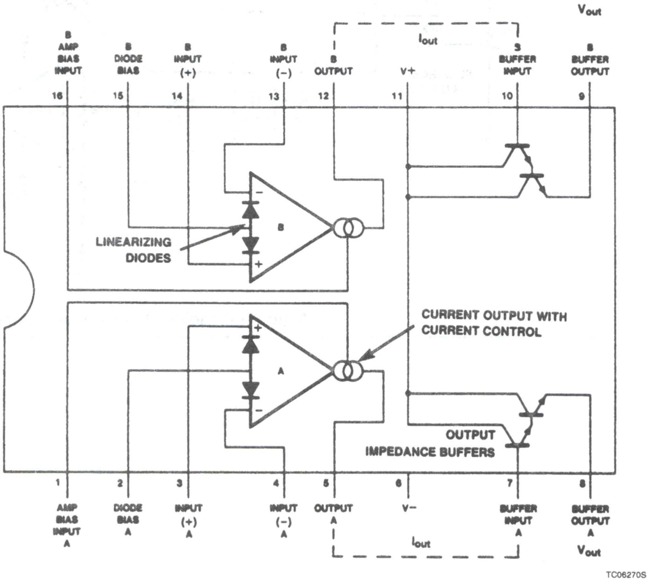

Vout
Iout
B AMP BIAS INPUT
B DIODE BIAS
B INPUT (+)
B INPUT (−)
B OUTPUT
V+
B BUFFER INPUT
B BUFFER OUTPUT
16
15
14
13
12
11
10
9
LINEARIZING DIODES
B
A
CURRENT OUTPUT WITH CURRENT CONTROL
OUTPUT IMPEDANCE BUFFERS
1
2
3
4
5
6
7
8
AMP BIAS INPUT A
DIODE BIAS A
INPUT (+) A
INPUT (−) A
OUTPUT A
V−
BUFFER INPUT A
BUFFER OUTPUT A
Iout
Vout
TC06270S

Figure 1. Pin Designation and Functional Diagram

bias current (I_{ABC}). This is particularly important in audio applications where an audible offset would be produced.

APPLICATIONS

An application employing both amplifiers and buffers internal to the NE5517 is the adjustable triangle-square wave generator shown in Figure 3.

The center oscillating frequency is set by the capacitor C at the output of amplifier A. The output amplitude is set by the resistor R connected between the non-inverting inputs, amplifier B output, buffer B input and ground.

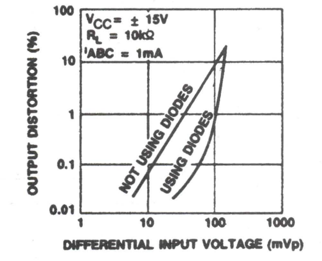


Figure 2. Output Distortion vs Input Voltage Showing Benefit of Diodes

The oscillating frequency is varied by changing V_C, which in turn controls the amplifier bias current (I_{ABC1}). If a positive voltage is applied to V_C, the center frequency will increase linearly with increasing voltage. If a negative is applied, the center frequency will decrease linearly with increasing negative voltage. This makes a very good programmable oscillator with variable amplitude.

By using a large value capacitor and negative control voltage, oscillations in the fractions of Hertz can be realized; a small capacitor and positive control voltage will give frequencies up to 500kHz. Graphs showing the linearity of control voltage versus frequency for different capacitor values are shown in Figure 4.

Pertinent calculations are:

$$f_C = \frac{I_{ABC1}}{4(C)(I_{ABC2})(R)}$$

Where: f_C = center frequency
I_{ABC1} = oscillator control current
I_{ABC2} = amplitude control current
R = amplitude control resistor
C = oscillator control capacitor

Also: Amplitude = (I_{ABC2}) (R)

Another very useful application is to use the NE5517 as a digitally-programmable amplifier. The entire circuit is shown in Figure 5.

The circuit consists of a Signetics microprocessor-compatible DAC, a transistor array, and the NE5517 configured as a voltage-controlled amplifier. This arrangement can also be used with the VCO explained earlier to program its oscillating frequency.

The pertinent equations governing this application are as follows:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{BW(10)}{256} \times \frac{I_{DAC\ MAX} \times q \times R_L}{2 \times KT}$$

Where: BW(10) = binary word decimal
$I_{DAC\ MAX}$ = maximum DAC output current (1mA)
R_L = load resistance (30k)
q/KT = 38.5 at 25°C

Also:

$$I_{DAC\ MAX} = 2 \times \frac{V_{REF}}{R_{REF}}$$

$$= 2 \times \frac{5k}{10k} = 1mA$$

Where: V_{REF} = supplied by DAC (5V)
R_{REF} = referenced resistor (10kΩ)

The $I_{DAC\ MAX}$ of 1mA is used to keep the transconductance within the linear range.

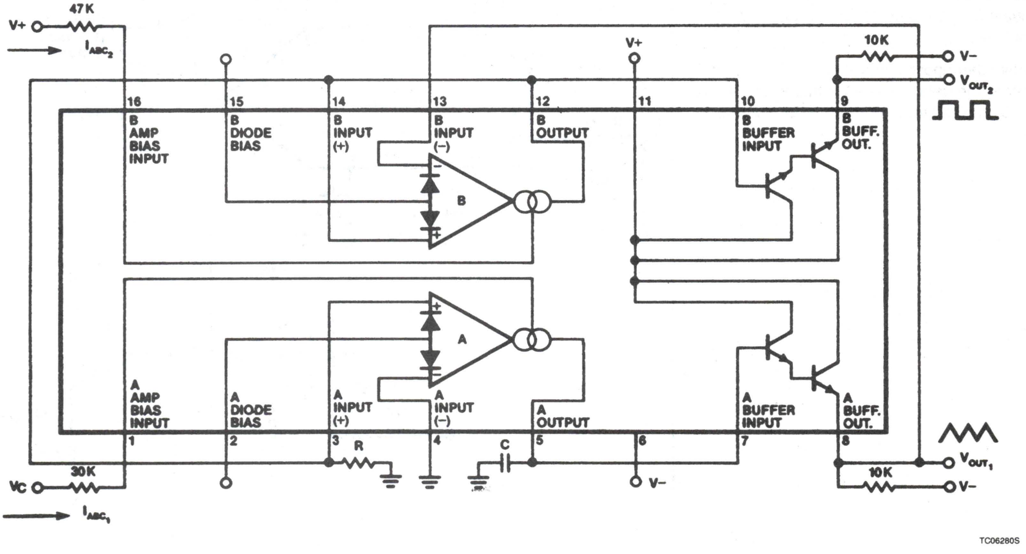
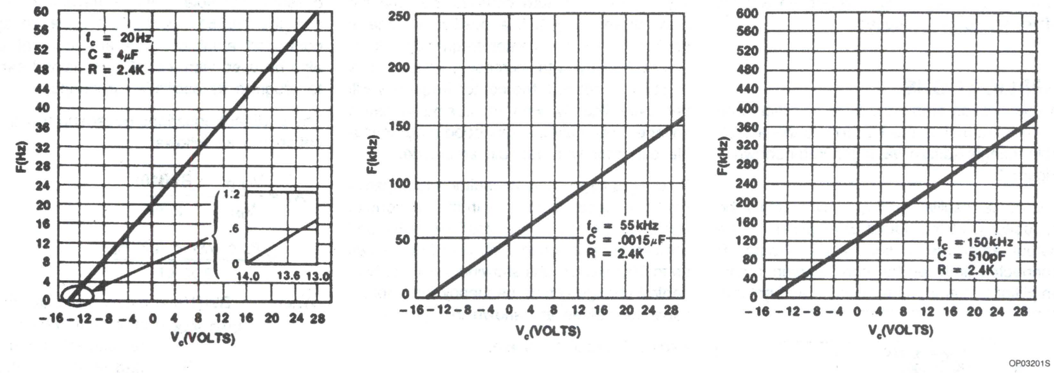


Figure 3. Triangle-Square Wave Generator

NE5517/A Transconductance Amplifier Applications AN145



a. b. c.

NOTE:
V_C Below −13.6V or above +30V will cause distortion.
Changing the C value will vary the frequency range.

Figure 4. Control Voltage (V_C) vs Frequency Data

The current mirror matches the current flow into the DAC and supplies the same amount to the 5517 control pin. Using a current output DAC is much faster than using a voltage output device to control the part. (If speed is not important, this can be done and the current mirror can be replaced with a resistor.) Also, the input attenuation has not been calculated into the gain equation. Therefore, Equation 5 pertains to the signal after the input divider.

Many other applications for the NE5517 exist; refer to the data sheet applications section in the Signetics Linear data book for numerous ideas.

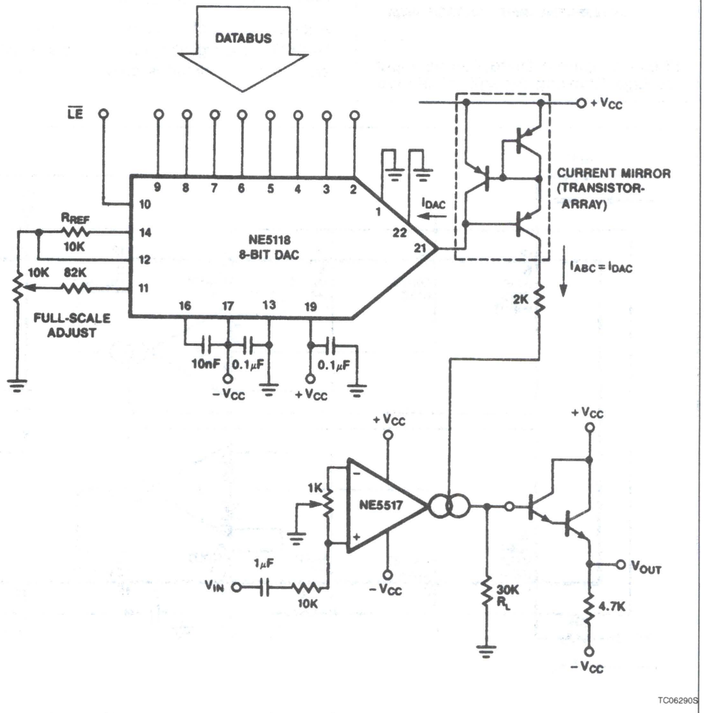

DATABUS
$\overline{LE}$
9 8 7 6 5 4 3 2
10
1
14
12
11
22
21
16 17 13 19
NE5118
8-BIT DAC
R_{REF}
10K
10K
82K
FULL-SCALE ADJUST
10nF
0.1µF
0.1µF
−V_{CC}
+V_{CC}
I_{DAC}
+V_{CC}
CURRENT MIRROR (TRANSISTOR-ARRAY)
$I_{ABC} = I_{DAC}$
2K
+V_{CC}
1K
NE5517
−
+
−V_{CC}
1µF
V_{IN}
10K
30K
R_L
+V_{CC}
V_{OUT}
4.7K
−V_{CC}
TC06290S

Figure 5. Digitally-Programmable Amplifier

Signetics

NE/SA/SE5212
Transimpedance Amplifier

Preliminary Specification

Linear Products

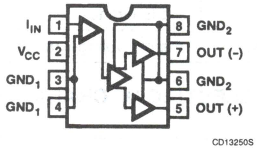
DESCRIPTION
The NE/SA/SE5212 is a low noise differential output amplifier, particularly suitable for signal recovery in fiber-optic receivers and in any other applications where very low signal levels obtained from high impedance sources need to be amplified.

FEATURES
- Extremely low noise: 2.5pA/$\sqrt{Hz}$
- Single 5V supply
- Large bandwidth: 150MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- 14kΩ differential transresistance

APPLICATIONS
- Fiber-optic receivers
- Wideband gain block
- General purpose instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers

PIN CONFIGURATION

N, FE, D-8 Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5212N
8-Pin Plastic SO	0 to +70°C	NE5212D8
8-Pin Ceramic DIP	0 to +70°C	NE5212FE
8-Pin Plastic SO	-40°C to +85°C	SA5212D8
8-Pin Plastic DIP	-40°C to +85°C	SA5212N
8-Pin Ceramic DIP	-40°C to +85°C	SA5212FE
8-Pin Plastic DIP	-55°C to +125°C	SE5212N
8-Pin Ceramic DIP	-55°C to +125°C	SE5212FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5212	SA5212	SE5212	
	Temperature Range				
T_A	Operating ambient	0 to 70	-40 to 85	-55 to 125	°C
T_J	Operating junction	-55 to 150	-55 to 150	-55 to 150	°C
T_{STG}	Storage	-65 to 150	-65 to 150	-65 to 150	°C
V_{CC}	Power Supply	6	6	6	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient temperature ranges		
	NE Grade	0 to 70	°C
	SA Grade	−40 to 85	°C
	SE Grade	−55 to 125	°C
T_J	Junction temperature ranges		
	NE Grade	0 to 90	°C
	SA Grade	−40 to 105	°C
	SE Grade	−55 to 145	°C
V_{CC}	Supply voltage range	4.5 to 5.5	V

DC ELECTRICAL CHARACTERISTICS

Minimum and Maximum limits apply over operating temperature range at V_{CC} = 5V, unless otherwise specified. Typical data applies at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.05	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	2.5	3.3	3.8	V
V_{OS}	Output offset voltage			0	80		0	120	mV
I_{CC}	Supply current		21	26	32	20	26	33	mA
I_{OMAX}	Output sink/source current		3	4		3	4		mA
I_B	Maximum input current (2% linearity)		±60	±80		±40	±80		μA
I_{MAX}	Maximum input current overload threshold		±80	±120		±60	±120		μA
P_D	Maximum power[1] dissipation								mW
	8-pin plastic DIP			1100			1100		
	8-pin plastic SO			750			750		
	8-pin Cerdip			750			750		

NOTE:

1: Package thermal resistances are as follows:
8-pin plastic DIP: 110°C/W
8-pin plastic SO: 160°C/W
8-pin Cerdip: 165°C/W

AC ELECTRICAL CHARACTERISTICS

Minimum and Maximum limits apply over operating temperature range at V_{CC} = 5V, unless otherwise specified. Typical data applies at V_{CC} = 5V and T_A = 25°C.

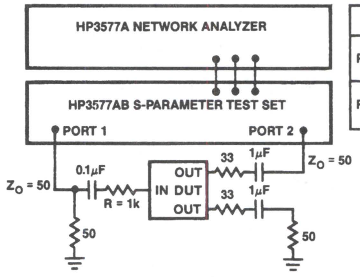
SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
R_T	Transresistance (Differential output)	f = 10MHz, R_L = inf	9.8	14	18.2	9.0	14	19	kΩ
R_O	Output resistance (Differential output)	f = 10MHz	14	30	42	14	30	46	Ω
R_T	Transresistance (Single-ended output)	f = 10MHz, R_L = inf	4.9	7	9.1	4.5	7	9.5	kΩ
R_O	Output resistance (Single-ended output)	f = 10MHz	7	15	21	7	15	23	Ω
f_{3dB}	Bandwidth (−3dB)	Test Circuit 1 D package, T_A = 25°C N, F packages, T_A = 25°C		120 100			120 100		MHz MHz
R_{IN}	Input resistance		75	110	143	70	110	150	Ω
C_{IN}	Input capacitance			10	15		10	18	pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	ΔV_{CC} = 5 ±0.5V		9.6			9.6		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	D package $\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.05			0.05		%/°C
I_N	Input RMS noise current spectral density	Test Circuit 2 f = 10MHz T_A = 25°C		2.5			2.5		$pA/\sqrt{Hz}$
I_T	Input RMS noise current	Δf = 100MHz, T_A = 25°C Test Circuit 2		30			30		nA
PSRR	Power supply rejection ratio[3] $V_{CC1} = V_{CC2}$	Any package f = 0.1MHz[1, 2] Test Circuit 3 ΔV_{CC} = 0.1V	26	33		20	33		dB
PSRR	Power supply rejection ratio (ECL configuration)	Any package f = 0.1MHz[1, 2] Test Circuit 4		23			23		dB
$V_{O\ MAX}$	Maximum output voltage swing differential	R_L = inf.	2.4	3.2		1.7	3.2		V_{P-P}

NOTES:

1. Circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
2. V_{CC1} and V_{CC2} are internally connected in all 8-pin packages.
3. Output referenced.

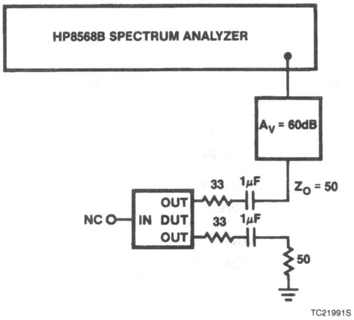
Transimpedance Amplifier

NE/SA/SE5212


HP3577A NETWORK ANALYZER
HP3577AB S-PARAMETER TEST SET
PORT 1
PORT 2
$Z_O = 50$
$Z_O = 50$
0.1µF
R = 1k
OUT
IN DUT
OUT
33
1µF
33
1µF
50
50

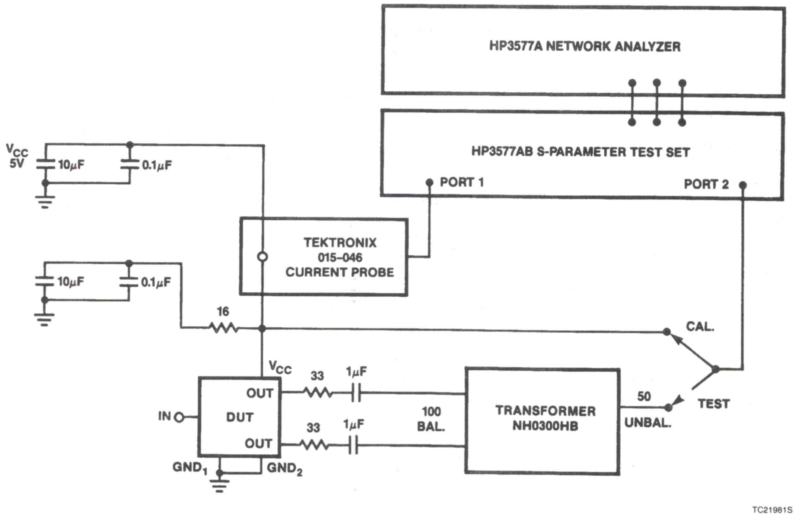
SINGLE-ENDED	DIFFERENTIAL
$R_t \cong \frac{V_{OUT}}{V_{IN}} R = S21 \times R$	$R_t \cong \frac{V_{OUT}}{V_{IN}} R = 2 \times S21 \times R$
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 66$

TC22001S


HP8568B SPECTRUM ANALYZER
$A_V = 60dB$
33
1µF
$Z_O = 50$
OUT
NC
IN DUT
OUT
33
1µF
50
TC21991S

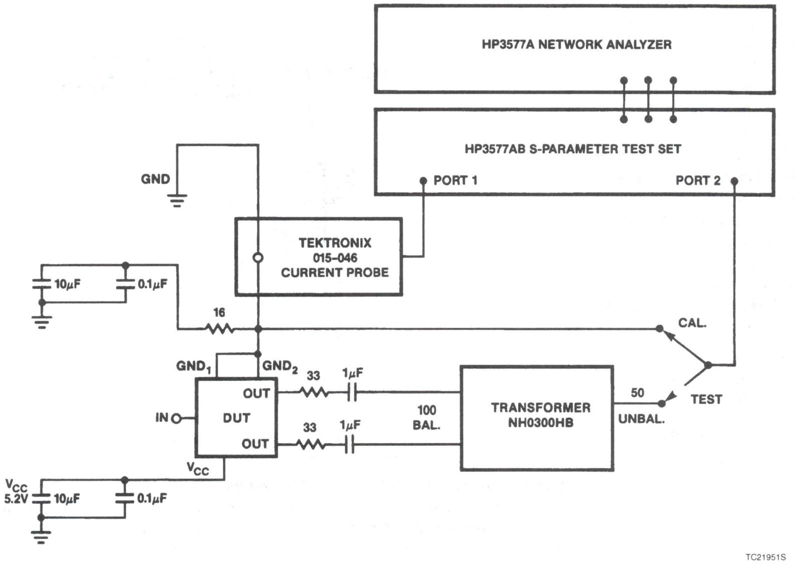
a. Test Circuit 1

b. Test Circuit 2


HP3577A NETWORK ANALYZER
HP3577AB S-PARAMETER TEST SET
PORT 1
PORT 2
V_{CC} 5V
10µF
0.1µF
TEKTRONIX 015-046 CURRENT PROBE
10µF
0.1µF
16
CAL.
V_{CC}
33
1µF
OUT
IN
DUT
OUT
33
1µF
100 BAL.
TRANSFORMER NH0300HB
50
UNBAL.
TEST
GND_1
GND_2
TC21981S

c. Test Circuit 3

Figure 1. Test Circuits


HP3577A NETWORK ANALYZER
HP3577AB S-PARAMETER TEST SET
PORT 1
PORT 2
GND
TEKTRONIX
015-046
CURRENT PROBE
10μF
0.1μF
16
CAL.
GND1
GND2
33
1μF
OUT
IN
DUT
OUT
33
1μF
100
BAL.
TRANSFORMER
NH0300HB
50
UNBAL.
TEST
VCC
VCC
5.2V
10μF
0.1μF
TC21951S

a. Test Circuit 4

Figure 1. Test Circuits

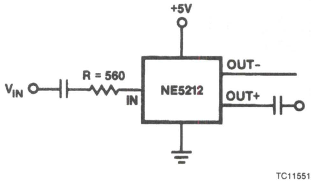
PRECAUTIONS

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. First of these is use of a well-regulated power supply. The supply must be capable of supplying varying amounts of current without significantly changing the voltage level. Next, of course, is proper power supply bypassing consisting of a good quality 0.1μF high-frequency capacitor in parallel with a 10μF tantalum capacitor. Some applications require an RF choke in series with the power supply line. These components should be mounted as close to the device pins as possible with the shortest leads possible.

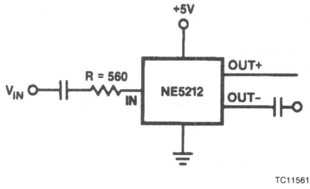
Seperate analog and digital ground leads should be maintained and printed circuit board ground plane should be employed whenever possible.

BASIC CONFIGURATION

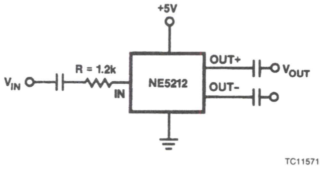
A trans-resistance amplifier is a current-to-voltage converter. The forward transfer function then is defined as voltage out divided by current in, and is stated in ohms. The lower the source resistance, the higher the gain. The NE5212 has a differential transresistance of 14kΩ typically and a single-ended transresistance of 7kΩ typically. The device has two outputs: inverting and non-inverting. The output voltage in the differential output mode is twice that of the output voltage in the single-ended mode. Although the device can be used without coupling capacitors, more care is required to avoid upsetting the internal bias nodes of the device. Figure 2 shows some basic configurations.



a. Non-Inverting 20dB Amplifier



b. Inverting 20dB Amplifier



c. Differential 20dB Amplifier

Figure 2

VARIABLE GAIN

Figure 3 shows a variable gain circuit using the NE5212 and the NE5230 low voltage op amp. This op amp is configured in a non-inverting gain of five. The output drives the gate of the SD210 DMOS FET. The series resistance of the FET changes with this output voltage which in turn changes the gain of the NE5212. This circuit has a distortion of less than 1% and a 25dB range, from −42.2dBm to −15.9dBm at 50MHz, and a 45dB range, from −60dBm to −14.9dBm at 10MHz with 0 to 1V of control voltage at V_C.

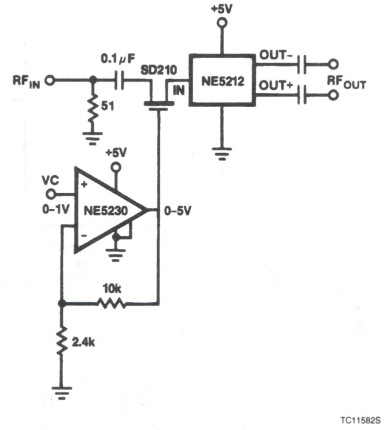


Figure 3. Variable Gain Circuit

16MHz CRYSTAL OSCILLATOR

Figure 4 shows a 16MHz crystal oscillator operating in the series resonant mode using the NE5212. The non-inverting input is fed back to the input of the NE5212 in series with a 2pF capacitor. The output is taken from the inverting output.

DIGITAL FIBER-OPTIC TRANSMITTER/RECEIVER

Figures 5a and b show a fiber-optic transmitter using off-the-shelf components and the NE5212. The circuit uses a Signetics TTL line driver, 74F3037, and a Hewlett-Packard HFBR-1404 LED. This combination is nearly ideal because LEDs are harder to turn off quickly than on, and because the unequal drive capabilities of the TTL totem-pole output configuration complement each other. This pre-bias current and the speed-up capacitor significantly decrease the transition times. The circuit will has rise and fall times of 3ns. It operates over the automotive temperature range at 170Mbaud. The design formulas presented here can be used to optimize the speed for other devices.

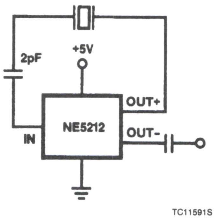


Figure 4. 16MHz Crystal Oscillator

The receiver shown in Figure 5b uses the NE5212, the Signetics 10116 ECL line receiver, and a Hewlett-Packard HFBR-2208 PIN. The circuit is a capacitor-coupled receiver and utilizes positive feedback in the last stage to provide the hysteresis. The amount of hysteresis can be tailored to the individual application by changing the values of the feedback resistors to maintain the desired balance between noise immunity and sensitivity. At room temperature, the circuit operates at 50Mbaud with a BER of 10E-10 and over the automotive temperature range at 40Mbaud with a BER of 10E-9. Higher speed experimental diodes have been used to operate this circuit at 220Mbaud with a BER of 10E-10.

The cost of the transmitter/receiver pair is about $50 with the standard parts.

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Signetics

Linear Products

AN100
An Overview of Data Converters

Application Note

INTRODUCTION

Large systems are comprised of many different subsystems, all of which must interface to complete the system. All types of circuits, including linear, digital and discrete, are often used in the subsystems.

Interface circuits provide the necessary function of tying the parts of a system together. These circuits are usually not purely linear or digital but contain both types of circuit functions. For instance, sense amplifiers are designed for interface between low level memory outputs and bipolar levels, while differential comparators are designed for interface between analog systems and logic systems. In general, this section will cover such devices as data converters, comparators, sense amplifiers, line drivers/receivers, and display drivers.

CONVERTERS

Digital communications, digital instruments and displays have created a demand for low cost reliable converters. Key factors in this demand are:

- The need to communicate with digital computers for processing and storage of analog signals.
- Severe limitations encountered in reliable analog data transmission over any considerable distance.
- The need for more easily readable displays.

General application areas for converters include: Data processing, data transmission, graphics and displays, audio systems, control systems and arithmetic operations.

SPECIFIC APPLICATIONS

Test Systems

- Transistor tester (Force I_B and I_C)
- Resistor matching
- Programmable power supplies
- Programmable pulse generators
- Programmable current source
- Function generators (ROM drive)

Arithmetic Operations

- Analog division by a digital word
- Analog quotient of 2 digital words
- Analog product of 2 digital words — squaring
- Addition and subtraction with analog output
- Magnitude comparison of 2 digital words
- Digital quotient of 2 analog variables
- Arithmetic operations with words from different logic families

Graphics and Displays

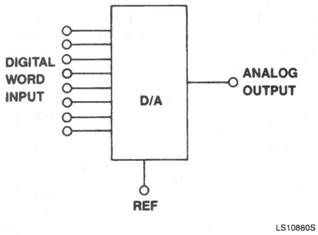
- Polar-to-rectangular conversion
- CRT character generation
- Chart recorder driver
- CRT display driver

Data Transmission

- Modem transmitter
- Differential line driver
- Party line multiplexing of analog signals
- Multilevel 2-wire data transmission
- Secure communications (constant power dissipation)

Control Systems

- Reference level generator for setpoint controllers
- Positive peak detector
- Negative peak detector
- Disc drive head positioner
- Microfilm head positioner



NOTES:
Output = Ref. × digital word

$$\text{Output} = \text{Ref.} \times \left(\frac{B_1}{2} + \frac{B_2}{4} + \ldots + \frac{B_N}{2^N}\right)$$

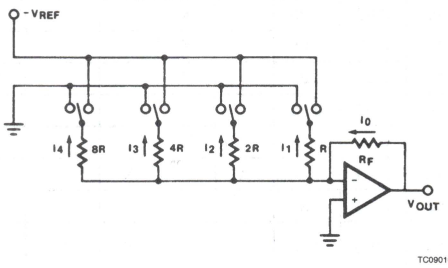
Figure 1. Conversion of a Digitally Coded Signal Input Into an Analog Signal Output

Audio Systems

- Digital AVC and reverberation
- Music distribution
- Organ tone generator
- Audio tracking A/D
- Speech compression and expansion
- Audio digitizing and decoding

DAC Building Blocks

The actual implementation of a D/A system contains four separate parts: A reference quantity; a set of binary switches to simulate binary coefficients $B_1 \ldots B_N$; a weighting network; and an output summing means.



NOTE:

$$V_{OUT} = \frac{R_F}{R} V_{REF} \times \left(b1 + \frac{b_2}{2} + \frac{b_4}{4} + \frac{b_8}{8}\right)$$

Figure 2. Binary-Weighted Ladder Employing Voltage Switching

DAC PRODUCTS SUMMARY

DEVICE	BITS	ACC. %	CONV. SPEED (µs)	OUTPUT		INT REF	INT. LATCH	PACKAGE			TEMPERATURE RANGE		COMMENTS
				V	I			N	D	F	Com'l	Mil	
NE5150	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits with RAM
NE5151	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits w/o RAM
NE5152	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits with RAM
TDA8442	6	0.78		X			X	X			X		4 × 6 Bits I^2C
TDA8444	6	0.78		X			X	X			X		8 × 6 Bits I^2C
MC1408-7	8	0.39	0.07		X			X		X	X		
MC1408-8	8	0.19	0.07		X			X	X	X	X		
MC1508-8	8	0.19	0.07		X					X		X	
DAC08	8	0.19	0.07		X					X		X	
DAC08A	8	0.10	0.07		X					X		X	
DAC08C	8	0.39	0.07		X			X		X	X		
DAC08E	8	0.19	0.07		X			X	X	X	X		
DAC08H	8	0.10	0.07		X			X		X	X		
NE5018	8	0.19	2.3	X		X	X	X	X	X	X		
SE5018	8	0.19	2.3	X		X	X			X		X	
NE5019	8	0.10	2.3	X		X	X	X	X	X	X		
SE5019	8	0.10	2.3	X		X	X			X		X	
NE5118	8	0.19	0.2		X	X	X	X	X	X	X		
SE5118	8	0.19	0.2		X	X	X			X		X	
NE5119	8	0.10	0.2		X	X	X	X	X	X	X		
SE5119	8	0.10	0.2		X	X	X			X	X		
PNA7518	8	0.19	0.013	X			X	X			X		30MHz sampling rate
TDA5702	8	0.39	0.04	X		X	X	X			X		25MSPs
MC3410C	10	0.10	0.25		X			X		X	X		
NE5020	10	0.10	5.0	X		X	X	X		X	X		
NE5410	10	0.05	0.25		X					X	X		± ¼ LSB DNL
SE5410	10	0.05	0.25		X					X		X	± ¼ LSB DNL
MC3410	10	0.05	0.25		X			X		X	X		± ½ LSB DNL
MC3510	10	0.05	0.25		X					X		X	± ½ LSB DNL
AM6012	12	0.05	0.25		X					X	X		± 1 LSB DNL
DAC800V	12	0.012	5.0	X		X		X		X	X		
DAC800I	12	0.012	1.0		X	X		X		X	X		
TDA1540D	14	0.012	0.5		X	X	X			X	X		serial input ± ½ LSB DNL
TDA1540	14	0.003	0.5		X	X	X	X		X	X		serial input
TDA1541	16	0.0008	1.0		X	X	X	X			X		serial input

Binary-Weighted Ladder Employing Voltage Switching

The disadvantages of a binary-weighted ladder employing voltage switching include: a wide range of resistor values which are used in weighting the network, and nodal capacitances which are charged/discharged during conversion (See Figure 2).

R-2R Ladder Network Employing Current Switching

The advantages of this type of network include: no need for a wide range of resistor values, and current switching eliminates transients in nodal parasite capacitances (See Figure 3).

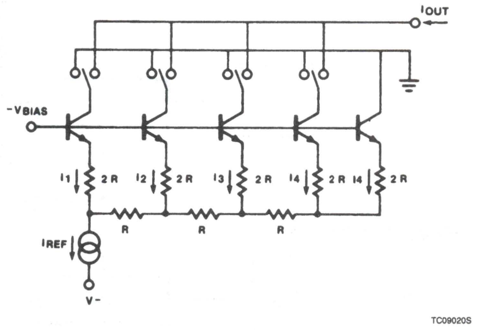
KEY SPECIFICATIONS

Speed

The conversion process should represent the input signal with the highest fidelity and minimal lag in time (real-time applications).

Settling Time

Settling time is a measure of a converter's speed and is defined as the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ± ½ LSB (See Figure 4).



NOTE:
$I_{OUT} = I_{REF} \times \left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8}\right)$

Figure 3. R-2R Ladder Network Employing Current Switching

Errors

Offset Error — The output voltage of DAC with zero code input. Offset can and usually is trimmed to zero with an offset zero adjust potentiometer (See Figure 5).

Gain Error — Deviation in output voltage from correct level when the input calls for a full-scale output. This error may be trimmed to zero (See Figure 6).

Relative Accuracy — The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full-scale (See Figure 7).

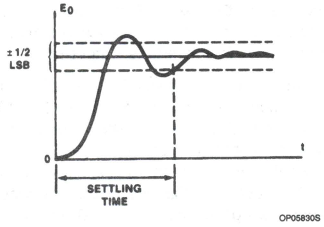


Figure 4. Settling Time

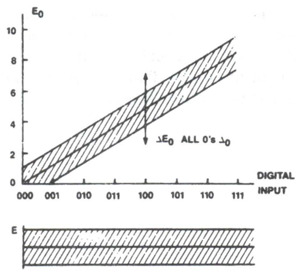


Figure 5. Offset Error

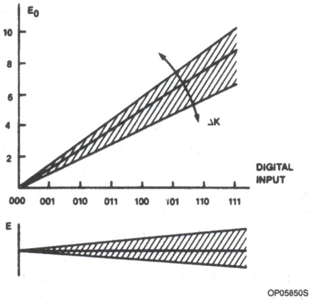


Figure 6. Gain Error

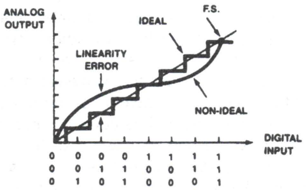


Figure 7. Relative Accuracy

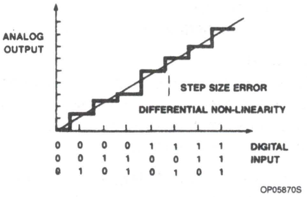


Figure 8. Differential Non-Linearity

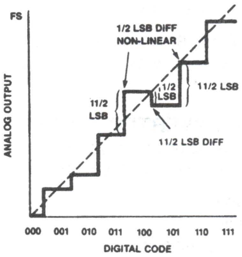


Figure 9. Non-Monotonic (Must be > ± ½ LSB Non-Linear)

An Overview of Data Converters AN100

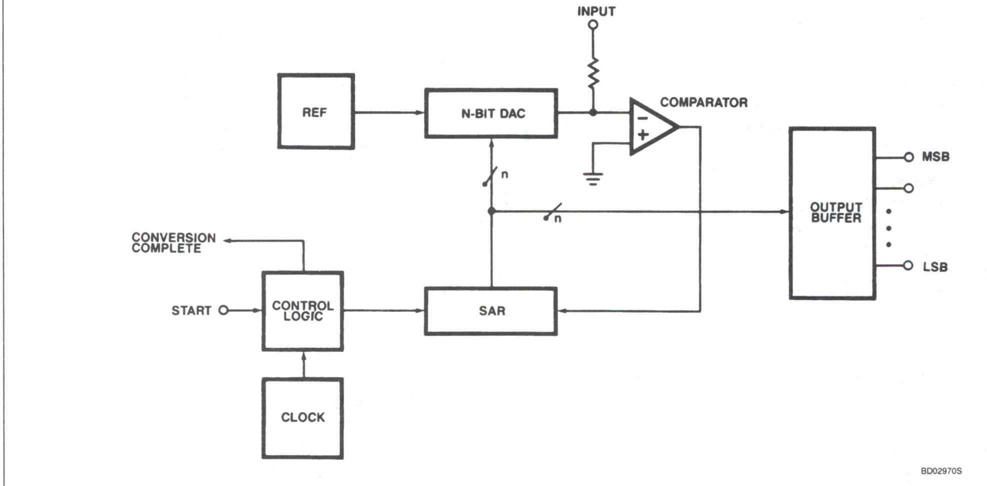


Figure 10. Block Diagram of a Successive Approximation A/D Converter

Differential Non-Linearity — Incremental error from any ideal LSB analog output change when the digital input is changed 1 LSB (See Figure 8).

Monotonicity — As the input code is incremented from one code to the next in sequence, the analog output will either increase or remain constant (See Figure 9).

Stability

Stability is a measure of the independence of converter parameters with respect to variations in external conditions such as temperature and supply voltage.

Temperature Coefficient — The effects of temperature changes of the output. Specified as % full-scale change.

Supply Rejection — Ability to resist changes in the output with supply changes, specified as % full-scale change.

Long Term Stability — Measure of how stable the output is over a long period of time.

A/D CONVERTER CIRCUITS

Analog-to-Digital conversion schemes generally fall into one of three categories:

1. Feedback
- Counting
- Tracking (up-down)
- Successive approximation

2. Integrating
- Single slope
- Dual slope
- Triple slope

3. Parallel (Flash)

The type of converter chosen for a given application depends upon many things; the accuracy required, the conversion speed necessary, the necessary immunity to noise, and cost are some of these considerations.

The successive approximation technique is the one most widely used, mainly because of its excellent tradeoffs in resolution, speed, accuracy, and cost.

Figure 10 shows a simplified block diagram of a successive approximation A/D converter. Upon receiving the start signal, the successive approximation register (SAR) is cleared and the most significant bit (MSB) of that register is set. The SAR output is connected to the input of the DAC, the output of which is compared with the unknown input. If the input is less than the DAC output, the MSB is cleared and the next bit is set; if the input is greater than the DAC output, the MSB is left high and the next bit is set. The input is again compared with the DAC output and the second bit cleared or left high, based on the same criteria as for the MSB. This process continues until all bits have been determined. The analog input should not change appreciably during the conversion time. If it did change during this time, the converted output would not be a true indication of the analog input. For this reason, it is common practice to use a sample-and-hold circuit at the converter analog input to hold the input value constant during the conversion process. A sample-and-hold circuit is not necessary if the signal at the input of the converter varies slowly enough and has a noise level low enough so that the input will not change a significant amount during the conversion. The allowable input change during this conversion is generally accepted as the value of ½ LSB (for n-bit accuracy).

Accuracy and speed are determined primarily by the properties of the DAC and the comparator. Linearity is determined primarily by the linearity of the DAC. If the DAC is non-monotonic, one or more codes will be missing from the A/D converter's output range.

Figure 11 is the transfer function of a 3-bit binary coded A/D converter with a 0 to +10V input range. A 3-bit ADC is shown for simplicity, but the principle applies to ADCs of any resolution. Note that there is a ½ LSB offset at the input such that the first count occurs when the input is equal to ½ LSB. The center of the range for the first step occurs, therefore, when the input is equal to the value of one LSB, and the error at the switch point is limited to ½ LSB. This error is known as the quantization error as it is derived from the smallest input quantity that can be resolved. If an ADC has a specified error of ½ LSB maximum, this means that any transition point can be as far as ½ LSB from where it should be.

An Overview of Data Converters AN100

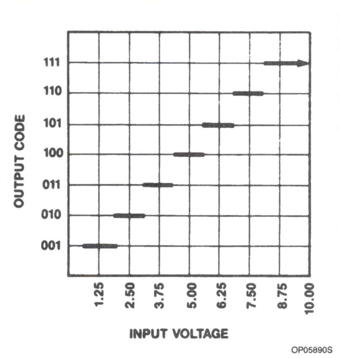


Figure 11. Transfer Function of an Ideal 3-bit ADC With a 0 to 10V Input Range

CONSIDERATIONS FOR A/D CONVERTERS

- Analog input signal range and resolution required
- Linearity requirement and stability
- Conversion speed required
- Monotonicity requirement: Can missing codes be tolerated?
- Character of input signal: Is it noisy, sampled, filtered, slowly varying?
- Transfer characteristics (type of coding)

A/D CONVERTER TERMS

Resolution

Resolution is the input change required to increment the output between the two adjacent codes. This term also refers to the number of bits in the output word and, hence, the number of discrete output codes the input analog signal can be broken into. Expressed in "bits" resolution.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output digital word (code) to the input analog signal, i.e., Binary, BCD.

Conversion Speed

The Conversion Speed is the speed at which an ADC can make repetitive data conversions.

Quantizing Error

Quantizing Error is an inherent error in the conversion process due to finite resolution (discrete output). See Figure 12.

Offset Error

An Offset Error is shown in Figure 13.

Gain Error

A Gain Error is shown in Figure 14.

Relative Accuracy

Relative Accuracy is the deviation of an actual bit transition from the ideal transition value at any level over the range of the ADC (% FS). See Figure 15.

Hysteresis Error

A Hysteresis Error is the code transition voltage dependence relative to the direction from which the transition is approached.

Monotonicity

Monotonicity is when the output code either increases or remains the same for increasing analog input signals. The opposite is true in the reverse direction.

Missing Codes

A Missing Code is a code combination that is skipped. See Figure 16.

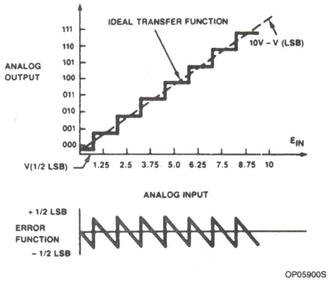
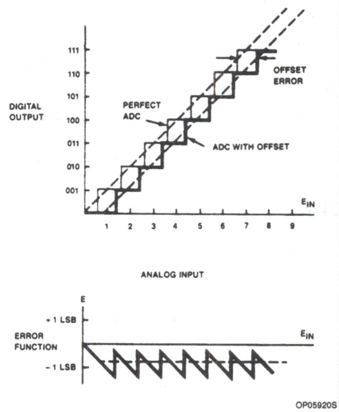
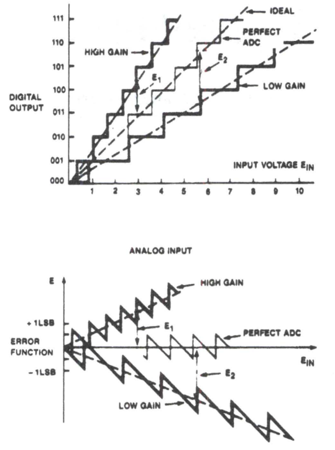


Figure 12. Quantizing Errors


111
110
101
100
011
010
001
DIGITAL OUTPUT
PERFECT ADC
ADC WITH OFFSET
OFFSET ERROR
E_{IN}
1 2 3 4 5 6 7 8 9
ANALOG INPUT
E
+1 LSB
ERROR FUNCTION
-1 LSB
E_{IN}

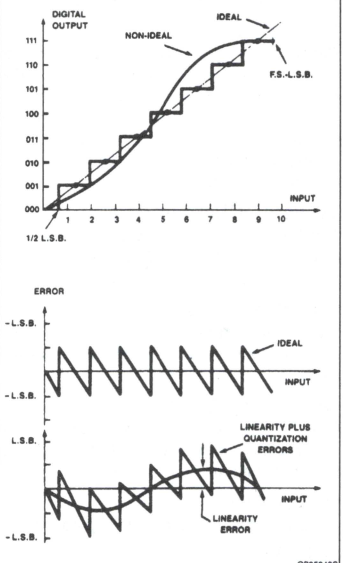
OP05920S

Figure 13. Offset Error


111
110
101
100
011
010
001
000
DIGITAL OUTPUT
IDEAL
PERFECT ADC
HIGH GAIN
E_2
E_1
LOW GAIN
INPUT VOLTAGE E_{IN}
1 2 3 4 5 6 7 8 9 10
ANALOG INPUT
E
HIGH GAIN
+1LSB
E_1
PERFECT ADC
ERROR FUNCTION
E_{IN}
-1LSB
E_2
LOW GAIN

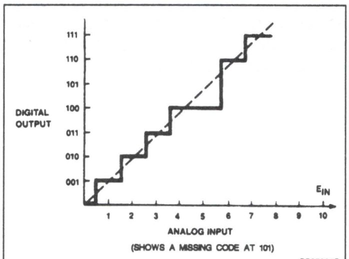
OP05910S

Figure 14. Gain Error


DIGITAL OUTPUT
IDEAL
NON-IDEAL
F.S.-L.S.B.
111
110
101
100
011
010
001
000
INPUT
1 2 3 4 5 6 7 8 9 10
1/2 L.S.B.
ERROR
-L.S.B.
IDEAL
INPUT
-L.S.B.
L.S.B.
LINEARITY PLUS QUANTIZATION ERRORS
INPUT
LINEARITY ERROR
-L.S.B.

OP05940S

Figure 15. Relative Accuracy


111
110
101
100
011
010
001
DIGITAL OUTPUT
E_{IN}
1 2 3 4 5 6 7 8 9 10
ANALOG INPUT
(SHOWS A MISSING CODE AT 101)

OP05931S

Figure 16. Missing Codes

Signetics

Analog-to-Digital Converters Selector Guide

Linear Products

DEVICE	BITS	ACC. %	CONV. SPEED (μs)	INPUT		THREE STATE OUTPUT	INT. REF.	INT. CLOCK	PACKAGE			TEMPERATURE RANGE	
				V	I				N	F	FE	Com'l	Mil
NE5036	6	0.78	23	X		X			X	X	X	X	
NE5037	6	0.78	9	X		X			X	X		X	
PNA7509	7	0.78		X		X			X			X	
ADC0801-1	8	0.10	73	X		X		X		X		X^1	
ADC0802-1	8	0.19	73	X		X		X	X	X		X^1	
ADC0803-1	8	0.19	73	X		X		X	X	X		X^1	
ADC0804-1	8	0.39	73	X		X		X	X	X		X^1	
ADC0805-1	8	0.39	73	X		X	X	X	X	X		X^1	
ADC0820B	8	0.19	2.5	X		X		X	X			X	
ADC0820C	8	0.39	2.5	X		X		X	X	X		X	X
NE5034	8	0.19	17	X		X		X		X		X	
TDA5703	8	0.39				X	X		X			X	
NE5030	10	0.05	4	X		X	X		X	X		X	
SE5030	10	0.1	4	X					X	X			X
TDA1534	14	0.003	8.5		X		X	X	X			X	

Signetics

Symbols and Definitions for Analog-to-Digital Converters (ADCs)

Linear Products

Absolute Accuracy Error

Absolute Accuracy Error at a given output code is the difference between the theoretical analog input voltage required to produce a given output code and the actual analog input voltage required to produce the same code. Since the same output code is produced by a finite band of input voltages, the "analog input voltage required" is defined as the midpoint of the band of input voltages that will produce that code.

Absolute accuracy error includes gain error, offset error and relative accuracy error and is typically expressed in LSBs or in percent of full-scale range (FSR).

Conversion Time

Conversion Time is the time required for a conversion cycle to be completed while meeting the specifications.

Differential Linearity Error

Differential Linearity Error of an ADC is the resolution for which the ADC is guaranteed to have no missing codes. This implies that all possible digital output codes will appear in an increasing sequence as the input voltage is increased.

Full-Scale Range (FSR)

The Full-Scale Range (FSR) of an ADC is the scale factor that determines the nominal conversion relationship; e.g., 2.5V span for a full-scale change in a fixed reference converter.

In a unipolar ADC of n bits, the ideal first code transition occurs at $FSR \times 2^{-N} \times \frac{1}{2}$ and the final code transition occurs at $FSR \times (1 - 2^{-N} \times \frac{3}{2})$. The ideal code transition from code C-1 to C occurs at $FSR \times (C - \frac{1}{2}) \times \frac{1}{2^N}$.

In a bipolar ADC, the ideal first code transition occurs at $FSR \times (2^N - 1) \times \frac{1}{2}$ and the final code transition occurs at $FSR \times (1 - 3 \times 2^{-N}) \times \frac{1}{2}$.

Gain Error

Gain Error is the deviation between the ideal and actual analog input voltage to cause the final code transition to a full-scale output code after nulling offset error. It is usually expressed in LSBs or in percent of FSR.

Integral Non-Linearity

Same as Relative Accuracy.

Least Significant Bit

The Least Significant Bit (LSB) is the lowest-order bit and carries the smallest weight. In an n-bit ADC, the weight of the LSB is 2^{-N} relative to the FSR of the ADC. It represents the smallest change that can be resolved by an n-bit ADC.

Missing Code

A missing code is a code combination that does not appear at the ADC's output (see Differential Linearity Error).

Most Significant Bit (MSB)

The Most Significant Bit (MSB) is the highest-order bit and carries the most weight. In an n-bit ADC, the weight of the MSB is ½ the full-scale range of the ADC.

Offset Error (Unipolar and Bipolar)

In an ADC, unipolar offset is the difference between the actual analog input voltage that causes the first code transition point and the ideal value to cause the first code transition, which is ½ LSB above analog ground. Similarly for bipolar offset, it is the difference between the actual analog input voltage that causes the code transition from 1 LSB below half-scale to half-scale and the ideal analog value to cause the same code transition which is ½ LSB above Analog Ground.

Power Supply Sensitivity

The Power Supply Sensitivity of an ADC is the change in the code transition points with changes in the DC power supply voltages. It is usually expressed in LSBs/V or in %FSR/V.

Quantization Uncertainty

ADCs of any resolution exhibit an inherent quantization uncertainty of ± ½ LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be eliminated.

Relative Accuracy

Relative Accuracy Error is the deviation of the ADC's actual code transition points from the ideal code transition points on a straight line which connects the ideal first code transition point and the final code transition point, after nulling offset error and gain error. It is generally expressed in LSBs or in percent of FSR.

Resolution

Resolution of an ADC is the number of bits at its output. The number of output states is 2^N, where N is the resolution of the converter.

Temperature Coefficients

In general, Temperature Coefficients are expressed either in ppm/°C or in LSBs/°C or as a change in the specified parameter over the temperature range. Measurements are usually made at room temperature and at the temperature extremes of the specified temperature range; the temperature coefficient is defined as the change in the parameter from its room temperature value divided by the corresponding temperature change.

Signetics

ADC0801/2/3/4/5-1
CMOS 8-Bit A/D Converters

Product Specification

Linear Products

DESCRIPTION

The ADC0801 family is a series of five CMOS 8-bit successive approximation A/D converters using a resistive ladder and capacitive array together with an auto-zero comparator. These converters are designed to operate with microprocessor-controlled buses using a minimum of external circuitry. The 3-state output data lines can be connected directly to the data bus.

The differential analog voltage input allows for increased common-mode rejection and provides a means to adjust the zero-scale offset. Additionally, the voltage reference input provides a means of encoding small analog voltages to the full 8 bits of resolution.

FEATURES

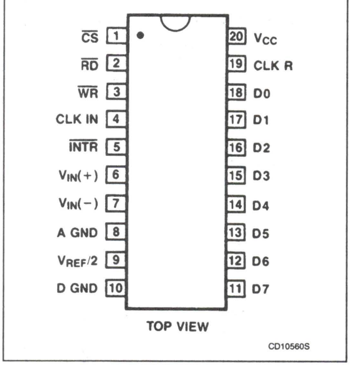
- **Compatible with most microprocessors**
- **Differential inputs**
- **3-State outputs**
- **Logic levels TTL and MOS compatible**
- **Can be used with internal or external clock**
- **Analog input range 0V to V_{CC}**
- **Single 5V supply**
- **Guaranteed specification with 1MHz clock**

APPLICATIONS

- **Transducer-to-microprocessor interface**
- **Digital thermometer**
- **Digitally-controlled thermostat**
- **Microprocessor-based monitoring and control systems**

PIN CONFIGURATION

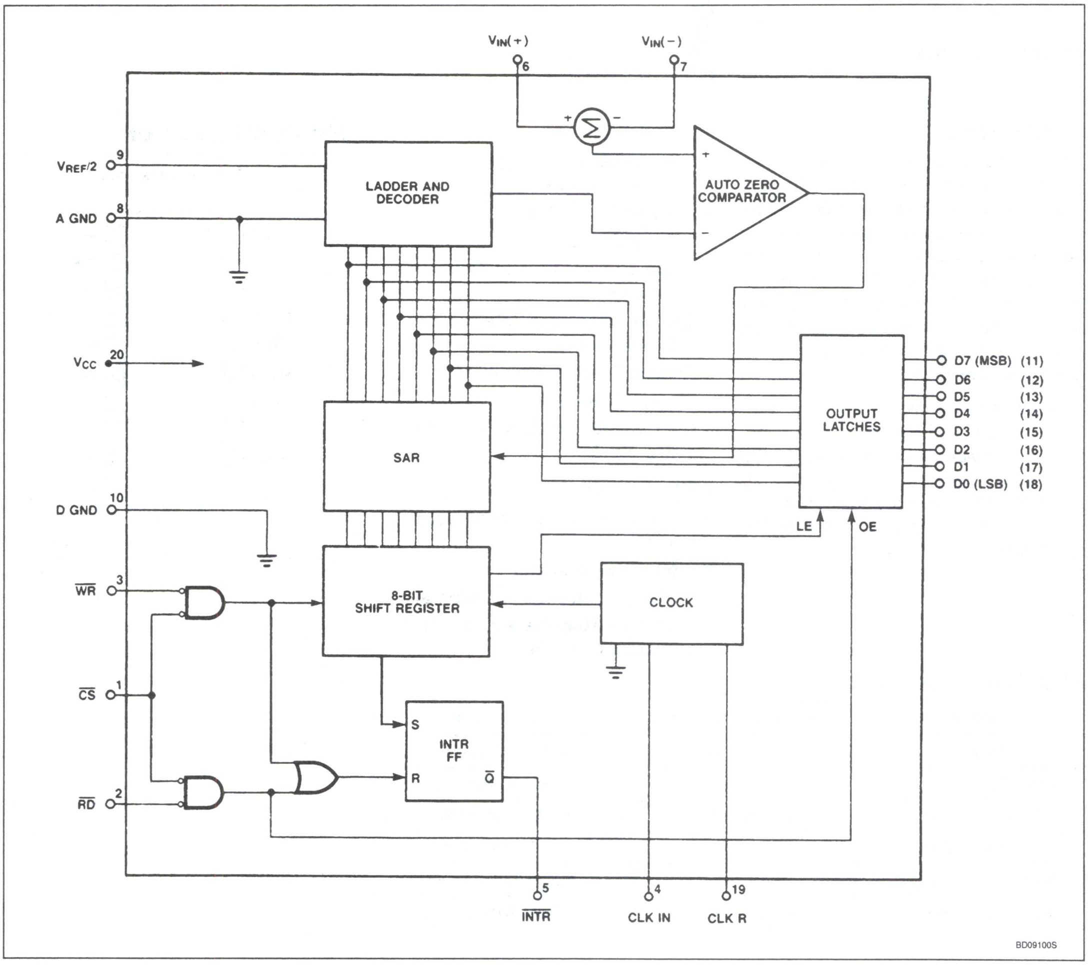
D, F, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Cerdip	−55°C to +125°C	ADC0801/02-1F
20-Pin Cerdip	−40°C to +85°C	ADC0801/02/03-1 LCF
20-Pin Plastic DIP	−40°C to +85°C	ADC0801/02/03/04/05-1 LCN
20-Pin Plastic DIP	0 to 70°C	ADC0804-1 CN
20-Pin Plastic SO	0 to 70°C	ADC0803/04-1 CD
20-Pin Plastic SO	−40°C to 85°C	ADC0803/04-1 LCD

BLOCK DIAGRAM


V_IN(+)
6
V_IN(−)
7
Σ
+
−
V_REF/2
9
A GND
8
LADDER AND DECODER
AUTO ZERO COMPARATOR
V_CC
20
OUTPUT LATCHES
D7 (MSB) (11)
D6 (12)
D5 (13)
D4 (14)
D3 (15)
D2 (16)
D1 (17)
D0 (LSB) (18)
SAR
D GND
10
LE
OE
WR
3
8-BIT SHIFT REGISTER
CLOCK
CS
1
S
INTR FF
R
Q̄
RD
2
5
INTR
4
CLK IN
19
CLK R
BD09100S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6.5	V
	Logic control input voltages	−0.3 to +16	V
	All other input voltages	−0.3 to (V_{CC} +0.3)	V
T_A	Operating temperature range ADC0801/02-1 F	−55 to +125	°C
	ADC0803/04-1 LCD	−40 to +85	°C
	ADC0801/02/03-1 LCF	−40 to +85	°C
	ADC0801/02/03/04/05-1 LCN	−40 to +85	°C
	ADC0803/04-1 CD	0 to +70	°C
	ADC0804-1 CN	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation $T_A = 25°C$ (still air)[1] F package N package D package	 1560 1690 1390	 mW mW mW

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 12.5mW/°C
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V$, $f_{CLK} = 1MHz$, $T_{MIN} \leqslant T_A \leqslant T_{MAX}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ADC0801/2/3/4/5			UNIT
			Min	Typ	Max	
	ADC0801 Relative accuracy error (adjusted)	Full-Scale adjusted			0.25	LSB
	ADC0802 Relative accuracy error (unadjusted)	$\frac{V_{REF}}{2} = 2.500V_{DC}$			0.50	LSB
	ADC0803 Relative accuracy error (adjusted)	Full-Scale adjusted			0.50	LSB
	ADC0804 Relative accuracy error (unadjusted)	$\frac{V_{REF}}{2} = 2.500V_{DC}$			1	LSB
	ADC0805 Relative accuracy error (unadjusted)	$\frac{V_{REF}}{2}$ = has no connection			1	LSB
R_{IN}	$\frac{V_{REF}}{2}$ Input resistance	$V_{CC} = 0V^2$	400	680		Ω
	Analog input voltage range		−0.05		V_{CC} +0.05	V
	DC common-mode error	Over analog input voltage range		1/16	1/8	LSB
	Power supply sensitivity	$V_{CC} = 5V \pm 10\%^1$		1/16		LSB

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 5.0V$, $f_{CLK} = 1MHz$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ADC0801/2/3/4/5			UNIT
			Min	Typ	Max	
Control inputs						
V_{IH}	Logical "1" input voltage	$V_{CC} = 5.25V_{DC}$	2.0		15	V_{DC}
V_{IL}	Logical "0" input voltage	$V_{CC} = 4.75V_{DC}$			0.8	V_{DC}
I_{IH}	Logical "1" input current	$V_{IN} = 5V_{DC}$		0.005	1	μA_{DC}
I_{IL}	Logical "0" input current	$V_{IN} = 0V_{DC}$	-1	-0.005		μA_{DC}
Clock in and clock R						
$V_{T}+$	Clock in positive-going threshold voltage		2.7	3.1	3.5	V_{DC}
$V_{T}-$	Clock in negative-going threshold voltage		1.15	1.8	2.1	V_{DC}
V_H	Clock in hysteresis $(V_{T+}) - (V_{T-})$		0.6	1.3	2.0	V_{DC}
V_{OL}	Logical "0" clock R output voltage	$I_{OL} = 360\mu A$, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
V_{OH}	Logical "1" clock R output voltage	$I_{OH} = -360\mu A$, $V_{CC} = 4.75V_{DC}$	2.4			V_{DC}
Data output and $\overline{INTR}$						
V_{OL}	Logical "0" output voltage					
	Data outputs	$I_{OL} = 1.6mA$, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
	$\overline{INTR}$ outputs	$I_{OL} = 1.0mA$, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
V_{OH}	Logical "1" output voltage	$I_{OH} = -360\mu A$, $V_{CC} = 4.75V_{DC}$	2.4			V_{DC}
		$I_{OH} = -10\mu A$, $V_{CC} = 4.75V_{DC}$	4.5			V_{DC}
I_{OZL}	3-State output leakage	$V_{OUT} = 0V_{DC}$, $\overline{CS}$ = Logical "1"	-3			μA_{DC}
I_{OZH}	3-State output leakage	$V_{OUT} = 5V_{DC}$, $\overline{CS}$ = Logical "1"			3	μA_{DC}
I_{SC}	+ Output short-circuit current	$V_{OUT} = 0V$, $T_A = 25°C$	4.5	12		mA_{DC}
I_{SC}	- Output short-circuit current	$V_{OUT} = V_{CC}$, $T_A = 25°C$	9.0	30		mA_{DC}
I_{CC}	Power supply current	$f_{CLK} = 1MHz$, $V_{REF/2}$ = Open, $\overline{CS}$ = Logical "1", $T_A = 25°C$		3.0	3.5	mA

NOTES:
1. Analog inputs must remain within the range: $-0.05 \leq V_{IN} \leq V_{CC} + 0.05V$.
2. See typical performace characteristics for input resistance at $V_{CC} = 5V$.

AC ELECTRICAL CHARACTERISTICS

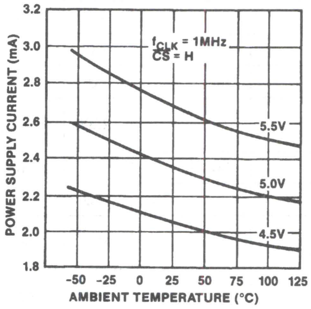
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	ADC0801/2/3/4/5			UNIT
					Min	Typ	Max	
	Conversion time			$f_{CLK} = 1MHz^1$	66		73	µs
f_{CLK}	Clock frequency[1]				0.1	1.0	3.0	MHz
	Clock duty cycle[1]				40		60	%
CR	Free-running conversion rate			$\overline{CS} = 0$, $f_{CLK} = 1MHz$ $\overline{INTR}$ tied to $\overline{WR}$			13690	conv/s
$t_{W(\overline{WR})L}$	Start pulse width			$\overline{CS} = 0$	30			ns
t_{ACC}	Access time	Output	$\overline{RD}$	$\overline{CS} = 0$, $C_L = 100pF$		75	100	ns
t_{1H}, t_{0H}	Three-State control	Output	$\overline{RD}$	$CL = 10pF$, $R_L = 10k\Omega$ See 3-State test circuit		70	100	ns
t_{W1}, t_{R1}	$\overline{INTR}$ delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
C_{IN}	Logic input = capacitance					5	7.5	pF
C_{OUT}	3-State output capacitance					5	7.5	pF

NOTE:

1. Accuracy is guaranteed at $f_{CLK} = 1MHz$. Accuracy may degrade at higher clock frequencies.

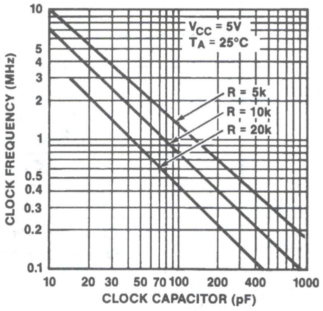
TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Current vs Temperature



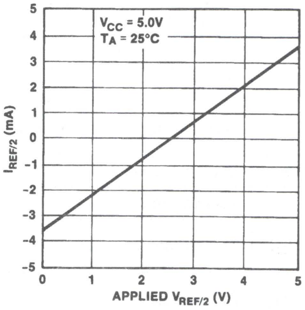
OP19000S

Clock Frequency vs Clock Capacitor



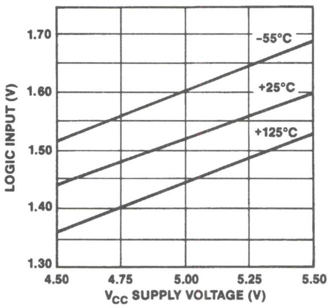
OP19010S

Input Current vs Applied Voltage at $V_{REF/2}$ Pin



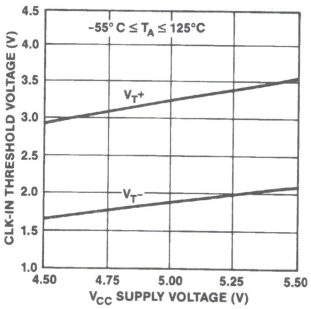
OP19020S

Logic Input Threshold Voltage vs Supply Voltage



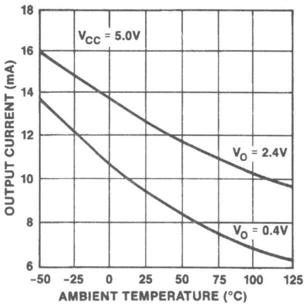
OP19030S

CLK-IN Threshold Voltage vs Supply Voltage



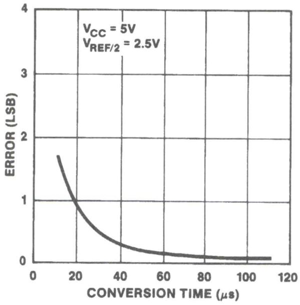
OP19040S

Output Current vs Temperature

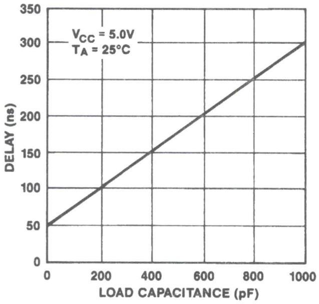


OP19050S

Full Scale Error vs Conversion Time

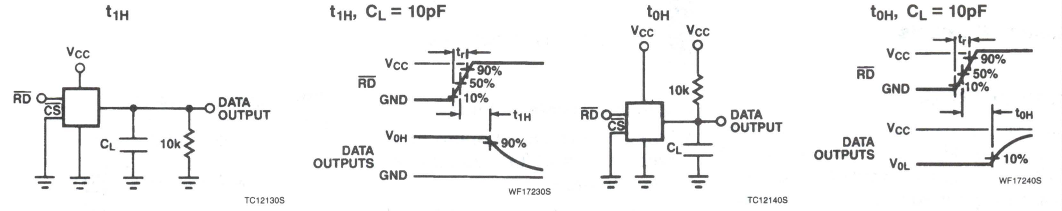


Delay From $\overline{RD}$ Falling Edge to Data Valid vs Load Capacitance



OP19070S

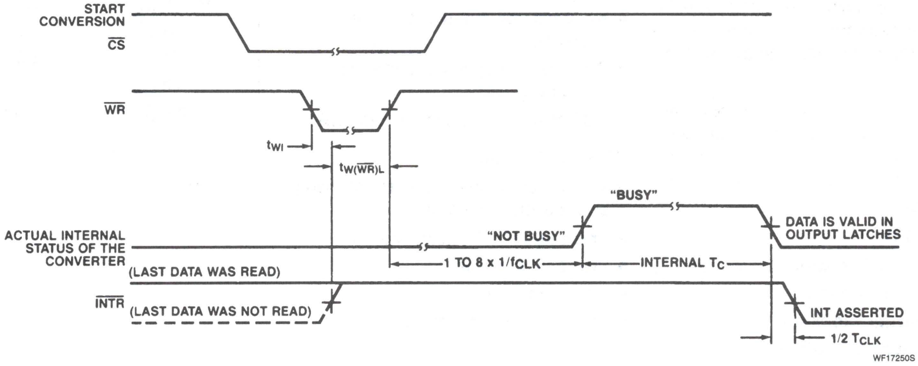
3-STATE TEST CIRCUITS AND WAVEFORMS (ADC0801-1)

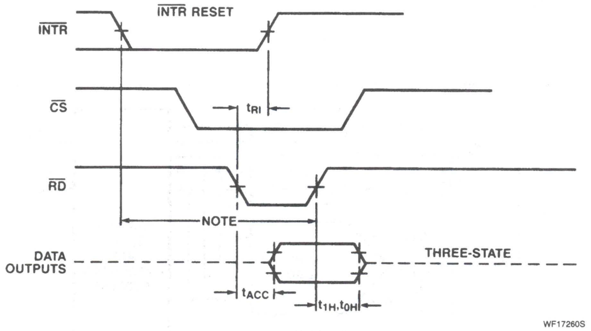

t_{1H}
V_{CC}
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C_L
10k
TC12130S
t_{1H}, C_L = 10pF
t_r
V_{CC}
$\overline{RD}$
GND
90%
50%
10%
t_{1H}
V_{OH}
DATA OUTPUTS
GND
90%
WF17230S
t_{0H}
V_{CC}
V_{CC}
10k
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C_L
TC12140S
t_{0H}, C_L = 10pF
t_r
V_{CC}
$\overline{RD}$
GND
90%
50%
10%
t_{0H}
V_{CC}
DATA OUTPUTS
V_{OL}
10%
WF17240S

NOTE:
t_r = 20ns

NOTE:
t_r = 20ns

TIMING DIAGRAMS (All timing is measured from the 50% voltage points)


START CONVERSION
$\overline{CS}$
$\overline{WR}$
t_{WI}
$t_{W(\overline{WR})L}$
"BUSY"
ACTUAL INTERNAL STATUS OF THE CONVERTER
"NOT BUSY"
DATA IS VALID IN OUTPUT LATCHES
1 TO 8 x 1/f_{CLK}
INTERNAL T_C
(LAST DATA WAS READ)
$\overline{INTR}$
(LAST DATA WAS NOT READ)
INT ASSERTED
1/2 T_{CLK}
WF17250S


$\overline{INTR}$ RESET
$\overline{INTR}$
$\overline{CS}$
t_{RI}
$\overline{RD}$
NOTE
DATA OUTPUTS
THREE-STATE
t_{ACC}
t_{1H}, t_{0H}
WF17260S

Output Enable and Reset $\overline{INTR}$

NOTE:
Read strobe must occur 8 clock periods ($8/f_{clk}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Signetics

Linear Products

ADC0820

8-Bit, High-Speed, µP-Compatible A/D Converter With Track/Hold Function

Preliminary Specification

DESCRIPTION

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5µs conversion time while dissipating a maximum 75mW of power. The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals slewing at less than 100mV/µs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

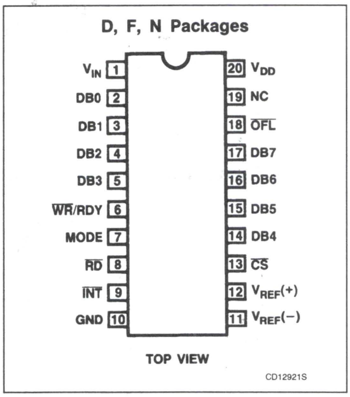
FEATURES

- **Built-in track-and-hold function**
- **No missing codes**
- **No external clocking**
- **Single supply — $5V_{DC}$**
- **Easy interface to all microprocessors, or operates stand-alone**
- **Latched 3-State outputs**
- **Logic inputs and outputs meet both MOS and TTL voltage level specifications**
- **Operates ratiometrically or with any reference value equal to or less than V_{DD}**
- **0V to 5V analog input voltage range with single 5V supply**
- **No zero- or full-scale adjust required**
- **Overflow output available for cascading**
- **0.3″ standard width 20-pin DIP**

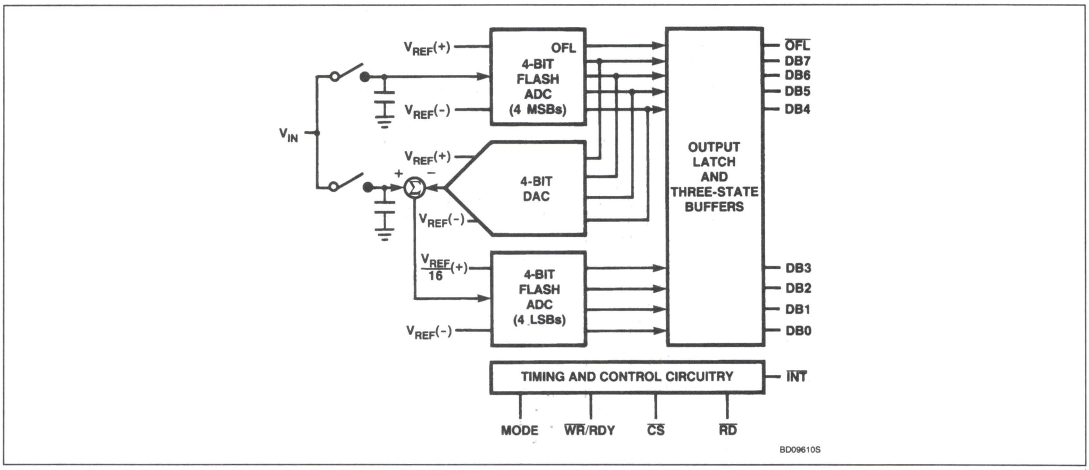
APPLICATIONS

- **Microprocessor-based monitoring and control systems**
- **Transducer/µP interface**
- **Process control**
- **Logic analyzers**
- **Test and measurement**

PIN CONFIGURATION


D, F, N Packages
V_IN 1
DB0 2
DB1 3
DB2 4
DB3 5
WR/RDY 6
MODE 7
RD 8
INT 9
GND 10
20 V_DD
19 NC
18 OFL
17 DB7
16 DB6
15 DB5
14 DB4
13 CS
12 V_REF(+)
11 V_REF(−)
TOP VIEW
CD12921S

BLOCK DIAGRAM


V_IN
V_REF(+)
V_REF(-)
OFL
4-BIT FLASH ADC (4 MSBs)
V_REF(+)
V_REF(-)
4-BIT DAC
Σ
+
−
V_REF/16 (+)
V_REF(-)
4-BIT FLASH ADC (4 LSBs)
OUTPUT LATCH AND THREE-STATE BUFFERS
OFL
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
TIMING AND CONTROL CIRCUITRY
INT
MODE
WR/RDY
CS
RD
BD09610S

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	ADC0820BNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820BNED
20-Pin Plastic DIP	0 to +70°C	ADC0820CNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820CNED
20-Pin Plastic DIP	−40°C to +85°C	ADC0820BSAN
20-Pin Plastic SO package	−40°C to +85°C	ADC0820BSAD
20-Pin Plastic DIP	−40°C to +85°C	ADC0820CSAN
20-Pin Plastic SO package	−40°C to +85°C	ADC0820CSAD
20-Pin Ceramic DIP	−55°C to +125°C	ADC0820BSEF
20-Pin Ceramic DIP	−55°C to +125°C	ADC0820CSEF

PIN DESCRIPTION

PIN NO	SYMBOL	DESCRIPTION
1	V_{IN}	Analog input; range = GND $\leqslant V_{IN} \leqslant V_{DD}$
2	DB0	3-state data output — Bit 0 (LSB)
3	DB1	3-state data output — Bit 1
4	DB2	3-state data output — Bit 2
5	DB3	3-state data output — Bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** $\overline{WR}$: With $\overline{CS}$ Low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see Figures 3a and 3b). **RD Mode** RDY: This is an open-drain output (no internal pull-up device). RDY will go Low after the falling edge of $\overline{CS}$; RDY will go 3-State when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see Figure 1).
7	Mode	Mode: Mode selection input — it is internally tied to GND through a 30μA current source. RD Mode: When mode is Low. WR-RD Mode: When mode is High.
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ Low, the 3-State data outputs (DB0 − DB7) will be activated when $\overline{RD}$ goes Low. $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (T_I ~ 800ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see Figures 3a and 3b). **RD Mode** With $\overline{CS}$ Low, the conversion will start with $\overline{RD}$ going Low; also, $\overline{RD}$ will enable the 3-State data outputs at the completion of the conversion. RDY going 3-State and $\overline{INT}$ going Low indicate the completion of the conversion (see Figure 1).

PIN DESCRIPTION (Continued)

PIN NO	SYMBOL	DESCRIPTION
9	$\overline{\text{INT}}$	**WR-RD Mode** $\overline{\text{INT}}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{\text{INT}}$ will go Low ~ 800ns (the preset internal time out, t_I) after the rising edge of $\overline{\text{WR}}$ (see Figure 3a); or $\overline{\text{INT}}$ will go Low after the falling edge of $\overline{\text{RD}}$, if $\overline{\text{RD}}$ goes Low prior to the 800ns time out (see Figure 3b). $\overline{\text{INT}}$ is reset by the rising edge of $\overline{\text{RD}}$ or $\overline{\text{CS}}$ (see Figures 3a and 3b). **RD Mode** $\overline{\text{INT}}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{\text{INT}}$ is reset by the rising edge of $\overline{\text{RD}}$ or $\overline{\text{CS}}$ (see Figure 1).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \leqslant V_{REF}(-) \leqslant V_{REF}(+)$
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \leqslant V_{REF}(+) \leqslant V_{DD}$.
13	$\overline{\text{CS}}$	$\overline{\text{CS}}$ must be Low in order for the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to be recognized by the converter.
14	DB4	3-State data output — Bit 4
15	DB5	3-State data output — Bit 5
16	DB6	3-State data output — Bit 6
17	DB7	3-State data output — Bit 7 (MSB)
18	$\overline{\text{OFL}}$	Overflow output — if the analog input is higher than the $V_{REF}(+)-\frac{1}{2}$ LSB, $\overline{\text{OFL}}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit).
19	NC	No connection
20	V_{DD}	Power supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	7	V
	Logic control inputs	-0.2 to $V_{DD} + 0.2$	V
	Voltage at other inputs and output	-0.2 to $V_{DD} + 0.2$	V
T_{STG}	Storage temperature range	-65 to $+150$	°C
P_D	Maximum power dissipation[3] $T_A = 25°C$ (still-air)		
	F package	1560	mW
	N package	1690	mW
	D package	1390	mW
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C
T_A	Operating ambient temperature range	$T_{MIN} \leqslant T_A \leqslant T_{MAX}$	
	ADC0820BSEF/CSEF	-55 to $+125$	°C
	ADC0820BSAN/CSAN/BSAD/CSAD	-40 to $+85$	°C
	ADC0820BNEN/CNEN/BNED/CNED	0 to $+70$	°C

NOTES:

1. Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
2. All voltages are measured with respect to GND, unless otherwise specified.
3. Derate above 25°C, at the following rates:
   F package at 12.5mW/°C.
   N package at 13.5mW/°C.
   D package at 11.1mW/°C.

DC ELECTRICAL CHARACTERISTICS RD mode (Pin 7 = 0), V_{DD} = 5V, $V_{REF}(+)$ = 5V, and $V_{REF}(-)$ = GND, unless otherwise specified. Limits apply from T_{MIN} to T_{MAX}.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[3]	Max	
	Resolution			8	8	8	bits
	Unadjusted error[1]	ADC0820B ADC0820C				± ½ ± 1	LSB LSB
R_{REF}	Reference resistance			1	1.6	4	kΩ
$V_{REF}(+)$	Input voltage			$V_{REF}(-)$		V_{DD}	V
$V_{REF}(-)$	Input voltage			GND		$V_{REF}(+)$	V
V_{IN}	Input voltage			GND − 0.1		V_{DD} + 0.1	V
	Maximum analog input leakage current	$\overline{CS}$ = V_{DD} V_{IN} = V_{DD} V_{IN} = GND		−3		3	µA
	Power supply sensitivity	V_{DD} = 5V± 5%			± 1⁄16	± ¼	LSB
$V_{IN(1)}$	Logical "1" input voltage	V_{DD} = 5.25V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.0		V_{DD}	V
			Mode	3.5		V_{DD}	V
$V_{IN(0)}$	Logical "0" input voltage	V_{DD} = 4.75V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	GND		0.8	V
			Mode	GND		1.5	V
$I_{IN(1)}$	Logical "1" input current	$V_{IN(1)}$ = 5V; $\overline{CS}$, $\overline{RD}$ $V_{IN(1)}$ = 5V; $\overline{WR}$ $V_{IN(1)}$ = 5V; Mode			 30	1 3 200	µA µA µA
$I_{IN(0)}$	Logical "0" input current	$V_{IN(0)}$ = 0V; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−1			µA
$V_{OUT(1)}$	Logical "1" output voltage	V_{DD} = 4.75V, I_{OUT} = −360µA; DB0 − DB7, $\overline{OFL}$, $\overline{INT}$		2.4	4.6		V
		V_{DD} = 4.75V, I_{OUT} = −10µA DB0 − DB7, $\overline{OFL}$, $\overline{INT}$		4.5	4.74		V
$V_{OUT(0)}$	Logical "0" output voltage	V_{DD} = 4.75V, I_{OUT} = 1.6mA; DB0 − DB7, $\overline{OFL}$, $\overline{INT}$, RDY			0.2	0.4	V
I_{OZ}	3-state output current	V_{OUT} = 5V; DB0 − DB7, RDY V_{OUT} = 0V; DB0 − DB7, RDY		 −3		3 	µA µA
I_{SOURCE}	Output source current	V_{OUT} = 0V, DB0 − DB7, $\overline{OFL}$ $\overline{INT}$		6 4.5	12 8		mA mA
I_{SINK}	Output sink current	V_{OUT} = 5V; DB0 − DB7, $\overline{OFL}$, $\overline{INT}$, RDY		7	20		mA
I_{DD}	Supply current	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0			6	15	mA
V_{DD}	Range			4.5		5.5	V

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

AC ELECTRICAL CHARACTERISTICS $V_{DD} = 5V$, $t_R = t_F = 20ns$, $V_{REF(+)} = 5V$, $V_{REF(-)} = 0V$, and $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS[4]			UNIT
				Min	Typ[3]	Max	
t_{CRD}	Conversion time for RD mode		Mode = 0, Figure 1		1.6	2.5	μs
t_{ACC0}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode = 0, Figure 1		$t_{CRD} + 20$	$t_{CRD} + 50$	ns
t_{CWR-RD}	Conversion time for WR-RD mode		Mode = V_{DD}, $t_{WR} = 600ns$, $t_{RD} = 600ns$; Figures 3a and 3b			1.52	μs
t_{WR}	Write time	Min	Mode = V_{DD}, Figures 3a and 3b[2]	600			ns
		Max				50	μs
t_{RD}	Read time	Min	Mode = V_{DD}, Figures 3a and 3b[2]	600			ns
t_{ACC1}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode = V_{DD}, $t_{RD} < t_I$; Figure 3b, $C_L = 15pF$		190	280	ns
			$C_L = 100pF$		210	320	ns
t_{ACC2}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode = V_{DD}, $t_{RD} > t_I$; Figure 3a, $C_L = 15pF$		70	120	ns
			$C_L = 100pF$		90	150	ns
t_I	Internal comparison time		Mode = V_{DD}; Figures 2 and 3a, $C_L = 50pF$		800	1300	ns
t_{1H}, t_{0H}	Three-state control (delay from rising edge of $\overline{RD}$ to Hi-Z state)		$R_L = 1k\Omega$, $C_L = 10pF$		100	200	ns
$t_{\overline{INT}L}$	Delay from rising edge of $\overline{WR}$ to falling edge of $\overline{INT}$		Mode = V_{DD}, $C_L = 50pF$ $t_{RD} > t_I$; Figure 3a			t_I	ns
			$t_{RD} < t_I$; Figure 3b		$t_{RD} + 200$	$t_{RD} + 290$	ns
$t_{\overline{INT}H}$	Delay from rising edge of $\overline{RD}$ to rising edge of $\overline{INT}$		Figures 1, 3a, and 3b, $C_L = 50pF$		125	225	ns
$t_{\overline{INT}HWR}$	Delay from rising edge of $\overline{WR}$ to rising edge of $\overline{INT}$		Figure 2, $C_L = 50pF$		175	270	ns
t_{RDY}	Delay from $\overline{CS}$ to RDY		Figure 1, $C_L = 50pF$, Mode = 0		50	100	ns
t_{ID}	Delay from $\overline{INT}$ to output valid		Figure 2		20	50	ns
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$		Mode = V_{DD}, $t_{RD} < t_I$; Figure 3b		200	290	ns
t_P	Delay from end of conversion to next conversion		Figures 1, 2, 3a, and 3b[2]	500			ns
SR	Slew rate, tracking				0.1		V/μs
C_{VIN}	Analog input capacitance				45		pF
C_{OUT}	Logic output capacitance				5		pF
C_{IN}	Logic input capacitance				5		pF

NOTES:

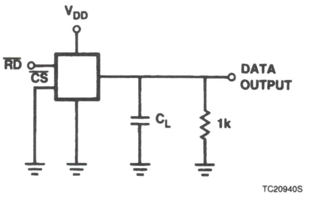
1. Unadjusted error includes offset, full-scale, and linearity errors.
2. Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified.
3. Typicals are at 25°C and represent most likely parametric norm.
4. Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

8-Bit, High-Speed, µP-Compatible A/D Converter With Track/Hold Function

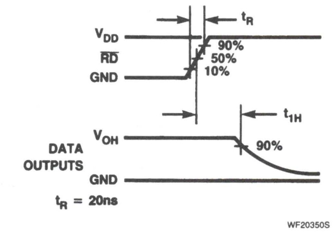
ADC0820

3-STATE TEST CIRCUITS AND WAVEFORMS

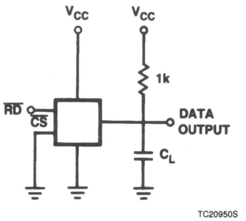
t_{1H}


V_{DD}
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C_L
1k
TC20940S

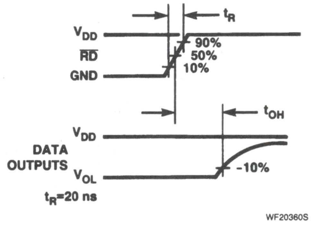
t_{1H} $C_L = 10pF$


t_R
V_{DD}
$\overline{RD}$
GND
90%
50%
10%
t_{1H}
V_{OH}
DATA OUTPUTS
90%
GND
t_R = 20ns
WF20350S

t_{0H}


V_{CC}
V_{CC}
1k
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C_L
TC20950S

t_{0H} $C_L = 10pF$


t_R
V_{DD}
$\overline{RD}$
GND
90%
50%
10%
t_{0H}
V_{DD}
DATA OUTPUTS
V_{OL}
-10%
t_R=20 ns
WF20360S

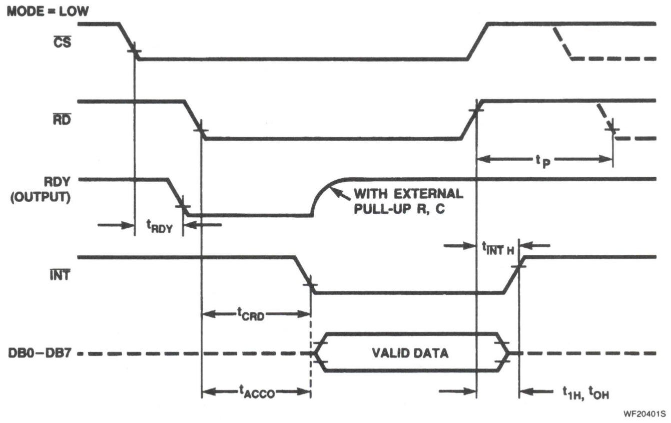

MODE = LOW
$\overline{CS}$
$\overline{RD}$
t_P
RDY (OUTPUT)
WITH EXTERNAL PULL-UP R, C
t_{RDY}
$t_{\overline{INT}H}$
$\overline{INT}$
t_{CRD}
DB0–DB7
VALID DATA
t_{ACCO}
t_{1H}, t_{0H}
WF20401S

Figure 1. RD Mode

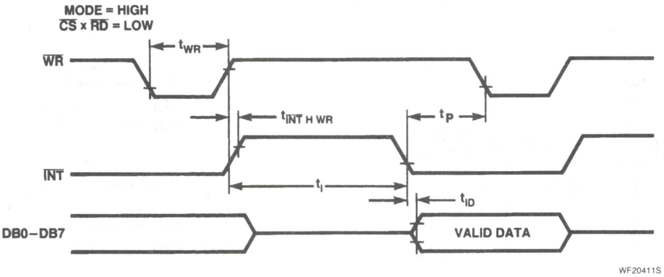
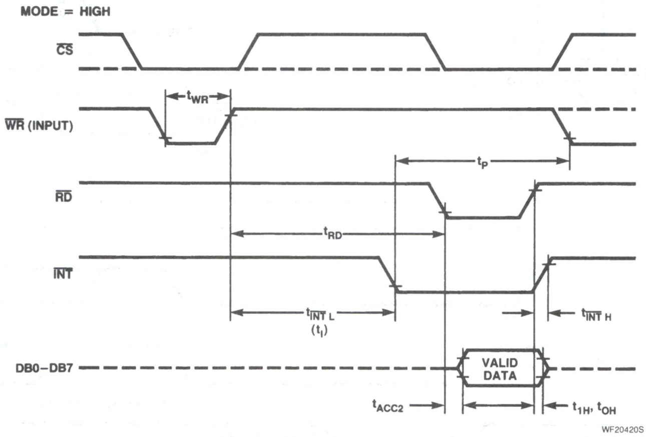
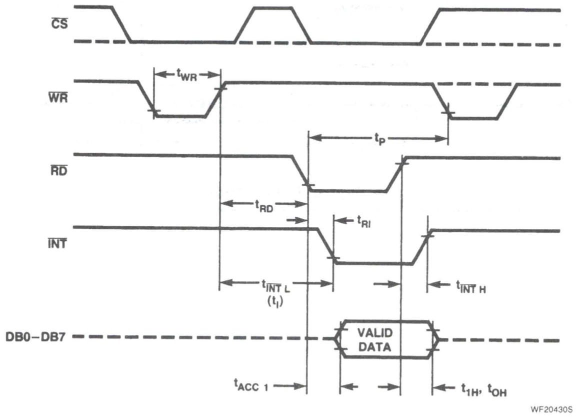

MODE = HIGH
$\overline{CS} \times \overline{RD}$ = LOW
$\overline{WR}$
t_{WR}
$t_{\overline{INT}\,H\,WR}$
t_P
$\overline{INT}$
t_I
t_{ID}
DB0–DB7
VALID DATA
WF20411S

Figure 2. Stand-Alone Mode


MODE = HIGH
$\overline{CS}$
$\overline{WR}$ (INPUT)
t_{WR}
t_P
$\overline{RD}$
t_{RD}
$\overline{INT}$
$t_{\overline{INT}\,L}$
(t_I)
$t_{\overline{INT}\,H}$
DB0–DB7
VALID DATA
t_{ACC2}
t_{1H}, t_{OH}
WF20420S

a. WR – RD Mode ($t_{RD} > t_I$)


$\overline{CS}$
$\overline{WR}$
t_{WR}
t_P
$\overline{RD}$
t_{RD}
t_{RI}
$\overline{INT}$
$t_{\overline{INT}\,L}$
(t_I)
$t_{\overline{INT}\,H}$
DB0–DB7
VALID DATA
$t_{ACC\,1}$
t_{1H}, t_{OH}
WF20430S

b. WR – RD Mode ($t_{RD} < t_I$)

Figure 3

8-Bit, High-Speed, µP-Compatible A/D Converter With Track/Hold Function

ADC0820

FUNCTIONAL DESCRIPTION

General Operation

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (Block Diagram). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

The Sampled-Data Comparator

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively-coupled input (Figure 4). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (Figure 4a) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_S, approximately 1.6V). In the second cycle (Figure 4b), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input ($V_{S'}$) becomes

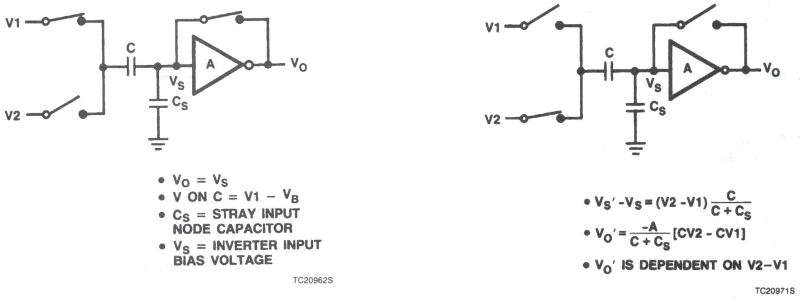
$$V_S' = V_S + (V2-V1)\,\frac{C}{C+C_S}$$

and the output will go High or Low depending on the sign of $V_S'-V_S$.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 5), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor (S switches) and opening all of the other switches. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

Architecture

In the ADC0820, 15 comparators are used in the MS and LS 4-bit flash A/D converters. The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.


V1
V2
C
A
V_O
V_S
C_S
• $V_O = V_S$
• V ON C = V1 − V_B
• C_S = STRAY INPUT NODE CAPACITOR
• V_S = INVERTER INPUT BIAS VOLTAGE
TC20962S
V1
V2
C
A
V_O
V_S
C_S
• $V_S' - V_S = (V2 - V1)\frac{C}{C+C_S}$
• $V_O' = \frac{-A}{C+C_S}[CV2 - CV1]$
• V_O' IS DEPENDENT ON V2−V1
TC20971S

a. Zeroing Phase

b. Compare Phase

Figure 4. Sampled Data Comparator

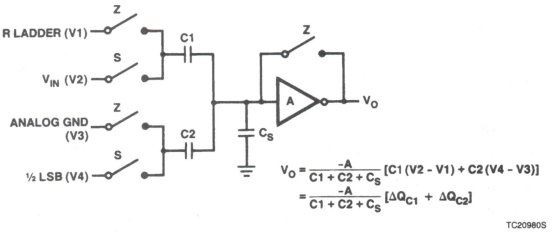

Z
R LADDER (V1)
S
V_{IN} (V2)
Z
ANALOG GND (V3)
S
½ LSB (V4)
C1
C2
Z
A
V_O
C_S
$V_O = \frac{-A}{C1+C2+C_S}[C1(V2-V1)+C2(V4-V3)]$
$= \frac{-A}{C1+C2+C_S}[\Delta Q_{C1} + \Delta Q_{C2}]$
TC20980S

Figure 5. ADC0820 Comparator (From MS Flash ADC)

To start a conversion in the WR-RD mode, the $\overline{\text{WR}}$ line is brought Low. At this instant the MS comparators go from zeroing to comparison mode (Figure 8). When $\overline{\text{WR}}$ is returned High after at least 600ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600ns later, the $\overline{\text{RD}}$ line may be pulled Low to latch the lower four data bits and finish the 8-bit conversion. When $\overline{\text{RD}}$ goes Low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{\text{WR}}$ is Low. In RD mode, sampling occurs during the first 800ns of $\overline{\text{RD}}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant, despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{\text{WR}}$ is Low the MS flash is in compare mode (connected to V_{IN}, and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

Digital Interface

The ADC0820 has two basic interface modes which are selected by strapping the Mode pin High or Low.

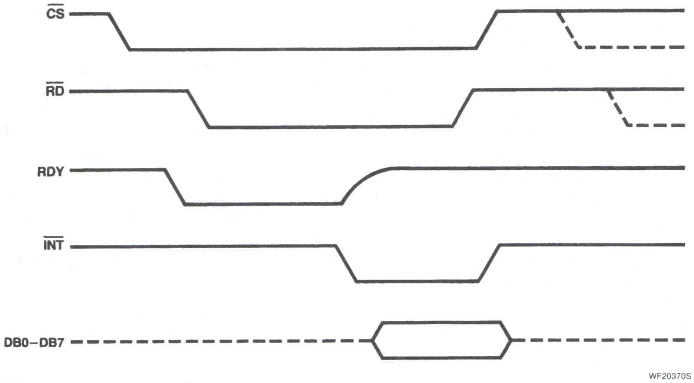
RD Mode (Figure 6a)

With the Mode pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{\text{RD}}$ Low until output data appears. An $\overline{\text{INT}}$ line is provided which goes Low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

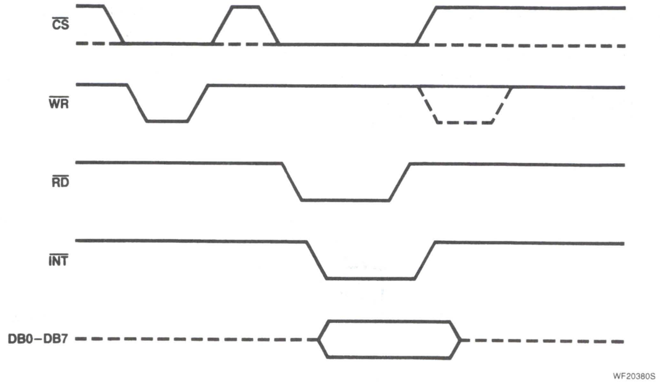
When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{\text{RD}}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800ns, the lower four bits are recovered.

WR Then RD Mode (Figures 6b and c)

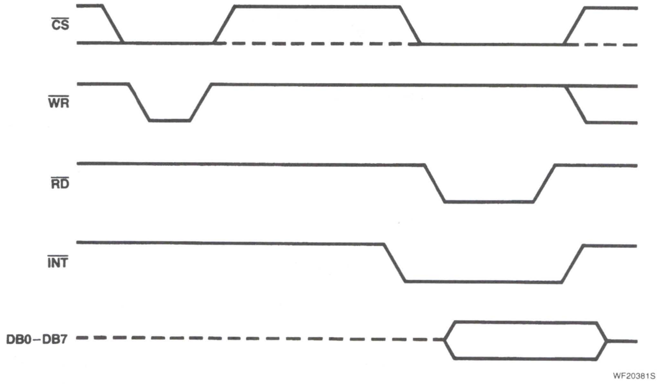
With the Mode pin tied High, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{\text{WR}}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for $\overline{\text{INT}}$ to go Low before reading the conversion result. $\overline{\text{INT}}$ will typically go Low 800ns after $\overline{\text{WR}}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{\text{INT}}$ and can exer-



a. RD Mode (Pin 7 is Low)



b. WR – RD Mode (Pin 7 is High and $t_{RD} < t_I$)



c. WR – RD Mode (Pin 7 is High and $t_{RD} > t_I$)

Figure 6

cise a Read after only 600ns. If this is done, $\overline{INT}$ will immediately go Low and data will appear at the outputs.

Stand-Alone (Figure 7)

For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied Low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800ns following $\overline{WR}$'s rising edge.

Other Interface Considerations

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50μs. When the MS flash ADC's sampled data comparators are in comparison mode ($\overline{WR}$ is Low), the input capacitors (C, Figure 5) must hold their charge. Switch leakage can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion, a new conversion cannot be started until this phase is complete. The minimum spec for this time is 500ns (t_P in Figure 1, 2, 3a, and 3b).

ANALOG CONSIDERATIONS

Reference and Input

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero- to full-scale input range of the A/D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF} = V_{REF}(+) - V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF} = 2V$, then 1 LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation and, in many cases, the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied, but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes.

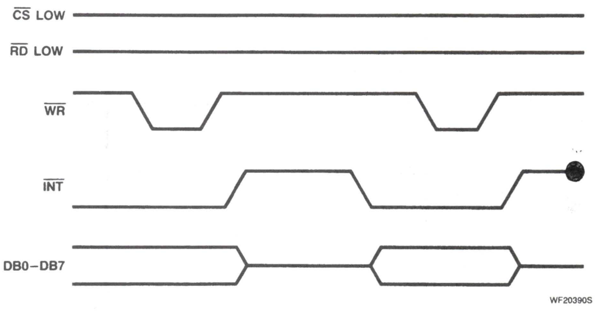

$\overline{CS}$ LOW
$\overline{RD}$ LOW
$\overline{WR}$
$\overline{INT}$
DB0–DB7
WF20390S

Figure 7. WR – RD Mode (Pin 7 is High) Stand-Alone Operation

Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. Figure 9 shows some of the configurations that are possible.

Input Current

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in Figure 10a. When a conversion starts ($\overline{WR}$ Low, WR-RD mode), all input switches close, connecting V_{IN} to 31 1pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase. In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5kΩ to 10kΩ). In addition, about 12pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in Figure 10b. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is Low. Since other factors force this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

Input Filtering

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect, the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is Low, so at least 600ns will be provided to charge the ADC's input capacitance. It is therefore not

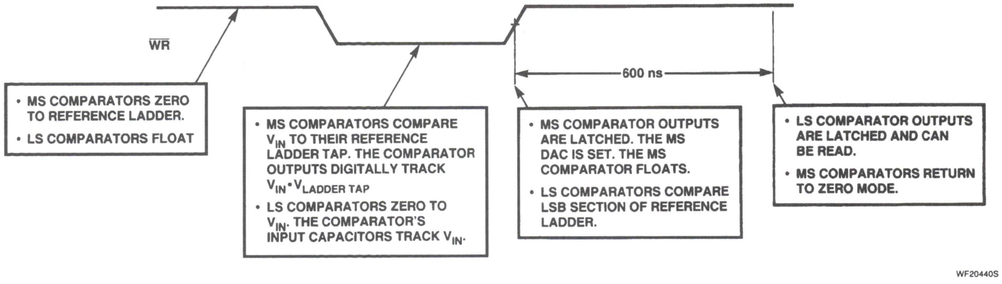
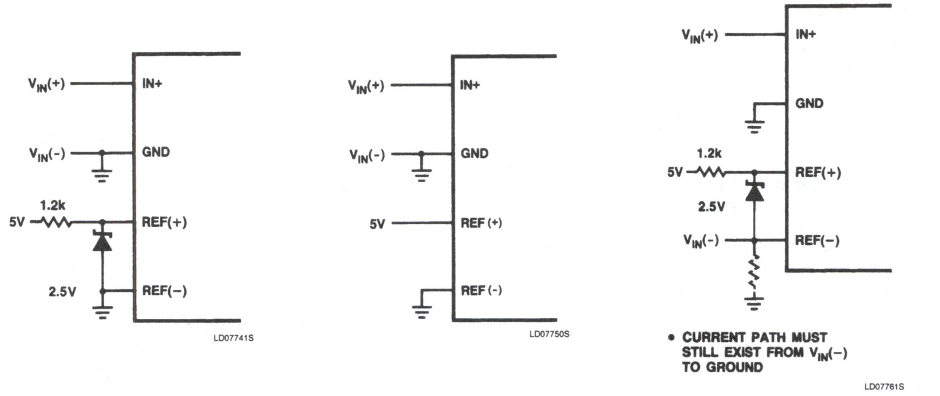
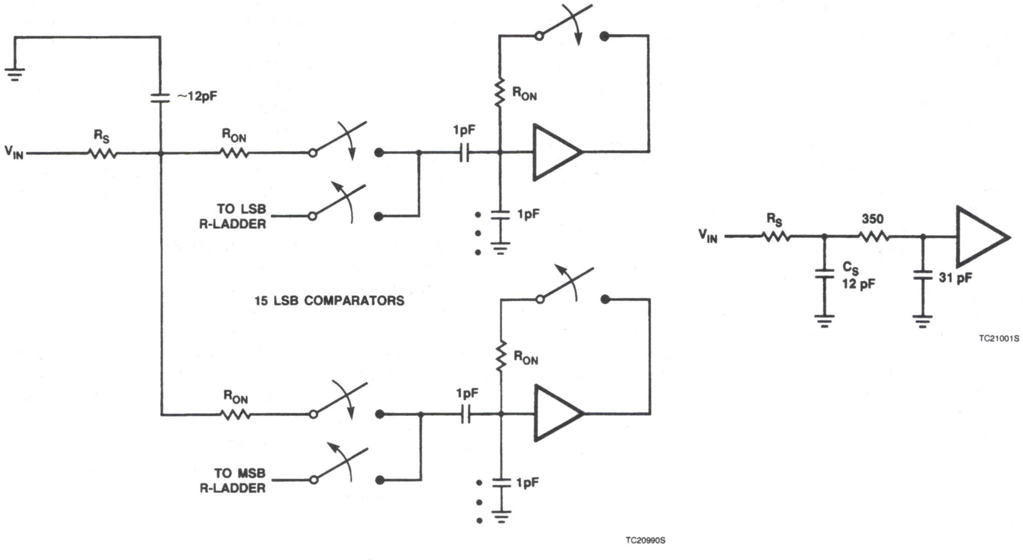

$\overline{WR}$
600 ns
• MS COMPARATORS ZERO TO REFERENCE LADDER.
• LS COMPARATORS FLOAT
• MS COMPARATORS COMPARE V_{IN} TO THEIR REFERENCE LADDER TAP. THE COMPARATOR OUTPUTS DIGITALLY TRACK $V_{IN} \cdot V_{LADDER\ TAP}$
• LS COMPARATORS ZERO TO V_{IN}. THE COMPARATOR'S INPUT CAPACITORS TRACK V_{IN}.
• MS COMPARATOR OUTPUTS ARE LATCHED. THE MS DAC IS SET. THE MS COMPARATOR FLOATS.
• LS COMPARATORS COMPARE LSB SECTION OF REFERENCE LADDER.
• LS COMPARATOR OUTPUTS ARE LATCHED AND CAN BE READ.
• MS COMPARATORS RETURN TO ZERO MODE.
WF20440S

Figure 8. Operating Sequence (WR – RD Mode)


$V_{IN}(+)$
IN+
$V_{IN}(-)$
GND
1.2k
5V
REF(+)
2.5V
REF(−)
LD07741S
5V
REF (+)
REF (-)
LD07750S
• CURRENT PATH MUST STILL EXIST FROM $V_{IN}(-)$ TO GROUND
LD07761S

a. External Reference 2.5V Full-Scale b. Power Supply as Reference c. Input not Referred to GND

Figure 9. Analog Input Options


~12pF
V_{IN}
R_S
R_{ON}
1pF
TO LSB R-LADDER
15 LSB COMPARATORS
TO MSB R-LADDER
TC20990S
350
C_S 12 pF
31 pF
TC21001S

a. b.

Figure 10

necessary to filter out these transients by putting an external cap on the V_{IN} terminal, if an input amplifier that can settle within 600ns is used to drive the input. The NE530 is a suitable op amp for driving the input of the ADC0820.

Inherent Sample-Hold

Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5µs, the time through which V_{IN} must be ½ LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is Low. Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100ns after the rising edge of $\overline{WR}$ (100ns due to internal logic propagation delay) will be the measured value.

Input signals with slew rates typically below 100mV/µs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1µs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7kHz waveforms.

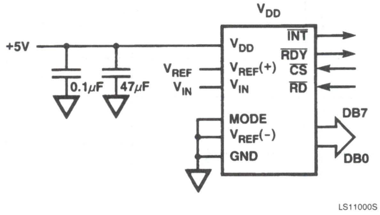

V_{DD}
+5V
0.1µF
47µF
V_{REF}
V_{IN}
V_{DD}
$V_{REF}(+)$
V_{IN}
MODE
$V_{REF}(-)$
GND
$\overline{INT}$
$\overline{RDY}$
$\overline{CS}$
$\overline{RD}$
DB7
DB0
LS11000S

Figure 11. 8-Bit Resolution Configuration

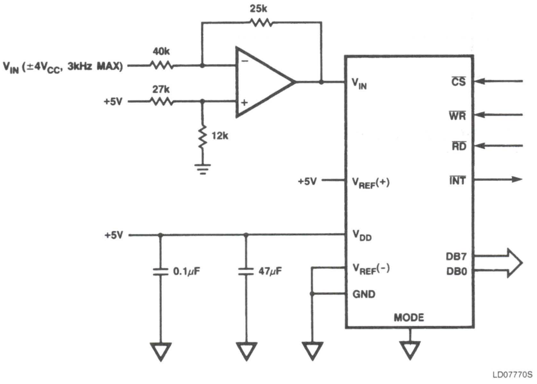

25k
40k
V_{IN} (±4V_{CC}, 3kHz MAX)
27k
+5V
12k
+5V
V_{IN}
$V_{REF}(+)$
V_{DD}
$V_{REF}(-)$
GND
MODE
$\overline{CS}$
$\overline{WR}$
$\overline{RD}$
$\overline{INT}$
DB7
DB0
0.1µF
47µF
LD07770S

Figure 12. Telecom A/D Converter

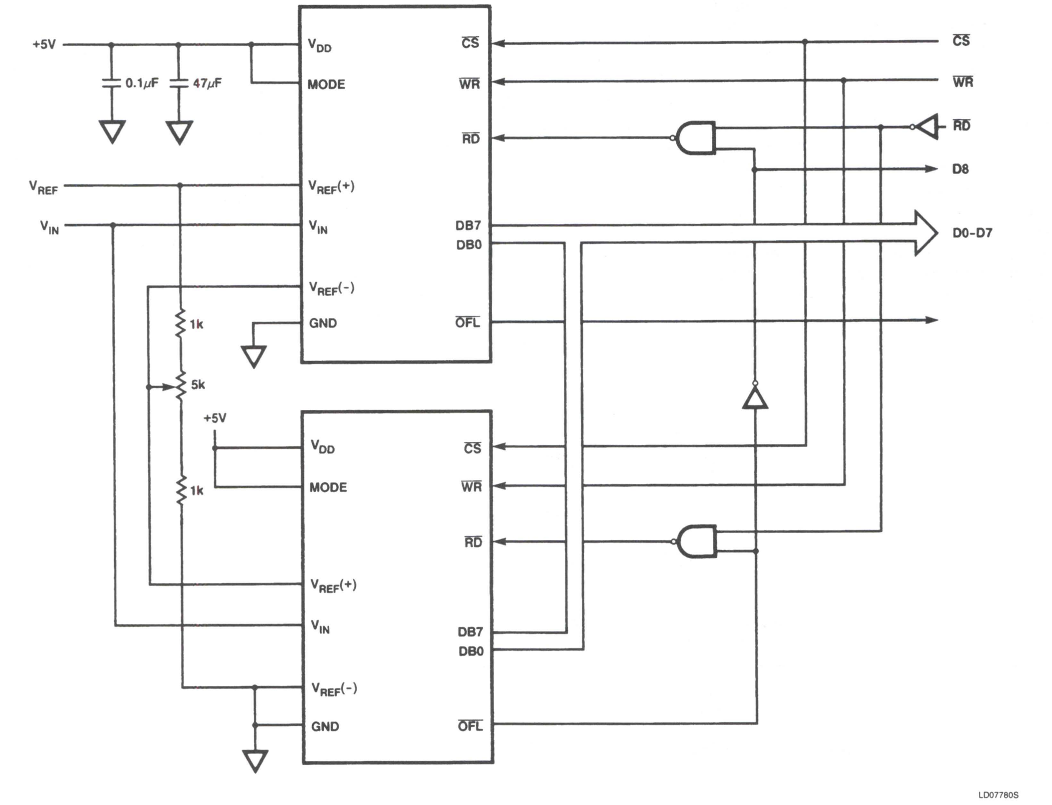

+5V
0.1µF
47µF
V_{REF}
V_{IN}
V_{DD}
MODE
$V_{REF}(+)$
V_{IN}
$V_{REF}(-)$
GND
$\overline{CS}$
$\overline{WR}$
$\overline{RD}$
DB7
DB0
$\overline{OFL}$
1k
5k
+5V
1k
V_{DD}
MODE
$V_{REF}(+)$
V_{IN}
$V_{REF}(-)$
GND
$\overline{CS}$
$\overline{WR}$
$\overline{RD}$
DB7
DB0
$\overline{OFL}$
$\overline{CS}$
$\overline{WR}$
$\overline{RD}$
D8
D0-D7
LD07780S

Figure 13. 9-Bit Resolution Configuration

Signetics

Linear Products

NE/SE5030
High-Speed Microprocessor-Compatible Analog-to-Digital Converter

Objective Specification

DESCRIPTION

The NE/SE5030 is a monolithic 10-bit, microprocessor-compatible Analog-to-Digital Converter which is manufactured on a high-speed bipolar process using thin film resistors. The conversion process is a new multi-step technique which combines parallel conversion and successive approximation, allowing complete 10-bit conversion in just 2.5 μs at the maximum 3MHz clock rate. The fast conversion rate makes the NE/SE5030 excellent for a wide range of applications where system throughput sampling rates up to 360kHz are required.

FEATURES

- **Microprocessor-compatible**
- **Fast conversion (2.5μs)**
- **Relative accuracy ¼ LSB typical**
- **2.5V signal input range**
- **Accomodates either unipolar or bipolar input**
- **TTL-compatible digital inputs/outputs**
- **No missing codes over temp range**
- **Three-state outputs**
- **High impedance analog input**
- **Low TC internal reference (5ppm/°C typical)**

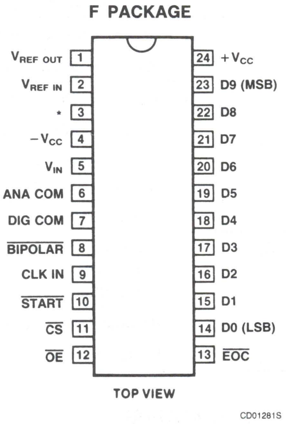
APPLICATIONS

- **Process control**
- **Test and measurement**
- **Machine tools**
- **Robotics**
- **Industrial monitoring**
- **High-speed waveform digitizing**
- **High-speed correlators**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Cerdip	0 to +70°C	NE5030F
24-Pin Cerdip	0 to +70°C	SE5030F

PIN CONFIGURATION



* Make no external connection

PIN NO.	SYMBOL	FUNCTION
1	$V_{REF\ OUT}$	2.5V reference output voltage of the temperature compensated internal reference.
2	$V_{REF\ IN}$	Reference input for the converter. (Connect pin 1 to pin 2 or connect an external 2.500V reference voltage to pin 2.)
3	*	Make no external connection.
4	V_{EE}	−5V (±5%) negative supply pin.
5	V_{IN}	Analog input voltage. Unipolar range 0V to $+V_{REF}$ Bipolar range $-V_{REF}/2$ to $+V_{REF}/2$
6	ANA COM	Analog common point to which all Analog signals are to be referenced.
7	DIG COM	Digital common point to which all digital signals are to be referenced.
8	$\overline{\text{BIPOLAR}}$	Logic input for selecting either unipolar or bipolar mode of operation. Logic high selects unipolar mode Logic low selects bipolar mode
9	CLOCK	Single phase clock signal input
10	$\overline{\text{START}}$	Start signal input. Low-going edge initiates a conversion cycle.
11	$\overline{\text{CS}}$	Chip Select. Must be low to enable conversion or read output data. Logic low causes normal operation (enables operation) Logic high inhibits conversion and holds output data lines in high impedance mode
12	$\overline{\text{OE}}$	Output enable. Logic low when $\overline{\text{CS}}$ is low enables output buffers Logic high puts outputs into the high impedance state
13	$\overline{\text{EOC}}$	End of Conversion output signal. This output voltage goes low after the end of a conversion. This output voltage is reset to a logic high by a low level on the $\overline{\text{OE}}$ pin.
14-23	D0 – D9	Three-state buffer outputs (D9 is MSB, D0 is LSB). When $\overline{\text{OE}}$ is low, the converted data word is available at these pins.
24	V_{CC}	+5V (±5%) positive supply voltage pin.

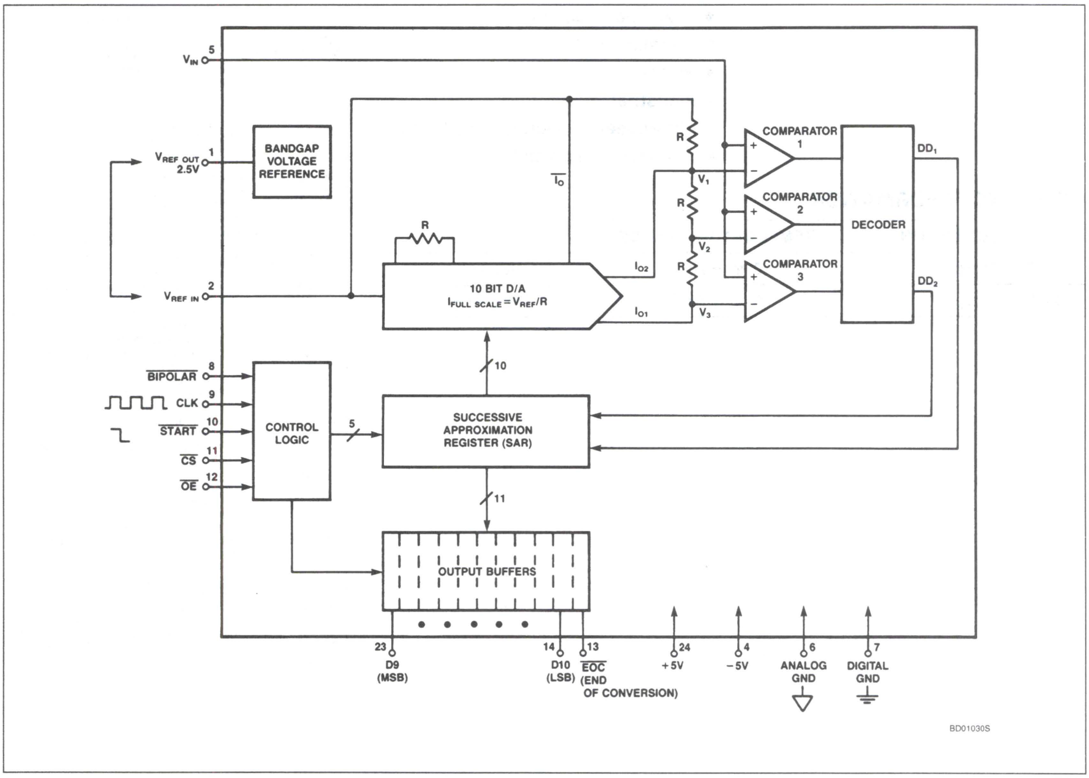
High-Speed Microprocessor-Compatible Analog-to-Digital Converter

NE/SE5030

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$+V_{CC}$	Positive supply voltage	+8	V
$-V_{CC}$	Negative supply voltage	−8	V
	Analog input range	±3.5	V
	Digital input voltage	−0.5 to V_{CC}	V
	Analog common to digital common	±1	V
	$V_{REF\ OUT}$ short-circuit to common	Indefinite	
	$V_{REF\ OUT}$ short-circuit to V_{CC}	60	seconds
	$V_{REF\ IN}$ applied voltage	0 to 5	V
	Digital output pins applied voltage to logic high output s	−0.5 to V_{CC}	V
	Digital output sink current	10	mA
T_A	Operating temperature range NE5030 SE5030	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−60 to +150	°C
P_D	Power dissipation	600	mW

BLOCK DIAGRAM



5 VIN
1 VREF OUT 2.5V
BANDGAP VOLTAGE REFERENCE
2 VREF IN
R
10 BIT D/A
IFULL SCALE = VREF/R
IO
IO2
IO1
R
V1
V2
V3
COMPARATOR 1
COMPARATOR 2
COMPARATOR 3
DECODER
DD1
DD2
10
8 BIPOLAR
9 CLK
10 START
11 CS
12 OE
CONTROL LOGIC
5
SUCCESSIVE APPROXIMATION REGISTER (SAR)
11
OUTPUT BUFFERS
23 D9 (MSB)
14 D10 (LSB)
13 EOC (END OF CONVERSION)
24 +5V
4 −5V
6 ANALOG GND
7 DIGITAL GND
BD01030S

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = –5V, T_A = 0 to 70°C for NE5030, T_A = –55 to +125°C for SE5030, F_{CLK} ≤3MHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		10	10	10	Bits
	Relative accuracy error[1, 2]			±1/4	±1/2	LSB
DNL	Differential linearity error[3]				10	bits
	Code width error			±1/4	±1/2	LSB
E_{FS}	Full-scale gain error	T_A = 25°C over operating temp range		±1 ±1	±2 ±5	LSB LSB
E_{UOS}	Unipolar offset error	T_A = 25°C over operating temp range			±0.5 ±1.0	LSB LSB
E_{BOS}	Bipolar offset error	T_A = 25°C over operating temp range			±0.5 ±1.0	LSB LSB
	Analog input range Unipolar Bipolar	 $\overline{\text{BIPOLAR}}$ = 2.0V $\overline{\text{BIPOLAR}}$ = 0.8V	 0 $-V_{REF}/2$		 $+V_{REF}$ $+V_{REF}/2$	 V V
I_B	Analog input bias current			1	5	µA
Z_{IN}	Analog input impedance		1	3		Megohms
V_{REF}	Reference voltage output	T_A = 25°C	2.495	2.500	2.505	V
TC_{REF}	Reference voltage drift[4]	over operating temp range		±1.25 (±5)	±2.5 (±10)	mV (ppm/°C)
$I_{L\ (REF)}$	Reference external load		2	2.5		mA
$I_{REF\ IN}$	Reference input current	$V_{REF\ IN}$ = 2.5V		2	3	mA
V_{CC}	Pos supply operating range		4.75	5	5.25	V
V_{EE}	Neg supply operating range		–4.75	–5	–5.25	V
PSR	Power supply rejection[5]	V_{CC} = 4.75 to 5.25V V_{EE} = –4.75 to –5.25V			±0.25	LSB
I_{CC}	Positive supply current	V_{CC} = 5.25V, V_{EE} = –5.25V		36	45	mA
I_{EE}	Negative supply current	V_{CC} = 5.25V, V_{EE} = –5.25V		50	60	mA
Logic inputs						
V_{IH}	Logic 1 input voltage		2.0			V
V_{IL}	Logic 0 input voltage				0.8	V
I_{IH}	Logic 1 input current	V_{IH} = 2.4V, T_A = 25°C V_{IH} = 2.4V, over operating temp range			10 20	µA µA
I_{IL}	Logic 0 input current	V_{IL} = 0.4V, T_A = 25°C V_{IL} = 0.4V, over operating temp range			200 400	µA µA
Logic outputs						
V_{OH}	Logic 1 output voltage	I_{OH} = –400µA, $\overline{CS}$ = $\overline{OE}$ = 0.8V	2.4	3.2		V
V_{OL}	Logic 0 output voltage	I_{OL} = 1.6mA, $\overline{CS}$ = $\overline{OE}$ = 0.8V		0.2	0.4	V
I_{OZ}	Three-state leakage	$\overline{OE}$ = 2.0V, V_{OL} = 0V or 5V, T_A = 25°C $\overline{OE}$ = 2.0V, V_{OL} = 0V or 5V, over temp		±10	±20 ±100	µA µA

NOTES:

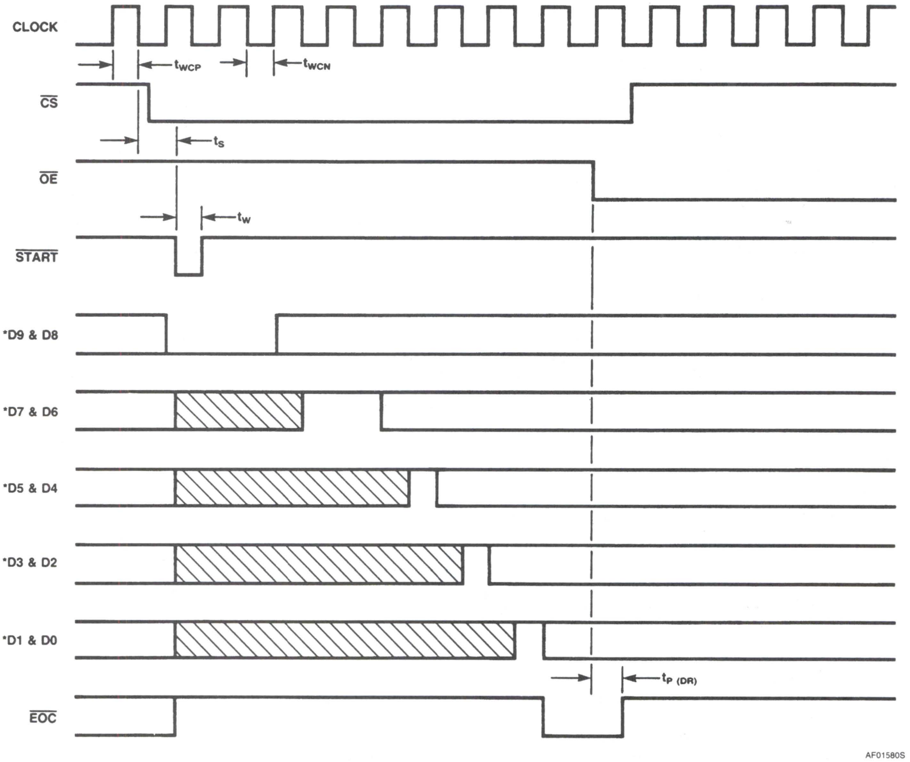
1. Specifications given in LSB refer to the weight of the least significant bit at the 10-bit level, which is 0.1% of the full scale voltage.
2. Relative accuracy is defined as the deviation of the actual code transition points from a straight line drawn between the first code transition point and the final code transition point.
3. Resolution for which the device is guaranteed to have no missing codes.
4. Deviation of the reference voltage output over the operating temperature range from its 25°C value.
5. Maximum change in the final code transition point. This will also result in a linear change in all lower order codes.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $V_{EE} = -5V$, $T_A = 25°C$, $f_{CLK} = 5MHz$

SYMBOL	PARAMETER	TO	FROM	EDGE	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
f_{CLK}	Max clock frequency				3.0[1]	4.0		MHz
t_{WCP}	Positive clock pulse width				90			ns
t_{WCN}	Negative clock pulse width				90			ns
t_{CONV}	Conversion time					$7.5/f_{CLK}$ [2]		ns
t_W	START pulse width				100			
t_S	Setup time	CLK	$\overline{START}$	HI-LOW	TBD	TBD		ns
$t_{P\ (DATA)}$	Access time	DB0 – DB9	$\overline{OE}$	HI-LOW		TBD	TBD	ns
$t_{P\ (3\text{-}STATE)}$	Disable time	Hi-Z	$\overline{OE}$	LOW-HI		TBD	TBD	ns
$t_{P\ (EDC)}$	Propagation delay	$\overline{EOC}$ Hi	$\overline{OE}$	HI-LOW		TBD	TBD	ns

NOTES:
1. Maximum clock frequency. Subject to change before product release.
2. Frequency in MHz.

TIMING DIAGRAM


CLOCK
t_{WCP}
t_{WCN}
$\overline{CS}$
t_S
$\overline{OE}$
t_W
$\overline{START}$
*D9 & D8
*D7 & D6
*D5 & D4
*D3 & D2
*D1 & D0
$t_{P\ (DR)}$
$\overline{EOC}$
AF01580S

* Timing diagram shows internal logic operation for the sake of short cycle operation. Data outputs are in Hi-Z state until $\overline{OE}$ and $\overline{CS}$ are both brought to a logic low.

High-Speed Microprocessor-Compatible Analog-to-Digital Converter

NE/SE5030

CIRCUIT DESCRIPTION

The SE/NE5030 is a microprocessor compatible, high speed, 10-bit Analog-to-Digital converter. The device uses a new multi-step parallel conversion scheme[1] which determines two bits of the digital word in each conversion step, permitting a fast 2.5μs conversion time.

Refer to the block diagram. The full-scale current of the DAC is V_{REF}/R. When conversion is initiated, the successive approximation register (SAR) directs the two MSB currents of the DAC (I9 and I8) to $\overline{I_O}$ and the remaining bit currents of the DAC (including the DAC R/2R termination current) to I_{O1}. This divides the input signal range into four equal subranges. The three latched comparators determine into which of these subranges the input voltage falls. The decoded outputs of these comparators determine the two MSBs (D9 and D8), which are stored in the SAR.

In each subsequent step, the SAR controls the DAC such that the complement of the previously determined bits are directed through I_{O2}; the bits currently being determined are directed through $\overline{I_O}$, and the remainder of the bits are directed through I_{O1}. In this manner the subrange containing the analog input voltage in the previous step is divided into four smaller subranges and two bits of the digital output are determined. At the end of five steps the SAR contains a 10-bit binary code which accurately represents the input signal to within ± ½ LSB.

FUNCTIONAL DESCRIPTION

With an external clock signal connected to the CLOCK IN pin, $\overline{\text{CS}}$ at a logic low, and $\overline{\text{OE}}$ at a logic high, a conversion cycle is initiated with the application of an external start pulse applied to the $\overline{\text{START}}$ pin. The SAR sequences through the conversion as described above. At the end of the conversion, the end-of-conversion flag ($\overline{\text{EOC}}$) goes low. The $\overline{\text{EOC}}$ flag can be used to interrupt a microprocessor or otherwise notify a processor or controller that a conversion is completed. $\overline{\text{OE}}$ may then be forced low (while holding $\overline{\text{CS}}$ low), enabling the three-state output buffers so that the converted word may be read. Bringing the $\overline{\text{OE}}$ pin low while the $\overline{\text{CS}}$ pin is low also resets the $\overline{\text{EOC}}$ flag to a logic high. It is recommended that $\overline{\text{OE}}$ be brought to a logic high prior to the application of another $\overline{\text{START}}$ pulse. If $\overline{\text{OE}}$ were to remain low during a conversion, the output buffers would be enabled and would switch states during the conversion. This switching can couple into the analog input through parasitic capacitances, causing erroneous conversion results.

The application of another START pulse while a conversion is in progress will halt the conversion in progress and begin a new conversion cycle. If a $\overline{\text{START}}$ pulse is received while the $\overline{\text{CS}}$ input is at a logic high, that $\overline{\text{START}}$ pulse is ignored. The outputs will be in the high impedance state as long as either $\overline{\text{CS}}$ or the $\overline{\text{OE}}$ input is at a logic high.

LOGIC INPUTS AND OUTPUTS

All the logic inputs ($\overline{\text{BIPOLAR}}$, CLOCK IN, $\overline{\text{START}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$) respond to TTL level signals and present one LS TTL load to the driving source. The logic outputs are capable of driving two TTL loads. If long digital lines or a heavily loaded bus must be driven, external logic buffers are recommended.

VOLTAGE REFERENCE

The internal voltage reference (2.5V ± 0.2%) is of a second order-corrected design. The output voltage is trimmed at the wafer level by the "Zener zap" technique to have a temperature coefficient of less than ± 10ppm/°C (average) over the operating temperature range. $V_{REF\ OUT}$ (Pin 1) and $V_{REF\ OUT}$ (Pin 2) are not internally connected and should be connected together close to the device. The voltage reference output (Pin 1) can provide up to 2mA to an external load for other system applications. The current drawn by any external load *must remain constant* during a conversion.

ANALOG INPUT

The analog input voltage to ge digitized is connected between V_{IN} (Pin 5) and Analog Common (Pin 6). The device operates in either a unipolar mode (input range of 0 to V_{REF}) or in a bipolar mode (input range of $-V_{REF}/2$ to $+V_{REF}/2$). The TTL compatible $\overline{\text{BIPOLAR}}$ input is used to select the mode.

When the $\overline{\text{BIPOLAR}}$ input is high, the device operates in the unipolar mode. The input range is then 0 to $+V_{REF}$ (2.5V nominal). The nominal value of the LSB is 2.44mV. The SE/NE5030 is designed to have a 1/2 LSB offset so that the analog input exactly corresponding to a given code will fall in the center of that code's input range. Thus, the ideal input voltage to cause the first transition (from 00 0000 0000 to 00 0000 0001) will occur for an input voltage of 1.22mV, and the final transition (from 11 1111 1110 to 11 1111 1111) will ideally occur for an input voltage of 2496.34mV, or 1.5 LSB below the 2.5V reference.

For bipolar operation, the $\overline{\text{BIPOLAR}}$ input is set to a logic low. This shifts the transfer curve of the A/D by $V_{REF}/2$ so that the input voltage range is now $-(V_{REF}/2)$ to $+(V_{REF}/2)$, or (−1.25V to +1.25V nominal). The ideal transition of code from 00 0000 0000 to 00 0000 0001 occurs at an input of −1248.78mV, and the final code transition (11 1111 1110 to 11 1111 1111 occurs at 1246.34mV.

The high input impedance of the SE/NE5030 analog input simplifies the requirements of the signal source driving the SE/NE5030, eliminating the need for specialized drive circuitry.

POWER SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

Since one LSB of the SE/NE5030 input is just 2.44mV, good layout and grounding techniques are crucial to attaining optimum performance.

The power supplies should be filtered, well regulated, and free of high-frequency noise. Use of noisy supplies will cause unstable output codes to be generated. The power supplies should be bypassed to Analog Common with tantalum or electrolytic capacitors in parallel with a small, high-frequency bypass. Suitable bypasses would be 22μF electrolytic capacitors with 0.1μF ceramic capacitors in parallel with them. These capacitors should be located close to the device.

Analog Common and Digital Common are not connected internally and should be connected together as close to the device as possible. Low impedance analog and digital common returns are important for optimum performance. The power supply returns should be connected to the Digital Common of the device. The Analog Common is the ground reference point for the internal voltage and should be connected directly to the Analog Common reference point of the system.

Coupling between the digital lines and the Analog Input should be minimized by careful printed circuit board layout. The layout should attempt to locate the analog circuitry and their interconnections as far from the logic circuitry as is possible. Use of wire wrap techniques or plug-in type boards is not recommended.

NOTE:

1. M. Kolluri: "A Multi-Step Parallel 10-Bit 1.5μs ADC," *ISSCC Digest of Technical Papers*, p 60 – 61; Feb 1984.

Signetics

NE5034
8-Bit High-Speed A/D Converter

Product Specification

Linear Products

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit analog-to-digital converter. It uses the successive approximation conversion technique, and includes the comparator, reference DAC, SAR, an internal clock and 3-State buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17μs. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

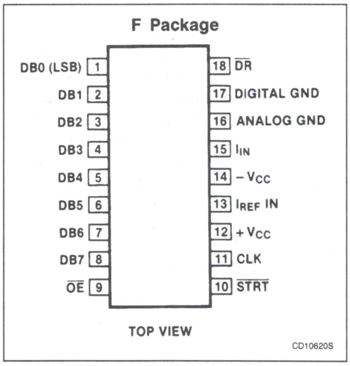
FEATURES

- **8-bit resolution and accuracy**
- **Accepts unipolar or bipolar inputs**
- **3-State output buffers for easy microprocessor interface**
- **Choice of internal or external clocking**
- **Short conversion time, 17μs typical using internal clock**

APPLICATIONS

- **All microprocessor-based monitoring and control systems requiring analog signal inputs**
- **Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls**
- **Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high-speed 8-bit building blocks**

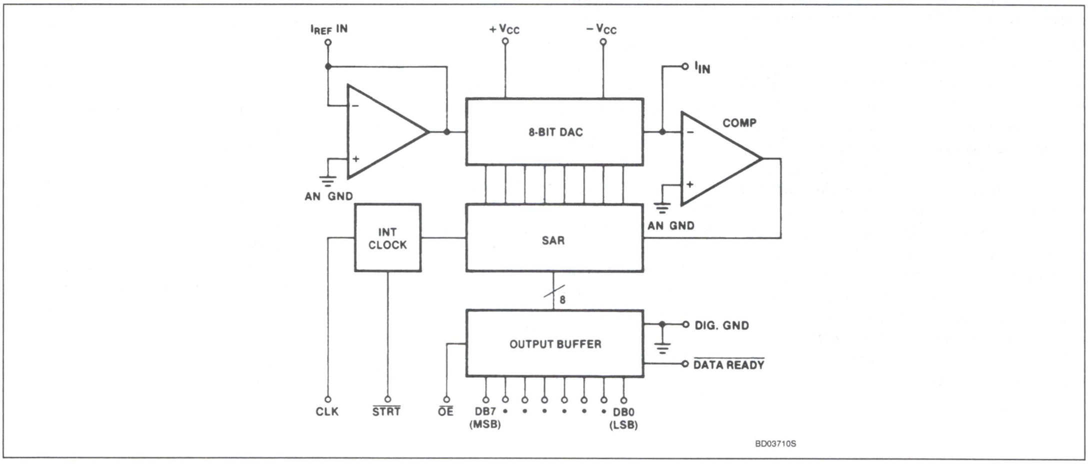
PIN CONFIGURATION


F Package
DB0 (LSB) 1
DB1 2
DB2 3
DB3 4
DB4 5
DB5 6
DB6 7
DB7 8
$\overline{OE}$ 9
18 $\overline{DR}$
17 DIGITAL GND
16 ANALOG GND
15 I_{IN}
14 $-V_{CC}$
13 I_{REF} IN
12 $+V_{CC}$
11 CLK
10 $\overline{STRT}$
TOP VIEW
CD10620S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Cerdip	0 to +70°C	NE5034F

BLOCK DIAGRAM


I_{REF} IN
$+V_{CC}$
$-V_{CC}$
I_{IN}
8-BIT DAC
COMP
AN GND
AN GND
INT CLOCK
SAR
8
OUTPUT BUFFER
DIG. GND
$\overline{DATA\ READY}$
CLK
$\overline{STRT}$
$\overline{OE}$
DB7 (MSB)
DB0 (LSB)
BD03710S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	0 to +6	V
$V_{CC}-$	Negative supply voltage	0 to −15	V
I_{REF}	Reference current	1.5	mA
I_{IN}	Analog input current	5.0	mA
V_O	Data output voltage	6.0	V
V_L	Analog GND to Digital GND Logic input voltage	1.0 −1 to $V_{CC}+$	V V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package	1500	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE:

1. Derate above 25°C at the following rates:
   F package at 12.0mW/°C.

DC ELECTRICAL CHARACTERISTICS $+V_{CC} = 5.0V$, $-V_{CC} = -12V$, $0°C \leqslant T_A \leqslant 70°C$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		8	8	8	Bits
	Relative accuracy error[1, 2]				±½	LSB
$V_{CC}+$	Positive supply range		4.75	5.0	5.25	V
$V_{CC}-$	Negative supply range		−11.4	−12	−12.6	V
ϵ_{FS}	Full-scale gain error	$I_{REF} = 1.0mA$, $T_A = 25°C$		±2	±5	LSB
ϵ_{ZS}	Zero-scale offset error	$I_{REF} = 1.0mA$, $T_A = 25°C$		±0.5	±1	LSB
PSR	Power supply rejection[3]	$I_{REF} = 1.0mA$, $V_{CC} = +4.75$ to $+5.25V$, $V_{CC} = -11.4$ to $-12.6V$			±½	LSB
V_{IH}	Logic 1 input voltage ($\overline{STRT}$ and $\overline{OE}$)		2.0			V
V_{IH}	Logic 1 input voltage ext. clock		2.4			V
V_{IL}	Logic 0 input voltage ($\overline{STRT}$ and $\overline{OE}$)				0.8	V
V_{IL}	Logic 0 input voltage ext clock				0.7	V
I_{IH}	Logic 1 input current ($\overline{STRT}$ and $\overline{OE}$)	$V_{IN} = 2.4V$			20	μA
I_{IH}	Logic 1 input current ext clock	$V_{IN} = 2.4V$		100		μA
I_{IL}	Logic 0 input current ($\overline{STRT}$ and $\overline{OE}$)	$V_{IN} = 0.4V$		−20	−100	μA
I_{IL}	Logic 0 input current ext. clock	$V_{IN} = 0.7V$		−100		μA
V_{OL}	Logic 0 output voltage	$I_{OL} = 1.6mA$, $\overline{OE} = 0.8V$			0.4	V
V_{OH}	Logic 1 output voltage	$I_{OH} = 400\mu A$, $\overline{OE} = 0.8V$	2.4			V
I_{OZ}	Three-state leakage	$\overline{OE} = 2.0V$, $V_{OL} = 0V$ or $5V$		±10		μA
I_{CC+}	Positive supply current	$V_{CC} = +5V$, $V_{CC} = -12V$		18	36	mA
I_{CC}	Negative supply current	$V_{CC} = +5V$, $V_{CC} = -12V$		−11	−22	mA

NOTES:

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 8-bit level which is 0.39% of the full-scale voltage.
3. Maximum change in full-scale.

AC ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -12V$, $T_A = 25°C$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Internal clock frequency			$C_L = 60pF$ (See Figure 1)		500		kHz
	External clock frequency						700	kHz
t_W	$\overline{STRT}$ pulse width			Clock freq. = 500kHz	400			ns
	External clock pulse width positive/negative				600			ns
t_S	Setup time[1]			See Figure 3	300			ns
t_{PD}	(Out data) propagation delay	data out	$\overline{OE}$	See Figure 2		50	200	ns
t_{PD}	(Out $\overline{DR}$) propagation delay	data ready out	8th clock	See Figure 3		700		ns
t_{PD}	(3-State) propagation delay	high impedance o/p	$\overline{OE}$	See Figure 2		60	200	ns
t_{PD}	(DB0) propagation delay	DB0	$\overline{DR}$	See Figure 3			500	ns
t_{PD}	(SDR) $\overline{STRT}$ low to $\overline{DR}$ high	data ready high	$\overline{STRT}$ low	See Figure 3		700		ns

NOTE:

1. See description of "Setup time".

TYPICAL PERFORMANCE CHARACTERISTICS

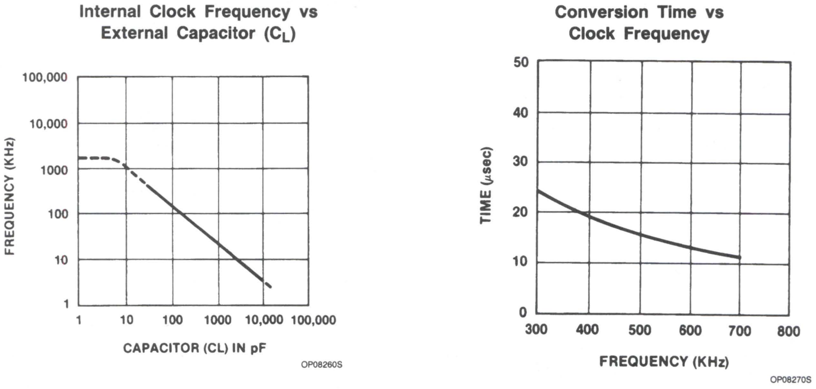
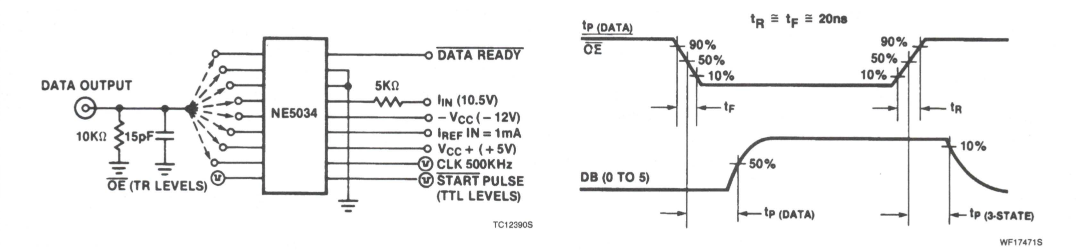
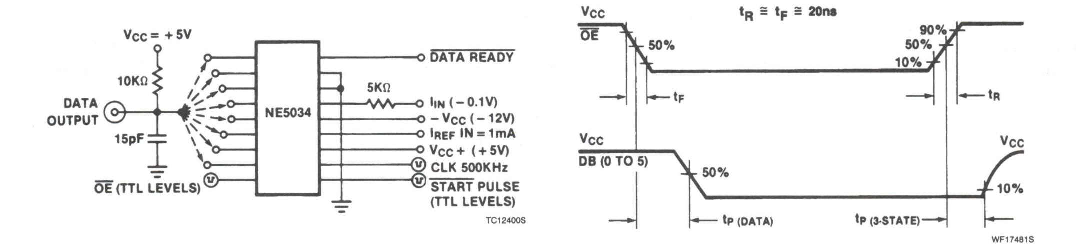


Figure 1

TEST LOAD CIRCUITS


DATA OUTPUT
10KΩ
15pF
$\overline{\text{OE}}$ (TR LEVELS)
NE5034
$\overline{\text{DATA READY}}$
5KΩ
I_{IN} (10.5V)
$-V_{CC}$ (−12V)
I_{REF} IN = 1mA
$V_{CC}+$ (+5V)
CLK 500KHz
$\overline{\text{START}}$ PULSE (TTL LEVELS)
TC12390S
$t_{P\,(DATA)}$
$\overline{\text{OE}}$
$t_R \cong t_F \cong 20ns$
90%
50%
10%
t_F
t_R
DB (0 TO 5)
$t_{P\,(DATA)}$
$t_{P\,(3\text{-}STATE)}$
WF17471S

a. Data Output High


V_{CC} = +5V
10KΩ
DATA OUTPUT
15pF
$\overline{\text{OE}}$ (TTL LEVELS)
NE5034
$\overline{\text{DATA READY}}$
5KΩ
I_{IN} (−0.1V)
$-V_{CC}$ (−12V)
I_{REF} IN = 1mA
$V_{CC}+$ (+5V)
CLK 500KHz
$\overline{\text{START}}$ PULSE (TTL LEVELS)
TC12400S
V_{CC}
$\overline{\text{OE}}$
$t_R \cong t_F \cong 20ns$
50%
90%
10%
t_F
t_R
V_{CC}
DB (0 TO 5)
$t_{P\,(DATA)}$
$t_{P\,(3\text{-}STATE)}$
WF17481S

b. Data Output Low

Figure 2

FUNCTIONAL PIN DEFINITIONS

$\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$)

This is an output pin used to indicate that a conversion is in progress. $\overline{\text{DR}}$ goes to a logic "1" when $\overline{\text{STRT}}$ is at a logic "0". At the completion of a conversion $\overline{\text{DR}}$ returns to a logic "0". There is a delay (MAX 0.5μs) from the time $\overline{\text{DR}}$ goes to "0" to the time DB0 data is valid.

DB0 – DB7

Eight 3-State data outputs each with a drive capability of one TTL load. DB0 is the LSB and DB7 is the MSB.

$\overline{\text{OE}}$

Output enable input. When $\overline{\text{OE}}$ is at a logic "1" the data outputs assume a high impedance state. With $\overline{\text{OE}}$ at a logic "0", data is placed on the outputs. Data appearing on the outputs is only valid if both $\overline{\text{OE}}$ and $\overline{\text{DR}}$ are at logic "0" (see note on $\overline{\text{DR}}$ timing).

$\overline{\text{STRT}}$

This pin is used to reset the converter and start a new conversion. A logic "0" applied to this pin for a minimum of 400ns will reset the converter to a condition with DB7 at a logic "1" and all other Data outputs at logic "0". It will also cause $\overline{\text{DR}}$ to go to a logic "1" (see timing diagrams for delay times). Conversion will start with the 1st clock pulse after $\overline{\text{STRT}}$ returns to a logic "1" (see notes on setup time required). A $\overline{\text{STRT}}$ pulse while a conversion is taking place will cause the conversion to be aborted and the converter will reset. (See notes on short-cycle operation).

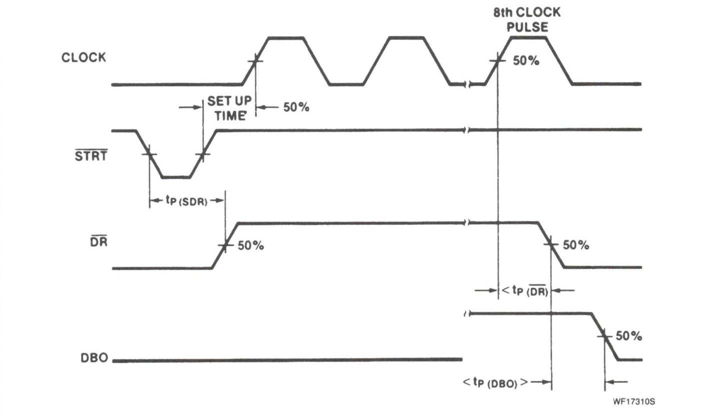

8th CLOCK PULSE
CLOCK
50%
SET UP TIME
50%
$\overline{\text{STRT}}$
$t_{P\,(SDR)}$
$\overline{\text{DR}}$
50%
50%
$t_{P\,(\overline{DR})}$
DBO
50%
$t_{P\,(DBO)}$
WF17310S

Figure 3

CLK IN

An external capacitor between this pin and ground generates the internal clock pulses. (See diagram for clock frequency vs capacitor value). In order to synchronize the internal clock, to the start pulse a diode (small signal type, e.g., 1N914) should be connected between $\overline{\text{STRT}}$ and CLK IN (see Figures 4 and 5). Without this diode the start pulse could occur at a time which could cause one of the conditions described in the Note on "setup" time. Applying an external TTL- or MOS-compatible clock to this pin slaves the NE5034 to external clock frequency. In this case, the diode is not required but the "set-up" time requirements should be noted.

BASIC CIRCUIT DESCRIPTION

The NE5034 is an 8-bit A/D converter which incorporates the successive-approximation conversion method. Upon receipt of the $\overline{\mathrm{STRT}}$ pulse, successive bits, beginning with the MSB (DB7), are applied to the input of the internal 8-bit current output DAC by the I^2L successive-approximation register (SAR) (see Block Diagram).

The comparator determines whether the output current of the DAC is greater or less than the input current converted from the unknown analog input voltage through an external input resistor. If the DAC output current is greater, the data latch for the trial bit is reset to a '0'; if it is less, the trial data bit stays at '1'. After all the bits from DB7 to DB0 have been tried, the SAR contains a valid 8-bit binary output code which accurately represents the unknown analog input to within ± ½LSB (± 0.2%). This binary output will now remain in the SAR until another $\overline{\mathrm{STRT}}$ pulse is applied.

During the successive-approximation sequence, the $\overline{\mathrm{DATA\ READY}}$ signal remains at '1'. Upon completion of the conversion, the signal goes to a '0', indicating that data is valid and ready. If the $\overline{\mathrm{OE}}$ input is left at a '0' during the conversion, the DATA OUTPUT shows the conversion sequence (see short cycle section). When the $\overline{\mathrm{OE}}$ line is made a logic '1', the output buffers will go to a high impedance state and will remain so until the $\overline{\mathrm{OE}}$ is returned to a '0' state.

TIMING DESCRIPTION

The timing diagram shown in Figure 7 shows the successive trial and decisions for each data bit.

With $\overline{\mathrm{STRT}}$ at a logic "0" the converter is reset to a condition with DB7 at a logic "1", DR at a logic "1" and DB0 – DB6 at logic "0".

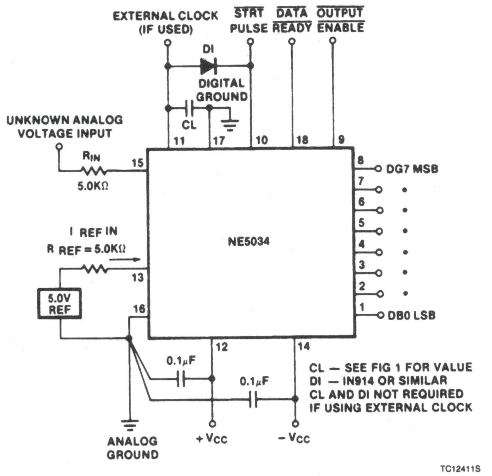
Conversion starts after $\overline{\mathrm{STRT}}$ returns to a logic "1". Starting with DB7 each bit is tried in turn, with the decision point being at the time of the positive-going edge of the clock. Starting with the first positive edge after $\overline{\mathrm{STRT}}$ returns to logic "1" (see note on "setup" time). The eighth positive-going edge makes the decision on DB0 (LSB) and also causes $\overline{\mathrm{DR}}$ to return to a logic "0" to indicate the conversion is complete. (See note on $\overline{\mathrm{DR}}$ timing.)

SHORT-CYCLE OPERATION

In applications where less than 8 bits of resolution are required, the NE5034 can be operated to achieve shorter conversion times. No hard wire changes are required to perform "short-cycling".

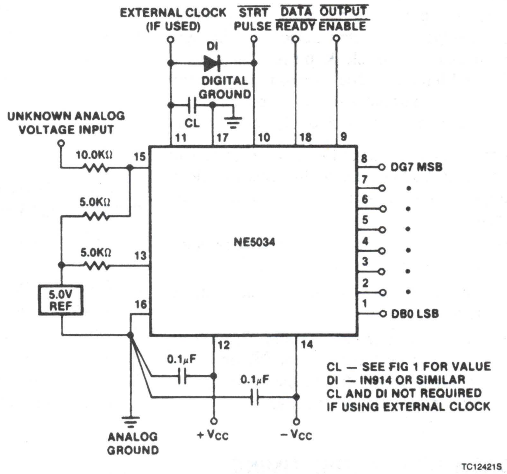
Conversion to X number of bits is completed at the end of X + 0.5 clock cycles (after a start pulse) $\overline{\mathrm{DR}}$ will still be at a logic "1" state.

$\overline{\mathrm{OE}}$ can be used to 3-State the outputs even during short-cycle operation.


EXTERNAL CLOCK (IF USED)
STRT PULSE
DATA READY
OUTPUT ENABLE
DI
DIGITAL GROUND
CL
UNKNOWN ANALOG VOLTAGE INPUT
RIN
5.0KΩ
I REF IN
R REF = 5.0KΩ
5.0V REF
NE5034
11
17
10
18
9
15
13
16
12
14
8
7
6
5
4
3
2
1
DG7 MSB
DB0 LSB
0.1μF
0.1μF
ANALOG GROUND
+Vcc
−Vcc
TC12411S

CL — SEE FIG 1 FOR VALUE
DI — IN914 OR SIMILAR
CL AND DI NOT REQUIRED
IF USING EXTERNAL CLOCK

Figure 4. Basic Setup Diagram
Unipolar Input Values (0 – 10V)


EXTERNAL CLOCK (IF USED)
STRT PULSE
DATA READY
OUTPUT ENABLE
DI
DIGITAL GROUND
CL
UNKNOWN ANALOG VOLTAGE INPUT
10.0KΩ
5.0KΩ
5.0KΩ
5.0V REF
NE5034
11
17
10
18
9
15
13
16
12
14
8
7
6
5
4
3
2
1
DG7 MSB
DB0 LSB
0.1μF
0.1μF
ANALOG GROUND
+Vcc
−Vcc
TC12421S

CL — SEE FIG 1 FOR VALUE
DI — IN914 OR SIMILAR
CL AND DI NOT REQUIRED
IF USING EXTERNAL CLOCK

Figure 5. Basic Setup Diagram
Bipolar Input Values (± 10V Ra

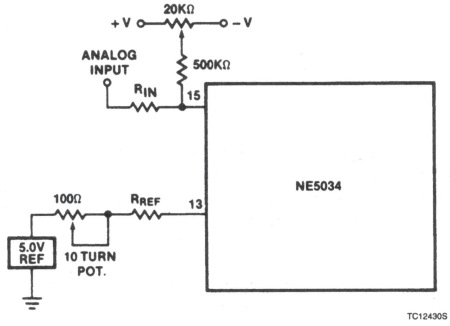

20KΩ
+V
−V
ANALOG INPUT
500KΩ
RIN
15
NE5034
100Ω
RREF
13
5.0V REF
10 TURN POT.
TC12430S

Figure 6. Suggested Zero-/Full-Scale Adjust Circuit

SETUP TIME

When using an external clock, the positive-going edge of the start pulse must be synchronized to the clock pulse. There is a "setup" time of 300ns required between the time of the start pulse returning to a logic "1" and the next positive-going edge of the clock.

If the positive edge of the start pulse occurs less than 300ns prior to the positive clock edge, one of the following conditions will occur:

a) The converter recognizes the clock pulse and converts as normal.
b) The conversion starts one clock pulse later.
c) The conversion never starts. This will be indicated by the fact that $\overline{\text{DR}}$ does not return to logic "0". In this case a new start pulse will be required.

DATA READY ($\overline{\text{DR}}$) TIMING

After $\overline{\text{DR}}$ returns to a logic "0", indicating a conversion is complete, there is a time delay of 500ns before the data at DB0 output (the Least Significant Bit) is valid.

ZERO OFFSET (NEGATIVE FULL-SCALE) CALIBRATION PROCEDURES

1. Apply continuous start pulses to the $\overline{\text{STRT}}$ input.
2. Apply ½ LSB in the case of unipolar operation, or ½ LSB above — FS in the case of bipolar operation to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the potentiometer connected to I_{IN} (see Figure 6) until the LSB flickers between '0' and '1', and all other data outputs remain '0' following each conversion.

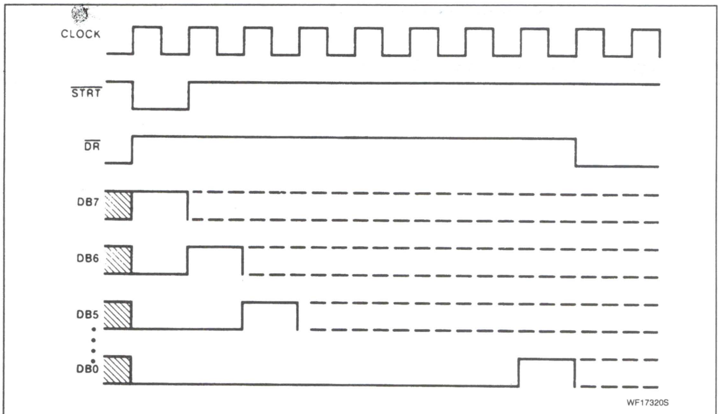
FULL-SCALE (POSITIVE FULL-SCALE) CALIBRATION:

1. Apply continuous start pulses to the $\overline{\text{STRT}}$ input.
2. Apply full-scale minus 1½ LSB to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the voltage applied to V_{REF} in (Figure 4) until the LSB varies between '0' and '1', and all other data outputs stay '1' after each conversion.

NOTES:
1. Where an input of ½ LSB is called for, the voltage is equal to: $\frac{FS}{256}$
2. The sequence of calibration should be:
   a. Zero offset
   b. Full-scale adjust
   c. Zero offset
   d. Full-scale adjust

OPERATING PRECAUTIONS

Analog and digital grounds should have separate returns. Noise and jitter on digital ground will degrade accuracy unless the input is referenced to a 'clean' analog ground.



NOTES:
1. $\overline{\text{OE}}$ = Logic '0'
2. See 'Short-Cycle' section

Figure 7. NE5034 Timing Diagram

UNIPOLAR BINARY OPERATION

A standard connection for a 0 to 10V unipolar binary operation, with $V_{REF\ IN}$ equal to +5V, is shown in Figure 4. The NE5034 can quantize full-scale ranges of 1V to 10V. It should be noted, however, that for smaller full-scale ranges, the accuracy and speed will degrade.

The input voltage versus output code relationship for unipolar operation is shown in Table 1. The full-scale range is 2 times $I_{REF\ IN}$.

Table 1. Unipolar — Binary

ANALOG INPUT 1, 2, 3	DIGITAL OUTPUT CODE
	MSB LSB
FS − 1 LSB	1 1 1 1 1 1 1 1
FS − 2 LSB	1 1 1 1 1 1 1 0
¾ FS	1 1 0 0 0 0 0 0
½ FS + 1 LSB	1 0 0 0 0 0 0 1
½ FS	1 0 0 0 0 0 0 0
½ FS − 1 LSB	0 1 1 1 1 1 1 1
¼ FS	0 1 0 0 0 0 0 0
1 LSB	0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full-scale; i.e., $2I_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals $(2^{-8})^{(FS)}$.
4. "FS" is full-scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

Table 2. Bipolar — Offset Binary

ANALOG INPUT 1, 3, 4	DIGITAL OUTPUT CODE
	MSB LSB
+(FS − 1 LSB)	1 1 1 1 1 1 1 1
+(FS − 2 LSB)	1 1 1 1 1 1 1 0
+(½ FS)	1 1 0 0 0 0 0 0
+(1 LSB)	1 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0 0
−(1 LSB)	0 1 1 1 1 1 1 1
−(½ FS)	0 1 0 0 0 0 0 0
−(FS − 1 LSB)	0 0 0 0 0 0 0 1
−FS	0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full-scale; i.e., $2I_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals $(2^{-8})^{(FS)}$.
4. "FS" is full-scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

BIPOLAR (OFFSET BINARY) OPERATION

A standard connection for a −5 to +5V or −10 to +10V bipolar operation is shown in Figure 5.

Signetics

NE5036
6-Bit A/D Converter (Serial Output)

Product Specification

Linear Products

DESCRIPTION

The NE5036 is an easy-to-use, low cost, successive-approximation Analog-to-Digital converter, fabricated in Bipolar/I^2L technology, and packaged in a convenient 8-pin miniDIP package.

With an external reference voltage, the NE5036 will accept input voltages between 0V and V_{REF}. Holding the $\overline{START}$ pin low for at least 8 clock pulses in duration will provide the 6-bit result of the conversion in a serial format.

FEATURES

- **Three-state output buffer for easy microprocessor interfacing**
- **Fast successive-approximation converter, 23µs**
- **TTL compatible inputs and outputs**
- **Easy interface to CMOS microprocessors**
- **Guaranteed no missing codes over full operating range**
- **Single supply operation, +5V**
- **High impedance analog inputs**
- **Positive true binary serial output**

APPLICATIONS

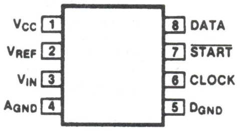
- **Temperature control**
- **µP-based appliances**
- **Light level monitor**
- **Electronic toys**
- **Joystick interface**
- **µP/transducer interface**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	0 to +70°C	NE5036FE
8-Pin Plastic DIP	0 to +70°C	NE5036N
14-Pin SO Package	0 to +70°C	NE5036D

PIN CONFIGURATIONS

FE, N Packages

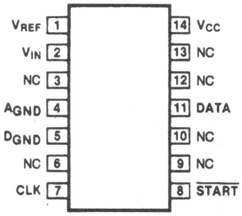


Vcc 1
VREF 2
VIN 3
AGND 4
8 DATA
7 START
6 CLOCK
5 DGND

TOP VIEW

CD10631S

D Package[1]



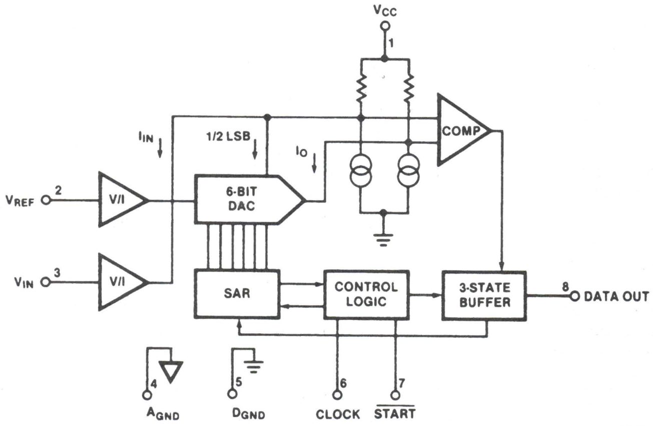
VREF 1
VIN 2
NC 3
AGND 4
DGND 5
NC 6
CLK 7
14 Vcc
13 NC
12 NC
11 DATA
10 NC
9 NC
8 START

TOP VIEW

CD10641S

NOTE:
1. SO and non-standard pinouts.

BLOCK DIAGRAM



Vcc
1
COMP
IIN
1/2 LSB
IO
VREF 2
V/I
6-BIT DAC
VIN 3
V/I
SAR
CONTROL LOGIC
3-STATE BUFFER
8 DATA OUT
4 AGND
5 DGND
6 CLOCK
7 START
BD07200S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\ (Analog)}$	Analog input voltage	7	V
$V_{IN\ (Digital)}$	Digital input voltage ($\overline{\text{START}}$ & CLOCK)	7	V
D_{OUT}	Data output pin		
	3-State mode	7	V
	Enabled mode	20	mA
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1]		
	FE package	780	mW
	N package	1160	mW
	D package	1090	mW

NOTE:

1. Derate above 25°C at the following rates:
   FE package at 6.0mW/°C.
   N package at 9.3mW/°C.
   D package at 8.3mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0°C \leq T_A \leq 70°C$, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Resolution		6	6	6	Bits
	Relative accuracy[1, 2]			¼	½	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full-scale gain error[2, 3, 4]	$V_{REF} = 2.0V$, $T_A = 25°C$		±1	±2	LSB
ϵ_{ZS}	Zero-scale offset error[2]	$V_{REF} = 2.0V$, $T_A = 25°C$		±½	−½, +2	LSB
PSR	Power supply rejection Max change in full-scale[2]	$V_{REF} = 2.0V$ $4.75V \leq V_{CC} \leq 5.5V$		±½	±1	LSB
I_{IN}	Analog input bias current	$0 \leq V_{IN} \leq 2.5V$		1	10	μA
I_{REF}	Reference bias current	$0 \leq V_{REF} \leq 2.5V$		1	10	μA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current			1	10	μA
I_{OH}	Logic '1' output current	$2.4V \leq V_{OH}$	300			μA
I_{OL}	Logic '0' output current	$V_{OL} \leq 0.4V$	1.6			mA
I_{OZ}	Three-state leakage current			±0.1	±40	μA
I_{CC}	Positive supply current			14	24	mA
P_D	Power dissipation				132	mW

NOTES:

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on the straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the code transition point (111110 to 111111) from its ideal value (accounting for offset error at 000000).
4. The analog input voltage (V_{IN}) range is from 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance V_{REF} can be any value from 1.5V to 2.5V.)

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0°C \leqslant T_A \leqslant 70°C$ unless otherwise specified. Typical values are specified at 25°C. (Refer to test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Max clock frequency				350			kHz
t_{CONV}	Conversion time						8	Clock cycles
t_W	Clock pulse width				1.3			μs
t_S	Setup time, $\overline{\text{START}}$ to clock[2]	Clock	$\overline{\text{START}}$		500			ns
$t_{P\ (OUT)}$	Propagation delay[1]	Data out	Clock	$T_A = 25°C$, $t_R = t_F < 20ns$			600	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay[1]	Data (3-State)	$\overline{\text{START}}$	$T_A = 25°C$, $t_R = t_F < 20ns$			600	ns

NOTES:

1. The time between the specified reference points on the clock and the output waveforms with the output changing (Low-to-High or High-to-Low).
2. The High-to-Low transition of the $\overline{\text{START}}$ pulse should occur at least 500ns prior to the negative edge of the clock pulse to insure its recognition. The $\overline{\text{START}}$ pulse should stay high for at least 500ns between conversions to guarantee proper recognition.

6-Bit A/D Converter NE5036

CIRCUIT DESCRIPTION

NE5036 is a complete 6-bit, serial output, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and the output buffer. An externally-generated clock source (maximum frequency = 350kHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter as shown in the Block Diagram.

Upon the $\overline{\text{START}}$ pin going low, successive approximation conversion commences after the first low-going edge of the clock pulse. Successive bits, beginning with the MSB (D5), are applied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to 0 and simultaneously the output buffer goes to 0. If it is less, that bit stays at 1 and the output buffer goes to 1. After the second High-to-Low transition of the clock pulse, the MSB (D5) data is valid. On successive clock pulses, successive bits are tried and the output buffer represents that bit. $\overline{\text{START}}$ has to stay low for at least 8 clock pulses for the conversion to be completed and to access the 6-bit result of the conversion. A conversion in process can be interrupted by issuing another $\overline{\text{START}}$ pulse.

When $\overline{\text{START}}$ is in a high state, the output buffer is in a high impedance state.

The timing diagram for the device is shown in Figure 1.

TRANSFER CHARACTERISTICS

The NE5036 is designed to have a nominal ½ LSB offset, so that the code transition points are located ½ LSB on either side of the exact analog input for a given code. Thus, the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V), plus any offset. Subsequent transition (to full-scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

The ideal transfer characteristic of NE5036 is shown in Figure 2.

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and Digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The leads to the analog inputs should be kept as short as possible to minimize input noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1μF and should be located close to the device to minimize the effects of noise spikes on V_{CC}.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance at these inputs at or below 2kΩ.

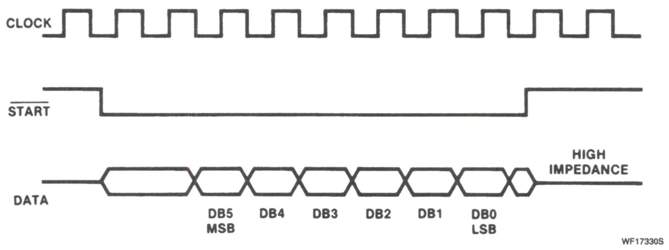


Figure 1. Timing Diagram

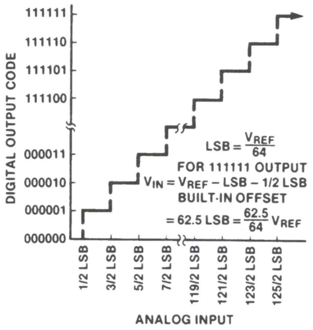
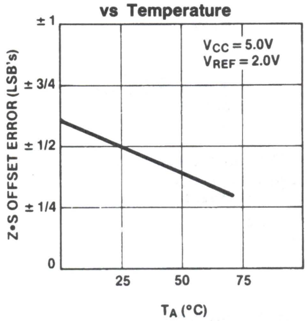


Figure 2. Ideal Transfer Characteristics

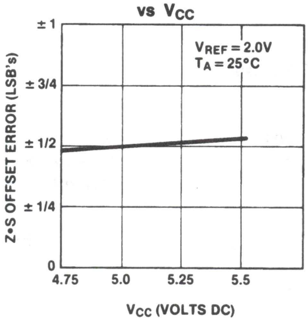
TYPICAL PERFORMANCE CHARACTERISTICS

Zero-Scale Offset Error vs Temperature



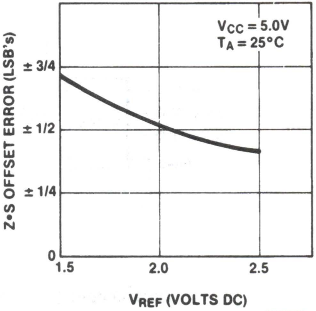
OP08290S

Zero-Scale Offset Error vs V_{CC}



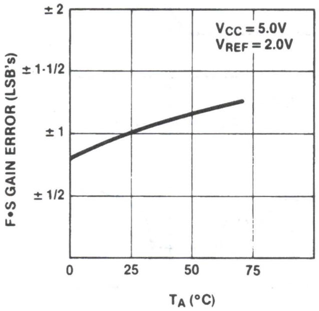
OP08300S

Zero-Scale Offset Error vs V_{REF}



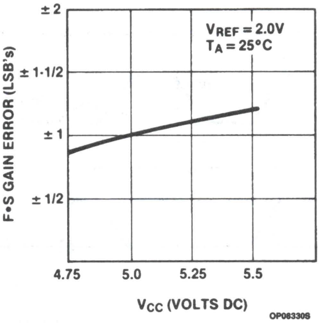
OP08310S

Full-Scale Gain Error vs Temperature



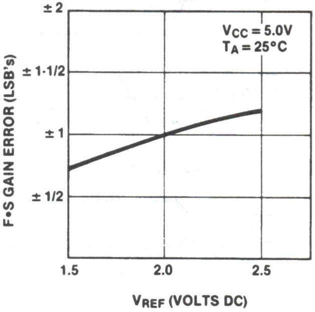
OP08320S

Full-Scale Gain Error vs V_{CC}



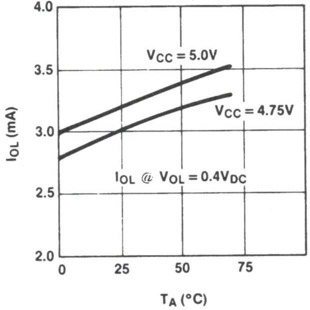
OP08330S

Full-Scale Gain Error vs R_{REF}



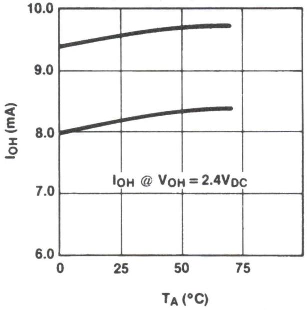
OP08340S

I_{OL} vs Temperature (Data Output)



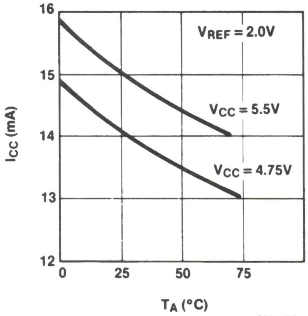
OP08350S

I_{OH} vs Temperature (Data Output)



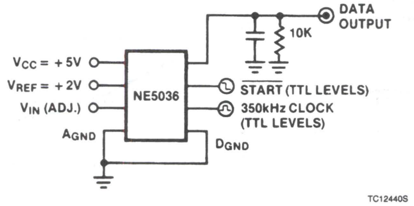
OP08360S

I_{CC} vs Temperature

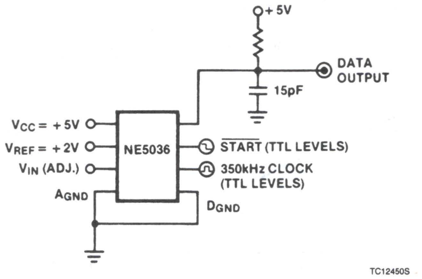


OP08370S

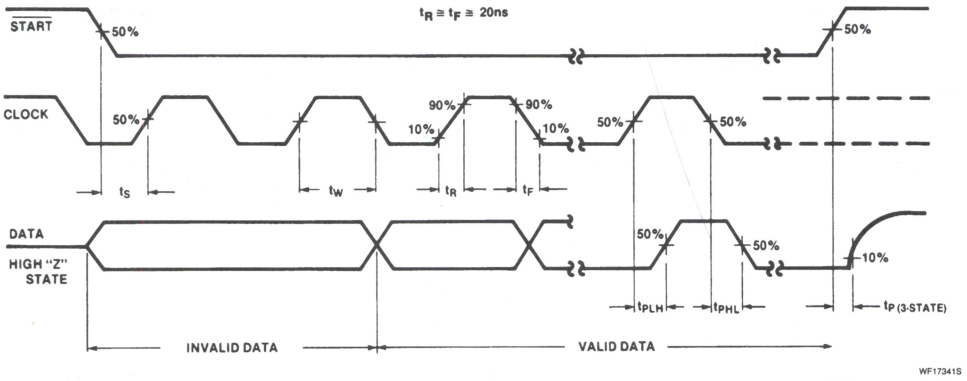
AC TEST CIRCUITS AND WAVEFORMS


DATA OUTPUT
10K
V_{CC} = +5V
V_{REF} = +2V
V_{IN} (ADJ.)
NE5036
START (TTL LEVELS)
350kHz CLOCK (TTL LEVELS)
A_{GND}
D_{GND}
TC12440S

Data Output (Low-to-High)

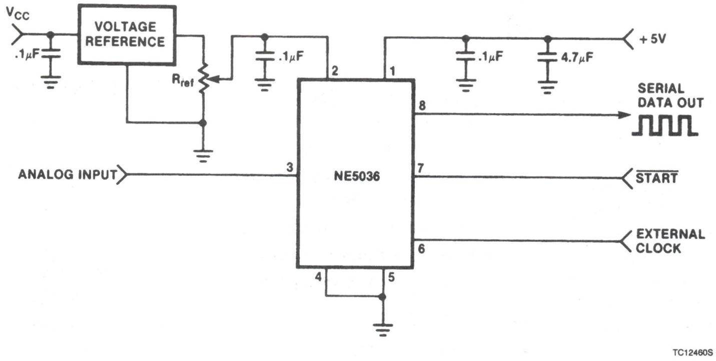

+5V
DATA OUTPUT
15pF
V_{CC} = +5V
V_{REF} = +2V
V_{IN} (ADJ.)
NE5036
START (TTL LEVELS)
350kHz CLOCK (TTL LEVELS)
A_{GND}
D_{GND}
TC12450S

Data Output (High-to-Low)

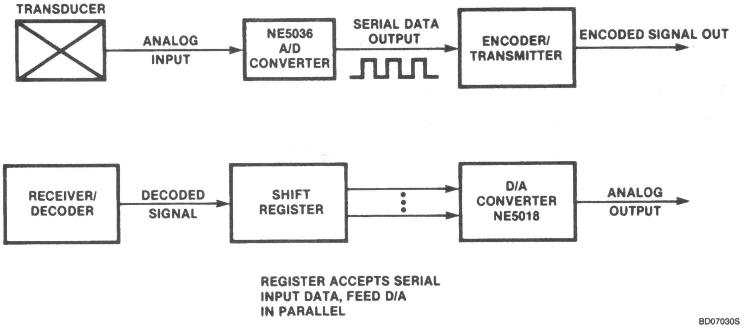

$t_R \cong t_F \cong$ 20ns
START
50%
50%
CLOCK
50%
90%
90%
10%
10%
50%
50%
t_S
t_W
t_R
t_F
DATA
HIGH "Z" STATE
50%
50%
10%
t_{PLH}
t_{PHL}
$t_{P\,(3\text{-STATE})}$
INVALID DATA
VALID DATA
WF17341S

Propagation Delay Time t_P (Data)

TYPICAL APPLICATIONS


VCC
.1μF
VOLTAGE REFERENCE
Rref
.1μF
2
1
.1μF
4.7μF
+5V
SERIAL DATA OUT
8
ANALOG INPUT
3
NE5036
7
START
EXTERNAL CLOCK
6
4
5
TC12460S

1. Basic NE5036 Configuration


TRANSDUCER
ANALOG INPUT
NE5036 A/D CONVERTER
SERIAL DATA OUTPUT
ENCODER/ TRANSMITTER
ENCODED SIGNAL OUT
RECEIVER/ DECODER
DECODED SIGNAL
SHIFT REGISTER
D/A CONVERTER NE5018
ANALOG OUTPUT
REGISTER ACCEPTS SERIAL INPUT DATA, FEED D/A IN PARALLEL
BD07030S

2. Digital Communications Using NE5036

Signetics

Linear Products

NE5037

6-Bit A/D Converter (Parallel Outputs)

Product Specification

DESCRIPTION

The NE5037 is a low cost, complete successive-approximation analog-to-digital (A/D) converter, fabricated using Bipolar/I^{2}L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9μs.

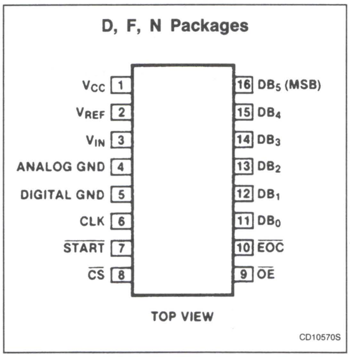
FEATURES

- **TTL-compatible inputs and outputs**
- **3-State output buffer**
- **Easy interface to CMOS microprocessors**
- **Fast conversion — 9μs**
- **Guaranteed no missing codes over full temp range**
- **Single-supply operation, +5V**
- **Positive true binary outputs**
- **High-impedance analog inputs**

APPLICATIONS

- **Temperature control**
- **μP-based appliances**
- **Light level monitors**
- **Head position sensing**
- **Electronic toys**
- **Joystick interface**

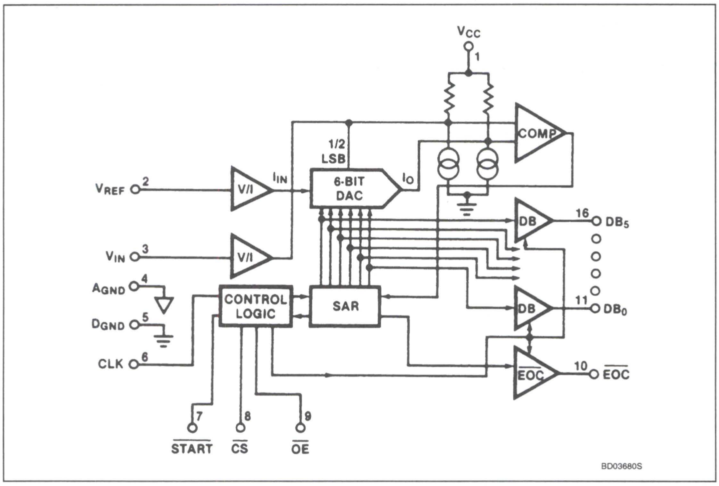
PIN CONFIGURATION


D, F, N Packages
VCC 1
VREF 2
VIN 3
ANALOG GND 4
DIGITAL GND 5
CLK 6
START 7
CS 8
16 DB5 (MSB)
15 DB4
14 DB3
13 DB2
12 DB1
11 DB0
10 EOC
9 OE
TOP VIEW
CD10570S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE5037F
16-Pin Plastic DIP	0 to +70°C	NE5037N
16-Pin Plastic SO package	0 to +70°C	NE5037D

BLOCK DIAGRAM


VCC
1
1/2 LSB
COMP
VREF 2
V/I
IIN
6-BIT DAC
IO
VIN 3
V/I
AGND 4
DGND 5
CLK 6
CONTROL LOGIC
SAR
DB
16 DB5
DB
11 DB0
EOC
10 EOC
7 START
8 CS
9 OE
BD03680S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN(Analog)}$	Analog input voltage	7	V
$V_{IN(Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5) 3-state mode Enabled mode (each output)	 7 5	 V mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 1190 1450 1090	 mW mW mW

NOTE:

1. Derate above 25°C at the following rates:
   F package = 9.5mW/°C.
   N package = 11.6mW/°C.
   D package = 8.7mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 1MHz; $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full-scale gain error[2,3,4]	$V_{REF} = 2.0V$, $T_A = 25°C$		±1	±2	LSB
ϵ_{ZS}	Zero-scale offset error[2]	$V_{REF} = 2.0V$, $T_A = 25°C$		±1/2	−1/2, +2	LSB
PSR	Power supply rejection Max change in full-scale[2]	$V_{REF} = 2.0V$ $4.75V \leqslant V_{CC} \leqslant 5.5V$		±1/2	±1	LSB
I_{IN}	Analog input bias current	$0 \leqslant V_{IN} \leqslant 2.5V$		1	10	µA
I_{REF}	Reference bias current	$0 \leqslant V_{REF} \leqslant 2.5V$		1	10	µA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	µA
I_{IL}	Logic '0' input current			1	10	µA
I_{OH}	Logic '1' output current[5]	$2.4V \leqslant V_{OH}$	300			µA
I_{OL}	Logic '0' output current[5]	$V_{OL} \leqslant 0.4V$	1.6			mA
I_{OZ}	3-State leakage current			±0.1	±40	µA
I_{CC}	Positive supply current			18	24	mA
P_D	Power dissipation				132	mW

NOTES:

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 6-bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the full-scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open-collector with a nominal 5kΩ internal pull-up resistor.

AC ELECTRICAL CHARACTERISTICS

$V_{CC}=5.0V$; $V_{REF}=2.0V$; Clock=1MHz; $0°C \leqslant T_A \leqslant 70°C$ unless otherwise specified. Typical values are specified at 25°C. (Refer to AC test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width				300			ns
	Minimum positive/negative clock pulse width				300			ns
t_{CONV}	Conversion time						9	Clock cycles
$t_{P\ (OUT\ DATA)}$	Propagation delay[1]	Data out	$\overline{OE}$	$T_A = 25°C$, $t_R = t_F \leqslant 20ns$			500	ns
$t_{P\ (OUT\ EOC)}$	Propagation delay[2]	$\overline{EOC}$	Clock	$T_A = 25°C$, $t_R = t_F \leqslant 20ns$			800	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay, 3-State	3-State Data	$\overline{OE}$	$T_A = 25°C$, $t_R = t_F \leqslant 20ns$			500	ns

NOTES:

1. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
2. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

6-Bit A/D Converter (Parallel Outputs) NE5037

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive-approximation method. The chip includes the internal control logic, the successive-approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally-generated clock source (max frequency = 1MHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter.

The $\overline{\text{CS}}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{\text{START}}$ pulse, the internal control logic resets the SAR. On the first low-going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I^{2}L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, which is converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to '0' and the corresponding output buffer goes to '0' simultaneously. If it is less, it stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low-going edge of the clock pulse (after the receipt of the start pulse), the $\overline{\text{EOC}}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{\text{OE}}$ pin must be set to a low level. $\overline{\text{EOC}}$ is reset to a high state when $\overline{\text{OE}}$ is low. When $\overline{\text{OE}}$ is in a '1' state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

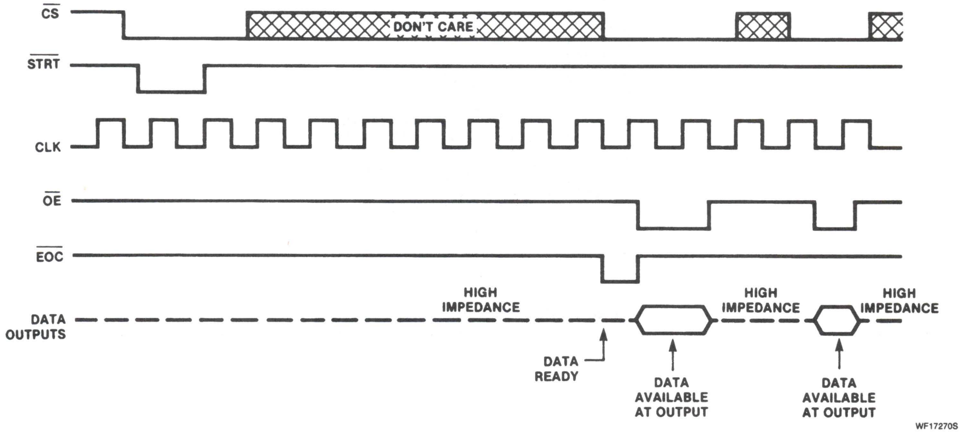


Figure 1. Timing Diagram

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal ½ LSB offset so that the code transition points are located ½ LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full-scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1μF located close to the device to minimize the effects of noise spikes.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance of these inputs at or below 2kΩ.

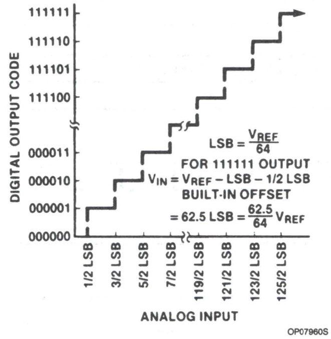
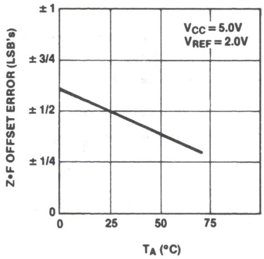


Figure 2. Ideal Transfer Characteristics

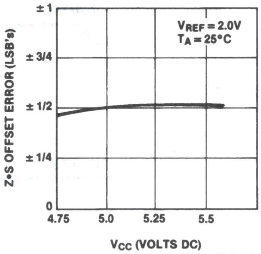
TYPICAL PERFORMANCE CHARACTERISTICS

Zero-Scale Offset Error vs Temp



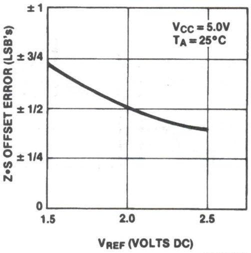
OP07970S

Zero-Scale Offset Error vs V_{CC}



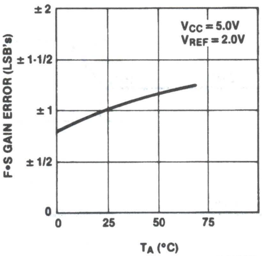
OP07980S

Zero-Scale Offset Error vs V_{REF}



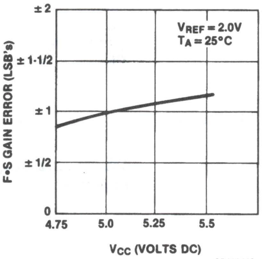
OP07990S

Full-Scale Gain Error vs Temp



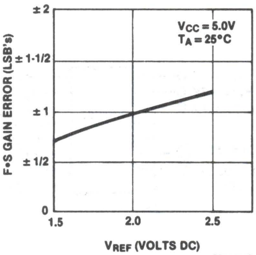
OP08000S

Full-Scale Gain Error vs V_{CC}



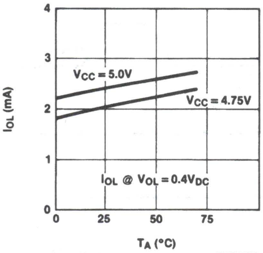
OP08010S

Full-Scale Gain Error vs V_{REF}



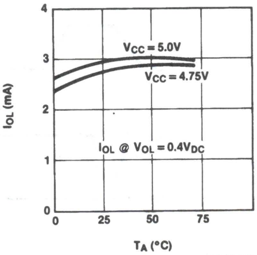
OP08020S

I_{OL} vs Temp (Data Outputs)



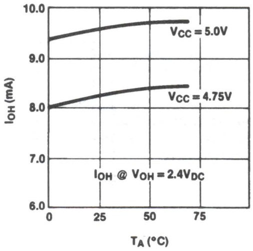
OP08030S

I_{OL} vs Temp ($\overline{EOC}$)



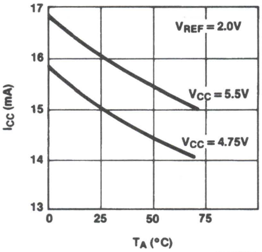
OP08040S

I_{OH} vs Temp (Data Outputs)



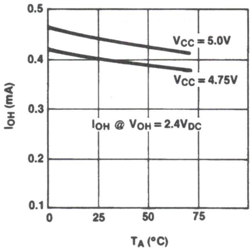
OP08050S

I_{CC} vs Temp



OP08060S

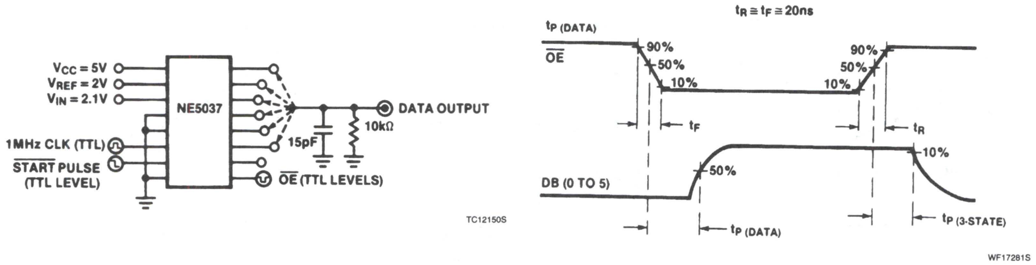
I_{OH} vs Temp ($\overline{EOC}$)



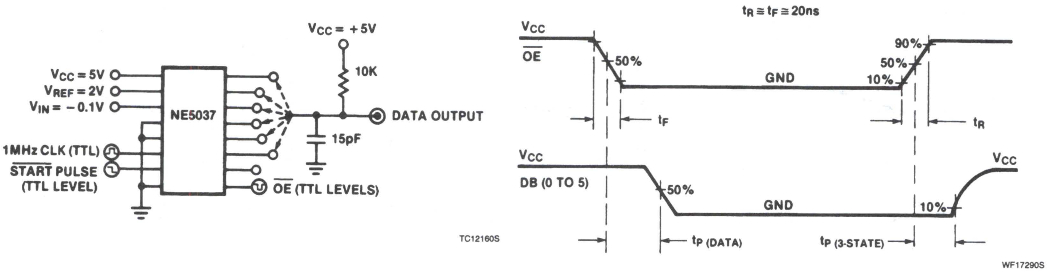
OP08070S

6-Bit A/D Converter (Parallel Outputs) NE5037

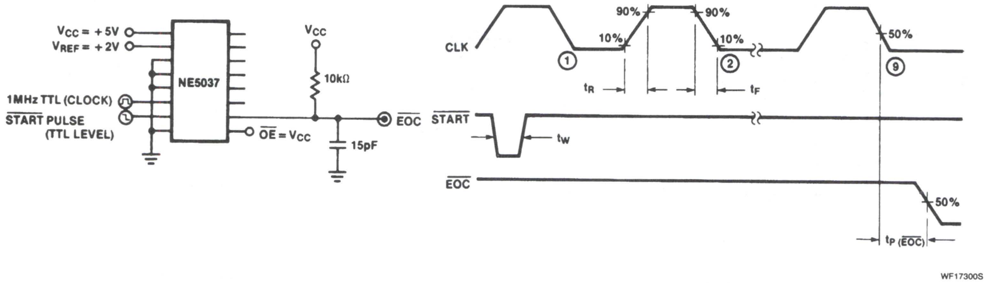
AC TEST CIRCUITS AND WAVEFORMS


V_{CC} = 5V
V_{REF} = 2V
V_{IN} = 2.1V
NE5037
1MHz CLK (TTL)
$\overline{START}$ PULSE (TTL LEVEL)
15pF
10kΩ
DATA OUTPUT
$\overline{OE}$ (TTL LEVELS)
TC12150S
$t_R \cong t_F \cong$ 20ns
$t_{P(DATA)}$
$\overline{OE}$
90%
50%
10%
t_F
t_R
DB (0 TO 5)
$t_{P(3\text{-}STATE)}$
WF17281S

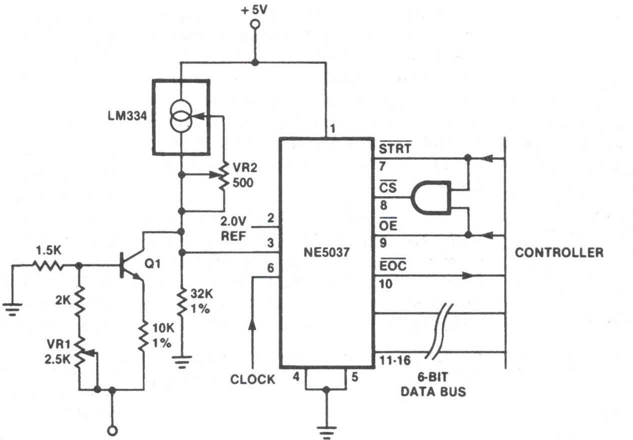
Propagation Delay Time $t_{P(Data)}$ and $t_{P(3\text{-}State)}$


V_{CC} = +5V
10K
V_{CC} = 5V
V_{REF} = 2V
V_{IN} = −0.1V
NE5037
1MHz CLK (TTL)
$\overline{START}$ PULSE (TTL LEVEL)
DATA OUTPUT
15pF
$\overline{OE}$ (TTL LEVELS)
TC12160S
$t_R \cong t_F \cong$ 20ns
V_{CC}
$\overline{OE}$
50%
GND
90%
10%
t_F
t_R
DB (0 TO 5)
$t_{P(DATA)}$
$t_{P(3\text{-}STATE)}$
WF17290S

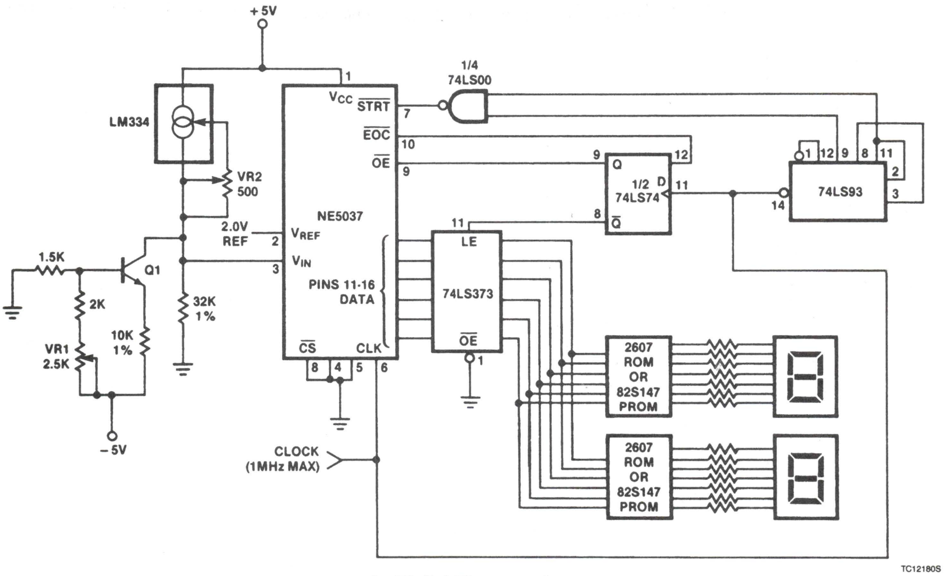
Data Output High


V_{CC} = +5V
V_{REF} = +2V
NE5037
1MHz TTL (CLOCK)
$\overline{START}$ PULSE (TTL LEVEL)
V_{CC}
10kΩ
$\overline{OE}$ = V_{CC}
15pF
$\overline{EOC}$
CLK
90%
10%
50%
①
②
⑨
t_R
t_F
$\overline{START}$
t_W
$\overline{EOC}$
$t_{P(\overline{EOC})}$
WF17300S

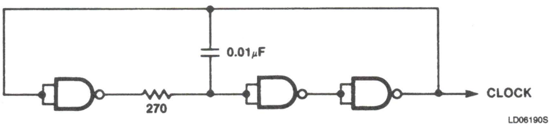
Propagation Delay Time EOC $t_{P(EOC)}$


+5V
LM334
VR2
500
1
NE5037
2.0V
REF
2
3
6
1.5K
Q1
2K
VR1
2.5K
10K
1%
32K
1%
−5V
CLOCK
4
5
$\overline{STRT}$
7
$\overline{CS}$
8
$\overline{OE}$
9
$\overline{EOC}$
10
11-16
6-BIT
DATA BUS
CONTROLLER
TC12170S

a. Temperature Sensor


+5V
LM334
VR2
500
1
V_{CC}
$\overline{STRT}$
7
$\overline{EOC}$
10
$\overline{OE}$
9
NE5037
2.0V
REF
2
V_{REF}
3
V_{IN}
PINS 11-16
DATA
$\overline{CS}$
CLK
8
4
5
6
1.5K
Q1
2K
VR1
2.5K
10K
1%
32K
1%
−5V
CLOCK
(1MHz MAX)
1/4
74LS00
9
Q
12
1/2
74LS74
D
11
8
$\overline{Q}$
11
LE
74LS373
$\overline{OE}$
1
14
74LS93
1
12
9
8
11
2
3
2607
ROM
OR
82S147
PROM
2607
ROM
OR
82S147
PROM
TC12180S

b. Digital Thermometer


0.01μF
270
CLOCK
LD06190S

c. Simple Clock Circuit

Figure 3

6-Bit A/D Converter (Parallel Outputs) NE5037

APPLICATION

- **0 to 63°C Temperature Sensor**

CIRCUIT DESCRIPTION

The temperature sensor of Figure 3 provides an input to Pin 3 of the NE5037 of 32mV/°C. This 32mV is the value of one LSB for the NE5037. The LM334 is a three-terminal temperature sensor and provides a current of 1μA for each °Kelvin. The 32kΩ resistor provides the 32mV for each microamp through it, while the transistor bleeds off 273μA of the temperature sensor (LM334) current, lowering the reading by 273°K, thus converting from Kelvin to Celsius.

To read temperature, conversion is started by sending a momentary low signal to Pin 7 of the NE5037. When Pin 10 of the NE5037 goes low, conversion is complete and a low is applied to Pin 9 of the NE5037 to read data on Pins 11 through 16. Note that this temperature data is in straight binary format.

The controller can be a microprocessor in a temperature control application, or discrete circuitry in a simple temperature reporting application. A temperature reporting (digital thermometer) circuit is shown in Figure 3b. The ROMs or PROMs must have the correct code for converting the data from the NE5037 (used as address for the ROMs or PROMs) to the appropriate segment driver codes.

The displayed output could easily be converted to degrees Fahrenheit (°F) by the controller of Figure 3a or through the (P)ROMs of Figure 3b. When doing this, a third (hundreds) digit (P)ROM and display will be needed for displaying temperatures above 99°F.

An inexpensive clock can be made from NAND gates or inverters, as shown in Figure 3c.

CIRCUIT ADJUSTMENT

Adjust VR2 for about ¼ of maximum resistance. With the sensor (LM334) stable at a known temperature near the lower end of the expected range of temperature readings, adjust VR1 for a drop of 2.73V across the (10kΩ) emitter resistor of Q1. Set reference voltage at Pin 2 of the NE5037 for 2V and adjust VR2 for a digital reading corresponding to the known temperature.

Because high accuracy is not necessary in many applications, this is often all the adjustment necessary and yields an indicated temperature that is within 3°C of actual temperature. Should higher accuracy be required, adjustment of the NE5037 reference voltage at Pin 2 is needed. After performing the above adjustments, bring the sensor temperature to a value near the maximum expected reading (but not above 63°C) and adjust the reference voltage at Pin 2 of the NE5037 for a digital output indication of the known temperature. Then stabilize the sensor again at a temperature near the low end of the expected range of readings and adjust VR1 for a digital indication of that known temperature. This procedure will provide an accuracy of ±1°C.

Signetics

PCF8591
8-Bit A/D and D/A Converter

Objective Specification

Linear Products

DESCRIPTION

The PCF8591 is a single-chip, single-supply, low power 8-bit CMOS data acquisition device. It contains an 8-bit successive approximation analog to digital converter, a four channel analog multiplexer and a digital to analog converter. The four analog inputs can be programmed as two differential inputs or four single-ended inputs. PCF8591 has a serial I^2C interface which allows for a maximum bus frequency of 100k bits per second.

FEATURES

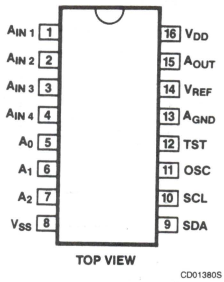
- **Single power supply**
- **Operating voltage 2.5V to 6V**
- **Low power consumption**
- **Serial I^2C bus**
- **Four analog inputs programmable as two differential or four single-ended**
- **On-chip sample-and-hold**
- **Auto-incremented channel selection**
- **8-bit successive approximation A/D conversion**
- **Multiplying DAC with one analog output**

APPLICATIONS

- **Control systems**
- **Low power converter for remote data acquisition**
- **Automotive**
- **Audio and TV**

PIN CONFIGURATION

D and N Packages



PIN NO.	SYMBOL	DESCRIPTION
1	$A_{IN\ 1}$	Analog input (A/D converter)
2	$A_{IN\ 2}$	Analog input (A/D converter)
3	$A_{IN\ 3}$	Analog input (A/D converter)
4	$A_{IN\ 4}$	Analog input (A/D converter)
5	A_0	Hardware address pin
6	A_1	Hardware address pin
7	A_2	Hardware address pin
8	V_{SS}	Negative supply
9	SDA	I^2C Bus data line
10	SCL	I^2C Bus clock line
11	OSC	Oscillator
12	TST	Testpin
13	A_{GND}	Analog ground (reference ground)
14	V_{REF}	Reference voltage
15	A_{OUT}	Analog output (D/A converter)
16	V_{DD}	Positive supply

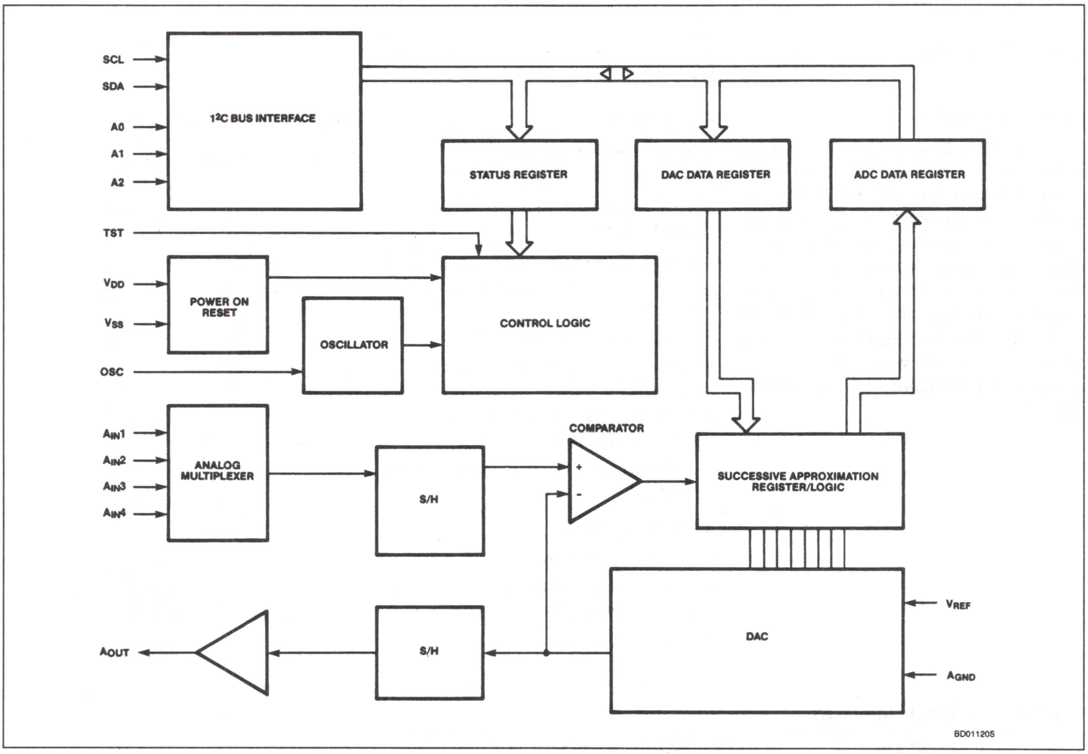
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to 85°C	PCF8591PN
16-Pin Plastic SO package	−40°C to 85°C	PCF8591TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to +8.0	V
V_I	Voltage on any pin	−0.5 to V_{DD} +0.5	V
I_I	Input current DC	10	mA
I_O	Output current DC	20	mA
I_{DD}, I_{SS}	V_{DD} or V_{SS} current	50	mA
P_{TOT}	Power dissipation per package	300	mW
P_D	Power dissipation per output	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

BLOCK DIAGRAM


SCL
SDA
A0
A1
A2
I²C BUS INTERFACE
STATUS REGISTER
DAC DATA REGISTER
ADC DATA REGISTER
TST
VDD
VSS
OSC
POWER ON RESET
OSCILLATOR
CONTROL LOGIC
AIN1
AIN2
AIN3
AIN4
ANALOG MULTIPLEXER
S/H
COMPARATOR
+
-
SUCCESSIVE APPROXIMATION REGISTER/LOGIC
DAC
VREF
AGND
AOUT
S/H
BD01120S

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.5V to 6V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{DD}	Supply voltage	Operating	2.5		6.0	V
I_{DD0}	Supply current	Standby $V_I = V_{SS}$ or V_{DD}; no load			15	μA
I_{DD1}	Supply current	Operating A_{OUT} off, f_{SCL} = 100kHz		125	250	μA
I_{DD2}	Supply current	A_{OUT} active, f_{SCL} = 100kHz		0.45	1.0	mA
V_{POR}	Power-on reset level		0.8		2.0	V
Digital inputs/output SCL, SDA, A0, A1, A2						
V_{IL}	Input voltage	LOW	0		0.3 × V_{DD}	V
V_{IH}	Input voltage	HIGH	0.7 × V_{DD}		V_{DD}	V
I_I	Input current	Leakage $V_I = V_{SS}$ to V_{DD}			250	nA
C_I	Input capacitance				5	pF
I_{OH}	SDA output current	Leakage HIGH at $V_{OH} = V_{DD}$			250	nA
I_{OL}	SDA output current	LOW at V_{OL} = 0.4V	3.0			mA
Reference voltage inputs V_{REF}, A_{GND}						
V_{REF}	Voltage range	Reference	V_{AGND}		V_{DD}	V
V_{AGND}	Voltage range	Analog ground	V_{SS}		V_{REF}	V
I_I	Input current	Leakage			250	nA
R_{REF}	Input resistance	V_{REF} to A_{GND}		100		kΩ
Oscillator OSC, EXT						
I_I	Input current	Leakage			250	nA
f_{OSC}	Oscillator frequency		0.75		1.25	MHz

D/A CHARACTERISTICS

V_{DD} = 5.0V; V_{SS} = 0V; V_{REF} = 5.0V; V_{AGND} = 0V; R_L = 10kΩ; C_L = 100pF; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Analog output						
V_{OA}	Output voltage range	No resistive load	V_{SS}		V_{DD}	V
V_{OA}	Output voltage range	R_L = 10kΩ	V_{SS}		0.9 V_{DD}	V
I_{LO}	Output current	Leakage A_{OUT} disabled			250	nA
Accuracy						
OS_e	Offset error	T_A = 25°C			50	mV
L_e	Linearity error				±1.5	LSB
G_e	Gain error	No resistive load			1	%
t_{DAC}	Settling time	To ½LSB full-scale step			90	μs
f_{DAC}	Conversion rate				11.1	kHz
SNRR	Supply noise rejection ratio	At f = 100Hz; $V_{DD} = 0.1V_{P-P}$		40		dB

A/D CHARACTERISTICS

V_{DD} = 5.0V; V_{SS} = 0V; V_{REF} = 5.0V; V_{AGND} = 0V; R_{SOURCE} = 10kΩ; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Analog inputs						
V_{IA}	Input voltage range		V_{SS}		V_{DD}	V
I_{IA}	Input current	Leakage			100	nA
C_{IA}	Input capacitance			10		pF
C_{ID}	Input capacitance	Differential		10		pF
V_{IS}	Single-ended voltage	Measuring range	V_{AGND}		V_{REF}	V
V_{ID}	Differential voltage	Measuring range; $V_{FS} = V_{REF} - V_{AGND}$	$\frac{-V_{FS}}{2}$		$\frac{+V_{FS}}{2}$	V
Accuracy						
OS_e	Offset error	T_A = 25°C			20	mV
L_e	Linearity error				±1.5	LSB
G_e	Gain error				1	%
GS_e	Gain error	Small-signal ΔV_{IN} = 16LSB			5	%
CMRR SNRR	Common-mode rejection ratio Supply noise rejection	At f = 100Hz; $V_{DDN} = 0.1V_{P-P}$		60 40		dB dB
t_{ADC}	Conversion time				90	μs
f_{ADC}	Sampling/conversion rate				11.1	kHz

NOTE:
1. The power-on reset circuit resets the I^{2}C bus logic when V_{DD} is less than V_{POR}.

FUNCTIONAL DESCRIPTION

Addressing

Each PCF8591 device in an I^{2}C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be set as the first byte after the start condition in the I^{2}C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figures 1 and 8).

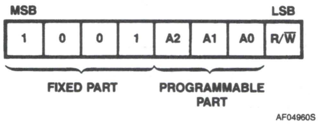


Figure 1. Address Byte

Control Byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Figure 2). If the auto-increment flag is set, the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will always be channel 0. After a power-on reset condition, all bits of the control register are reset to 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high impedance state.

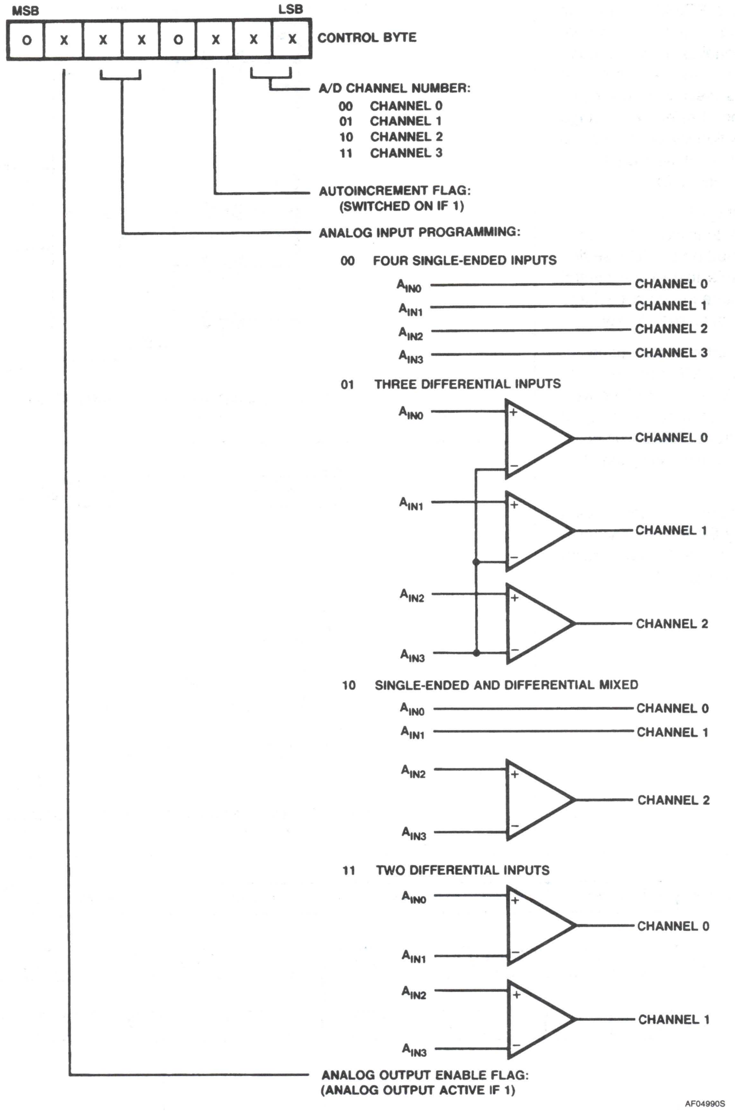

MSB
LSB
0 X X X 0 X X X
CONTROL BYTE
A/D CHANNEL NUMBER:
00 CHANNEL 0
01 CHANNEL 1
10 CHANNEL 2
11 CHANNEL 3
AUTOINCREMENT FLAG:
(SWITCHED ON IF 1)
ANALOG INPUT PROGRAMMING:
00 FOUR SINGLE-ENDED INPUTS
A_IN0 CHANNEL 0
A_IN1 CHANNEL 1
A_IN2 CHANNEL 2
A_IN3 CHANNEL 3
01 THREE DIFFERENTIAL INPUTS
A_IN0 CHANNEL 0
A_IN1 CHANNEL 1
A_IN2 CHANNEL 2
A_IN3
10 SINGLE-ENDED AND DIFFERENTIAL MIXED
A_IN0 CHANNEL 0
A_IN1 CHANNEL 1
A_IN2 CHANNEL 2
A_IN3
11 TWO DIFFERENTIAL INPUTS
A_IN0 CHANNEL 0
A_IN1
A_IN2 CHANNEL 1
A_IN3
ANALOG OUTPUT ENABLE FLAG:
(ANALOG OUTPUT ACTIVE IF 1)
AF04990S

Figure 2. Control Byte

D/A Conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analog voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap decoder switches one of these taps to the DAC output line (see Figure 3).

The analog output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analog output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle, the unity gain amplifier is equipped with a track-and-hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analog output A_{OUT} is given by the formula shown in Figure 4. The waveforms of a D/A conversion sequence as shown in Figure 5.

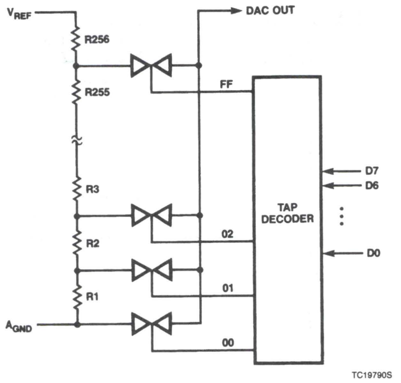

V_{REF}
DAC OUT
R256
R255
FF
R3
R2
R1
A_{GND}
02
01
00
TAP DECODER
D7
D6
D0
TC19790S

Figure 3. DAC Resistor Divider Chain

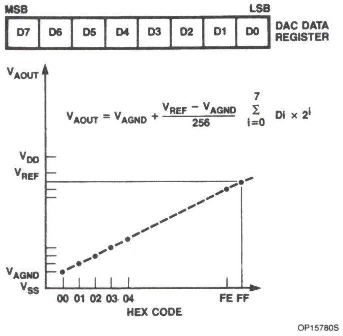


Figure 4. DAC Data and DC Conversion Characteristics

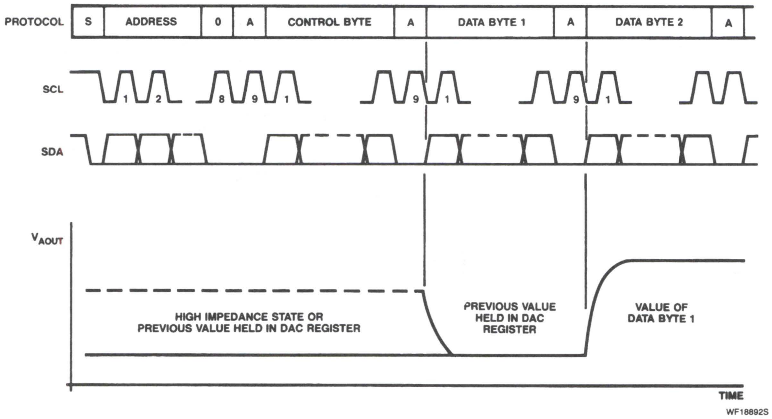

PROTOCOL
S
ADDRESS
0
A
CONTROL BYTE
A
DATA BYTE 1
A
DATA BYTE 2
A
SCL
1
2
8
9
1
9
1
9
1
SDA
V_{AOUT}
HIGH IMPEDANCE STATE OR PREVIOUS VALUE HELD IN DAC REGISTER
PREVIOUS VALUE HELD IN DAC REGISTER
VALUE OF DATA BYTE 1
TIME
WF18892S

Figure 5. D/A Conversion Sequence

A/D Conversion

The A/D converter makes use of the successive-approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Figure 6).

Once a conversion cycle is triggered, an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Figure 7). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set, the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition, the first byte read is a hexadecimal 80. The protocol of an I²C bus read cycle is shown in Figure 8.

The maximum A/D conversion rate is given by the actual speed of the I²C bus.

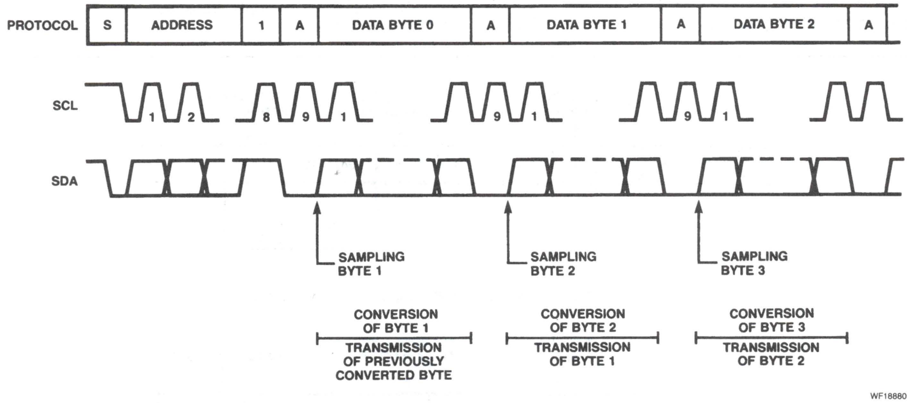
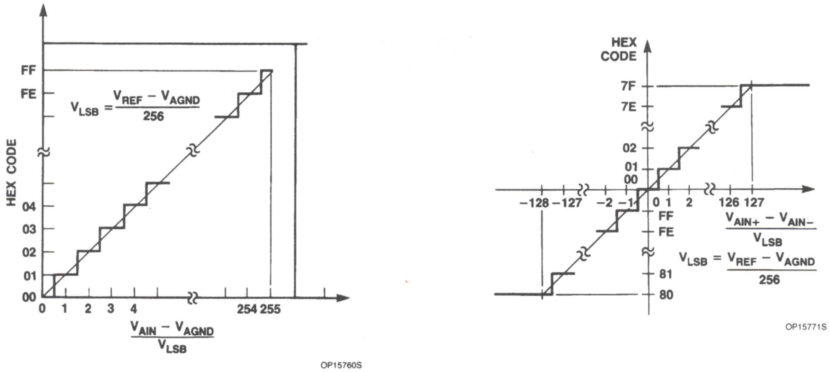

PROTOCOL
S
ADDRESS
1
A
DATA BYTE 0
A
DATA BYTE 1
A
DATA BYTE 2
A
SCL
1
2
8
9
1
9
1
9
1
SDA
SAMPLING BYTE 1
SAMPLING BYTE 2
SAMPLING BYTE 3
CONVERSION OF BYTE 1
TRANSMISSION OF PREVIOUSLY CONVERTED BYTE
CONVERSION OF BYTE 2
TRANSMISSION OF BYTE 1
CONVERSION OF BYTE 3
TRANSMISSION OF BYTE 2
WF18880S

Figure 6. A/D Conversion Sequence



a. A/D Conversion Characteristics of Single-Ended Inputs

b. A/D Conversion Characteristics of Differential Inputs

Figure 7

Reference Voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and A_{GND}). The A_{GND} pin has to be connected to the system analog ground and may have a DC offset with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and A_{GND} pins. This allows the use of the D/A converter as a one-quadrant multiplier (see Figure 4).

The A/D converter may also be used as a one- or two-quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

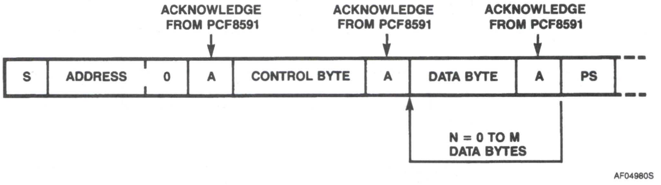
Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator, the EXT pin has to be connected to V_{SS}. At the EXT pin the oscillator frequency is available.

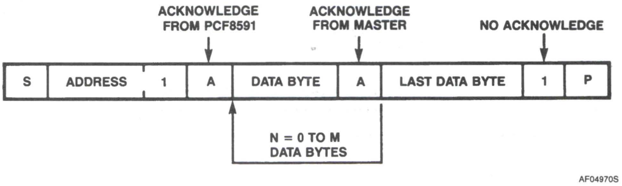
If the OSC_{TEST} pin is connected to V_{DD}, the oscillator output OSC is switched to a high impedance state, allowing the user to feed an external clock signal to OSC.

Bus Protocol

After a start condition, a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode, a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.


ACKNOWLEDGE FROM PCF8591
ACKNOWLEDGE FROM PCF8591
ACKNOWLEDGE FROM PCF8591
S
ADDRESS
0
A
CONTROL BYTE
A
DATA BYTE
A
PS
N = 0 TO M DATA BYTES
AF04980S

a. Bus Protocol for Write Mode, D/A Conversion


ACKNOWLEDGE FROM PCF8591
ACKNOWLEDGE FROM MASTER
NO ACKNOWLEDGE
S
ADDRESS
1
A
DATA BYTE
A
LAST DATA BYTE
1
P
N = 0 TO M DATA BYTES
AF04970S

b. Bus Protocol for Read Mode, A/D Conversion

Figure 8

8-Bit A/D and D/A Converter PCF8591

CHARACTERISTICS OF THE I^{2}C BUS

The I^{2}C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the stop condition (P).

System Configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

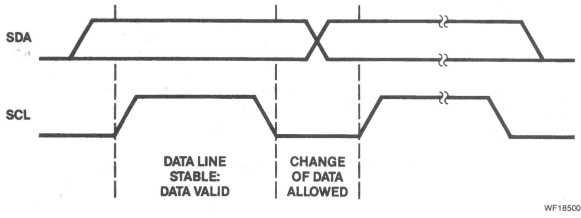

SDA
SCL
DATA LINE STABLE: DATA VALID
CHANGE OF DATA ALLOWED
WF18500S

Figure 9. Bit Transfer

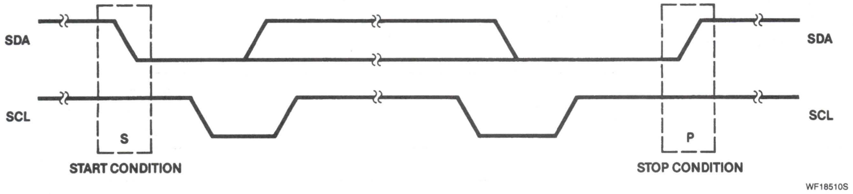

SDA
SCL
S
START CONDITION
P
STOP CONDITION
SDA
SCL
WF18510S

Figure 10. Definition of Start and Stop Condition

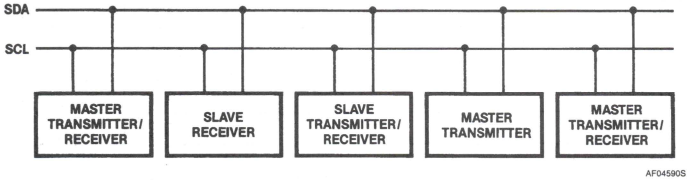

SDA
SCL
MASTER TRANSMITTER/ RECEIVER
SLAVE RECEIVER
SLAVE TRANSMITTER/ RECEIVER
MASTER TRANSMITTER
MASTER TRANSMITTER/ RECEIVER
AF04590S

Figure 11. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. A master receiver must signal an end-of-data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

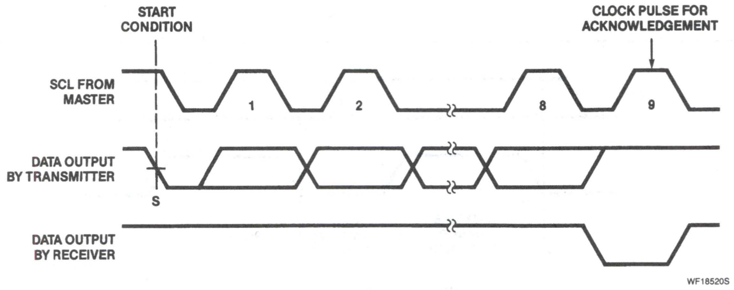


Figure 12. Acknowledgement on the I^{2}C Bus

Timing Specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{SCL}	SCL clock frequency			100	kHz
t_{SW}	Tolerable spike width on bus			100	ns
t_{BUF}	Bus free time	4.0			μs
t_{SU}, t_{STA}	Start condition setup time	4.0			μs
t_{HD}, t_{STA}	Start condition hold time	4.7			μs
t_{LOW}	SCL LOW time	4.7			μs
t_{HIGH}	SCL HIGH time	4.0			μs
t_R	SCL and SDA rise time			1.0	μs
t_F	SCL and SDA fall time			0.3	μs
t_{SU}, t_{DAT}	Data setup time	250			ns
t_{HD}, t_{DAT}	Data hold time	0			ns
t_{VD}, t_{DAT}	SCL LOW to data out valid			3.4	μs
t_{SU}, t_{STO}	Stop condition setup time	4.0			μs

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to V_{GND} or V_{REF}.

In order to prevent excessive ground and supply noise, and to minimize cross-talk of the digital-to-analog signal paths, the user has to design the printed circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10μF) are recommended for power supply and reference voltage inputs.

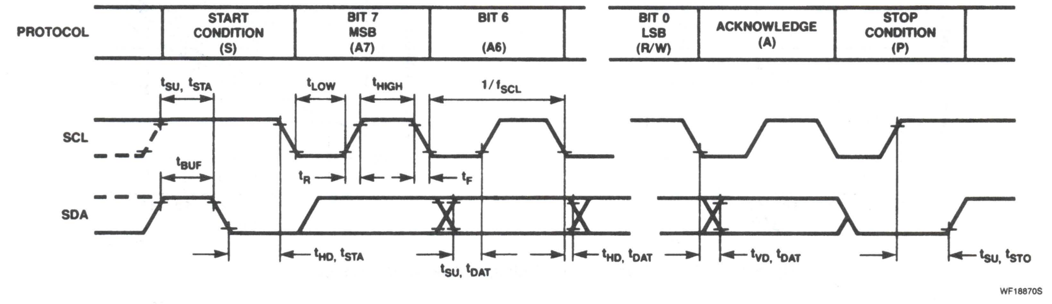

PROTOCOL
START CONDITION (S)
BIT 7 MSB (A7)
BIT 6 (A6)
BIT 0 LSB (R/W)
ACKNOWLEDGE (A)
STOP CONDITION (P)
tSU, tSTA
tLOW
tHIGH
1/fSCL
SCL
tBUF
tR
tF
SDA
tHD, tSTA
tSU, tDAT
tHD, tDAT
tVD, tDAT
tSU, tSTO
WF18870S

Figure 13. I^2C Bus Timing Diagram

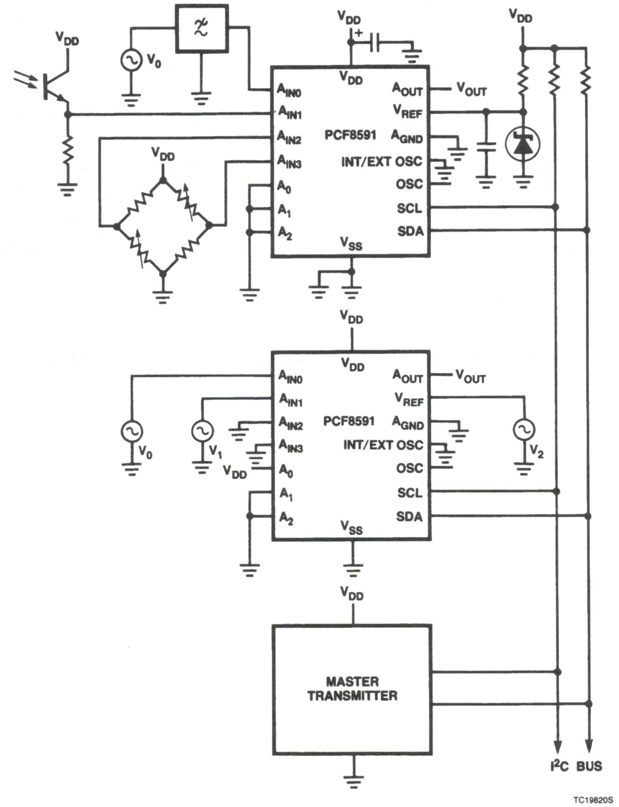
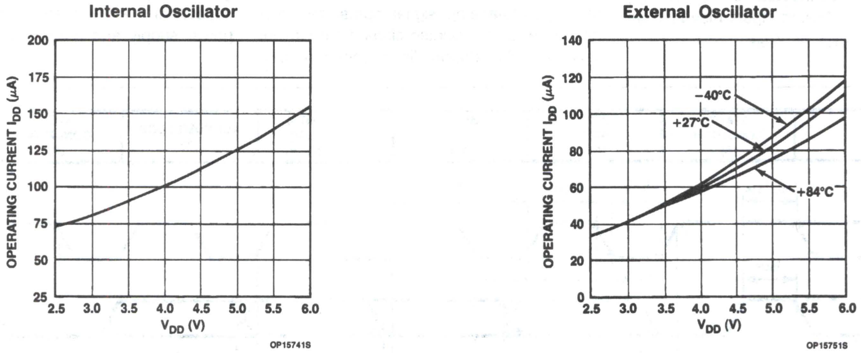
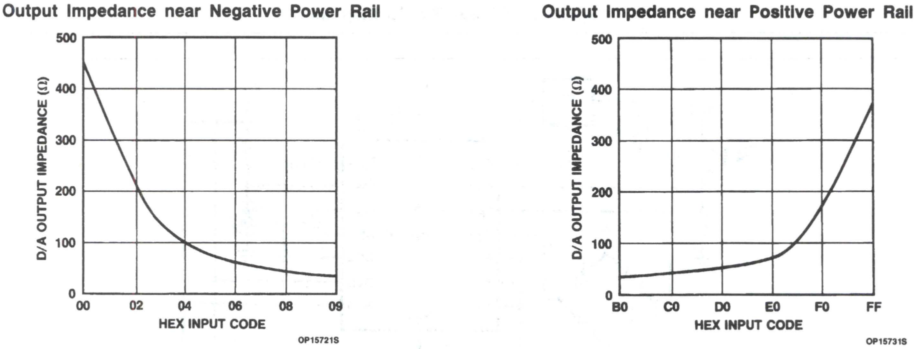

VDD
V0
AIN0
AIN1
AIN2
AIN3
A0
A1
A2
PCF8591
AOUT
VREF
AGND
INT/EXT OSC
OSC
SCL
SDA
VSS
VOUT
V1
V2
MASTER TRANSMITTER
I²C BUS
TC19820S

Figure 14. Application Diagram

TYPICAL PERFORMANCE CHARACTERISTICS



Operating Current vs. Supply Voltage (Analog Output Disabled)



NOTES:

The x-axis represents the hex input-code equivalent of the output voltage.

$V_{DD} = V_{REF} = 5.12V$ and $V_{SS} = V_{AGND}$

Output Impedance of Analog Ouput Buffer Near Power Rails

Signetics

PNA7509
7-Bit Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analog-to-digital converter designed for video applications. The device converts the analog input signal into 7-bit binary coded digital words at a sampling rate of 22MHz.

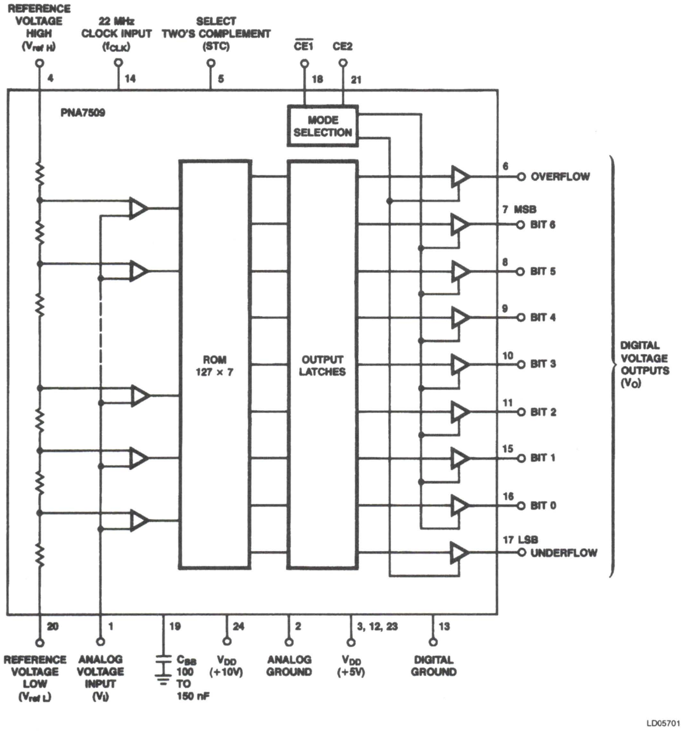
The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge-triggered and can be switched into 3-State mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

FEATURES

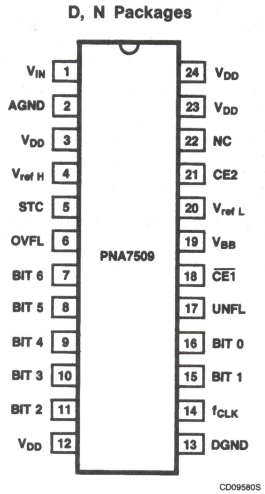
- **7-bit resolution**
- **22MHz clock frequency**
- **No external sample and hold required**
- **High input impedance**
- **Binary or two's complement 3-State TTL outputs**
- **Overflow and underflow 3-state TTL outputs**
- **Low reference current (250µA typ.)**
- **Positive supply voltages (+5V, +10V)**
- **Low power consumption (400mW typ.)**
- **Available in SO package**

BLOCK DIAGRAM



REFERENCE VOLTAGE HIGH ($V_{ref\,H}$)
4
22 MHz CLOCK INPUT (f_{CLK})
14
SELECT TWO'S COMPLEMENT (STC)
5
$\overline{CE1}$
18
CE2
21
PNA7509
MODE SELECTION
ROM 127 × 7
OUTPUT LATCHES
6 OVERFLOW
7 MSB BIT 6
8 BIT 5
9 BIT 4
10 BIT 3
11 BIT 2
15 BIT 1
16 BIT 0
17 LSB UNDERFLOW
DIGITAL VOLTAGE OUTPUTS (V_O)
20
REFERENCE VOLTAGE LOW ($V_{ref\,L}$)
1
ANALOG VOLTAGE INPUT (V_I)
19
C_{BB} 100 TO 150 nF
24
V_{DD} (+10V)
2
ANALOG GROUND
3, 12, 23
V_{DD} (+5V)
13
DIGITAL GROUND
LD05701S

PIN CONFIGURATION



D, N Packages
V_{IN} 1
AGND 2
V_{DD} 3
$V_{ref\,H}$ 4
STC 5
OVFL 6
BIT 6 7
BIT 5 8
BIT 4 9
BIT 3 10
BIT 2 11
V_{DD} 12
24 V_{DD}
23 V_{DD}
22 NC
21 CE2
20 $V_{ref\,L}$
19 V_{BB}
18 $\overline{CE1}$
17 UNFL
16 BIT 0
15 BIT 1
14 f_{CLK}
13 DGND
PNA7509
CD09580S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{IN}	Analog voltage input
2	AGND	Analog ground
3	V_{DD}	Positive supply voltage (+5V)
4	V_{REFH}	Reference voltage HIGH
5	STC	Select two's complement
6	OVFL	Overflow
7	bit 6	Most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD}	Positive supply voltage (+5V)
13	DGND	Digital ground
14	f_{CLK}	22MHz clock input
15	bit 1	
16	bit 0	Least-significant bit (LSB)
17	UNFL	Underflow
18	$\overline{CE1}$	Chip enable input 1
19	V_{BB}	Back bias output
20	V_{REFL}	Reference voltage LOW
21	CE2	Chip enable input 2
22	NC	Not connected
23	V_{DD}	Positive supply voltage (+5V)
24	V_{DD}	Positive supply voltage (+10V)

APPLICATIONS

- **High-speed A/D conversion**
- **Video signal digitizing**
- **Radar pulse analysis**
- **High energy physics research**
- **Transient signal analysis**

7-Bit Analog-to-Digital Converter PNA7509

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	PNA7509N
24-Pin Plastic SO (SOT-101)	0 to +70°C	PNA7509D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pins 3, 12, 23)	7	V
V_{DD}	Supply voltage range (Pin 24)	12	V
V_{IN}	Input voltage range	7	V
V_{OUT}	Output current	5	mA
P_D	Power dissipation	400	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS $V_{DD} = V_{3,\ 12,\ 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $C_{BB} = 100nF$; $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (Pins 3, 12, 23)	4.5		5.5	V
V_{DD}	Supply voltage (Pin 24)	9.5		10.5	V
I_{DD}	Supply current (Pins 3, 12, 23)		60	TBD	mA
I_{DD}	Supply current (Pin 24)		10	TBD	mA
Reference voltages					
V_{REFL}	Reference voltage LOW (Pin 20)	2.4	2.5	2.6	V
V_{REFH}	Reference voltage HIGH (Pin 4)	5.0	5.1	5.2	V
I_{REF}	Reference current	175	250	375	mA
Inputs					
	Clock input (Pin 14)				
V_{IL}	Input voltage LOW	−0.3		0.8	V
V_{IH}	Input voltage HIGH	3.0		5.5	V
	Digital input levels (Pins 5, 18, 21)*				
V_{IL}	Input voltage LOW	0		0.8	V
V_{IH}	Input voltage HIGH	2.0		5.5	V
	Input current				
$-I_{5,\ 21}$	at $V_{5,\ 21-13} = 0V$	TBD		100	μA
I_{18}	at $V_{18-13} = 5V$	TBD		100	μA
	Input leakage current				
I_{LI}	(except Pins 5, 18, 21)			10	μA
	Analog Input levels (Pin 1)				
	at $V_{REFL} = 2.5V$; $V_{REFH} = 5.1V$				
$V_{IN\ P\text{-}P}$	Input voltage amplitude (peak-to-peak value)		2.6		V
V_{IN}	Input voltage (underflow)		2.5		V
V_{IN}	Input voltage (overflow)		5.1		V
$V_I - V_{REFL}$	Offset input voltage (underflow)		10		mV
$V_I - V_{REFH}$	Offset input voltage (overflow)		−10		mV
$C_{1,\ 2}$	Input capacitance	TBD		60	pF
Outputs					
	Digital voltage outputs (Pins 6 to 11 and 15 to 17)				
	Output voltage LOW				
V_{OL}	at $I_O = 2mA$	0		−0.4	V
	Output voltage HIGH				
V_{OH}	at $-I_O = 0.5mA$	2.4		V_{DD}	V

*When Pin 5 is LOW, binary coding is selected.
When Pin 5 is HIGH, two's complement is selected.
If Pins 5, 18 and 21 are open-circuit, Pins 5, 21 are HIGH and Pin 18 is LOW.
For output coding, see Table 1; for mode selection, see Table 2.

AC ELECTRICAL CHARACTERISTICS $V_{DD} = V_{3,\ 12,\ 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $V_{REFL} = 2.5V$; $V_{REFH} = 5.1V$; $f_{CLK} = 22MHz$; $C_{BB} = 100nF$; $T_A = 0$ to $+70°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Timing (see also Figure 1)					
	Clock input (Pin 14)				
f_{CLK}	clock frequency	1		22	MHz
t_{LOW}	clock cycle time LOW	20			ns
t_{HIGH}	clock cycle time HIGH	20			ns
	Input rise and fall times[1]				
t_R	rise time			3	ns
t_F	fall time			3	ns
	Analog input[1]				
BW	Bandwidth (−3 dB)				
	at $V_{1-2(P\text{-}P)} = 2.2V$	10			MHz
dG	Differential gain				
	at $f_I = \leqslant 4.5MHz$[2]			5	%
dp	Differential phase				
	at $f_I = \leqslant 4.5MHz$[2]			5	deg
P_E	Phase error				
	at $f_I = \leqslant 4.5MHz$[3]			±10	deg
S/N	Signal-to-noise ratio				
	at $V_{1-2(P\text{-}P)} = 2.2V$;				
	$f_I = \leqslant 4.5MHz$; $B = \pm 1$ MHz	36			dB
	Harmonics				
	at $V_{1-2(P\text{-}P)} = 2.2V$;				
	$f_I = 3.6MHz$				
f_0	Fundamental		0	0	dB
f_{2nd}	2nd harmonic			tbd	dB
f_{3rd}	3rd harmonic			tbd	dB
f_{4th}	4th harmonic			tbd	dB
f_{5th}	5th harmonic			tbd	dB
f_{6th}	6th harmonic			tbd	dB
f_{7th}	7th harmonic			tbd	dB
	Harmonics				
	at $V_{1-2(P\text{-}P)} = 2.2V$;				
	$f_I = 4.5MHz$				
f_0	Fundamental		0	0	dB
f_{2nd}	2nd harmonic			tbd	dB
f_{3rd}	3rd harmonic			tbd	dB
f_{4th}	4th harmonic			tbd	dB
f_{5th}	5th harmonic			tbd	dB
f_{6th}	6th harmonic			tbd	dB
f_{7th}	7th harmonic			tbd	dB
	Digital outputs[2, 4]				
t_{HOLD}	Output hold time	6	15		ns
t_D	Output delay time		20	28	ns
t_{CY}	Internal delay		3		clocks
	Propagation delay time				
t_{PD}	at $f_{CLK} = 20.25MHz$	154		176	ns
t_{DT}	3-State delay time (see Figure 2)	t_{BF}	10	20	ns
C_{OL}	Capacitive output load[2]	0		15	pF
	Transfer function				
	Non-linearity				
INL	integral			±1	LSB
DNL	differential			±1/2 = 0.4%	LSB

NOTES:

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sine wave (peak-to-peak value of the analog input voltage at $V_{IN} = 1.8V$) amplitude modulated with a sine wave voltage ($V_{IN} = 0.7V$) at $f_I \leqslant 4.5MHz$.
3. Sine wave voltage with increasing amplitude at $f_I \leqslant 4.5MHz$ (minimum amplitude $V_{IN} = 0.25V$; maximum amplitude $V_{IN} = 2.5V$).
4. The timing values of the digital output Pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5V.

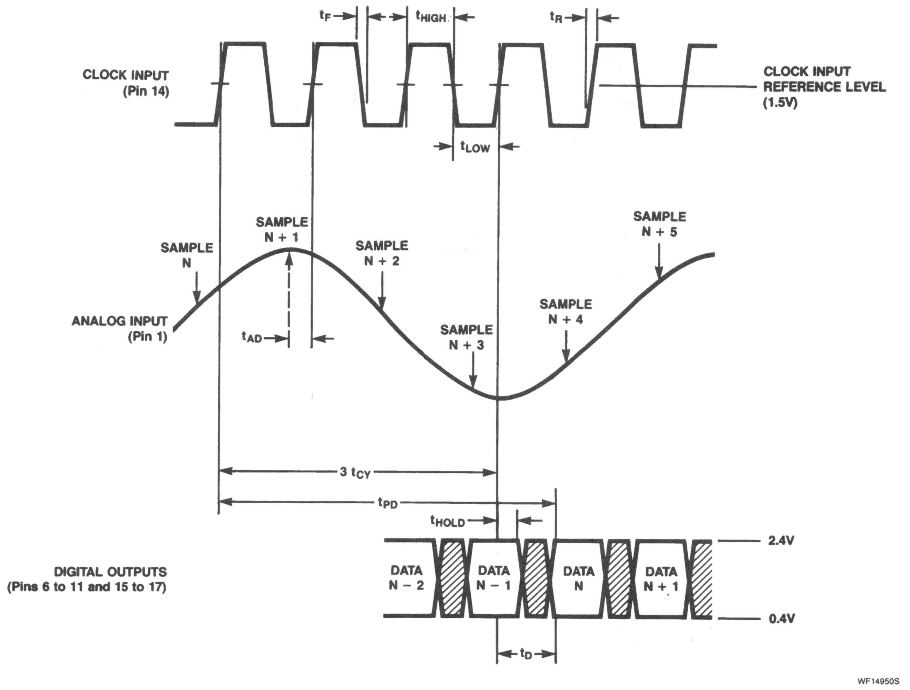
7-Bit Analog-to-Digital Converter PNA7509

Table 1. Output Coding (V_{REFL} = 2.5V; V_{REFH} = 5.1V)

STEP	$V_{1,2}$ (Typ)	UNFL	OVFL	BINARY Bit 6 – Bit 0	TWO's COMPLEMENT Bit 6 – Bit 0
Underflow	< 2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
Overflow	⩾ 5.07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

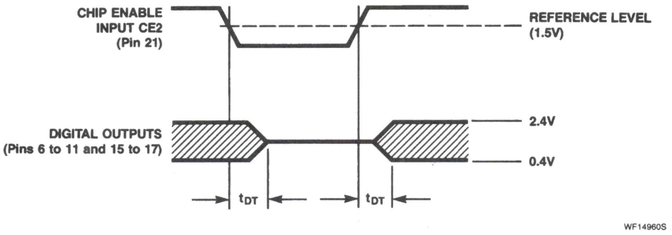
Table 2. Mode Selection

CE1	CE2	BIT 0 to BIT 6	UNFL, OVFL
X	0	High impedance	High impedance
0	1	Active	Active
1	1	High impedance	Active



t_F
t_{HIGH}
t_R
CLOCK INPUT (Pin 14)
CLOCK INPUT REFERENCE LEVEL (1.5V)
t_{LOW}
SAMPLE N
SAMPLE N + 1
SAMPLE N + 2
SAMPLE N + 3
SAMPLE N + 4
SAMPLE N + 5
ANALOG INPUT (Pin 1)
t_{AD}
3 t_{CY}
t_{PD}
t_{HOLD}
DIGITAL OUTPUTS (Pins 6 to 11 and 15 to 17)
DATA N – 2
DATA N – 1
DATA N
DATA N + 1
2.4V
0.4V
t_D
WF14950S

Figure 1. Timing Diagram



CHIP ENABLE INPUT CE2 (Pin 21)
REFERENCE LEVEL (1.5V)
DIGITAL OUTPUTS (Pins 6 to 11 and 15 to 17)
2.4V
0.4V
t_{DT}
t_{DT}
WF14960S

Figure 2. Timing Diagram for 3-State Delay

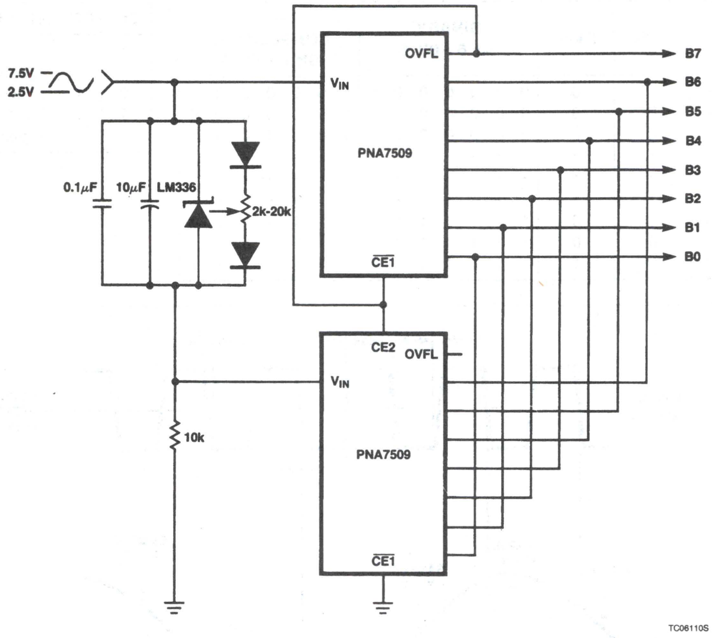

7.5V
2.5V
0.1μF
10μF
LM336
2k-20k
10k
VIN
PNA7509
OVFL
CE1
CE2
VIN
PNA7509
OVFL
CE1
B7
B6
B5
B4
B3
B2
B1
B0
TC06110S

Figure 3

Signetics

Linear Products

AN108

An Amplifying, Level-Shifting Interface for the PNA7509 Video A/D Converter

Application Note

Author: Nick Gray

The NE5539 is well-suited for use as a level-shifting amplifier at the input of the PNA7509 video speed analog-to-digital converter. Designing this circuit is straightforward and relatively simple.

The first step is to determine the gain that is required. Since the PNA7509 requires a maximum input of 5.0 V_{DC} and a minimum input of 2.5V_{DC} the required amplifier gain is

$$A_V = \frac{5.0 - 2.5}{V_{MAX} - V_{MIN}} = \frac{2.5}{V_{MAX} - V_{MIN}}.$$

where V_{MAX} is the maximum level of the amplifier input signal, and V_{MIN} is the minimum level of the amplifier input signal.

This gain must be greater than unity as the gain of a non-inverting amplifier such as this is

$$A_V = 1 + (R_F/R_I).$$

The ratio of R_F to R_I is then

$$R_F/R_I = A_V - 1.$$

The task is now to select R_F and R_I. These resistors should be low enough to swamp out the effects of any stray capacitance. If R_I is arbitrarily chosen, R_F is found to be

$$R_F = \frac{1.5\ R_I}{V_{MAX} - V_{MIN}}.$$

The required offset voltage, V_O, is then found to be

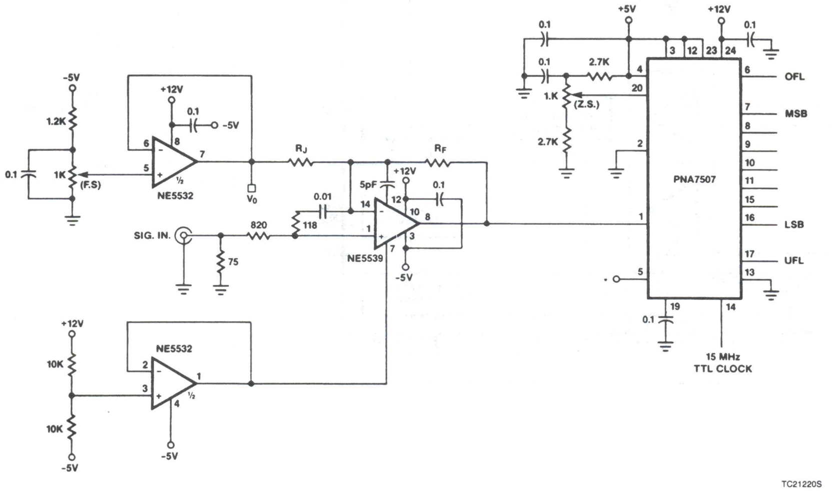
$$V_O = V_{MAX} - [(5 - V_{MAX})\ (R_I/R_F)].$$

Because the NE5539 input cannot be driven closer to its negative supply than about 4.7V, that negative supply must be −4.7V or more negative in order to accommodate an input signal whose minimum potential is 0V. The NE5539 output must never come any closer to the supply rail than about 5.5V, and the maximum output required to drive the PNA7509 is 5V, so the positive supply must be at least 5 + 5.5V, or 10.5V. If we use standard power supply potentials of +12V and −5V, this would satisfy these requirements, except we must insure that the negative supply is at least as negative as −4.7V. Tests have been conducted that indicate satisfactory operation with the positive supply between 10.5V and 13.5V, and the negative supply between −4.7V and −5.7V. Furthermore, because the NE5539 is sensitive to unbalance in the supplies, it is necessary to insure that its Pin 7 potential is close to halfway between the positive and the negative supply. Two resistors and an op amp driving Pin 7 nicely provide this balance. Another op amp is used to set the offset voltage.

The three diodes are used to drop the 12V supply to 10V for the PNA7509. If available and desired, a separate 10V supply could be used without the diodes.

Other components are shown for the convenience of the user. The potentiometer at Pin 5 of the NE5514 is used to adjust V_O. The potentiometer at Pin 12 of the NE5514 sets the voltage at the low end of the PNA7509 reference ladder, so is a zero-scale adjustment. The potentiometer at Pin 3 of the NE5514 sets the high end voltage on the PNA7509 reference ladder and is, effectively, a full-scale adjustment. It is also possible to use a signal divider at the NE5539 input for full-scale adjustment. R_F can also be made variable to provide full-scale adjustment. Care should be exercised, however, when introducing potentiometers into feedback loops or into high-frequency signal paths.

The NE5514 was chosen for its low input offset voltage temperature coefficient.



NOTE:
*Pin 5 should be grounded for binary output, or tied to a logic high for two's complement output.

Signetics

TDA1534

14-Bit Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA1534 is a complete monolithic 14-bit analog-to-digital converter (ADC) which uses the successive approximation conversion technique and includes a 14-bit DAC, SAR, comparator, reference source, and clock on the chip. The digital functions are implemented with ECL logic with TTL level shifters interfacing with the device pins.

FEATURES

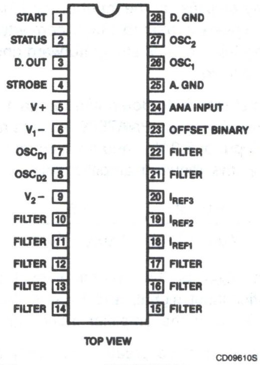
- **½ LSB linearity over temperature**
- **¼ LSB linearity at 25°C**
- **Accepts unipolar or bipolar signals**
- **TTL compatible logic lines**
- **Internal clock**
- **Internal reference**
- **High signal-to-noise ratio (84dB typ)**

APPLICATIONS

- **Automotive**
- **Digital audio**
- **Digital signal processing**
- **Instrumentation**
- **Medical electronics**
- **Industrial**

PIN CONFIGURATION

N Package

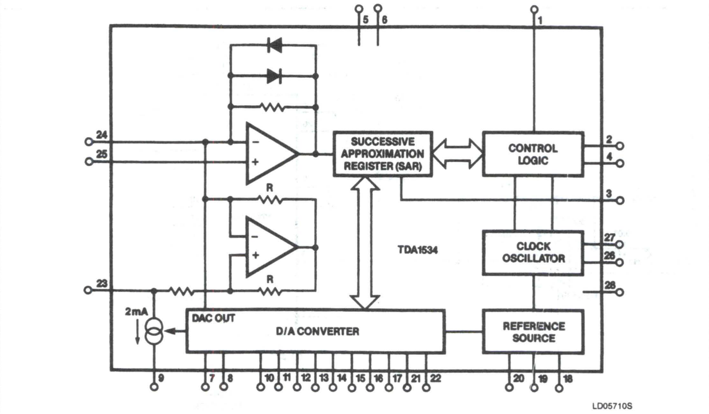

START 1
STATUS 2
D. OUT 3
STROBE 4
V+ 5
V_1− 6
OSC_{D1} 7
OSC_{D2} 8
V_2− 9
FILTER 10
FILTER 11
FILTER 12
FILTER 13
FILTER 14
28 D. GND
27 OSC_2
26 OSC_1
25 A. GND
24 ANA INPUT
23 OFFSET BINARY
22 FILTER
21 FILTER
20 I_{REF3}
19 I_{REF2}
18 I_{REF1}
17 FILTER
16 FILTER
15 FILTER
TOP VIEW
CD09610S

PIN NO.	DESCRIPTION
1	Start Conversion
2	Status Out
3	Data Out
4	Data Strobe
5	Positive Supply Voltage
6	Negative Supply Voltage 1
7	Oscillator Input
8	Oscillator Input
9	Negative Supply Voltage 2
10	Filter
11	
12	
13	
14	
15	Filter
16	
17	
18	I_{REF1}
19	I_{REF2}
20	I_{REF3}
21	Filter
22	
23	Offset Binary Input
24	Analog Signal Input
25	Analog Ground
26	Oscillator
27	Oscillator
28	Digital Ground

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
Plastic 28-Pin DIP	−20°C to +70°C	TDA1534N

BLOCK DIAGRAM


5
6
1
24
25
SUCCESSIVE APPROXIMATION REGISTER (SAR)
CONTROL LOGIC
2
4
3
R
R
TDA1534
CLOCK OSCILLATOR
27
26
28
23
2mA
DAC OUT
D/A CONVERTER
REFERENCE SOURCE
9
7
8
10
11
12
13
14
15
16
17
21
22
20
19
18
LD05710S

14-Bit Analog-to-Digital Converter **TDA1534**

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_+	Positive supply voltage (Pin 5)	7	V
V_1-	Negative supply voltage (Pin 6)	−7	V
V_2-	Negative supply voltage (Pin 6)	−20	V
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C
P_D	Power dissipation (25°C)	3.5	W

DC ELECTRICAL CHARACTERISTICS $V+ = 5V$, $V_1- = -5V$, $V_2- = -17V$, $T_A = +25°C$, unless otherwise specified.

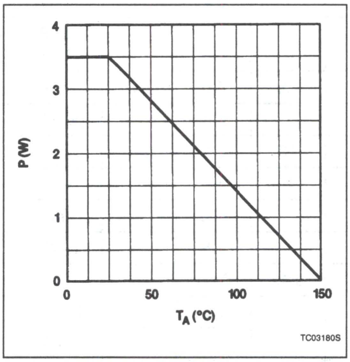
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution			14		bits
ϵ_L	Linearity			±¼		LSB
		−20°C to +70°C		±½		LSB
I_{FS}	Full-scale analog input current	Pin 23 shorted to ground	3.8	4.0	4.2	mA
TC_A	Tempco of analog input current	Pin 23 shorted to ground		±30		ppm/°C
V_O	Zero-scale offset voltage	Pin 23 shorted to ground	10	20	30	mV
TC_{VO}	Tempco of zero-scale offset voltage	0 to 50°C, Pin 23 grounded		80		μV/°C
I_{OS}	Zero-scale offset current	Pin 23 shorted to ground		500		nA
TC_{IO}	Tempco of input offset current	Pin 23 shorted to ground		1.5		nA/°C
I_{BO}	Offset binary current		0.45	0.50	0.55	I_{FS}
TC_{IBO}	Tempco of offset binary current			30		10^{-6}/°C
I_{IL}	Start conversion input current (Pin 1)	$V_{IL} < 0.8V$			−1.6	mA
I_{IH}	Start conversion input current (Pin 1)	$V_{IL} > 2.0V$			40	μA
I_{OL}	Output low current (Pins 2, 3, 4)	$V_{OL} < 0.6V$	6.4	16		mA
I_{OH}	Output high current (Pins 2, 3, 4)	$V_{OH} > 2.4V$	160	400		μA
S/N	Signal-to-noise ratio[1]		80	84		dB
V+	Positive supply voltage (Pin 5)		4	5	6	V
V_1-	Negative supply voltage (Pin 6)			−5		V
V_2-	Negative supply voltage (Pin 9)		−16.5	−17	−18	V
$I_{CC}+$	Positive supply current			30	40	mA
I_{CC-1}	Negative supply current			−37	−45	mA
I_{CC-2}	Negative supply current			−10	−13	mA
P_D	Power dissipation			500		mW

AC ELECTRICAL CHARACTERISTICS $V+ = 5V$, $V_1- = -5V$, $V_2- = -17V$, $T_A = +25°C$, unless otherwise specified.

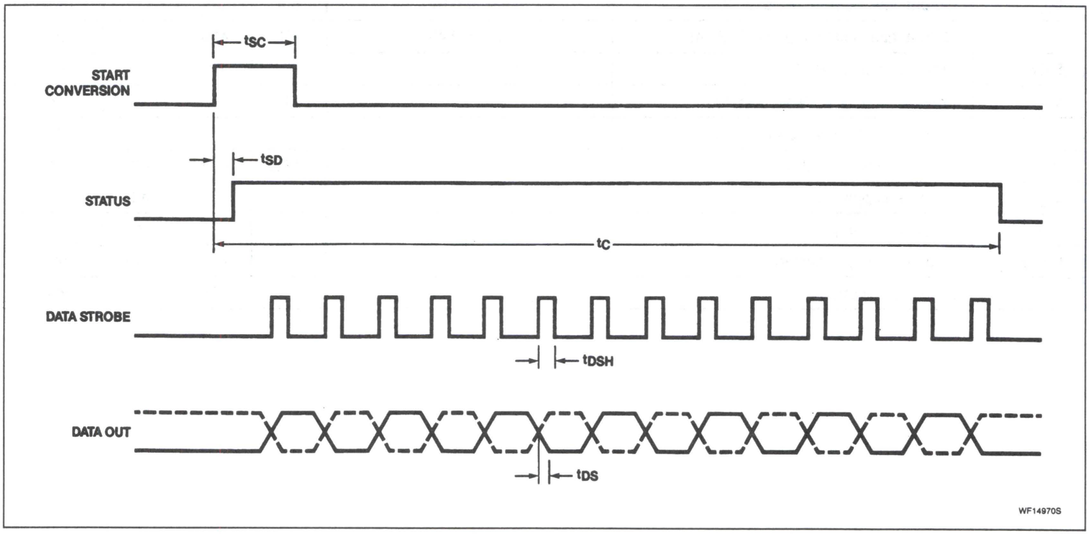
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{CONV}	Conversion time	Clock capacitor = 220pF Pins 26 – 27 (± 1%)		8.5		µs
t_{SC}	Start conversion pulse width	(Pin 1)	0.2			µs
t_{SD}	STATUS out delay time	(Pin 2)		60		ns
t_{DS}	DATA setup time	(Pin 3)		25		ns
t_{DSH}	DATA STROBE pulse duration	(Pin 4)		125		ns

NOTES:
Signal-to-noise ratio within 10Hz and 20kHz bandwidth of a 1kHz full-scale sinewave, generated at a sample rate of 44kHz.

POWER DERATING CURVE



SWITCHING TIME WAVEFORMS


t_{SC}
START CONVERSION
t_{SD}
STATUS
t_C
DATA STROBE
t_{DSH}
DATA OUT
t_{DS}
WF14970S

FUNCTIONAL OPERATION AND USE

The TDA1534 Analog-to-Digital Converter (ADC) incorporates a 14-bit Digital-to-Analog Converter (DAC) that is functionally equivalent to the TDA1540 14-bit DAC. This DAC uses a unique **Dynamic Element Matching** scheme (Electronic Components and Applications, Vol. 2, No. 4, August 1980, by R.J. v. d. Plassche; IEEE Journal of Solid State Circuits, Vol. SC14, June 1979, pp. 552-556, by R.J. v. d. Plassche and D. Goedhardt) that insures 14-bit accuracy.

The Dynamic Element Matching technique requires an oscillator for current switching. In the TDA1534, the frequency of this oscillator is determined by the value of a capacitor between Pins 7 and 8. With the suggested 820pF capacitor, the internal clock frequency is about 160kHz. The capacitor value vs. oscillator frequency is a linear relationship. The conversion speed bears no relationship to this switching frequency because the switched currents are filtered and are simply DC values on the chip. The value of the ten filter capacitors is not particularly critical; −30% to +100% tolerance being allowed.

The acceptable frequency range for the Dynamic Element Marching oscillator is 150kHz to 250kHz. The minimum value arises from the fact that the divide-by-four action of the Dynamic Element Matching operation makes too low a frequency fall into the audio passband. The maximum value is needed because at high frequencies the oscillator jitter becomes too great a part of the clock period and causes inaccuracy in the Dynamic Element Matching current division and a loss of accuracy. It is suggested that the oscillator frequency be chosen so that it is close to the 150kHz minimum to keep the jitter from approaching ½ clock period. This would provide greatest accuracy.

The **Dynamic Element Matching** scheme takes each bit current and divides it in four. Two of these currents are combined to produce the current of the next lower bit. To insure that this current is half of its next higher bit, the two currents that are summed are sequenced in a predetermined pattern. For example, if the currents A, B, C, and D, we might first combine currents A and C, then A and D, then B and D, then A and B, etc., to allow for any small differences between individual currents, making the average current exactly half that of the next higher bit. In this way, high accuracy is obtained with high yield and relatively low cost. The disadvantage here is the requirement for the ten filter (decoupling) capacitors and the relatively large negative supply of 17V (use of 18V is quite permissible).

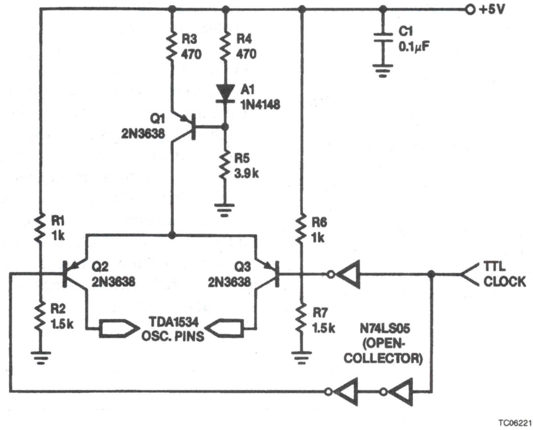


Figure 1. An Example of a Dual Current Source That may be Used to Drive the Oscillator Pins When an External Oscillator is Required. Note That Timing and the Number of Clock Cycles are Very Important for Proper Operation

The **Reference Source** is a temperature-corrected bandgap type. The 162Ω resistor at Pin 19 trims the bandgap PTC (positive temperature coefficient), while the 1200Ω resistor at Pin 20 is used to temperature-correct the reference with an NTC (negative temperature coefficient) that essentially cancels out the effect of the PTC, yielding a reference voltage that is constant over temperature. The 3.3nF (0.003µF) capacitor at Pin 18 is used for stabilizing the reference and offers a little noise filtering. It should be noted, however, that it is not reasonable to increase this capacitor to achieve additional noise filtering as its primary function is for circuit stabilization and the 3.3nF value is needed for this.

The **Clock Oscillator** with timing capacitor at Pins 26 and 27 is the A/D clock, which operates at about 3.5MHz with a 220pF capacitor between these two pins. The relationship between oscillator frequency and capacitance is linear, but a higher frequency (lower capacitance) will cause a loss of converter accuracy. A lower frequency (higher capacitance) will cause the conversion time to increase, although this will *not* result in an accuracy improvement. These pins can be driven in a complementary manner with two identical current sources if it is desired to use an external clock. See Figure 1 for a possible circuit to use with external clock drive. It is important that the Start Conversion signal begin within 10µs of the center of the time that the clock is at a logic low, that the clock have a 50% duty cycle, and that exactly 30 clock cycles occur during each conversion cycle. The converter requires 30 clock cycles for one conversion, yielding an 8.5µs conversion time at 3.5MHz clock frequency.

The **Status** output goes high to indicate a conversion in progress, and can be conveniently used to control a sample-and-hold amplifier such as the TDA1535. When the **Start Conversion** input (Pin 1) is brought high, the **Status** output immediately goes high, but there is a delay of two external clock periods (about ½µs) before conversion begins. The **Status** pin may, therefore, be connected to the Sample/Hold control pin of a Sample-and-Hold amplifier (as long as the input interprets a logic high to be a "Hold" signal), eliminating the need for two separate commands: one to the sample-and-hold amplifier and another to the A/D converter. See Figure 2.

Note that the TDA1535 acquisition time is stated at 2µs, yet conversion begins about ½µs after the Status output goes high. The acquisition time is the time it takes the sample-and-hold amplifier output to make a full range swing when going from sample (track) to hold. When the sample-and-hold is in the track or sample mode and goes to the hold mode, as is the case when the status output goes from a logic low to a logic high, the time for the sample-and-hold output to settle is much less, and the ½µs is sufficient time for the sample-and-hold amplifier to settle when going from the sample or track mode to the hold mode.

There are about 3 external clock periods (about 1.5 internal clock periods — the internal clock being half the frequency of the external clock), or about 850ns, between the rise of the **Start Conversion** input to the fall of the first **Data Strobe** output, the center of the MSB data valid time.

The **Start Conversion** pulse must have a very fast rise time to insure that the **Status Output** goes high with minimum delay. With excessive delay in the **Status Output**, the sample-and-hold amplifier could go into the hold mode *after* the MSB is determined, adding inaccuracy to the conversion. Normal TTL switching speeds are adequate. Once a conversion has been started, the signal at the **Start Conversion** input will have no effect, so it is not possible to short cycle the TDA1534.

Data at the **Data Output** pin appears MSB (Most Significant Bit) first and the **Data Strobe** output pulses only appear while a conversion is in progress, going low each time a valid bit is present at the **Data Out** pin. Data should only be considered valid at the falling edge of this **Data Strobe** output, so a negative *edge-triggered* serial-in, parallel-out register should be used for serial-to-parallel conversion. Since shift register decoding is done within the TDA1534, there is no need to externally determine when the MSB is valid and when to stop clocking data into the shift register. The **Data Strobe** is used to directly load the shift register, simplifying circuit design. See Figure 2.

Pin 23 is the **Offset Binary** input pin. With this pin grounded, the converter will accept input currents in the range of 0 to 4mA. With a capacitor between Pin 23 and ground, the acceptable linear range of input currents is −2mA to +2mA, and the converter operates in the so-called "Offset Binary" mode. This pin should not be left floating as the converter accuracy could suffer due to energy from the Dynamic Element Matching oscillator feeding into the input, effectively adding 160kHz noise there.

The **Analog Signal Input**, Pin 24, is a virtual ground, so a series resistor is needed to limit the input current range to −2mA to +2mA with Pin 23 grounded through a capacitor, or to 0 to 4mA with Pin 23 at AC ground.

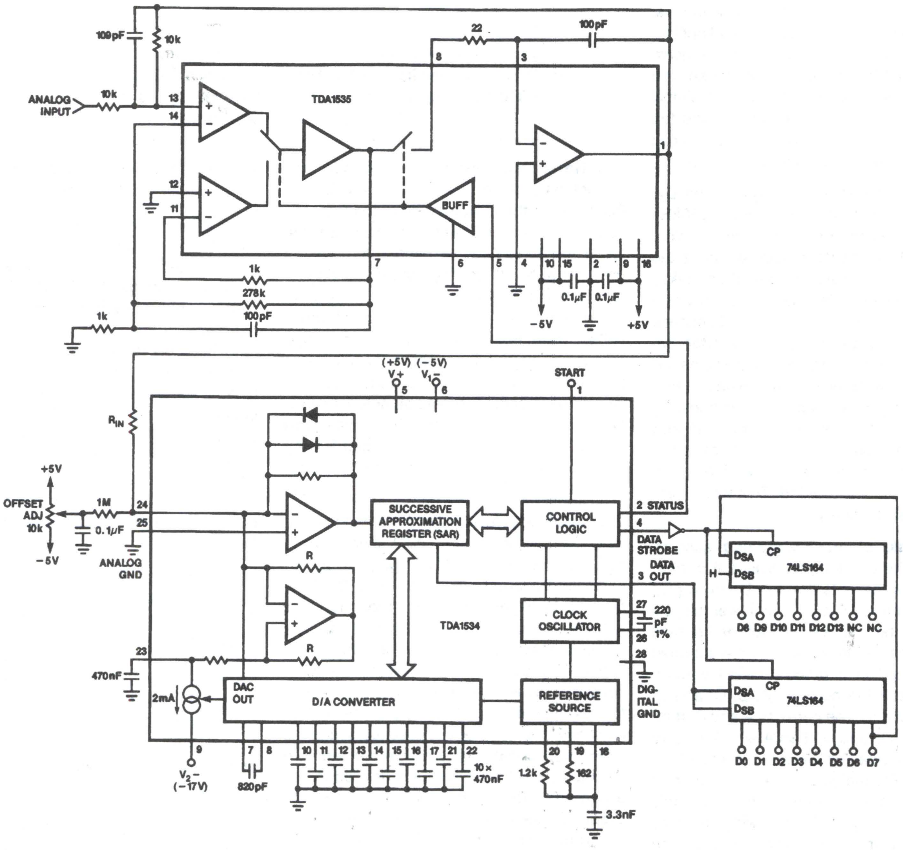

109pF
10k
22
100pF
ANALOG INPUT
10k
13
14
TDA1535
8
3
12
11
1
BUFF
7
6
5
4
10
15
2
9
16
1k
278k
100pF
1k
0.1μF
0.1μF
−5V
+5V
(+5V) (−5V)
V+
V_1−
5
6
START
1
R_{IN}
+5V
OFFSET ADJ 10k
−5V
1M
0.1μF
24
25
ANALOG GND
SUCCESSIVE APPROXIMATION REGISTER (SAR)
CONTROL LOGIC
2 STATUS
4
DATA STROBE
DATA
3 OUT
D_{SA}
CP
D_{SB}
H
74LS164
D8 D9 D10 D11 D12 D13 NC NC
R
R
TDA1534
CLOCK OSCILLATOR
27
220 pF 1%
26
28
DIG-ITAL GND
23
470nF
2mA
DAC OUT
D/A CONVERTER
REFERENCE SOURCE
D_{SA}
CP
D_{SB}
74LS164
D0 D1 D2 D3 D4 D5 D6 D7
9
V_2−
(−17V)
7
8
820pF
10
11
12
13
14
15
16
17
21
22
10× 470nF
20
19
18
1.2k
162
3.3nF
TC06231S

Figure 2. The Status Output Can Be Used to Control a Sample-and-Hold Amplifier, While the Data Strobe Output Controls a Serial-to-Parallel Shift Register

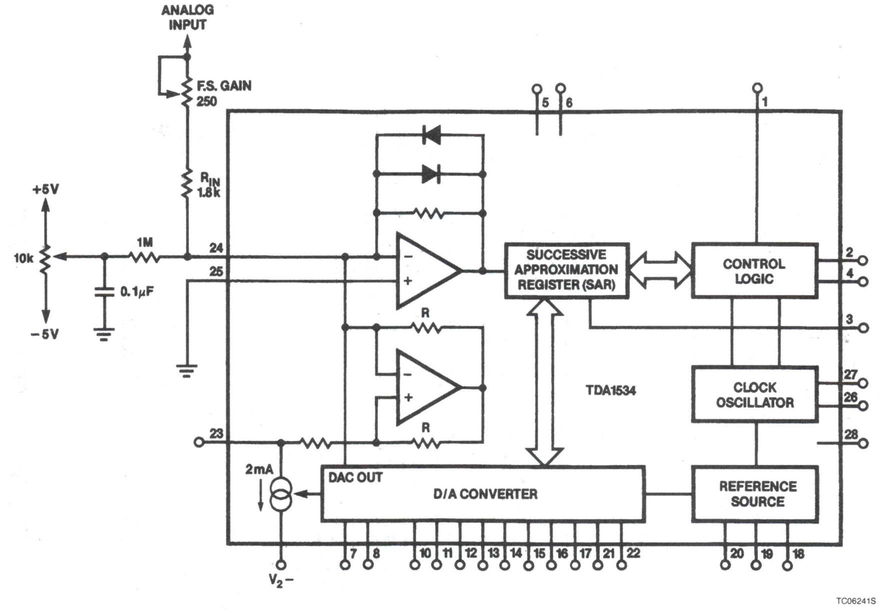


Figure 3. Zero-Scale Offset and Full-Scale Gain Adjustment

ZERO-SCALE OFFSET ADJUST

The analog signal input at Pin 24 is a current input and, to compensate for the zero-scale offset error, it is necessary to inject the proper current at Pin 24. This is easily accomplished by connecting the wiper of a potentiometer to Pin 24 in series with a 1MΩ resistor. Figure 3 illustrates how this may be accomplished.

FULL-SCALE GAIN ADJUSTMENT

Since the analog signal is a current input, the value of this current being determined by the analog voltage input and the value of the input resistor, R_{IN}, the Full-Scale Gain Adjustment, is simply making R_{IN} an adjustable resistor, or rheostat. The problem with a single adjustable resistor, however, is the fact that potentiometers have a rather large temperature coefficient. A gain adjustment that is reasonably stable would be a fixed film resistor in series with a rheostat, with the majority of the resistance in the fixed resistor. Figure 3 illustrates how this is accomplished.

AMBIENT TEMPERATURE CONSIDERATIONS

The TDA1534 is tested and rated for operation over the commercial temperature range (−20°C to +70°C). Above 70°C, the digital portion of the converter ceases to function and the converter will not operate at all. At temperatures much below −20°C the base-emitter junction voltage of the transistors increases to the point where the −17V supply is not sufficient to provide enough voltage to properly bias all the transistors that are stacked upon each other and accuracy begins to suffer. Increasing the negative supply to −19V *should* allow lower temperature operation, but behavior below −20°C is unknown and not guaranteed.

LAYOUT PRECAUTIONS

Layout of high bit count data converters requires a great deal of caution if maximum accuracy is to be realized. Just a little noise, as little as a few hundred microvolts, can cause errors as high as a few counts.

As is the case with all A/D converters, the analog ground and the digital ground must be connected together as close to the device as is possible. This is the only point on the board where the analog and digital grounds should be connected together. The signal return line should have its own path from the signal source return to the A/D converter analog ground to prevent ground noise fluctuations from detracting from converter accuracy. Neither the signal input line nor the signal return line should be run parallel to lines carrying digital information and should be as short as is reasonably possible.

As always with any linear IC, the power supplies should be as stable as possible and should be bypassed as close to the power supply pins as possible.

The oscillator should be located as close to the converter package as possible, as should the resistors and capacitor at Pins 18, 19, 20 and 23. The entire path from the input source to Pin 24 should be as short as possible, as should the trace from the STATUS output to the sample-and hold control input (if the STATUS output is used to control the sample-and-hold amplifier).

Signetics

TDA5703

Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA5703 is an 8-bit analog-to-digital converter (ADC) designed for video and professional applications. The TDA5703 converts the analog input signal into 8-bit binary-coded digital words at a sampling rate of up to 25MHz.

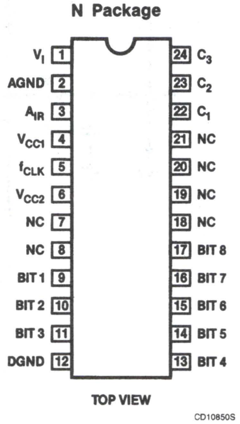
FEATURES

- **8-bit binary coded resolution**
- **Digitizing rates up to 25MHz**
- **Internal reference**
- **Only 3 external capacitors required**
- **Two voltage supply connections:**
  - **analog +5V**
  - **digital +5V**
- **1V full-scale analog input (75Ω external resistor tied to V_{CC1})**
- **Full-scale bandwidth; 11MHz at 3dB**
- **Low power consumption; typically 250mW**
- **24-lead plastic DIP**

APPLICATION

- **Video data conversion**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	V_I	Analog voltage input
2	AGND	Analog ground
3	A_{IR}	Analog input reference
4	V_{CC1}	Analog supply voltage
5	f_{CLK}	Clock input
6	V_{CC2}	Digital supply voltage
7	NC	Not connected
8	NC	Not connected
9	Bit 1	Least significant bit (LSB)
10	Bit 2	
11	Bit 3	
12	DGND	Digital ground
13	Bit 4	
14	Bit 5	
15	Bit 6	
16	Bit 7	
17	Bit 8	Most significant bit (MSB)
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	NC	Not connected
22	C_1	Decoupling for internal reference
23	C_2	
24	C_3	

ORDERING INFORMATION

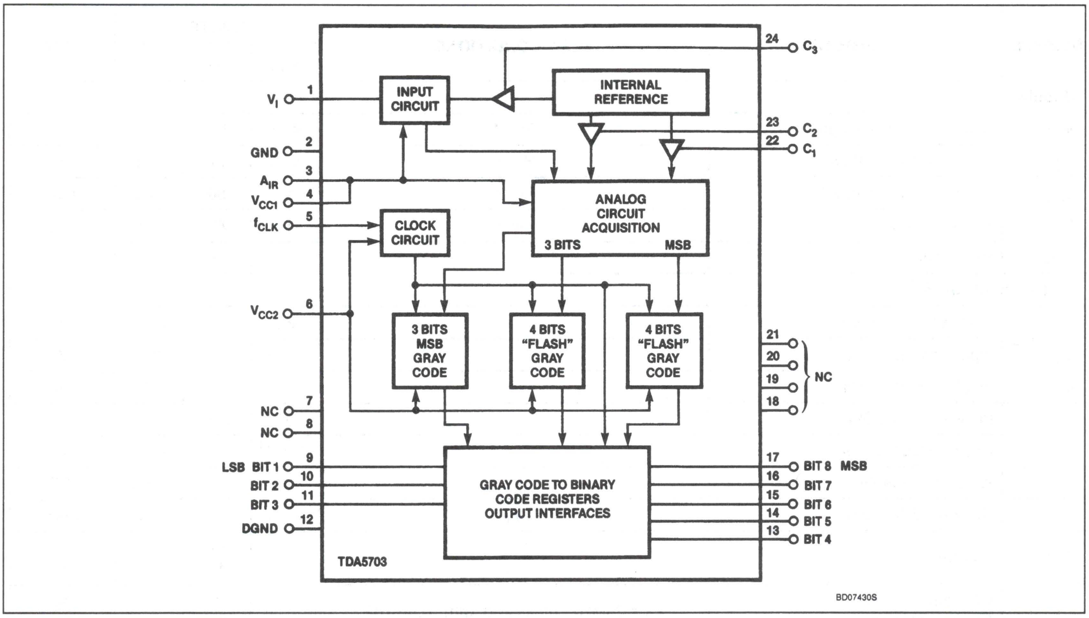
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101 BE17)	0 to +70°C	TDA5703N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltages at Pin 4 at Pin 6	8 8	V V
V_{IN}	Input voltage at Pins 1 and 5	8	V
I_{OUT} I_O	Output current at Pins 9, 10, 11, 13, 14, 15, 16 and 17	10	mA
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Junction temperature	+125	°C
T_A	Operating ambient temperature range	0 to +70	°C

Analog-to-Digital Converter TDA5703

BLOCK DIAGRAM



TDA5703
INPUT CIRCUIT
INTERNAL REFERENCE
ANALOG CIRCUIT ACQUISITION
3 BITS
MSB
CLOCK CIRCUIT
3 BITS MSB GRAY CODE
4 BITS "FLASH" GRAY CODE
4 BITS "FLASH" GRAY CODE
GRAY CODE TO BINARY CODE REGISTERS OUTPUT INTERFACES
V_I 1
GND 2
A_IR 3
V_CC1 4
f_CLK 5
V_CC2 6
NC 7
NC 8
LSB BIT 1 9
BIT 2 10
BIT 3 11
DGND 12
BIT 4 13
BIT 5 14
BIT 6 15
BIT 7 16
BIT 8 MSB 17
18
19
20
21
NC
C_1 22
C_2 23
C_3 24
BD07430S

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{CC1}	Analog supply voltage	Pin 4	4.75	5.0	5.25	V
V_{CC2}	Digital supply voltage	Pin 6	4.75	5.0	5.25	V
I_{CC1}	Analog supply current	Pin 4	55	80	105	mA
I_{CC2}	Digital supply current	Pin 6	55	80	105	mA
Res	Resolution			8		bits
Digital input levels[1]						
V_{IH}	Input voltage HIGH		2.2		V_{CC2}	V
V_{IL}	Input voltage LOW		−0.3		0.8	V
I_{IH}	Input current HIGH				10	μA
I_{IL}	Input current LOW		−7	350		μA
	Analog input levels		V_{CC1}^{-1}		V_{CC1}	V
	Absolute linearity	V_1	−1.5		+1.5	LSB
	Differential linearity	V_1	−1.5		+1	LSB
BW	Bandwidth	1dB		6.0		MHz
		3dB	6.0	10		MHz
	Differential phase	$F_0 = 25MHz$, measured with TDA5702		1		deg.
	Differential gain			2.3		%
	Offset error			40		mV
R_{IN}	Input resistance			80		kΩ
C_{IN}	Input capacitance			5		pF
Digital output levels ($I_O = 10mA$)						
V_{OH}	Output voltage HIGH		2.4			V
V_{OL}	Output voltage LOW				0.40	V
C_O	External capacitance	C_1, C_2, C_3		100		nF
Temperature						
T_A	Operating ambient temperature range		0		+70	°C

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Timing						
f_C	Maximum conversion rate		25			MHz
t_{DELAY}	Aperture delay[1]			19		ns
t_D	Digital output delay[1]			28		ns
t_{PWH}	Pulse width conversion HIGH[1]		20			ns
t_{PWL}	Pulse width conversion LOW[1]		20			ns

NOTE:

1. See Timing Diagram, Figure 1

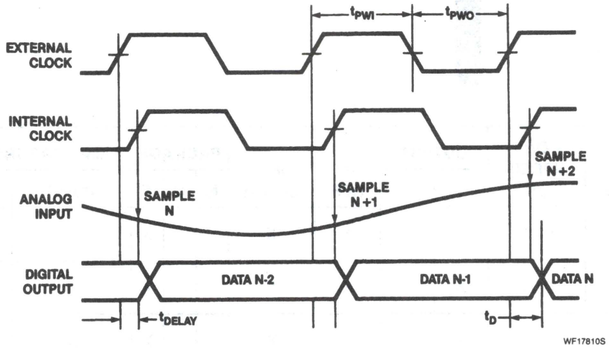

t_{PWI}
t_{PWO}
EXTERNAL CLOCK
INTERNAL CLOCK
ANALOG INPUT
SAMPLE N
SAMPLE N+1
SAMPLE N+2
DIGITAL OUTPUT
DATA N-2
DATA N-1
DATA N
t_{DELAY}
t_D
WF17810S

Figure 1. Timing Diagram

Digital-to-Analog Converter Selector Guide

DEVICE	BITS	ACC %	CONV SPEED (μs)	OUTPUT		INT REF	INT LATCH	PACKAGE			TEMPERATURE RANGE		COMMENTS
				V	I			N	D	F	Com'l	Mil	
NE5150	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits with RAM
NE5151	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits without RAM
NE5152	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits with RAM
TDA8442	6	0.78		X			X	X			X		4 × 6 Bits I^2C
TDA8444	6	0.78		X			X	X			X		8 × 6 Bits I^2C
MC1408-7	8	0.39	0.07		X			X		X	X		
MC1408-8	8	0.19	0.07		X			X	X	X	X		
MC1508-8	8	0.19	0.07		X					X		X	
DAC08	8	0.19	0.07		X					X		X	
DAC08A	8	0.10	0.07		X					X		X	
DAC08C	8	0.39	0.07		X			X		X	X		
DAC08E	8	0.19	0.07		X			X	X	X	X		
DAC08H	8	0.10	0.07		X			X		X	X		
NE5018	8	0.19	2.3	X		X	X	X	X	X	X		
SE5018	8	0.19	2.3	X		X	X			X		X	
NE5019	8	0.10	2.3	X		X	X	X	X	X	X		
SE5019	8	0.10	2.3	X		X	X			X		X	
NE5118	8	0.19	0.2		X	X	X	X	X	X	X		
SE5118	8	0.19	0.2		X	X	X			X		X	
NE5119	8	0.10	0.2		X	X	X	X	X	X	X		
SE5119	8	0.10	0.2		X	X	X			X	X		
PNA7518	8	0.19	0.013	X			X	X			X		30MHz Sampling Rate
TDA5702	8	0.39	0.04	X		X	X	X			X		25 MSPs
MC3410C	10	0.10	0.25		X			X		X	X		
NE5020	10	0.10	5.0	X		X	X	X		X	X		
NE5410	10	0.05	0.25		X					X	X		± ¼ LSB DNL
SE5410	10	0.05	0.25		X					X		X	± ¼ LSB DNL
MC3410	10	0.05	0.25		X			X		X	X		± ½ LSB DNL
MC3510	10	0.05	0.25		X					X		X	± ½ LSB DNL
AM6012	12	0.05	0.25		X					X	X		± 1 LSB DNL
DAC800V	12	0.012	5.0	X		X		X		X	X		
DAC800I	12	0.012	1.0		X	X		X		X	X		

Digital-to-Analog Converter Selector Guide

			CONV SPEED	OUTPUT				PACKAGE			TEMPERATURE RANGE		
DEVICE	BITS	ACC %	(μs)	V	I	INT REF	INT LATCH	N	D	F	Com'l	Mil	COMMENTS
TDA1540D	14	0.012	0.5		X	X	X			X	X		Serial Input ± ½ LSB DNL
TDA1540	14	0.003	0.5		X	X	X	X		X	X		Serial Input
TDA1541	16	0.0008	1.0		X	X	X	X			X		Serial Input

Symbols and Definitions for Digital-to-Analog Converters (DACs)

Absolute Accuracy Error

Absolute Accuracy Error of a DAC at an input code is the difference between the theoretical output voltage/current at a digital input code and the actual analog output voltage/current produced at the same code.

Absolute Accuracy Error includes gain error, offset error and relative accuracy error and is typically expressed in LSBs or in percent of full-scale range (FSR).

Differential Linearity Error

Differential Linearity Error of a DAC is the difference between the actual step size between any two adjacent codes and the ideal step size (which is equal to 1 LSB of the DAC). A differential linearity error of greater than 1 LSB can lead to non-monotonicity.

Full-Scale Range (FSR)

The Full-Scale Range (FSR) of a DAC is the scale factor that determines the nominal conversion relationship; e.g., 10V span for a full-scale code change in a fixed reference converter.

In a unipolar DAC of n bits, the output voltage/current is 0V/mA with all bits OFF. With all bits turned ON, the output voltage/current is FSR $\times (1-2^{-N})$.

In a bipolar DAC, the output voltage/current is $-$FSR/2 with all bits OFF. With all bits turned ON, the output voltage/current is FSR $\times (1-2^{-(N-1)})$.

Integral Non-Linearity

Same as Relative Accuracy.

Least Significant Bit

The Least Significant Bit (LSB) is the lowest-order bit and carries the smallest weight. In an n-bit DAC, the weight of the LSB is 2^{-N} relative to the FSR of the DAC. It represents the smallest discrete step that can be attained in the output of the DAC.

Monotonicity

A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases from any code to the next higher code.

Most Significant Bit (MSB)

The Most Significant Bit (MSB) is the highest order bit and carries the most weight. The weight of the MSB is ½ the FSR of the DAC.

Offset Error (Unipolar and Bipolar)

In a DAC, unipolar offset is the actual analog output voltage/current with all the bits turned OFF. Offset Error causes a shift in the transfer characteristic of the DAC. Similarly for bipolar offset, it is the actual output voltage/current with the digital input at half-scale.

Power Supply Sensitivity

The Power Supply Sensitivity of a DAC is the change in the DAC output with changes in the DC power supply voltages. It is usually expressed in LSBs/V or in %FSR/V.

Relative Accuracy

Relative Accuracy Error is the deviation of the DAC's actual output voltage/current from the ideal output voltage/current on a straight line connecting the end points of the transfer characteristic after nulling offset error and gain error. It is generally expressed in LSBs or in %FSR.

Resolution

Resolution of a DAC is the number of bits at its input. The number of discrete output steps is 2^N where N is the resolution of the converter.

Settling Time

The time required, following a prescribed change in the digital inputs, for the output of the DAC to reach and remain within a specified fraction (typically ± ½ LSB) of its final value. This parameter is usually specified for a full-scale change.

Temperature Coefficients

In general, Temperature Coefficients are expressed either in ppm/°C or in LSBs/°C or as a change in the specified parameter over the temperature range. Measurements are usually made at room temperature and at the temperature extremes of the specified temperature range; the Temperature Coefficient is defined as the change in the parameter from its room temperature value divided by the corresponding temperature change.

Signetics

AN101
Applying the DAC08

Application Note

Linear Products

Reference Amplifier Setup

The DAC08 Series are multiplying D-to-A converters in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by this equalization where $I_{REF} = I_{14}$.

$$I_{FS} = \frac{255}{256} \times I_{REF}$$

In positive reference applications shown in Figure 1, an external positive reference voltage forces current through R14 into the V_{REF} (+) terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (−) at Pin 15, shown in Figure 2. Reference current flows from ground through R14 into V_{REF}(+) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15 as shown in Figure 3. The negative common-mode range of the reference amplifier is given by the following equation:

$$V_{CM-} = V- + (I_{REF} \cdot 1k\Omega) + 2.5V$$

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into 2 resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full-scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer TC effects is shown in Figure 4.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from Pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications".

Multiplying Operation

The DAC08 Series provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

Reference Amplifier Compensation for Multiplying Applications

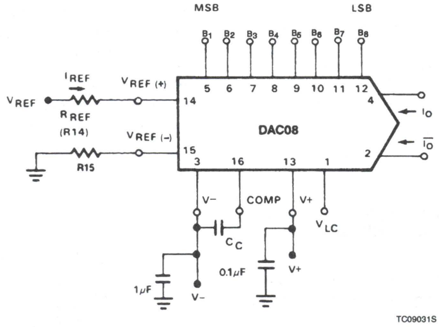
AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V−. The value of this capacitor depends on the impedance presented to Pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37 and 75pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest multiplying response, low values of R14 enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and CC = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5. This technique provides lowest full-scale transition times. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs, which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC08 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −11V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC08 is pow-



NOTES:

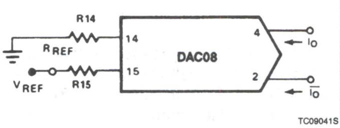
$I_{FS} \approx + \frac{V_{REF}}{R_{REF}} \times \frac{255}{256}$ $I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation typical values are:
$V_{REF} = +10.000V$, $R_{REF} = 5{,}000\Omega$, $R15 \approx R_{REF}$,
$C_C = 0.01\mu F$, $V_{LC} = 0V$(ground)

Figure 1. Basic Positive Reference Operation

ered from a +5V supply. Minimum input logic swing is given by the following equation:

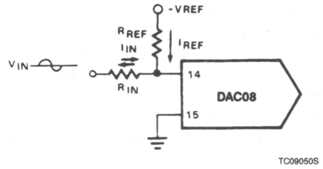
$$V- + (I_{REF} \cdot 1k\Omega) + 2.5V$$



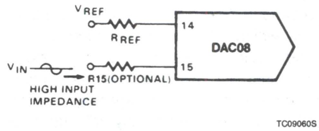
$$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

R_{REF} sets I_{FS}, R15 is for bias current cancellation.

Figure 2. Basic Negative Reference Operation



$I_{REF} \geqslant$ Peak Negative Swing of I_{IN}



$+V_{REF}$ must be above Peak Positive Swing of V_{IN}

Figure 3. Accomodating Bipolar References

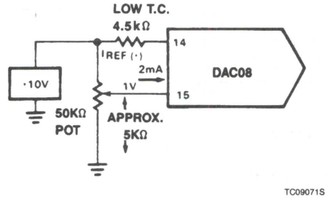


Figure 4. Recommended Full-Scale Adjustment Circuit

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control in (Pin 1, V_{LC}). Figure 6 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see Figure 7. For general setup of the logic control circuit, it should be noted that Pin 1 may source up to 200μA. External circuitry should be designed to accommodate this current.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at Pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is applied to any input bit, that current is turned off at Pin 4 and turned on at Pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}. Do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by the equation:

$$V- + (I_{REF} \cdot 1k\Omega) + 3.0V$$

Note that lower values of I_{REF} will allow a greater output compliance.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as balanced-bridge A/D circuits, as well as driving center-tapped coils and transformers.

Power Supplies

The DAC08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leqslant$ 1mA is recommended.

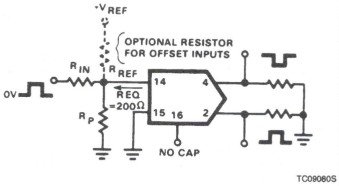


Figure 5. Pulsed Reference Operation

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8V total must be applied between Pins 2 and 4, and Pin 3 to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated by this equation:

$$P_D = (I+)(V+) + (I+)(V-) + (I_{REF})(V-)$$

A useful feature of the DAC08 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

Temperature Performance

The linearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10ppm/°C with zero-scale output current and drift essentially negligible compared to ½ LSB.

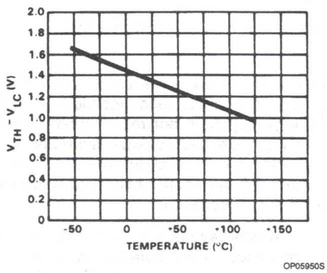


Figure 6. $V_{TH} - V_{LC}$ vs Temperature

Full-scale output drift performance will be best with +10.0V references, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift.

Applying the DAC08 AN101

Settling times of the DAC08 decrease approximately 10% at −55°C, and an increase of about 15% at +125°C is typical.

Settling Time

The DAC08 is capable of extremely fast settling times (typically 70ns at I_{REF} = 2.0mA).

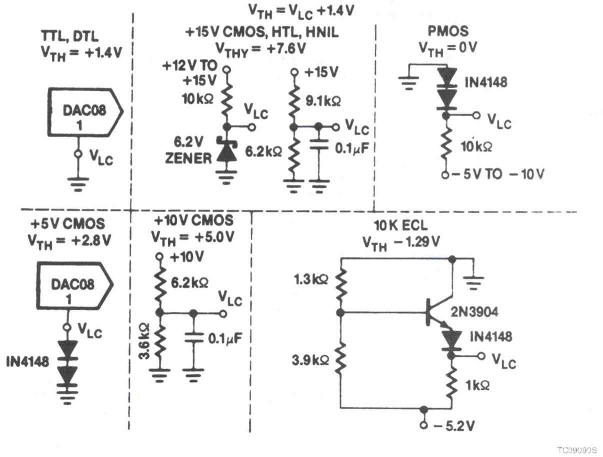
Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within ½ LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 70ns, thus determining the overall settling time of 70ns. Settling to 6-bit accuracy requires about 55 to 60ns. The output capacitance, including the package, is approximately 15pF. Therefore, the output RC time constant dominates settling time if R_L > 500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA. Therefore, a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 8 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasite capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value; thus, settling time may be observed at lower values of I_{REF}.

The DAC08 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. 0.1μF capacitors at the supply pins provide full transient performance.



NOTE:
Do not exceed negative logic input range of DAC

Figure 7. Interfacing With Various Logic Families

Applying the DAC08

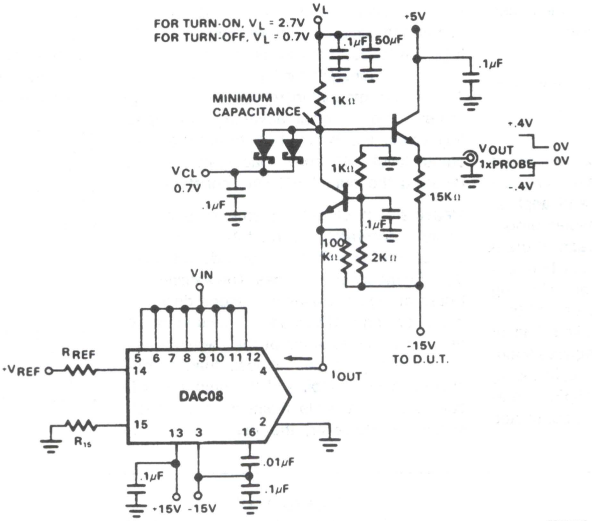
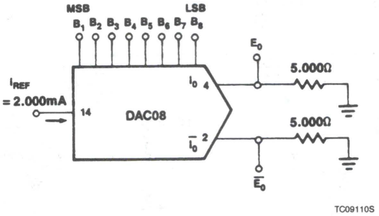

V$_L$
FOR TURN-ON, V$_L$ = 2.7V
FOR TURN-OFF, V$_L$ = 0.7V
.1μF
50μF
+5V
.1μF
MINIMUM CAPACITANCE
1KΩ
+.4V
0V
V$_{OUT}$
1xPROBE
0V
-.4V
V$_{CL}$
0.7V
.1μF
1KΩ
15KΩ
.1μF
100 KΩ
2KΩ
V$_{IN}$
R$_{REF}$
+V$_{REF}$
5 6 7 8 9 10 11 12
14
4
I$_{OUT}$
DAC08
15
13
3
16
2
R$_{15}$
.01μF
.1μF
.1μF
+15V
-15V
-15V TO D.U.T.
TC09100S

Figure 8. Settling Time Measurement

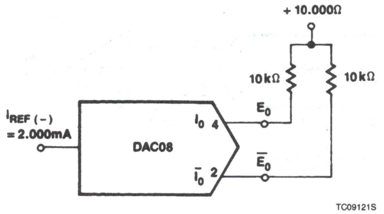
TYPICAL APPLICATIONS


MSB
LSB
B$_1$ B$_2$ B$_3$ B$_4$ B$_5$ B$_6$ B$_7$ B$_8$
E$_0$
5.000Ω
I$_{REF}$ = 2.000mA
14
DAC08
I$_0$ 4
$\overline{I_0}$ 2
5.000Ω
$\overline{E_0}$
TC09110S

	B$_1$	B$_2$	B$_3$	B$_4$	B$_5$	B$_6$	B$_7$	B$_8$	I$_O$ (mA)	$\overline{I_O}$ (mA)	E$_O$	$\overline{E_O}$
Full-scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full-scale − LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half-scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half-scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half-scale − LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero-scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero-scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

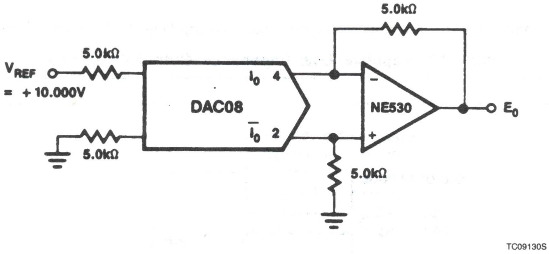
Figure 9. Basic Unipolar Negative Operation

TYPICAL APPLICATIONS (Continued)


+ 10.000Ω
10kΩ
10kΩ
IREF (−)
= 2.000mA
DAC08
I0 4
Ī0 2
E0
Ē0
TC09121S

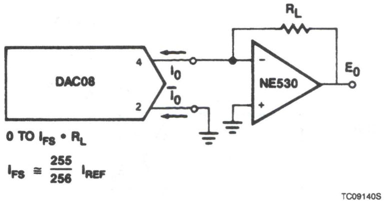
	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O	$\overline{E_O}$
Pos full-scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos full-scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero-scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg full-scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg full-scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Figure 10. Basic Bipolar Output Operation


5.0kΩ
5.0kΩ
VREF
= +10.000V
DAC08
I0 4
Ī0 2
5.0kΩ
NE530
−
+
E0
5.0kΩ
TC09130S

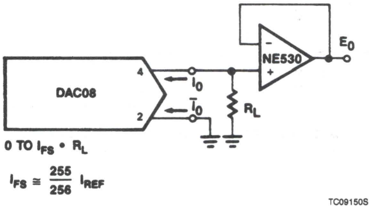
	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O
Pos full-scale	1	1	1	1	1	1	1	1	+9.920
Pos full-scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero-scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero-scale	0	1	1	1	1	1	1	1	−0.040
Neg full-scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg full-scale	0	0	0	0	0	0	0	0	−9.920

Figure 11. Symmetrical Offset Binary Operation


R_L
DAC08
4
2
I_O
Ī_O
NE530
E_O
0 TO I_FS • R_L
I_FS ≅ 255/256 I_REF
TC09140S

NOTE:
For complementary output (operation as negative logic DAC), connect inverting input of op amp to I_O (Pin 2); connect $\overline{I_O}$ (Pin 4) to ground.

Figure 12. Positive Low Impedance Output Operation


NE530
E_O
DAC08
4
2
I_O
Ī_O
R_L
0 TO I_FS • R_L
I_FS ≅ 255/256 I_REF
TC09150S

NOTE:
For complementary output (operation as a negative logic DAC), connect non-inverting input of op amp to I_O (Pin 2); connect $\overline{I_O}$ (Pin 4) to ground.

Figure 13. Negative Low Impedance Output Operation

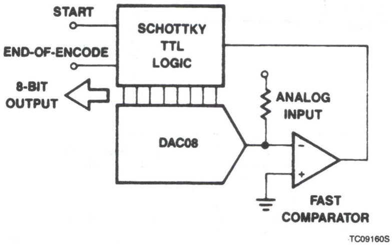
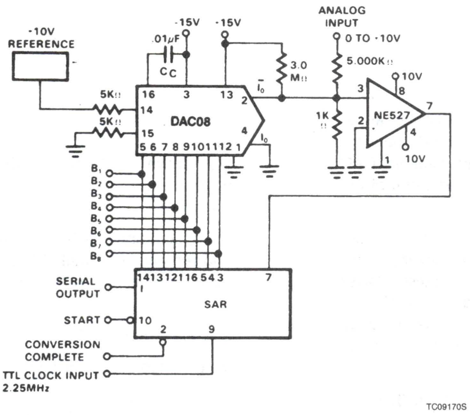
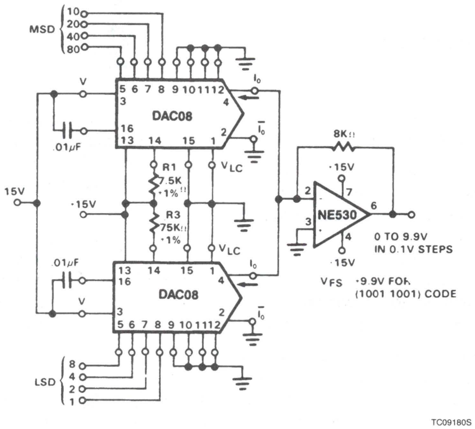

START
END-OF-ENCODE
8-BIT OUTPUT
SCHOTTKY TTL LOGIC
ANALOG INPUT
DAC08
FAST COMPARATOR
TC09160S

Figure 14. Low Cost 8-Bit 1μs A-to-D Converter


-10V
REFERENCE
.01μF
-15V
-15V
CC
ANALOG
INPUT
0 TO -10V
5.000KΩ
3.0
MΩ
10V
5KΩ
5KΩ
DAC08
NE527
1K
10V
B1
B2
B3
B4
B5
B6
B7
B8
SERIAL
OUTPUT
START
SAR
CONVERSION
COMPLETE
TTL CLOCK INPUT
2.25MHz
TC09170S

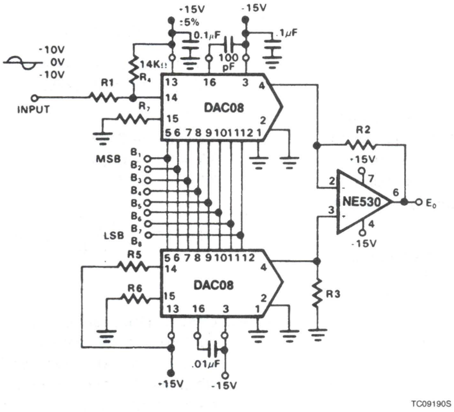
NOTE:
Connect "start" to "conversion complete" for continuous conversions.

Figure 15. 3 IC Low Cost A-to-D Converter


MSD
10
20
40
80
V
DAC08
.01μF
R1
7.5K
-1%Ω
VLC
15V
-15V
R3
75KΩ
-1%
8KΩ
-15V
NE530
0 TO 9.9V
IN 0.1V STEPS
-15V
VFS -9.9V FOR
(1001 1001) CODE
.01μF
V
DAC08
LSD
8
4
2
1
TC09180S

NOTE:
Output is directly proportional to positive power supply.

Figure 16. Low Cost 2-Digit BCD DAC

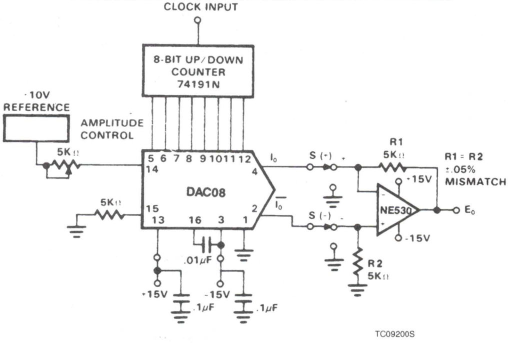

-15V
-15V
±5%
0.1μF
.1μF
100
pF
-10V
0V
-10V
14KΩ
R4
R1
INPUT
R7
DAC08
R2
-15V
MSB
B1
B2
B3
B4
B5
B6
B7
B8
LSB
NE530
E0
-15V
R5
R6
DAC08
R3
.01μF
-15V
-15V
TC09190S

Bipolar input offset binary output } Performs 2 quadrant multiplications — AC input controls output polarity.

NOTES:
1. R1 = R2 = R3
2. R4 = R5
3. E_O DC to 20kHz = ±5V
4. E_O DC to 10kHz = ±10V

Figure 17. DC-Coupled Digital Attenuator/ Programmable Gain Amplifier

OUTPUT TYPE (E_O)	SWITCH S(+)	CONDITIONS S(−)
Unipolar positive	+	GND
Unipolar negative	GND	−
Bipolar	+	−


CLOCK INPUT
8-BIT UP/DOWN
COUNTER
74191N
-10V
REFERENCE
AMPLITUDE
CONTROL
5KΩ
DAC08
5KΩ
S(-)
S(-)
R1
5KΩ
R1 = R2
±.05%
MISMATCH
-15V
NE530
E0
-15V
R2
5KΩ
.01μF
-15V
-15V
.1μF
.1μF
TC09200S

NOTES:
1. Bipolar output is symmetrical around zero, adjustable peak-to-peak amplitude.
2. For triangle wave, count up to full, reverse and count down.
3. For positive-going sawtooth, count up to full, clear, repeat.
4. For negative-going sawtooth, count down, clear, repeat.
5. For other waveforms, use a ROM programmed with the desired function.

Figure 18. High-Speed Waveform Generator

Signetics

AN105
Digital Attenuator

Application Note

Linear Products

Figure 1 shows a DC-coupled Digital Attenuator or Programmable Gain Amplifier.

Pin 14 of the DAC is a Virtual Ground. Current must always flow into Pin 14, so the current through R4 must be greater than that through R1 when the input signal is at its most negative usable value. If the input signal value goes low enough to cause the current through R1 to be greater than that through R4, output clipping will occur.

To extend the operating frequency range, the compensation cap, C_C, needs to be minimized, which implies that the resistance at Pin 14 (R1 and R4) must be minimized. If the voltage to which R4 and R5 are returned has any noise on it at all, R4 and R5 should be formed of two series resistors with the junction of them bypassed with 0.1μF to ground. Pin 15 could be grounded with a small sacrifice in accuracy and temperature drift. R6 and R7 compensate for reference amplifier input offset.

R1 and R4 should be chosen such that, when the input is at peak usable signal, the total current into Pin 14 does not exceed 4mA. When the input is most negative, R1 current must be less than R4 current (remember, Pin 14 is always at 0V). Also, when the input is at its absolute positive peak value, current into Pin 14 should not exceed 5mA. Minimum compensation capacitor, (C_C), in pF is 15 times the parallel combination of R1 and R4 in kΩ.

With a single DAC, there is a DC offset at the circuit output that varies with the digital word input. To eliminate this, we use a second DAC to subtract this offset at the sum node of the op amp.

Example 1: Input signal is to be $20V_{P\text{-}P}$, centered at 0V. Maximum input frequency is to be 15kHz. Power supplies available are ± 15V, both regulated. Determine values of all resistors for maximum gain of unity.

Solution 1: At minimum input (−10V), reference current, I_{REF} is

$$I_{REF} = \frac{15V}{R4} + \frac{(-10V)}{R1}$$

If minimum $I_{REF} = 0$, then

$$\frac{15V}{R4} = \frac{10V}{R1}$$

and $R4 = (1.5)(R1)$

Therefore, 60% of I_{REF} comes through R4. If we let I_{REF} go to about 3.9mA (4mA is max. recommended), R4 current is found to be $I_{R4} = (0.6)\ (3.9mA) = 2.34mA$ and $R4 = 6.4k$.

The balance of the reference current I_{R1} is found to be

$I_{R1} = 3.9mA - I_{R4}$
or
$I_{R1} = 3.9mA - 234mA = 1.56mA$
and
$R1 = 6.4k$

Using commonly available values, and remembering that R4 current must exceed R1 current, we set

$R1 = 6.8k$
and $R4 = 6.2k$.

Maximum reference current is now

$$I_{REF}(max) = \frac{15V}{6.2k} + \frac{10V}{6.8k} = 3.9mA.$$

The parallel combination of R1 and R4 is found to be 3.24k, so minimum compensation capacitor value is

$C_C(min) = (3.24)(15)pF = 48.6pF.$

If we use 50pF, from the graph we find f_{MAX} to be 370kHz. For unity gain,

$R2 = R1 = 6.8k$
$R3 = R2 = 6.8k$
$R5 = R1 = 6.8k$

$$R6 = R7 = \frac{(R1)(R4)}{R1 + R4} = 3.24k$$

(use 3.3k)

Example 2: Usable input signal is $12V_{P\text{-}P}$, centered at 0V, with occasional excursion to twice this amplitude, which we do not care about. Maximum input frequency is to be

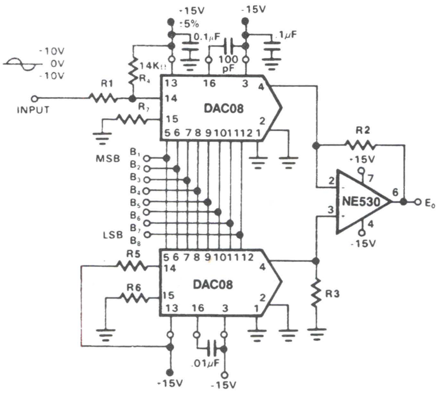


Figure 1

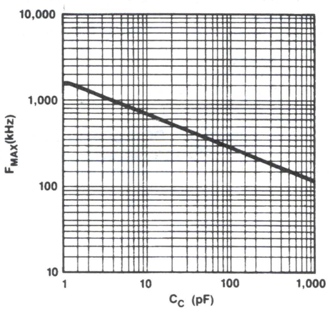


Figure 2

500kHz. Available power supplies are +5V logic supply, +15V, −15V, all regulated. Determine values of all resistors and C_C for maximum gain of 2.

Solution 2: To extend the frequency response, we want minimum compensation capacitor value; therefore, we need minimum R1 and R4 values, so we want to return R4 to as low a regulated supply as is possible; we will use the 5V logic supply.

At minimum usable input,

$$I_{REF} = \frac{5V}{R4} - \frac{6V}{R1}$$

or, for

$$I_{REF} = 0,\ \frac{5V}{R4} = \frac{6V}{R1}$$

therefore, 55% of I_{REF} comes through R4, and

R4 = (5/6)R1.

Because peak input goes to +12V, this condition should not cause I_{REF} to exceed 5mA, and

$$\frac{12V}{R1} + \frac{5V}{R4} = 5mA$$

Recall that R4 = (5/6)R1

$$\frac{12V}{R1} + \frac{5}{(5/6)(R1)} = 5mA$$

$$\frac{12V}{R1} + \frac{6V}{R1} = 5mA$$

R1 = 3.6k
and R4 = (5/6)R1 = 3.0k.

Because the reference source will be the 5V logic supply, which will be noisy, we will split R4 into two resistors and bypass their junction with 0.1µF to ground. Furthermore, to be sure that R4 current exceeds R1 current, we will increase R1 to 4.3k. The absolute maximum reference current is now

$$I_{REF}(max) = \frac{12V}{4.3k} + \frac{5V}{3k} = 4.46mA.$$

The parallel combination of R1 and R4 is 1.77k, so minimum compensation capacitor is

$C_C(min) = (15)(1.77) = 26.5pF.$

If we use 27pF, the graph tells us the maximum frequency is about 470kHz, which is 6% lower than desired. If we wanted to further extend this frequency range, we find that we can reduce R4 to two resistors of 1.1k and 1.2k, bringing the absolute maximum reference current to

$$I_{REF}(max) = \frac{12V}{4.3k} + \frac{5V}{2.3k} = 4.96mA$$

and the maximum usable reference current becomes

$$I_{REF} = \frac{6V}{4.3k} + \frac{5V}{2.3k} = 3.57mA,$$

below the 5mA and 4mA respective desired maximum values. Now the resistance at Pin 14 is the parallel combination of R1 and R4, or 1.5k, and the minimum compensation capacitor becomes

$C_C(min) = (15)(1.5)pF = 22pF.$

The graph tells us we can just go to 500kHz.

Signetics

Linear Products

AM6012
12-Bit Multiplying D/A Converter

Product Specification

DESCRIPTION

The AM6012 12-bit multiplying Digital-to-Analog converter provides high-speed and 0.025% differential nonlinearity over its full commercial temperature range.

The D/A converter uses a 3-bit segment generator for the MSBs in conjunction with a 9-bit R-2R diffused resistor ladder to provide 12-bit resolution without costly trimming processes. This technique guarantees a very uniform step size (up to ± ½ LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs.

The dual complementary outputs of the AM6012 increase its versatility, and effectively double the peak-to-peak output swing. Digital inputs, in addition, can be configured to accept all popular logic families.

While the device requires a reference input of 1mA for a 4mA full-scale current, operation is nearly independent of power supply voltage shifts. The power supply rejection ratio is ±0.001% FS/% ΔV. The devices will work from +5, −12V to ±18V rails, with as low as 230mW power consumption typical.

FEATURES

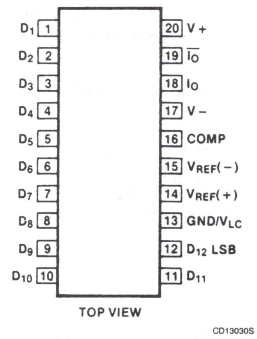
- **12-bit resolution**
- **Accurate to within ±0.05%**
- **Monotonic over temperature**
- **Fast settling time, 250ns typical**
- **Trimless design for low cost**
- **Differential current outputs**
- **High-speed multiplying capability**
- **Full-scale current, 4mA (with 1mA reference)**
- **High output compliance voltage, −5 to +10V**
- **Low power consumption, 230mW**

APPLICATIONS

- **CRT displays, computer graphics**
- **Robotics and machine tools**
- **Automatic test equipment**
- **Programmable power supplies**
- **CAD/CAM systems**
- **Data acquisition and control systems**
- **Analog-to-digital converter systems**

PIN CONFIGURATION

F Package

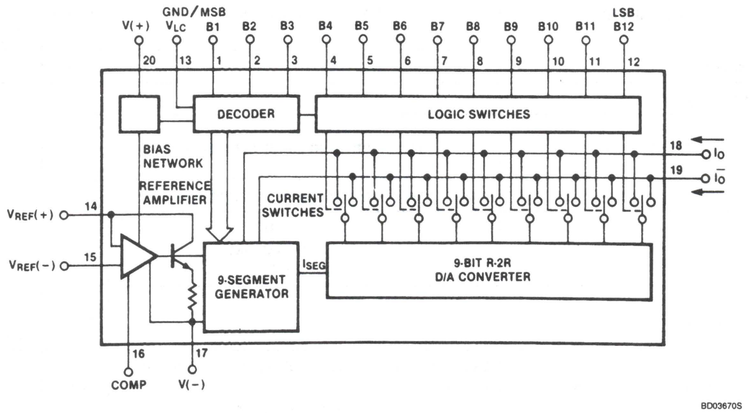


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Cerdip	0 to +70°C	AM6012F

12-Bit Multiplying D/A Converter AM6012

BLOCK DIAGRAM


GND/MSB
V(+)
VLC
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB
B12
20
13
1
2
3
4
5
6
7
8
9
10
11
12
DECODER
LOGIC SWITCHES
BIAS NETWORK
REFERENCE AMPLIFIER
CURRENT SWITCHES
18
Io
19
Io
VREF(+)
14
VREF(−)
15
ISEG
9-SEGMENT GENERATOR
9-BIT R-2R D/A CONVERTER
16
17
COMP
V(−)
BD03670S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature AM6012F	0 to +70	°C
T_{STG}	Storage temperature range	−65°C to +150	°C
T_{SOLD}	Lead soldering temperature 10sec max	300	°C
V_S	Power supply voltage	±18	V
	Logic inputs	−5V to +18	V
	Voltage across current outputs	−8V to +12	V
V_{REF}	Reference inputs V_{14}, V_{15}	V− to V+	
V_{REF}	Reference input differential voltage (V_{14} to V_{15})	±18	V
I_{REF}	Reference input current (I_{14})	1.25	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] F package	1560	mW

NOTE:

1. Derate above 25°C, at the following rate:
   F package at 12.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V+ = +15V$, $V- = -15V$, $I_{REF} = 1.0mA$, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		12			Bits
	Monotonicity		12			Bits
DNL	Differential nonlinearity	Deviation from ideal step size			±0.025	%FS
			12			Bits
NL	Nonlinearity	Deviation from ideal straight line			±.05	%FS
I_{FS}	Full-scale current	$V_{REF} = 10.000V$ $R_{14} - R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.935	3.999	4.063	mA
TCI_{FS}	Full-scale tempco			±10	±40	ppm/°C
				±0.001	±0.004	%FS/°C
V_{OC}	Output voltage compliance	DNL Specification guaranteed over compliance range $R_{OUT} > 10M\Omega$ typ.	−5		+10	V
I_{FSS}	Symmetry	$I_{FS} - \overline{I_{FS}}$		±0.4	±2.0	µA
I_{ZS}	Zero-scale current				0.10	µA
V_{IL}	Logic input levels Logic "0"				0.8	V
V_{IH}	Logic "1"		2.0			
I_{IN}	Logic input current	$V_{IN} = -5$ to $+18V$			40	µA
V_{IS}	Logic input swing	$V- = -15V$	−5		+18	V
I_{REF}	Reference current range		0.2	1.0	1.1	mA
I_{15}	Reference bias current		0	−0.5	−2.0	µA
dI/dt	Reference input slew rate	$R_{14(eq)} = 800\Omega$ $C_C = 0pF$	4.0	8.0		mA/µs
$PSSI_{FS+}$	Power supply sensitivity	$V+ = +13.5V$ to $+16.5V$, $V- = -15V$		±0.0005	±0.001	%FS/%
$PSSI_{FS-}$		$V- = -13.5V$ to $-16.5V$, $V+ = +15V$		±0.00025	±0.001	
V+	Power supply range	$V_{OUT} = 0V$	4.5		18	V
V−			−18		−10.8	
I+	Power supply current	$V+ = +5V$, $V- = -15V$		5.7	8.5	mA
I−				−13.7	−18.0	
I+		$V+ = +15V$, $V- = -15V$		5.7	8.5	
I−				−13.7	−18.0	
P_D	Power dissipation	$V+ = +5V$, $V- = -15V$		234	312	mW
		$V+ = +15V$, $V- = -15V$		291	397	

AC ELECTRICAL CHARACTERISTICS $V+ = +15V$, $V- = -15V$, $I_{REF} = 1.0mA$, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_S	Settling time	To ± ½ LSB, all bits ON or OFF, $T_A = 25°C$		250	500	ns
t_{PLH} t_{PHL}	Propagation delay — all bits	50% to 50%		25	50	ns
C_{OUT}	Output capacitance			20		pF

12-Bit Multiplying D/A Converter AM6012

CIRCUIT DESCRIPTION

The AM6012 is a 12-bit DAC which uses diffused resistors and requires no trimming to guarantee monotonicity over the temperature range. A segmented DAC design guarantees a more uniform step size over the temperature range than is normally available with trimmed 12-bit converters. The converter features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In many converter applications, uniform step size is more important than conformance to an ideal straight line. Many 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ±½ LSB (±0.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. The AM6012 uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current-switched R-2R DAC since it is slower, has a voltage output, and, if implemented at the 12-bit level, would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

With the segmented DAC approach, the 4096 required output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources. The resistors which determine monotonicity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

With the segmented DAC approach, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high-speed fully-differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long-term characteristics are not degraded.

DIFFERENTIAL VS INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The graphs in Figure 1 define the manner in which these parameters are specified. The left graph shows a portion of the transfer curve of a DAC with ½ LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT screen where the AM6012 is used as a display driver. On the right is a portion of the transfer curve of a DAC specified for 2 LSB INL with ½ LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e., the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, two LSB gaps can cause large errors at those input levels (assuming ½ LSB quantizing levels). It can be seen from the two figures that the DNL-specified D/A converter will yield much finer grained data than the INL-specified part, thus improving the ability of the A/D to resolve changes in the analog input.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at Pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at Pin 18 and turned on at Pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required, it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

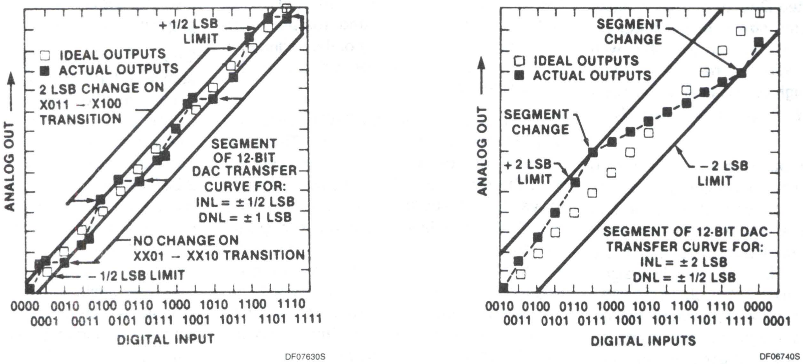
Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

DIFFERENTIAL LINEARITY COMPARISON

D/A Converter With ±½ LSB INL, ±1 LSB DNL

D/A Converter With ±2 LSB INL, ±½ LSB DNL



Video Deflection by DACs

Video Deflection by DACs

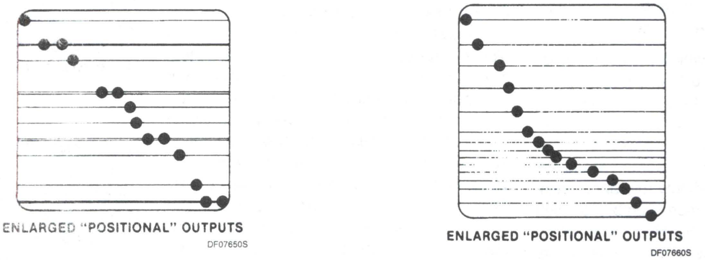


Figure 1

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V– supplies of –10V or less, $I_{REF} \leqslant 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc., remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to ½ LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within ½ LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATIONS INFORMATION

Reference Amplifier Setup

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at Pin 15. Reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors (Figure 2a).

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM-} = V− plus (I_{REF} × 3kΩ) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to Pin 14. For R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 5, 12 and 25pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin (see Figure 2b).

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from I_{REF} = 0 to I_{REF} = 1mA in 250ns.

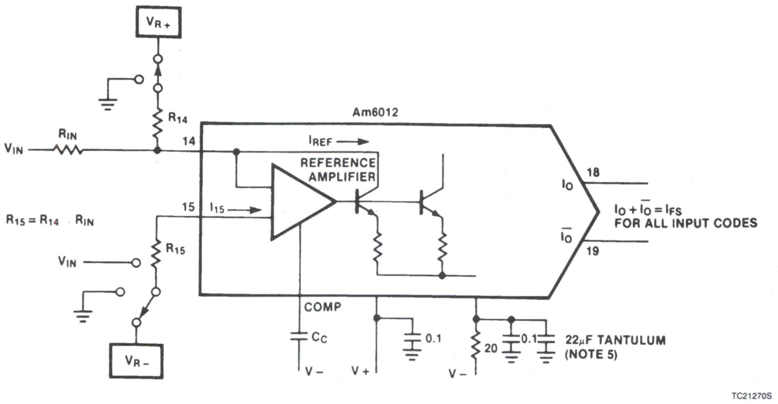
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at Pin 14 is 800Ω and C_C = 0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −5 and +10V. This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by:

V− plus (I_{REF} × 3kΩ) plus 1.8V.

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 13, V_{LC}). For TTL interface, simply ground Pin 13. When interfacing ECL, an $I_{REF} \leqslant 1$mA is recommended. For general setup of the logic control circuit, it should be noted that Pin 13 will sink 1.1mA typical. External circuitry should be designed to accommodate this current (Figure 3).


V_{R+}
R_{14}
R_{IN}
V_{IN}
14
Am6012
I_{REF}
REFERENCE AMPLIFIER
18
I_O
$I_O + \overline{I_O} = I_{FS}$ FOR ALL INPUT CODES
$R_{15} = R_{14} \cdot R_{IN}$
15
I_{15}
$\overline{I_O}$
19
V_{IN}
R_{15}
COMP
C_C
0.1
20
0.1
22μF TANTULUM (NOTE 5)
V−
V+
V−
V_{R-}
TC21270S

REFERENCE CONFIGURATION	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive reference	V_{R+}	0V	N/C	0.01μF	V_{R+}/R_{14}
Negative reference	0V	V_{R-}	N/C	0.01μF	$-V_{R-}/R_{14}$
Lo impedance bipolar reference	V_{R+}	0V	V_{IN}[1]		$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$[2]
Hi impedance bipolar Reference	V_{R+}	V_{IN}	N/C[1]		$(V_{R+} - V_{IN})/R_{14}$[3]
Pulsed reference[4]	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

NOTES:

1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least 5pF × $R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at Pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V− with 20Ω and bypass with 22μF tantulum capacitor.
6. Reference current and reference resistor — there is a 1-to-4 scale factor between the reference current (I_{REF}) and the full-scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10V}{4mA} = 10k\Omega \qquad R_{14} = R_{15}$$

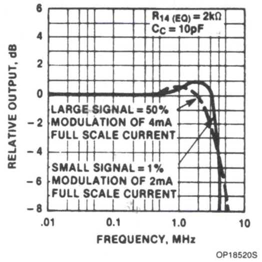
a. Reference Amplifier Biasing

Minimum Size Compensation Capacitor ($I_{FS} = 4mA$, $I_{REF}=1.0mA$)

$R_{14(EQ)}$ (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

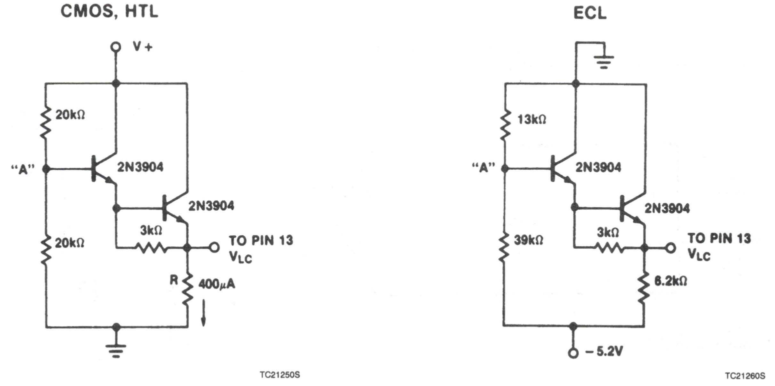
NOTE:
A 0.01μF capacitor is recommended for fixed reference operation.

Reference Amplifier Frequency Response



b.

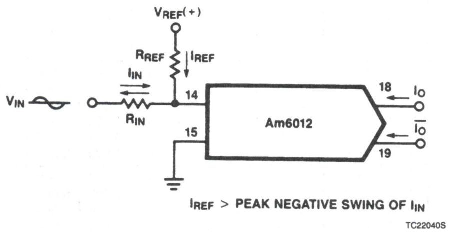
Figure 2


CMOS, HTL
V+
20kΩ
"A"
2N3904
2N3904
3kΩ
20kΩ
TO PIN 13
VLC
R
400μA
TC21250S
ECL
13kΩ
"A"
2N3904
2N3904
39kΩ
3kΩ
TO PIN 13
VLC
6.2kΩ
−5.2V
TC21260S

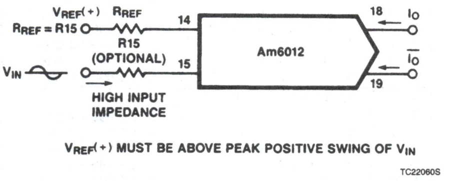
NOTE:
1. Set the voltage 'A' to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically −5V to +13.5V when operating the DAC on ±15V supplies.

Figure 3. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs

ACCOMMODATING BIPOLAR REFERENCE

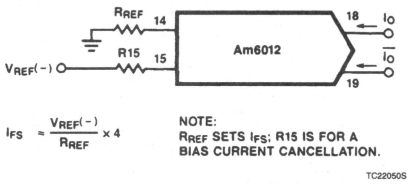

VREF(+)
RREF
IREF
IIN
VIN
RIN
14
15
Am6012
18
IO
IO
19
IREF > PEAK NEGATIVE SWING OF IIN
TC22040S

NOTE:
I_{REF} > Peak negative swing of I_{IN}.


VREF(+) RREF
RREF = R15
R15
(OPTIONAL)
VIN
HIGH INPUT
IMPEDANCE
14
15
Am6012
18
IO
IO
19
VREF(+) MUST BE ABOVE PEAK POSITIVE SWING OF VIN
TC22060S

NOTE:
$V_{REF}(+)$ Must be above peak positive swing of V_{IN}.

BASIC NEGATIVE REFERENCE OPERATION

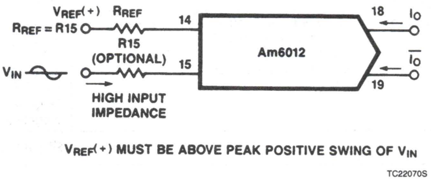

RREF
14
R15
15
VREF(−)
Am6012
18
IO
IO
19
IFS ≈ VREF(−)/RREF × 4
NOTE:
RREF SETS IFS; R15 IS FOR A
BIAS CURRENT CANCELLATION.
TC22050S

NOTE:

$$I_{FS} \approx \frac{V_{REF}(-)}{R_{REF}} \times 4$$

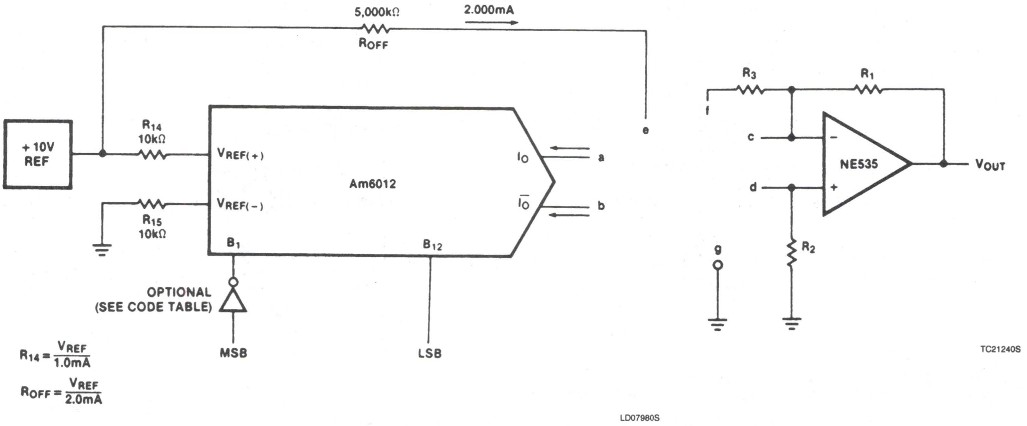
R_{REF} sets I_{FS}; R15 is for a bias current cancellation.

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT


VREF(+) RREF
RREF = R15
R15
(OPTIONAL)
VIN
HIGH INPUT
IMPEDANCE
14
15
Am6012
18
IO
IO
19
VREF(+) MUST BE ABOVE PEAK POSITIVE SWING OF VIN
TC22070S

12-Bit Multiplying D/A Converter AM6012

APPLICATION CIRCUITS



CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0 (mA)	$\bar{I}_0$ (mA)	V_{OUT}
Unipolar	Straight binary; one polarity with true input code, true zero output.	a − c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b − g	Positive full-scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
		R1 = R2 = 2.5k	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a − g	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
		b − c	Positive full-scale −LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
		R1 = R2 = 2.5k	Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000
Symmetrical Offset	Straight offset binary; offset half-scale, symmetrical about zero, no true zero output.	a − c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b − d	Positive full-scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
		f − g	(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
		R1 = R3 = 2.5k	(−) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
		R2 = 1.25k	Negative full-scale −LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976
	1's complement; offset half-scale, symmetrical about zero, no true zero output, MSB complemented (need inverter at B1).	a − c	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b − d	Positive full-scale −LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
		f − g	(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
		R1 = R3 = 2.5k	(−) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
		R2 = 1.25k	Negative full-scale −LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976
Offset with True Zero	Offset binary; offset half-scale, true zero output.	e − a − c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
		b − g	Positive full-scale −LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
		R1 = R2 = 5k	+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			−LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0049
			Negative full-scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9951
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−10.000
	2's complement; offset half-scale, true zero output, MSB complemented (need inverter at B1).	e − a − c	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1			
		b − g	Positive full-scale −LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
		R1 = R2 = 5k	+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.049
			Negative full-scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9951
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−10.000

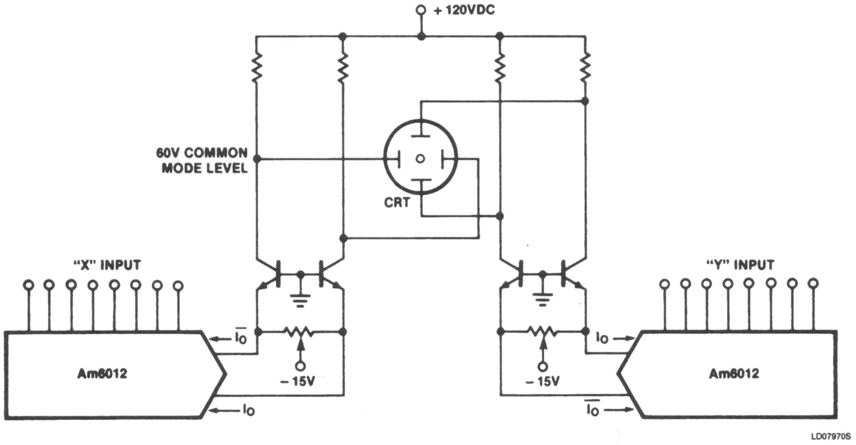
Figure 4. AM6012 Logic Inputs

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

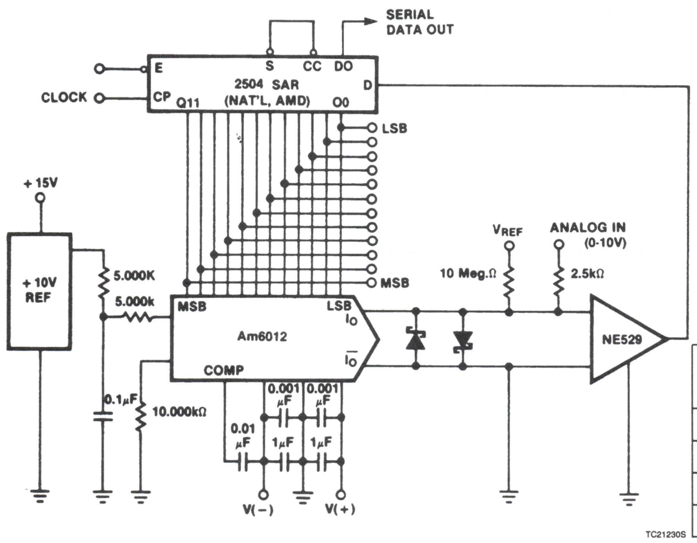
12-Bit Multiplying D/A Converter AM6012

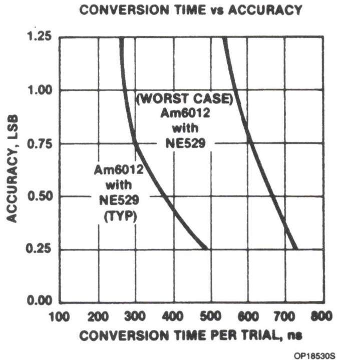
APPLICATION CIRCUITS


+120VDC
60V COMMON MODE LEVEL
CRT
"X" INPUT
"Y" INPUT
Am6012
Am6012
$\overline{I_O}$
I_O
–15V
–15V
I_O
$\overline{I_O}$
LD07970S

NOTES:
1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

Figure 5. CRT Display Driver

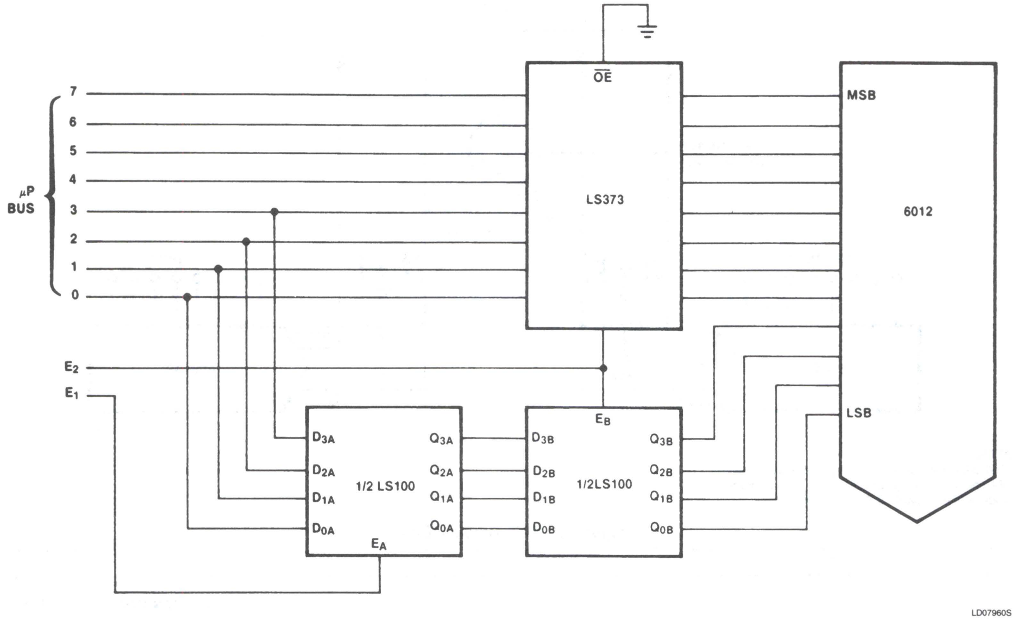

SERIAL DATA OUT
E
S
CC
DO
D
2504 SAR (NAT'L, AMD)
CLOCK
CP
Q11
Q0
LSB
MSB
+15V
+10V REF
5.000K
5.000k
MSB
LSB
Am6012
I_O
$\overline{I_O}$
COMP
0.1μF
10.000kΩ
0.001 μF
0.001 μF
0.01 μF
1μF
1μF
V(–)
V(+)
V_{REF}
ANALOG IN (0-10V)
10 Meg.Ω
2.5kΩ
NE529
TC21230S



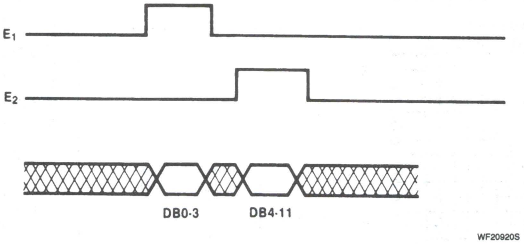
CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
NE529	100	150
TOTAL	383ns	705ns
× 13	5.0μs	9.1μs

Figure 6. 12-Bit High-Speed A/D Converter

APPLICATION CIRCUITS


µP
BUS
7
6
5
4
3
2
1
0
E2
E1
OE
LS373
MSB
6012
LSB
EB
D3A
D2A
D1A
D0A
1/2 LS100
Q3A
Q2A
Q1A
Q0A
EA
D3B
D2B
D1B
D0B
1/2LS100
Q3B
Q2B
Q1B
Q0B
LD07960S

a. Interface With 8-Bit Microprocessor Bus


E1
E2
DB0-3
DB4-11
WF20920S

b. Timing Sequence

NOTE:
Data remains on inputs of DAC until updated by E2 pulse. Timing will depend on processor used.

Figure 7

DAC08 Series
8-Bit High-Speed Multiplying D/A Converter

Product Specification

Linear Products

DESCRIPTION

The DAC08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20-to-1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC08 attractive for portable and military aerospace applications.

FEATURES

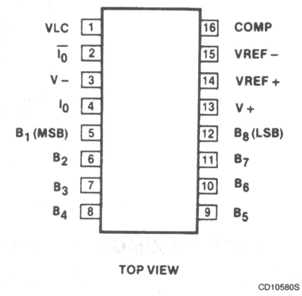
- **Fast settling output current — 70ns**
- **Full-scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance −10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift — ±10ppm/°C**
- **Wide power supply range — ±4.5V to ±18V**
- **Low power consumption — 37mW at ±5V**

ORDERING INFORMATION

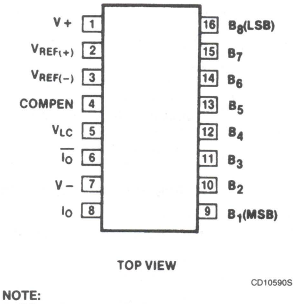
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Hermetic Cerdip	−55°C to +125°C	DAC08F
16-Pin Hermetic Cerdip	−55°C to +125°C	DAC08AF
16-Pin Plastic DIP	0 to +70°C	DAC08CN
16-Pin Hermetic Cerdip	0 to +70°C	DAC08CF
16-Pin Plastic DIP	0 to +70°C	DAC08EN
16-Pin Hermetic Cerdip	0 to +70°C	DAC08EF
16-Pin Plastic SO	0 to +70°C	DAC08ED
16-Pin Hermetic Cerdip	0 to +70°C	DAC08HF
16-Pin Plastic DIP	0 to +70°C	DAC08HN

PIN CONFIGURATIONS

F, N Packages



D Package[1]



NOTE:
1. SO and non-standard pinouts.

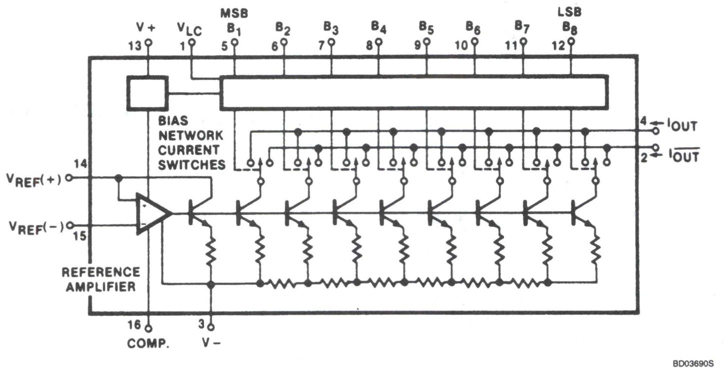
APPLICATIONS

- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High-speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**
- **Programmable gain and attentuation**
- **Analog-Digital multiplication**

8-Bit High-Speed Multiplying D/A Converter

DAC08 Series

BLOCK DIAGRAM


V+
13
V_LC
1
MSB
B1
5
B2
6
B3
7
B4
8
B5
9
B6
10
B7
11
LSB
B8
12
BIAS
NETWORK
CURRENT
SWITCHES
4
I_OUT
2
I_OUT
14
V_REF(+)
V_REF(−)
15
REFERENCE
AMPLIFIER
16
COMP.
3
V−
BD03690S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+ to V−	Power supply voltage	36	V
$V_5 - V_{12}$	Digital input voltage	V− to V− plus 36V	
V_{LC}	Logic threshold control	V− to V+	
V_0	Applied output voltage	V− to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1090	mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating temperature range		
	DAC08, DAC08A	−55 to +125	°C
	DAC08C, E, H	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Derate above 25°C, at the following rates:
F package at 9.5mW/°C.
N package at 11.6mW/°C.
D package at 8.7mW/°C.

DC ELECTRICAL CHARACTERISTICS

Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned.

$V_{CC} = \pm 15V$, $I_{REF} = 2.0mA$, Output characteristics refer to both I_{OUT} and $I_{\overline{OUT}}$ unless otherwise noted. DAC08C, E, H: $T_A = 0°C$ to 70°C. DAC08/08A: $T_A = -55°C$ to 125°C.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution Monotonicity		8 8	8 8	8 8	8 8	8 8	8 8	Bits Bits
	Relative accuracy Differential non-linearity	Over temperature range			±0.39 ±0.39			±0.19 ±0.19	%FS %FS
TCI_{FS}	Full-scale tempco			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change < ½ LSB	−10		+18	−10		+18	V
I_{FS4}	Full-scale current	$V_{REF} = 10.000V$, R_{14}, $R_{15} = 5.000k\Omega$	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full-scale symmetry	$I_{FS4} - I_{FS2}$		±2.0	±16		±1.0	±8.0	μA
I_{ZS}	Zero-scale current			0.2	4.0		0.2	2.0	μA
I_{FSR}	Full-scale output current range	R_{14}, $R_{15} = 5.000k\Omega$ $V_{REF} = +15.0V$, $V- = -10V$ $V_{REF} = +25.0V$, $V- = -12V$	2.1 4.2			2.1 4.2			mA
V_{IL} V_{IH}	Logic input levels Low High	$V_{LC} = 0V$	2.0		0.8	2.0		0.8	V
I_{IL} I_{IH}	Logic input current Low High	$V_{LC} = 0V$ $V_{IN} = -10V$ to $+0.8V$ $V_{IN} = 2.0V$ to 18V		−2.0 0.002	−10 10		−2.0 0.002	−10 10	μA
V_{IS}	Logic input swing	$V- = -15V$	−10		+18	−10		+18	V
V_{THR}	Logic threshold range	$V_S = \pm 15V$	−10		+13.5	−10		+13.5	V
I_{15}	Reference bias current			−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference input slew rate		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$ PSI_{FS-}	Power supply sensitivity Positive Negative	$I_{REF} = 1mA$ $V+ = 4.5$ to $5.5V$, $V- = -15V$; $V+ = 13.5$ to $16.5V$, $V- = -15V$ $V- = -4.5$ to $-5.5V$, $V+ = +15V$; $V- = -13.5$ to -16.5, $V+ = +15V$		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01	%FS/%VS
I+ I−	Power supply current Positive Negative	$V_S = \pm 5V$, $I_{REF} = 1.0mA$		3.1 −4.3	3.8 −5.8		3.1 −4.3	3.8 −5.8	mA
I+ I−	Positive Negative	$V_S = +5V, -15V$, $I_{REF} = 2.0mA$		3.1 −7.1	3.8 −7.8		3.1 −7.1	3.8 −7.8	
I+ I−	Positive Negative	$V_S = \pm 15V$, $I_{REF} = 2.0mA$		3.2 −7.2	3.8 −7.8		3.2 −7.2	3.8 −7.8	
P_D	Power dissipation	±5V, $I_{REF} = 1.0mA$ +5V, −15V, $I_{REF} = 2.0mA$ ±15V, $I_{REF} = 2.0mA$		37 122 156	48 136 174		37 122 156	48 136 174	mW

DC ELECTRICAL CHARACTERISTICS (Continued)

Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned.

$V_{CC} = \pm 15V$, $I_{REF} = 2.0mA$, Output characteristics refer to both I_{OUT} and $I_{\overline{OUT}}$, unless otherwise noted. DAC08C, E, H: $T_A = 0°C$ to 70°C. DAC08/08A: $T_A = -55°C$ to 125°C.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08H DAC08A			UNIT
			Min	Typ	Max	
	Resolution Monotonicity		8 8	8 8	8 8	Bits Bits
	Relative accuracy Differential non-linearity	Over temperature range			±0.1 ±0.19	%FS %FS
TCI_{FS}	Full-scale tempco			±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change ½ LSB	−10		+18	V
I_{FS4}	Full-scale current	$V_{REF} = 10.000V$, R_{14}, $R_{15} = 5.000k\Omega$	1.984	1.992	2.000	mA
I_{FSS}	Full-scale symmetry	$I_{FS4} - I_{FS2}$		±1.0	±4.0	μA
I_{ZS}	Zero-scale current			0.2	1.0	μA
I_{FSR}	Full-scale output current range	R_{14}, $R_{15} = 5.000k\Omega$ $V_{REF} = +15.0V$, $V- = -10V$ $V_{REF} = +25.0V$, $V- = -12V$	2.1 4.2			mA
V_{IL} V_{IH}	Logic input levels Low High	$V_{LC} = 0V$	 2.0		0.8	V
I_{IL} I_{IH}	Logic input current Low High	$V_{LC} = 0V$ $V_{IN} = -10V$ to $+0.8V$ $V_{IN} = 2.0V$ to 18V		−2.0 0.002	−10 10	μA
V_{IS}	Logic input swing	$V- = -15V$	−10		+18	V
V_{THR}	Logic threshold range	$V_S = \pm 15V$	−10		+13.5	V
I_{15}	Reference bias current			−1.0	−3.0	μA
dI/dt	Reference input slew rate		4.0	8.0		mA/μs
$PSSI_{FS+}$ PSI_{FS-}	Power supply sensitivity Positive Negative	$I_{REF} = 1mA$ $V+ = 4.5$ to $5.5V$, $V- = -15V$; $V+ = 13.5$ to $16.5V$, $V- = -15V$ $V- = -4.5$ to $-5.5V$, $V+ = +15V$; $V- = -13.5$ to -16.5, $V+ = +15V$		0.0003 0.002	0.01 0.01	%FS/%VS
I+ I−	Power supply current Positive Negative	$V_S = \pm 5V$, $I_{REF} = 1.0mA$		3.1 −4.3	3.8 −5.8	mA
I+ I−	Positive Negative	$V_S = +5V$, $-15V$, $I_{REF} = 2.0mA$		3.1 −7.1	3.8 −7.8	
I+ I−	Positive Negative	$V_S = \pm 15V$, $I_{REF} = 2.0mA$		3.2 −7.2	3.8 −7.8	
P_D	Power dissipation	±5V, $I_{REF} = 1.0mA$ +5V, −15V, $I_{REF} = 2.0mA$ ±15V, $I_{REF} = 2.0mA$		37 122 156	48 136 174	mW

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			DAC08H DAC08A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_S	Settling time	To ± ½ LSB, all bits switched on or off, $T_A = 0°C$		70	135		70	135		70	135	ns
t_{PLH} t_{PHL}	Propagation delay Low-to-High High-to-Low	$T_A = 25°C$, each bit. All bits switched		35	60		35	60		35	60	ns

TEST CIRCUITS

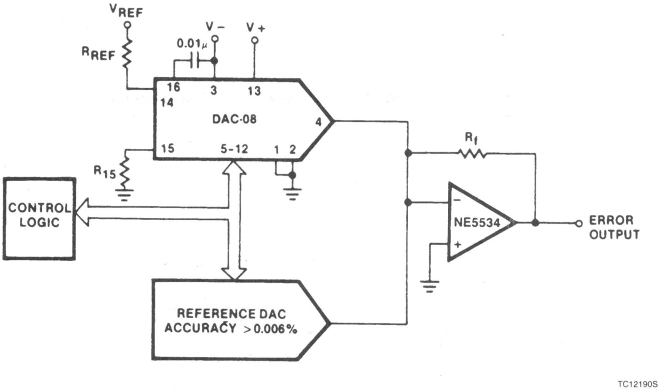

V_REF
V−
V+
0.01μ
R_REF
16
3
13
14
DAC-08
4
15
5-12
1 2
R_f
R_15
CONTROL LOGIC
NE5534
−
+
ERROR OUTPUT
REFERENCE DAC ACCURACY >0.006%
TC12190S

Figure 1. Relative Accuracy Test Circuit

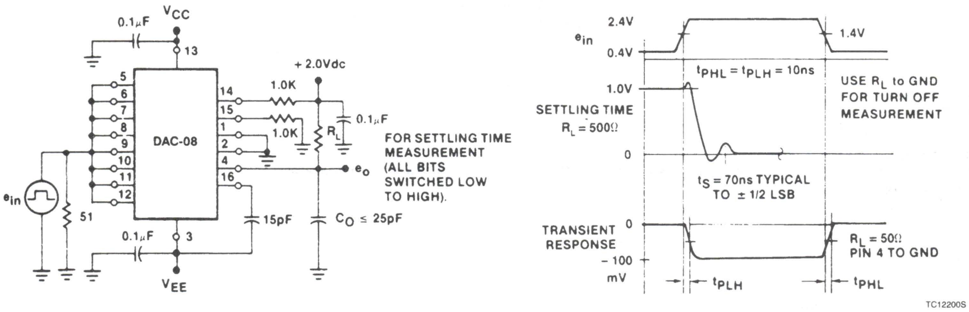
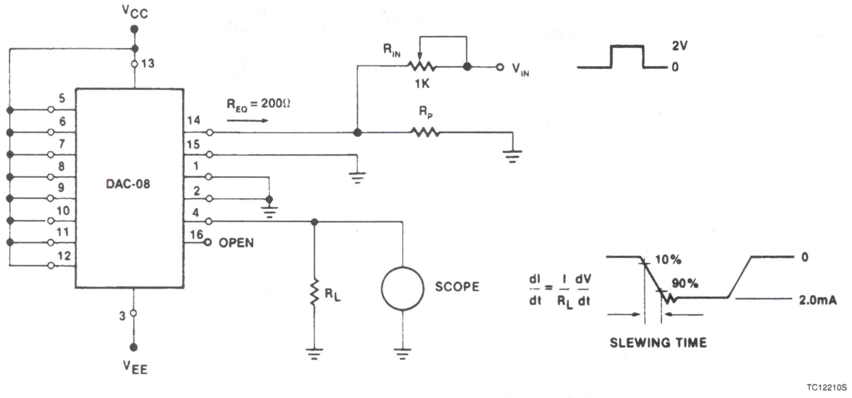

0.1μF
V_CC
13
5
6
7
8
9
10
11
12
DAC-08
14
15
1
2
4
16
+2.0Vdc
1.0K
1.0K
0.1μF
R_L
e_o
FOR SETTLING TIME MEASUREMENT (ALL BITS SWITCHED LOW TO HIGH).
e_in
51
0.1μF
3
15pF
C_O ≤ 25pF
V_EE
2.4V
e_in
0.4V
1.4V
t_PHL = t_PLH = 10ns
USE R_L to GND FOR TURN OFF MEASUREMENT
1.0V
SETTLING TIME
R_L = 500Ω
0
t_S = 70ns TYPICAL TO ± 1/2 LSB
TRANSIENT RESPONSE
0
−100
mV
R_L = 50Ω
PIN 4 TO GND
t_PLH
t_PHL
TC12200S

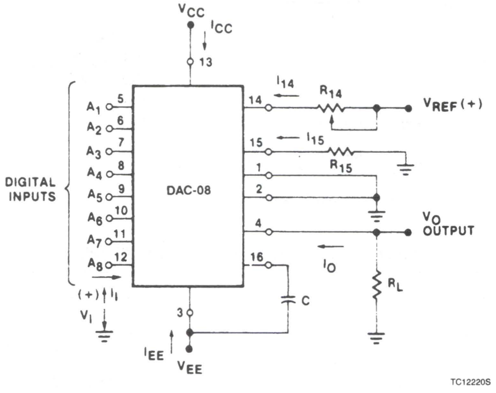
Figure 2. Transient Response and Settling Time

TEST CIRCUITS (Continued)



V_{CC}
13
5
6
7
8
9
10
11
12
DAC-08
14
15
1
2
4
16
OPEN
$R_{EQ} = 200\Omega$
R_{IN}
1K
V_{IN}
R_P
R_L
SCOPE
3
V_{EE}
2V
0
$\frac{dI}{dt} = \frac{I}{R_L} \frac{dV}{dt}$
10%
90%
0
2.0mA
SLEWING TIME
TC12210S

Figure 3. Reference Current Slew Rate Measurement



V_{CC}
I_{CC}
13
I_{14}
R_{14}
$V_{REF}(+)$
A_1 5
A_2 6
A_3 7
A_4 8
A_5 9
A_6 10
A_7 11
A_8 12
DIGITAL INPUTS
DAC-08
14
15
I_{15}
R_{15}
1
2
4
V_O OUTPUT
16
I_O
R_L
C
$(+)$ I_I
V_I
3
I_{EE}
V_{EE}
TC12220S

NOTES:
(See text for values of C.)
Typical values $R_{14} = R_{15} = 1k$
$V_{REF} = +2.0V$
$C = 15pF$
V_I and I_I apply to inputs A_1 through A_8
The resistor tied to Pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right\}$$

where $K \cong \frac{V_{REF}}{R_{14}}$

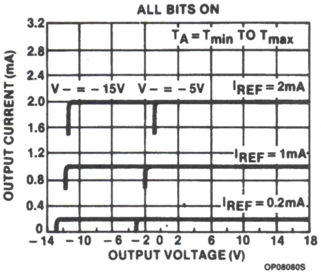
and A_N = '1' if A_N is at High Level
A_N = '0' if A_N is at Low Level

Figure 4. Notation Definitions

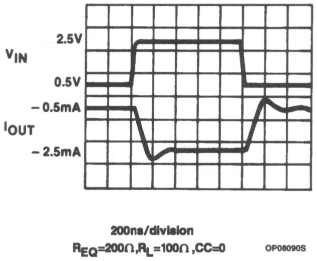
8-Bit High-Speed Multiplying D/A Converter DAC08 Series

TYPICAL PERFORMANCE CHARACTERISTICS

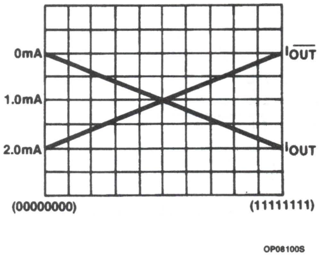
Output Current vs Output Voltage (Output Voltage Compliance)



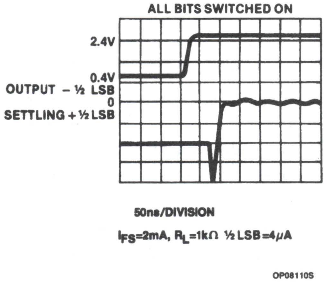
Fast Pulsed Reference Operation



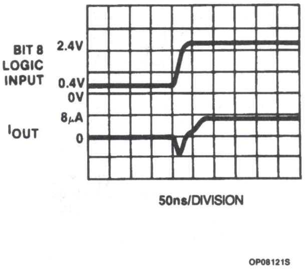
True and Complementary Output Operation



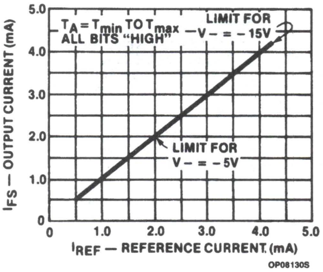
Full-Scale Settling Time



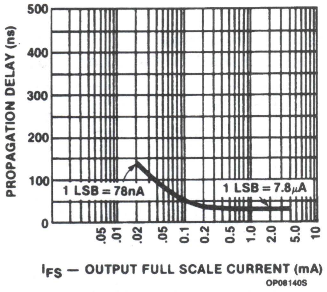
LSB Switching



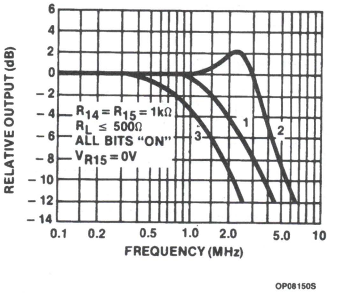
Full-Scale Current vs Reference Current



LSB Propagation Delay vs IFS



Reference Input Frequency Response



NOTES:

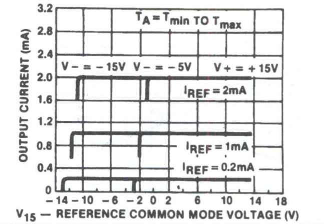
Curve 1: CC = 15pF, V_{IN} = 2.0V P-P centered at +1.0V

Curve 2: CC = 15pF, V_{IN} = 50mV P-P centered at +200mV

Curve 3: CC = 0pF, V_{IN} = 100mV P-P centered at 0V and applied through 50Ω connected to Pin 14. +2.0V applied to R_{14}.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

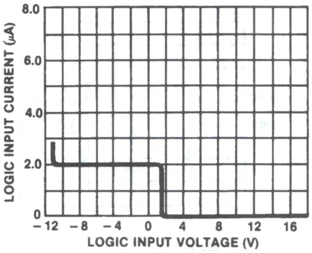
Reference AMP Common-Mode Range All Bits On



POSITIVE COMMON-MODE RANGE IS ALWAYS (V+) -1.5V.

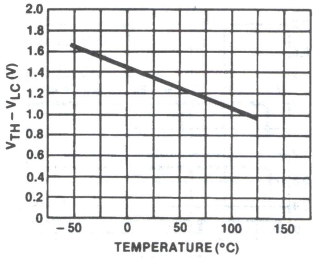
OP08161S

Logic Input Current vs Input Voltage



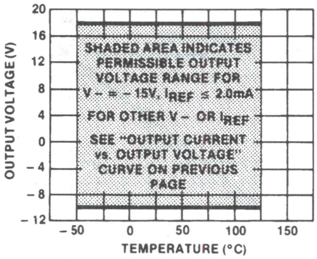
OP08170S

$V_{TH} - V_{LC}$ vs Temperature



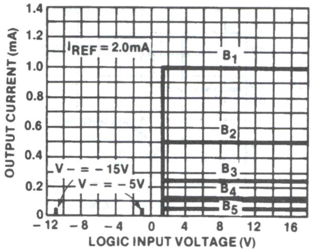
OP08180S

Output Voltage Compliance vs Temperature



OP08110S

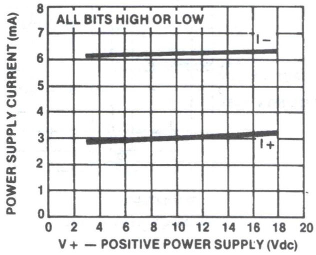
Bit Transfer Characteristics



OP08120S

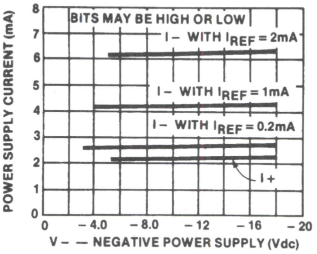
NOTE:
B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than ½ LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0V over the operating temperature range (V_{LC} = 0.0V).

Power Supply Current vs V+



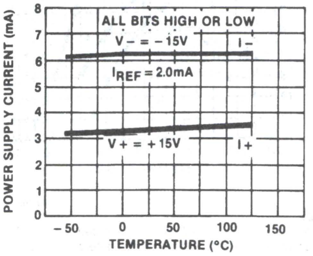
OP08130S

Power Supply Current vs V−



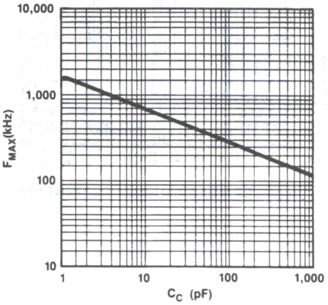
OP08220S

Power Supply Current vs Temperature



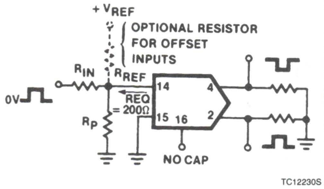
OP08230S

Maximum Reference Input Frequency vs Compensation Capacitor Value



OP08240S

TYPICAL APPLICATION



NOTES:
REQ = RIN|| RP
Typical Values
RIN = 5kΩ
+VIN = 10V

Pulsed Referenced Operation

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as R_{14} value is increased. This is in order to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF, respectively. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors with the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods applies and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the DAC08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC08 series has a very low full-scale current drift over the operating temperature range.

The DAC08 series is guaranteed accurate to within ±½ LSB at +25°C at a full-scale output current of 1.992mA. The relative accuracy test circuit is shown in Figure 1. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA, then the DAC08 full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ±½ part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the DAC08 series.

Monotonicity

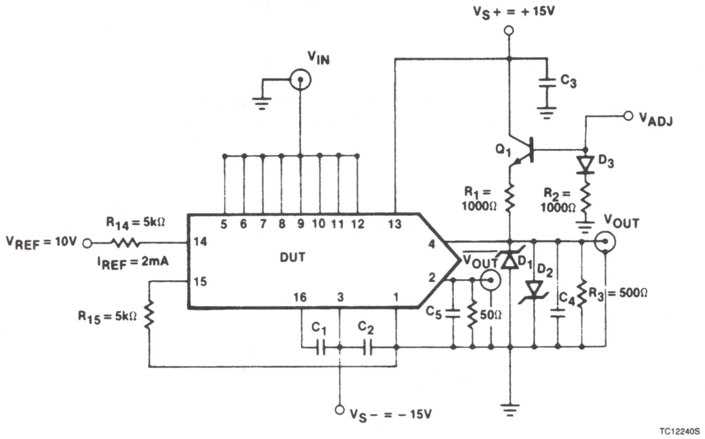
A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC08 series is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst-case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within ½ LSB for 8-bit accuracy. This time applies when $R_L < 500\Omega$ and $C_O < 25pF$. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the DAC functions in a positive-going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

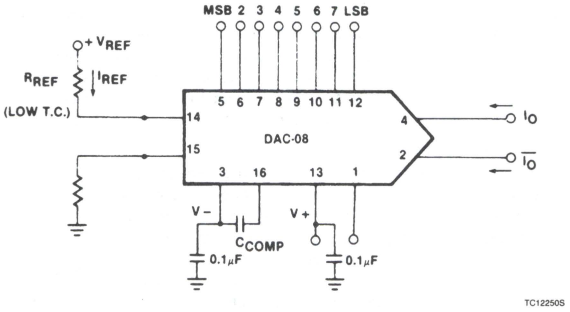
Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.

SETTLING TIME AND PROPAGATION DELAY


$V_S+ = +15V$
V_{IN}
C_3
V_{ADJ}
Q_1
D_3
$R_1 = 1000\Omega$
$R_2 = 1000\Omega$
V_{OUT}
$R_{14} = 5k\Omega$
$V_{REF} = 10V$
$I_{REF} = 2mA$
5 6 7 8 9 10 11 12 13
14
DUT
15
4
2
$\overline{V_{OUT}}$
D_1
D_2
C_4
$R_3 = 500\Omega$
$R_{15} = 5k\Omega$
16 3 1
C_1
C_2
C_5
50Ω
$V_S- = -15V$
TC12240S

NOTES:
D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
$C_1 = 0.01\mu F$
C_2, $C_3 = 0.1\mu F$
Q_1 = 2N3904
C_4, C_5 = 15pF and includes all probe and fixturing capacitance.

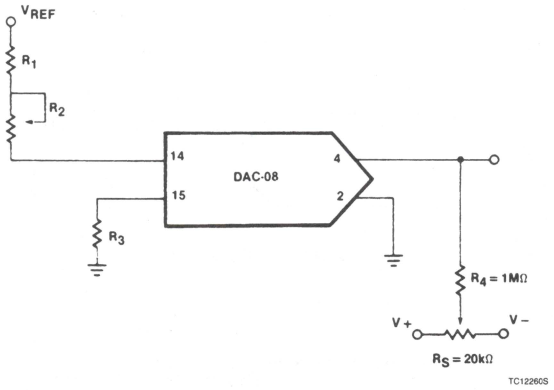
BASIC DAC08 CONFIGURATION


MSB 2 3 4 5 6 7 LSB
$+V_{REF}$
R_{REF}
I_{REF}
(LOW T.C.)
5 6 7 8 9 10 11 12
14
15
DAC-08
4
2
I_O
$\overline{I_O}$
3 16 13 1
V−
V+
C_{COMP}
$0.1\mu F$
$0.1\mu F$
TC12250S

NOTE:

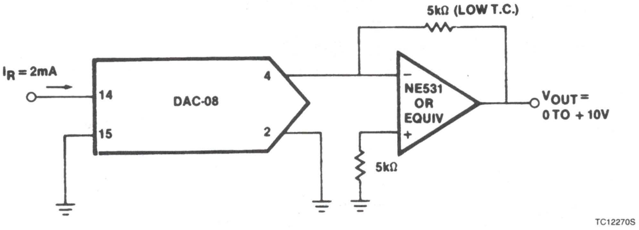
$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$; $I_O + \overline{I}_O = I_{FS}$ for all logic states

RECOMMENDED FULL-SCALE AND ZERO-SCALE ADJUST

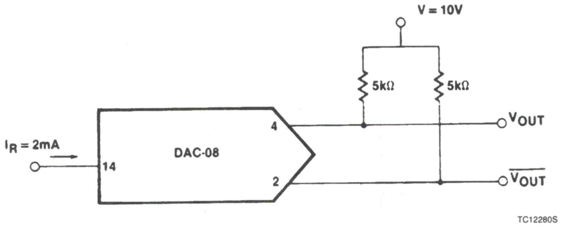

V_{REF}
R_1
R_2
14
15
4
2
DAC-08
R_3
$R_4 = 1M\Omega$
V +
V −
$R_S = 20k\Omega$
TC12260S

NOTES:
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \simeq 0.1\ R_1$ to minimize pot. contribution to full-scale drift

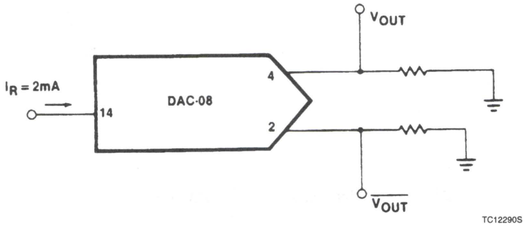
UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT


5kΩ (LOW T.C.)
$I_R = 2mA$
14
15
4
2
DAC-08
−
+
NE531 OR EQUIV
5kΩ
V_{OUT} = 0 TO + 10V
TC12270S

UNIPOLAR VOLTAGE OUTPUT FOR HIGH IMPEDANCE OUTPUT

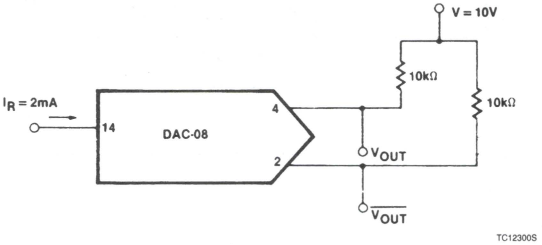

V = 10V
5kΩ
5kΩ
I_R = 2mA
14
DAC-08
4
2
V_{OUT}
$\overline{V_{OUT}}$
TC12280S

a. Positive Output


V_{OUT}
I_R = 2mA
14
DAC-08
4
2
$\overline{V_{OUT}}$
TC12290S

b. Negative Output

BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)


V = 10V
10kΩ
10kΩ
I_R = 2mA
14
DAC-08
4
2
V_{OUT}
$\overline{V_{OUT}}$
TC12300S

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
Positive full-scale	1	1	1	1	1	1	1	1	−9.920V	+10.000
Positive FS − 1LSB	1	1	1	1	1	1	1	0	−9.840V	+9.920
+Zero-scale + 1LSB	1	0	0	0	0	0	0	1	−0.080V	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale − 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Negative full scale − 1LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Negative full scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Signetics

Linear Products

AN106
Using the DAC08 Without Negative Supply

Application Note

USING THE DAC08 WITHOUT A NEGATIVE SUPPLY

The DAC08 can be used without a negative supply if a few precautions are observed:

1. V_{CC} must be in the range of 10V to 30V.
2. $V_{REF(-)}$ must be at least 3V more positive than Pin 3 at all times.
3. Pins 2 and 4 must always be at least 5V above Pin 3 for reference currents up to 2mA, and at least 8V above Pin 3 for reference currents above 2mA.
4. Pin 1 must be at least 5V above Pin 3.

Figure 1 shows the DAC08 in a circuit without a negative supply with two MC1489s used as level shifters. The need for level shifters is implied from requirement 4 above, since the logic threshold is about 1.35V above Pin 1. V_O must be the same potential as the positive logic supply because of the internal circuitry of the MC1489.

If $V_{REF(+)}$ is a very stable source with no ripple or noise, R1 and R2 can be a single resistor. The same is true of R3 and R4 if $V_{REF(-)}$ is a very stable source. Resistor values are determined as follows:

$$R1 + R2 = \frac{V_{REF(+)} - V_{REF(-)}}{I_{REF}}$$

$$R3 + R4 = R1 + R2$$

where I_{REF} is reference current through R1 and R2
(Pin 14 is at $V_{REF(-)}$ potential)

The value of the compensation capacitor, C_C, is determined by the relationship:

$$C_C = 15 \ (R1 + R2)$$

where C_C is in pF and R1 and R2 are in kΩ.

V_O (DAC08 Pin 1 and MC1489 Pin 7) must be at least 5V for DAC08 reference currents at or below 2mA, and at least 8V for reference currents above 2mA. V_O must also be equal to the positive potential of the logic supply, as mentioned above. It should be noted that the MC1489 inverts the logic inputs.

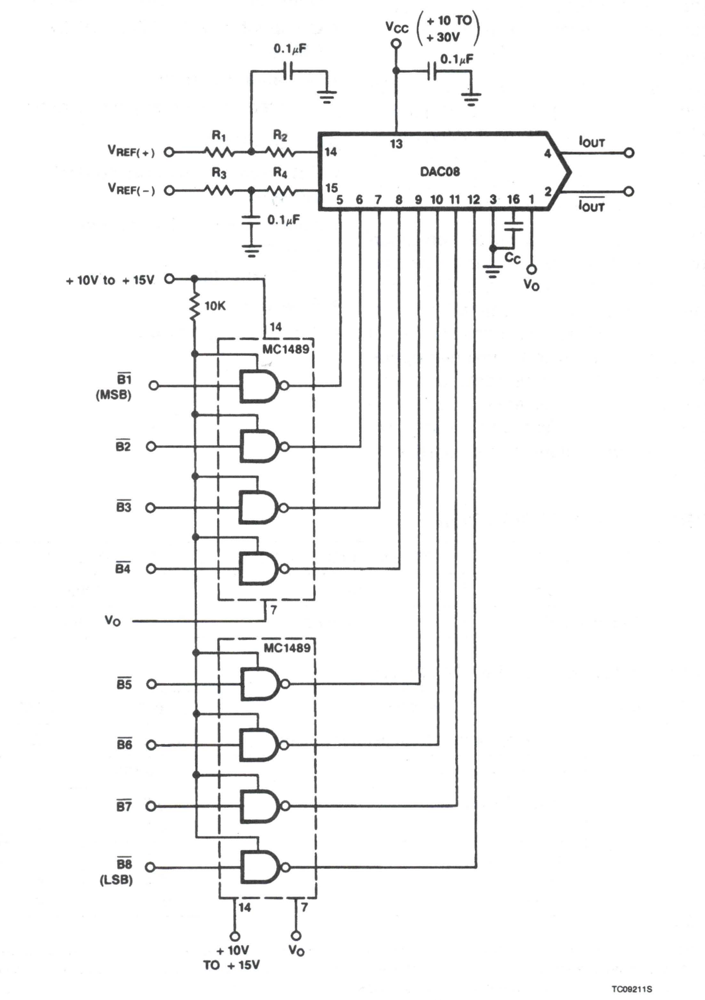
EXAMPLE

Power supply voltages of +5V and +15V are available and the input logic is TTL. The need is for a DAC with a full-scale output of 2mA.

- V_O is set to +5V
- V_{CC} for the DAC08 and the MC1489 are set to +15V
- If $V_{REF(+)}$ and $V_{REF(-)}$ are set to +15V and +5V respectively,

$$R1 + R2 = \frac{15 - 5}{I_{REF}} = \frac{10V}{2mA} = 5k\Omega$$

- R3 + R4 should also add up to 5kΩ.
- C_C is 15(5)pF = 75pF.



VCC (+10 TO +30V)
0.1μF
0.1μF
VREF(+)
VREF(−)
R1
R2
R3
R4
0.1μF
14
15
13
DAC08
5 6 7 8 9 10 11 12 3 16 1
4
2
IOUT
$\overline{IOUT}$
CC
VO
+10V to +15V
10K
14
MC1489
$\overline{B1}$ (MSB)
$\overline{B2}$
$\overline{B3}$
$\overline{B4}$
7
VO
MC1489
$\overline{B5}$
$\overline{B6}$
$\overline{B7}$
$\overline{B8}$ (LSB)
14
7
+10V TO +15V
VO
TC09211S

Figure 1. Using the DAC08 Without a Negative Supply

DAC800

12-Bit D/A Converter

Objective Specification

DESCRIPTION

The DAC800 is a single-chip converter with 12-bit linearity, obtained without trimming. It is pin compatible with the industry standard DAC80 (no external reference can be used) and has a faster settling time. This converter has thin film application resistors, a low temperature coefficient bandgap reference, and an output amplifier (V models).

The DAC800 provides for both bipolar and unipolar outputs. The V models allow output ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. The current models have an output range of either ±1mA or 0 to −2mA.

The DAC800 has a maximum non-linearity error of ±½ LSB over the full temperature range, 0°C to +70°C. Additionally, the DAC800 offers maximum total error over the full temperature range of ±0.15% of full-scale for unipolar operation and ±0.12% of full-scale for bipolar operation. The total error includes the effects of gain, offset, and linearity drift with gain and offset errors adjusted to zero at 25°C.

FEATURES

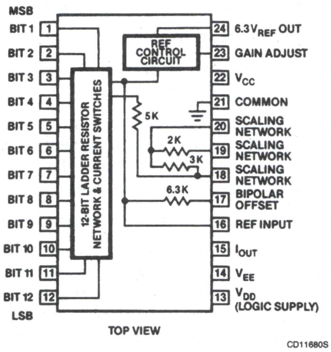
- **Maximum non-linearity ±½ LSB**
- **Guaranteed monotonicity 0°C to +70°C**
- **Current or voltage output models**
- **Internal reference**
- **Unipolar and bipolar operation**
- **Compatible with TTL/LSTTL/CMOS**
- **No laser trimming**
- **Excellent power supply rejection**

APPLICATIONS

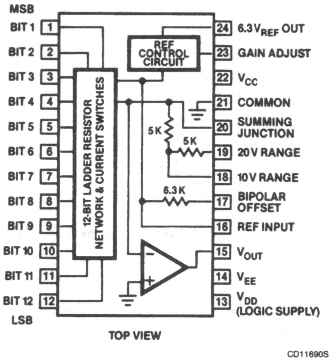
- **Data acquisition and control systems**
- **Analog-to-digital converter systems**
- **Automatic test equipment**
- **Robotics**
- **Waveform generation**

PIN CONFIGURATIONS

Current Model
F Package


MSB
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
LSB
1
2
3
4
5
6
7
8
9
10
11
12
12-BIT LADDER RESISTOR NETWORK & CURRENT SWITCHES
REF CONTROL CIRCUIT
5K
2K
3K
6.3K
24
23
22
21
20
19
18
17
16
15
14
13
6.3 V_{REF} OUT
GAIN ADJUST
V_{CC}
COMMON
SCALING NETWORK
SCALING NETWORK
SCALING NETWORK
BIPOLAR OFFSET
REF INPUT
I_{OUT}
V_{EE}
V_{DD} (LOGIC SUPPLY)
TOP VIEW
CD11680S

Voltage Model
F Package


MSB
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
LSB
1
2
3
4
5
6
7
8
9
10
11
12
12-BIT LADDER RESISTOR NETWORK & CURRENT SWITCHES
REF CONTROL CIRCUIT
5K
5K
6.3K
−
+
24
23
22
21
20
19
18
17
16
15
14
13
6.3 V_{REF} OUT
GAIN ADJUST
V_{CC}
COMMON
SUMMING JUNCTION
20 V RANGE
10 V RANGE
BIPOLAR OFFSET
REF INPUT
V_{OUT}
V_{EE}
V_{DD} (LOGIC SUPPLY)
TOP VIEW
CD11690S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Cerdip	0 to +70°C	DAC800IF
24-Pin Cerdip	0 to +70°C	DAC800VF

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{CC}, V_{EE} V_{DD}	Power Supply	±16.5 +16.5	V V
	Logic Levels High Low	 +16.5 0	 V V

NOTE:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12-Bit D/A Converter DAC800

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 15V$, $V_{EE} = -15V$, $V_{DD} = 5V$, $0°C < T_A < +70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		12			Bits
	Monotonicity		12			Bits
NL	Non-linearity				± ½	LSB
DNL	Differential nonlinearity			± ½	± 1	LSB
	Gain error[1]	$T_A = 25°C$		± 0.1	± 0.2	% of FSR
	Gain tempco			± 10	± 30	ppm/°C
	Offset error[1]			± 0.05	± 0.15	% of FSR[3]
	Offset tempco[2]	Unipolar connection		± 1	± 3	ppm of FSR/°C
	Offset tempco[2]	Bipolar connection		± 7	± 15	ppm of FSR/°C
	Bipolar drift	Full-scale drift for bipolar connection		± 10	± 25	ppm of FSR/°C
	Total error[4]	Upipolar connection		± 0.06	± 0.15	% of FSR
	Total error[4]	Bipolar connection		± 0.05	± 0.12	% of FSR
t_S	Settling time to 0.01% of FSR[6]	20V range		3	5	μs
t_S	Settling time to 0.01% of FSR[6]	10V range		2.5	4	μs
t_S	Settling time to 0.01% of FSR[6]	1 LSB change, major carry		1.5		μs
t_S	Settling time to 0.01% of FSR[7]	10 to 100Ω load		300		ns
t_S	Settling time to 0.01% of FSR[7]	1kΩ load		1		μs
I_{FS}	Full-scale current	I Model only	1.7	2	2.3	mA
	Converter output impedance	I Model only		10		MΩ
	Converter output compliance	I Model only	−2.5		+2.5	V
SR	Amplifier slew rate[6]		10	15		V/μs
I_{OUT}	Amplifier output current	V Model only	± 5			mA
	Amplifier DC output impedance	V Model only		0.05		Ω
	Amplifier duration output Short-circuit to ground[8]	V Model only				
V_{REF}	Reference voltage output		6.23	6.30	6.37	V
	Reference voltage tempco			± 10	± 30	ppm/°C
	Reference output source current		1.5	2.5		mA

NOTES:

1. Adjustable to zero with external trim potentiometer.
2. To maintain drift specs internal resistors must be used on current output model.
3. FSR means full-scale range and is 20V for ± 10V range, 10V for ± 5V range, etc.
4. Includes the effects of gain, offset, and linearity drift. Gain and offset errors are adjusted to zero at 25°C.
5. Power dissipation is an additional 20mW when V_{DD} is operated at +15V.
6. $R_L = 2k\Omega$, $C_L = 200pF$, $T_A = 25°C$ for V models only.
7. $C_L = 10pF$, $T_A = 25°C$ for I models.
8. Typical operating conditions for amplifier duration output short-circuit to ground is indefinite at this time.

12-Bit D/A Converter DAC800

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 15V$, $V_{EE} = -15V$, $V_{DD} = 5V$, $0°C < T_A < +70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	Logic input high		2		16.5	V
V_{IL}	Logic input low		0		0.8	V
I_{IH}	Logic high input current	$V_{IN} = 2.4V$			20	μA
I_{IL}	Logic low input current	$V_{IN} = 0.4V$	-20			μA
V_{CC}, V_{EE}, V_{DD}	Power supply sensitivity			±0.0005	±0.001	% of FSR/%V
V_{CC}, V_{EE}			±13.5	±15	±16.5	V
V_{DD}[1]			4.5	5	16.5	V
I_{CC}				11	14	mA
I_{EE}			-20	-17		mA
I_{DD}				6.5	8	mA

NOTE:

1. Power dissipation is an additional 20mW when V_{DD} is operated at +15V.

POWER SUPPLY CONNECTIONS

Any noise present on the power supply pins of the DAC800 creates additional error. For optimum performance this noise should be limited as much as possible. This can be accomplished by bypassing the power supply pins with appropriate capacitors. Decoupling capacitors on the order of 1μF are recommended, the best types being tantalum or electrolytic. Electrolytic capacitors have poor high frequency characteristics and, if used, should be paralleled with a 0.01μF ceramic capacitor.

LOGIC INPUTS

The logic inputs of the DAC800 are compatible with TTL, LSTTL, and CMOS over the operating range of V_{DD} (5V to 15V) as well as over temperature (0°C to +70°C). The input switching threshold is TTL (about 1.4V) and is independent of the supply voltage, V_{DD}.

Logic input coding for the DAC800 is complementary. The specific code will be complementary straight binary (CSB) for unipolar output connections and complementary offset binary (COB) for bipolar output connections. For bipolar output connections, complementary two's complement (CTC) can be realized by inverting the MSB with an external inverter. The relationship between the digital input and analog output for the three codes is shown in Table 1.

VOLTAGE REFERENCE

The DAC800 has an internal 6.3V reference with a ±1% tolerance. The reference is connected internally to the converter, to the bipolar offset resistor, and to Pin 16, which does not allow the use of an external reference. The reference is brought out on Pin 24 for external use, if needed, and can typically supply 2.5mA. If the external load varies, an external buffer is recommended to isolate the reference from load variations.

EXTERNAL GAIN/OFFSET ADJUSTMENTS

The gain and offset of the DAC800 can be adjusted with external potentiometers. The potentiometer configuration required for gain adjustment is shown in Figure 1. The 10MΩ resistor should have a tolerance of 20% or less and the potentiometer and 10MΩ resistor should have a temperature coefficient of 200ppm/°C or less.

The potentiometer configuration required for offset adjustment is shown in Figure 2 and its equivalent circuit in Figure 3. From the equivalent circuit it can be seen that this configuration adds/subtracts a current from the converter output current. The 3.9MΩ resistor should have a tolerance of 20% or less and the potentiometer and 3.8MΩ resistor should have a temperature coefficient of 200ppm/°C or less. Both adjustment circuits should be located close to the DAC800 to prevent noise pickup. If full-scale accuracy is not required, then the gain adjust pin may be grounded to minimize noise pick-up.

The effects of gain and offset adjustment are shown in Figures 4 and 5. Figure 4 shows that gain adjustment rotates the transfer function about the origin and has no impact on the origin. Figure 5 shows that offset adjustment translates the transfer function along the Analog Output axis. Note that this changes the output for full-scale. The objective of the adjustment procedure is to fix the end points of the transfer function at the ideal points. For this reason the adjustment sequence must be to first adjust the offset and then the gain. Offset adjustment is accomplished by setting all logic inputs to a logic high ("1") and adjusting the offset so that the output corresponds to its most negative value (zero for unipolar outputs and full-scale for bipolar outputs). Gain adjustment is accomplished by setting all logic inputs to a logic low ("0") and adjusting the gain such that the output corresponds to its most positive value (fullscale -1 LSB).

VOLTAGE MODEL OUTPUT CONNECTIONS

The DAC800 voltage models have internal scaling resistors which provide output ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. The use of the internal resistors minimizes gain and offset drift since excellent thermal tracking with other on-chip components limits this effect. Figures 6a, b, and c show the different output configurations.

Table 1. Coding Relationships

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	CSB	COB	CTC
000000000000	+Full-scale −1 LSB	+Full-scale −1 LSB	−1 LSB
011111111111	+½ Full-scale	Zero	−Full-scale
100000000000	+½ Full-scale −1 LSB	−1 LSB	+Full-scale −1 LSB
111111111111	Zero	−Full-scale	Zero

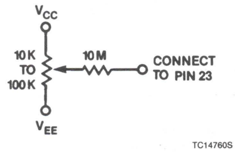

V_CC
10K TO 100K
10M
CONNECT TO PIN 23
V_EE
TC14760S

Figure 1. Gain Adjust Circuit

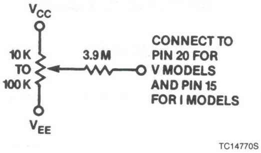

V_CC
10K TO 100K
3.9M
CONNECT TO PIN 20 FOR V MODELS AND PIN 15 FOR I MODELS
V_EE
TC14770S

Figure 2. Offset Adjust Circuit

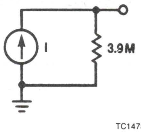

I
3.9M
TC14780S

Figure 3. Offset Adjust Equivalent Circuit

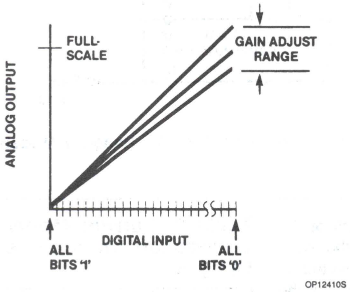


Figure 4. Gain Adjust Effects

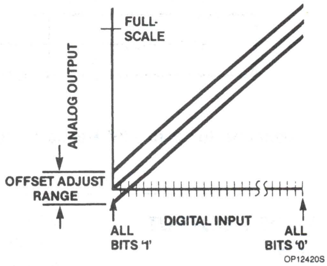
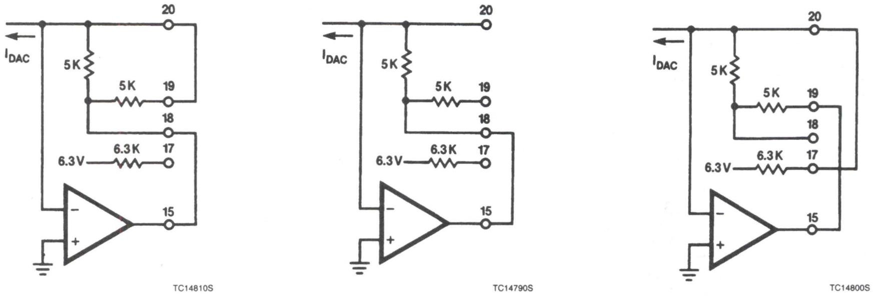


Figure 5. Offset Adjust Effects

12-Bit D/A Converter DAC800



NOTE:
*Connect Pin 17 to Pin 20 for ±2.5 range and to ground for 0 to 5V range

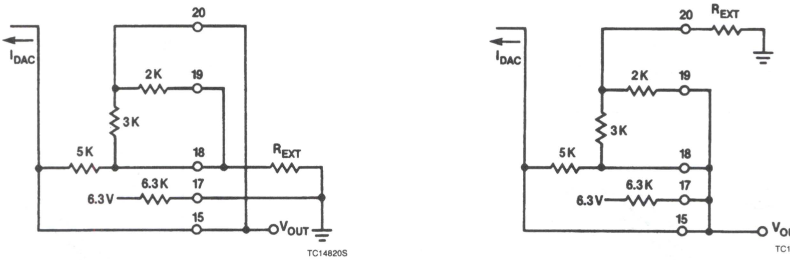
NOTE:
*Connect Pin 17 to Pin 20 for ±5V and to ground for 0 to 10V range

a. Connections for 0 to 5V Range and ±2.5V Range (V Model)

b. Connections for 0 to 10V Range and ±5V Range (V Model)

c. Connections for ±10V Range (V Model)

Figure 6



a. Connections for 0 to −2V Range (I Model)

b. Connections for +1V Range (I Model)

Figure 7

CURRENT MODEL OUTPUT CONNECTIONS

Internal resistors are provided for the current model which can be used with an external op amp or configured as a restrictive load for output ranges of 0 to −2V or ±1V. Use of these internal resistors is required to maintain gain and bipolar offset drift specifications.

Output ranges of 0 to −2V and ±1V are obtainable with the addition of a single external resistor (exclude the gain and offset adjustment components). Figures 7a and b show the necessary connections for these output ranges. The internal resistors of the DAC800 have wide tolerances, and the external resistor, R_{EXT}, will have to be selected for each unit. Nominal values will be 32Ω for the unipolar connection and 0Ω for the bipolar connection.

The current output can also be used to drive the summing junction of an external op amp used as a voltage-to-current converter. This has the advantage of faster settling time than the voltage model. Figure 8 shows the general configuration and Table 2 lists the available output ranges and required connections.

Table 2. Current Model Connection for Various Output Ranges

OUTPUT RANGE	CONNECT		
	OUT TO	19 TO	17 TO
±10V	19	Out	15
±5V	18	NC	15
±2.5V	18	15	15
0 to +10V	18	NC	GND
0 to +5V	18	15	GND

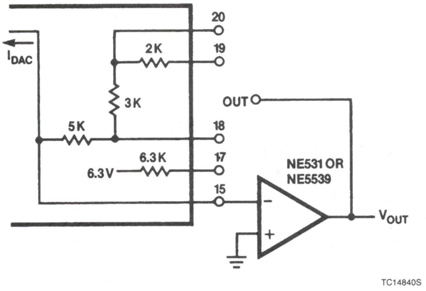

20
19
18
17
15
2K
3K
5K
6.3K
6.3V
I_{DAC}
OUT
NE531 OR
NE5539
V_{OUT}
TC14840S

Figure 8. General Configuration for Current Model Using External Op Amp

Signetics

MC1508-8/1408-8/1408-7
8-Bit Multiplying D/A Converter

Product Specification

Linear Products

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high-speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

FEATURES

- **Fast settling time — 70ns (typ)**
- **Relative accuracy ±0.19% (max error)**
- **Non-inverting digital inputs are TTL and CMOS compatible**
- **High-speed multiplying rate 4.0mA/μs (input slew)**
- **Output voltage swing +0.5V to −5.0V**
- **Standard supply voltages +5.0V and −5.0V to −15V**
- **Military qualifications pending**

APPLICATIONS

- **Tracking A-to-D converters**
- **2½-digit panel meters and DVMs**
- **Waveform synthesis**
- **Sample-and-hold**
- **Peak detector**
- **Programmable gain and attenuation**
- **CRT character generation**
- **Audio digitizing and decoding**
- **Programmable power supplies**
- **Analog - digital multiplication**
- **Digital - digital multiplication**
- **Analog - digital division**
- **Digital addition and subtraction**
- **Speech compression and expansion**
- **Stepping motor drive**
- **Modems**
- **Servo motor and pen drivers**

CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, an R-2R ladder, and 8 high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

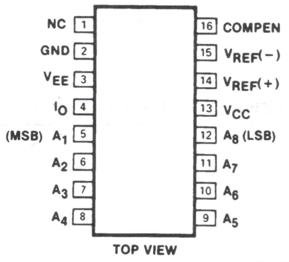
The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

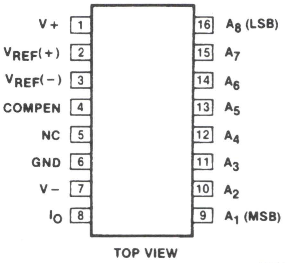
PIN CONFIGURATIONS

F, N Packages


NC 1
GND 2
VEE 3
IO 4
(MSB) A1 5
A2 6
A3 7
A4 8
16 COMPEN
15 VREF(−)
14 VREF(+)
13 VCC
12 A8 (LSB)
11 A7
10 A6
9 A5
TOP VIEW

CD10600S

D Package[1]

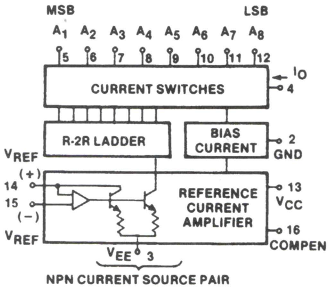

V+ 1
VREF(+) 2
VREF(−) 3
COMPEN 4
NC 5
GND 6
V− 7
IO 8
16 A8 (LSB)
15 A7
14 A6
13 A5
12 A4
11 A3
10 A2
9 A1 (MSB)
TOP VIEW

CD10610S

NOTE:

1. SO and non-standard pinouts.

BLOCK DIAGRAM


MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8
5 6 7 8 9 10 11 12
IO
4
CURRENT SWITCHES
R-2R LADDER
BIAS CURRENT
2
GND
VREF (+)
14
15
(−) VREF
REFERENCE CURRENT AMPLIFIER
13
VCC
16
COMPEN
VEE 3
NPN CURRENT SOURCE PAIR

BD03700S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	−55°C to +125°C	MC1508-8F
16-Pin Plastic DIP	0 to +70°C	MC1408-7N
16-Pin Cerdip	0 to +70°C	MC1408-7F
16-Pin SO package	0 to +70°C	MC1408-8D

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive power supply voltage	+5.5	V
V_{EE}	Negative power supply voltage	−16.5	V
$V_5 - V_{12}$	Digital input voltage	0 to V_{CC}	V
V_O	Applied output voltage	−5.2 to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1080	mW
T_{SOLD}	Lead soldering temperature (10sec)	300	°C
T_A	Operating temperature range		
	MC1508	−55 to +125	°C
	MC1408	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.6mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS[1]

Pin 3 must be 3V more negative than the potential to which R_{15} is returned.

$V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $\frac{V_{REF}}{R_{14}} = 2.0mA$ unless otherwise specified.

MC1508: $T_A = -55°C$ to $125°C$. MC1408: $T_A = 0°C$ to $75°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy	Error relative to full-scale I_O, Figure 3			±0.19			±0.19			±0.39	%
t_S	Settling time[1]	To within ½ LSB, includes t_{PLH}, $T_A = +25°C$, Figure 4		70			70			70		ns
t_{PLH} t_{PHL}	Propagation delay time Low-to-High High-to-Low	$T_A = +25°C$, Figure 4		35	100		35	100		35	100	ns
TCI_O	Output full-scale current drift			−20			−20			−20		ppm/°C
V_{IH} V_{IL}	Digital input logic level (MSB) High Low	Figure 5	2.0		0.8	2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (MSB) High Low	Figure 5 $V_{IH} = 5.0V$ $V_{IL} = 0.8V$		0 −0.4	0.04 −0.8		0 −0.4	0.04 −0.8		0 −0.4	0.04 −0.8	mA
I_{15}	Reference input bias current	Pin 15, Figure 5		−1.0	−5.0		−1.0	−5.0		−1.0	−5.0	μA
I_{OR}	Output current range	Figure 5 $V_{EE} = -5.0V$ $V_{EE} = -7.0V$ to $-15V$	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
I_O $I_{O(min)}$	Output current Off-state	Figure 5 $V_{REF} = 2.000V$, $R14 = 1000\Omega$ All bits low	1.9	1.99 0	2.1 4.0	1.9	1.99 0	2.1 4.0	1.9	1.99 0	2.1 4.0	mA μA
V_O	Output voltage compliance	$E_r \leqslant 0.19\%$ at $T_A = +25°C$, Figure 5 $V_{EE} = -5V$ V_{EE} below $-10V$		−0.6, +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5		−0.6, +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5		−0.6, +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5	V_{DC}
SRI_{REF}	Reference current slew rate	Figure 6		8.0			8.0			8.0		mA/μs
PSRR(−)	Output current power supply sensitivity	$I_{REF} = 1mA$		0.5	2.7		0.5	2.7		0.5	2.7	μA/V
I_{CC} I_{EE}	Power supply current Positive Negative	All bits low, Figure 5		+2.5 −6.5	+22 −13		+2.5 −6.5	+22 −13		+2.5 −6.5	+22 −13	mA
V_{CCR} V_{EER}	Power supply voltage range Positive Negative	$T_A = +25°C$, Figure 5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	V_{DC}
P_D	Power Dissipation	All bits low, Figure 5 $V_{EE} = -5.0V_{DC}$ $V_{EE} = -15V_{DC}$		34 110	170 305		34 110	170 305		34 110	170 305	mW

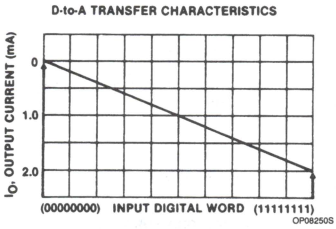
NOTE:

1. All bits switched.

8-Bit Multiplying D/A Converter

MC1508-8/1408-8/1408-7

TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated and Pin 15 grounded, with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increasing values of R_{14} to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply).

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15}, as shown in Figure 2. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

Capacitive bypass to ground is recommended when a DC reference voltage is used. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors and the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious degradation of accuracy.

Signetics' MC1508/MC1408 does not need a range control because the design extends the compliance range down to 4.5V (or 8V — see above) above the negative supply voltage without significant degradation of accuracy. Signetics' MC1508/MC1408 can be used in sockets designed for other manufacturers' MC1508/MC1408 without circuit modification.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the MC1508/MC1408 is essentially constant over the operating temperature range because of the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current; however, the MC1508/MC1408 has a very low full-scale current drift over the operating temperature range.

The MC1508/MC1408 series is guaranteed accurate to within ± ½ LSB at +25°C at a full-scale output current of 1.99mA. The relative accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA; then the MC1508/MC1408's full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ± ½ part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the MC1508/MC1408.

Monotonicity

A monotonic converter is one which always provides an analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The MC1508/MC1408 is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within ½ LSB for 8-bit accuracy. This time applies when $R_L < 500\Omega$ and $C_O < 25pF$. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, good ground planes, and avoidance of ground loops are all mandatory.

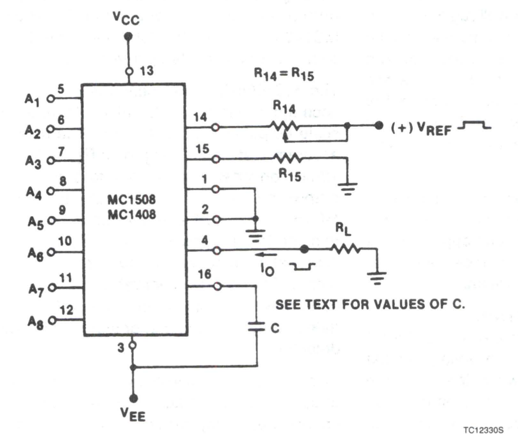

V_{CC}
13
$R_{14} = R_{15}$
A_1 5
A_2 6
A_3 7
A_4 8
A_5 9
A_6 10
A_7 11
A_8 12
MC1508
MC1408
14
R_{14}
(+) V_{REF}
15
R_{15}
1
2
4
R_L
16
I_O
SEE TEXT FOR VALUES OF C.
C
3
V_{EE}
TC12330S

Figure 1. Positive V_{REF}

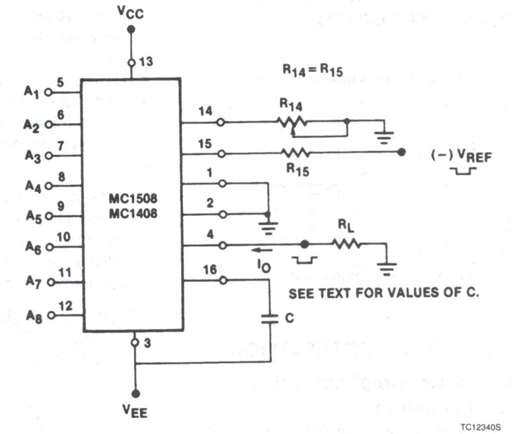

V_{CC}
13
$R_{14} = R_{15}$
A_1 5
A_2 6
A_3 7
A_4 8
A_5 9
A_6 10
A_7 11
A_8 12
MC1508
MC1408
14
R_{14}
15
R_{15}
(−) V_{REF}
1
2
4
R_L
16
I_O
SEE TEXT FOR VALUES OF C.
C
3
V_{EE}
TC12340S

Figure 2. Negative V_{REF}

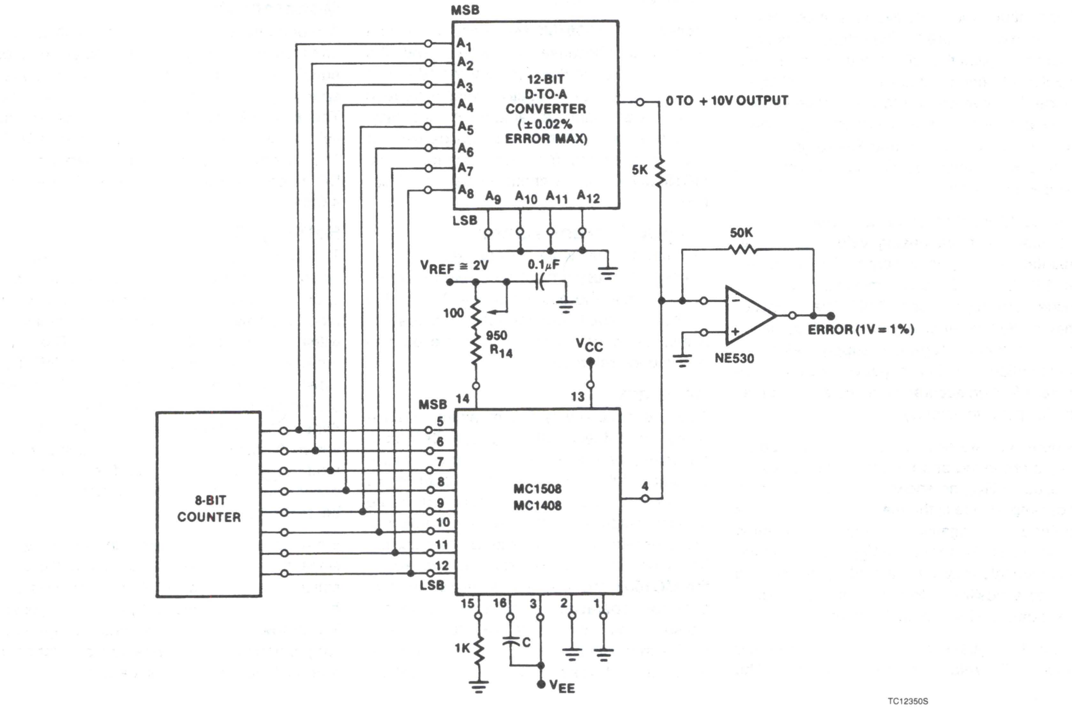

MSB
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
A_9
A_{10}
A_{11}
A_{12}
LSB
12-BIT
D-TO-A
CONVERTER
(±0.02%
ERROR MAX)
0 TO +10V OUTPUT
5K
50K
$V_{REF} \cong 2V$
0.1µF
100
950
R_{14}
V_{CC}
NE530
ERROR (1V = 1%)
MSB
14
13
5
6
7
8
9
10
11
12
LSB
8-BIT
COUNTER
MC1508
MC1408
4
15
16
3
2
1
1K
C
V_{EE}
TC12350S

Figure 3. Relative Accuracy

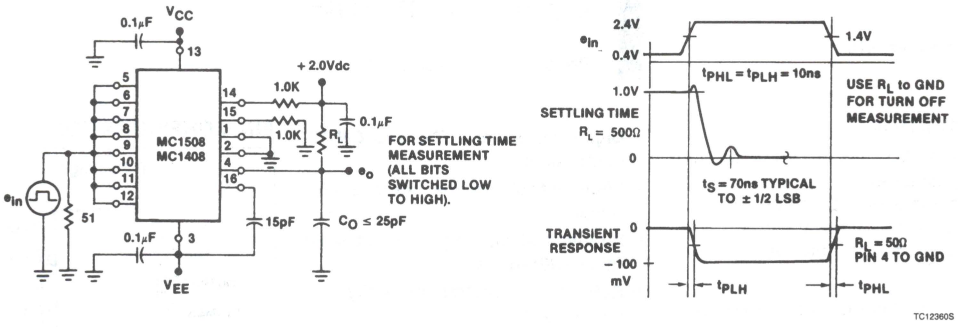
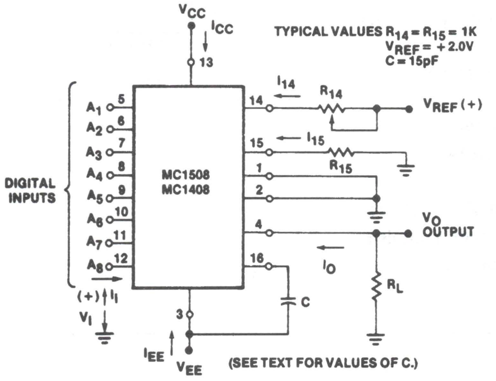

0.1μF
VCC
13
+2.0Vdc
1.0K
14
15
1
2
4
16
1.0K
0.1μF
RL
MC1508
MC1408
5
6
7
8
9
10
11
12
ein
51
0.1μF
3
VEE
15pF
CO ≤ 25pF
eo
FOR SETTLING TIME MEASUREMENT (ALL BITS SWITCHED LOW TO HIGH).
2.4V
ein
0.4V
1.4V
tPHL = tPLH = 10ns
USE RL to GND FOR TURN OFF MEASUREMENT
1.0V
SETTLING TIME
RL = 500Ω
0
tS = 70ns TYPICAL TO ± 1/2 LSB
TRANSIENT RESPONSE
0
−100 mV
RL = 50Ω
PIN 4 TO GND
tPLH
tPHL
TC12360S

Figure 4. Transient Response and Settling Time


VCC
ICC
13
TYPICAL VALUES R14 = R15 = 1K
VREF = +2.0V
C = 15pF
I14
R14
14
VREF (+)
15
I15
R15
1
2
4
VO OUTPUT
16
IO
RL
C
DIGITAL INPUTS
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
MC1508
MC1408
(+)
II
VI
3
IEE
VEE
(SEE TEXT FOR VALUES OF C.)

VI AND II APPLY TO INPUTS A1 THROUGH A8

THE RESISTOR TIED TO PIN 15 IS TO TEMPERATURE COMPENSATE THE BIAS CURRENT AND MAY NOT BE NECESSARY FOR ALL APPLICATIONS.

$$I_O = K \left\{ \frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right\}$$

where $K \cong \frac{V_{REF}}{R_{14}}$

and A_N = "1" IF A_N IS AT HIGH LEVEL
A_N = "0" IF A_N IS AT LOW LEVEL

TC22080S

Figure 5. Notation Definitions

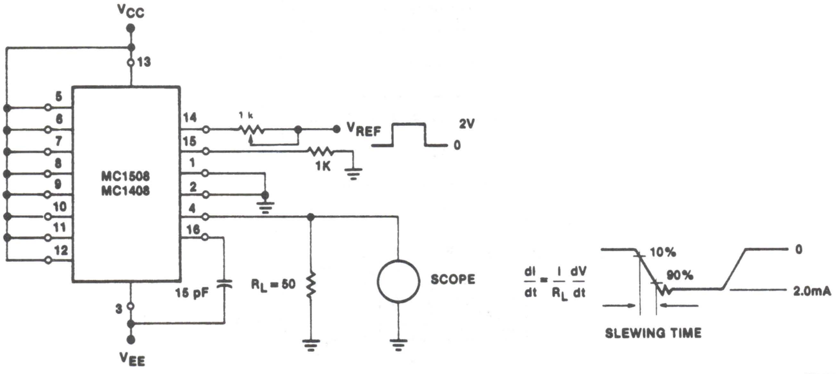

VCC
13
5
6
7
8
9
10
11
12
MC1508
MC1408
14
15
1
2
4
16
1k
VREF
2V
0
1K
15 pF
RL = 50
SCOPE
3
VEE
$\frac{di}{dt} = \frac{1}{R_L}\frac{dV}{dt}$
10%
90%
0
2.0mA
SLEWING TIME
TC22090S

Figure 6. Reference Current Slew Rate Measurement

Signetics

Linear Products

MC3410, MC3510, MC3410C

10-Bit High-Speed Multiplying D/A Converter

Product Specification

DESCRIPTION

The MC3410 series are 10-bit Multiplying Digital-to-Analog Converters. They are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The Signetics' design provides complete 10-bit accuracy without laser trimming, and guaranteed monotonicity over temperature. Segmented current sources, in conjunction with an R-2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

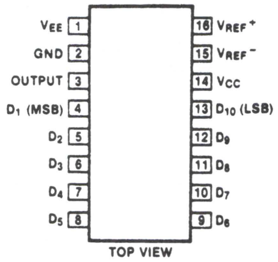
- **10-bit resolution and accuracy (± 0.05%)**
- **Guaranteed monotonicity over temperature**
- **Fast settling time — 250ns typical**
- **Digital inputs are TTL and CMOS compatible**
- **Wide output voltage compliance range**
- **High-speed multiplying input slew rate — 20mA/μs**
- **Reference amplifier internally-compensated**
- **Standard supply voltages +5V and −15V**

APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

PIN CONFIGURATION

F Package

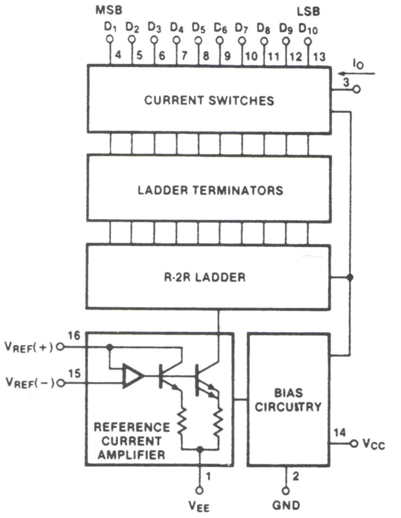


VEE 1
GND 2
OUTPUT 3
D1 (MSB) 4
D2 5
D3 6
D4 7
D5 8
16 VREF+
15 VREF−
14 VCC
13 D10 (LSB)
12 D9
11 D8
10 D7
9 D6
TOP VIEW

CD13260S

TOP VIEW

BLOCK DIAGRAM



MSB
LSB
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10
4 5 6 7 8 9 10 11 12 13
IO
3
CURRENT SWITCHES
LADDER TERMINATORS
R-2R LADDER
VREF(+)
16
VREF(−)
15
REFERENCE CURRENT AMPLIFIER
BIAS CIRCUITRY
14
VCC
1
VEE
2
GND

BD09980S

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	MC3410F
16-Pin Cerdip	0 to +70°C	MC3410CF
16-Pin Cerdip	-55°C to +125°C	MC3510F

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$ unless otherwise noted

SYMBOL	PARAMETER	RATING	UNIT
V_{CC} V_{EE}	Power supply	+7.0 -18	V_{DC} V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	0.5, -5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating ambient temperature range MC3510 MC3410, 3410C	 -55 to +125 0 to +70	 °C °C
T_J	Junction temperature, ceramic package	+150	°C
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package	1190	mW

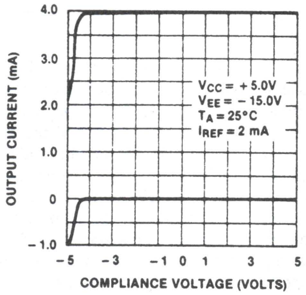
NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = +5.0V_{DC}$, $V_{EE} = -15_{DC}$, $\frac{V_{REF}}{R16} = 2.0mA$, all digital inputs at high logic level.

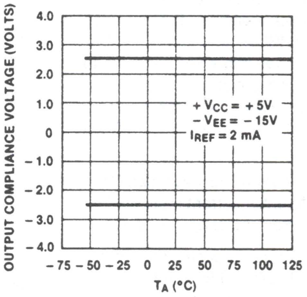
MC3510: $T_A = -55°C$ to $+125°C$, MC3410 Series: $T_A = 0°C$ to $+70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3410, MC3510			MC3410C			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy (error relative to full-scale I_O)	$T_A = 25°C$			±0.05			±0.1	%
					1/4			1/2	LSB
TCE_r	Relative accuracy drift (relative to full-scale I_O)			2.5			2.5		ppm/°C
	Monotonicity	Over temperature	10			10			Bits
t_S	Settling time to within ±1/2 LSB (all bits LOW-to-HIGH)	$T_A = 25°C$		250			250		ns
t_{PLH} t_{PHL}	Propagation delay time	$T_A = 25°C$		35 20			35 20		ns
TCI_O	Output full scale current drift				60			70	ppm/°C
V_{IH}	Digital input logic levels (all bits) HIGH-level, Logic "1" LOW-level, Logic "0"		2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) HIGH-level, $V_{IH} = 5.5V$ LOW-level, $V_{IL} = 0.8V$			-0.05	+.04 -0.4		-0.05	+.04 -0.4	mA
$I_{REF(15)}$	Reference input bias current (Pin 15)			-1.0	-5.0		-1.0	-5.0	μA
I_{OR}	Output current range			4.0	5.0		4.0	5.0	mA
I_{OH}	Output current (all bits high)	$V_{REF} = 2.000V$, $R_{16} = 1000\Omega$	3.8	3.996	4.2	3.8	3.996	4.2	mA
I_{OL}	Output current (all bits low)	$T_A = 25°C$		0	2.0		0	4.0	μA
V_O	Output voltage compliance	$T_A = 25°C$			-2.5 +0.2			-2.5 +0.2	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20			20		mA/μs
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0			2.0		μs
PSRR(−)	Output current power supply sensitivity			0.003	0.01		0.003	0.02	%/%
C_O	Output capacitance	$V_O = 0$		25			25		pF
C_I	Digital input capacitance (all bits high)			4.0			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			-11.4	+18 -20		-11.4	+18 -20	mA
V_{CC} V_{EE}	Power supply voltage range	$T_A = 25°C$	+4.75 -14.25	+5.0 -15	+5.25 -15.75	+4.75 -14.25	+5.0 -15	+5.25 -15.75	V_{DC}
	Power consumption (all bits low) (all bits high)			220 200	380		220 200	380	mW



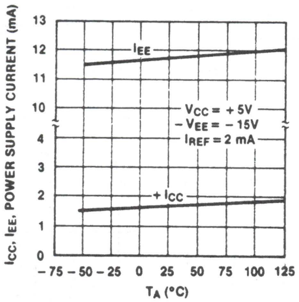
OP19630S

Figure 1. Output Current vs Output Compliance Voltage



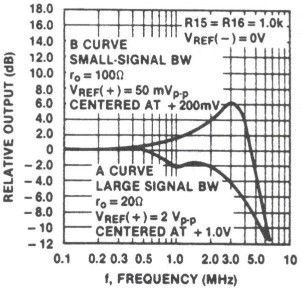
OP19640S

Figure 2. Maximum Output Compliance Voltage vs Temperature



OP19650S

Figure 3. Power Supply Current vs Temperature



OP19660S

Figure 4. Reference Amplifier Frequency Response

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

CIRCUIT DESCRIPTION

The MC3410 consists of four segment current sources which generate the two most significant bits (MSBs), and an R-2R DAC implemented with ion-implanted resistors for scaling the remaining eight least significant bits (LSBs) (See Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R-2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor R_{16} (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R_{16} should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R_{16} to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R_{16} should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R_{16} and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R_{16} increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R_{16} = 1.0kΩ, and settling time is ≈ 10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

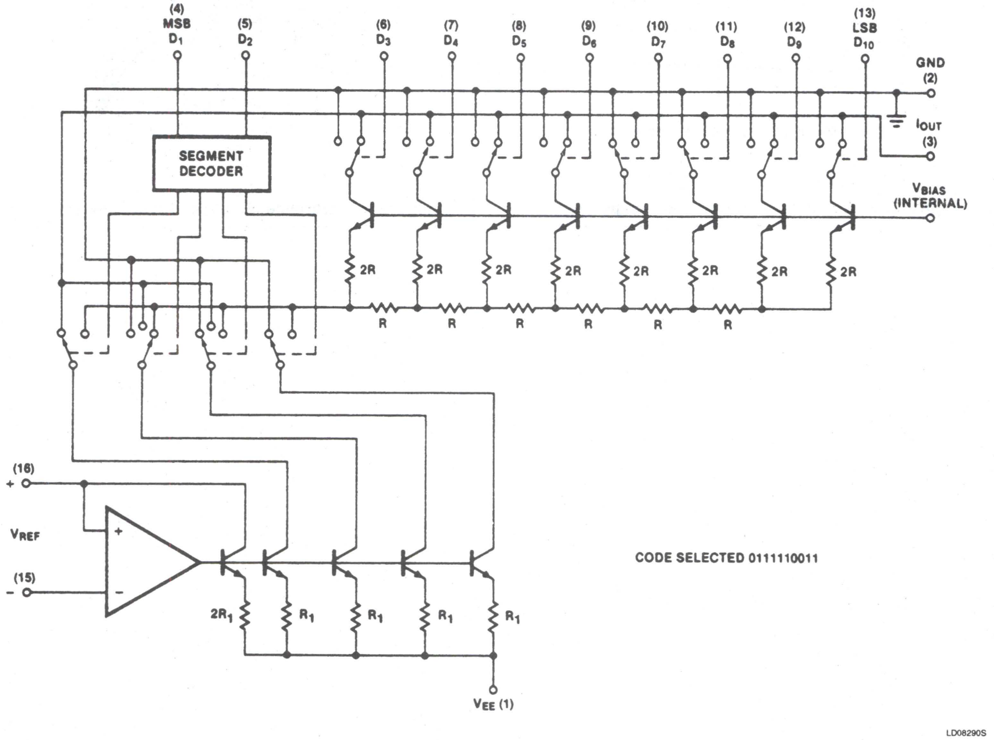
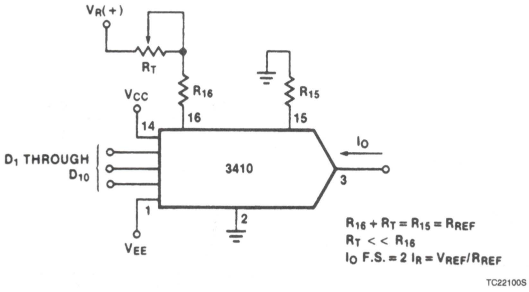
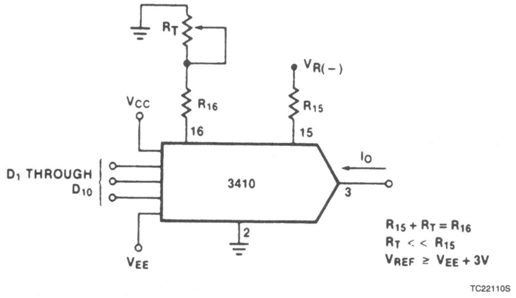


Figure 5. MC3410 Equivalent Circuit



a. Positive Reference Voltage



b. Negative Reference Voltage

Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +0.2V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full-scale current drift with temperature.

The MC3510 and the MC3410 are accurate to within ±0.05% at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The MC3410, MC3510 and MC3410C are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ± ½ LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (< 0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to −2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

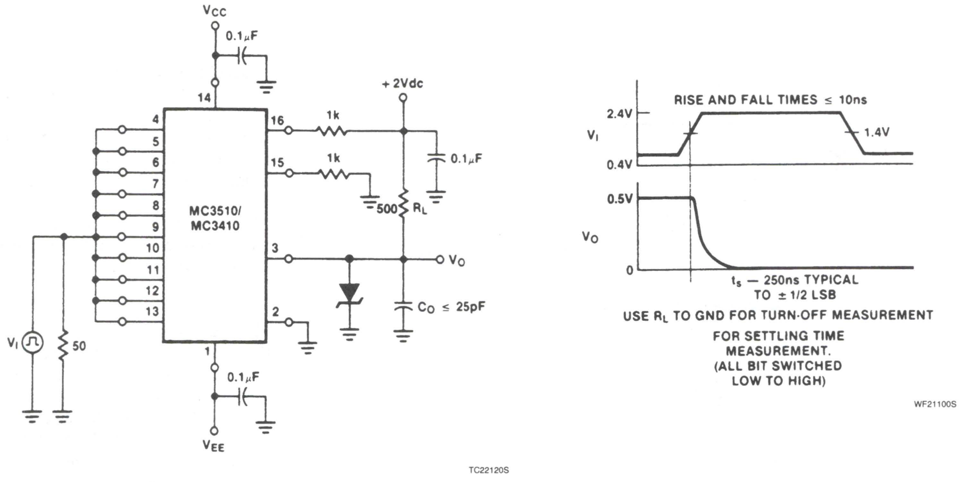

VCC
0.1μF
14
+2Vdc
16
1k
15
1k
0.1μF
500
RL
MC3510/
MC3410
4
5
6
7
8
9
10
11
12
13
3
VO
2
CO ≤ 25pF
VI
50
1
0.1μF
VEE
TC22120S
RISE AND FALL TIMES ≤ 10ns
2.4V
VI
1.4V
0.4V
0.5V
VO
0
ts — 250ns TYPICAL
TO ± 1/2 LSB
USE RL TO GND FOR TURN-OFF MEASUREMENT
FOR SETTLING TIME
MEASUREMENT.
(ALL BIT SWITCHED
LOW TO HIGH)
WF21100S

Figure 7. Settling Time

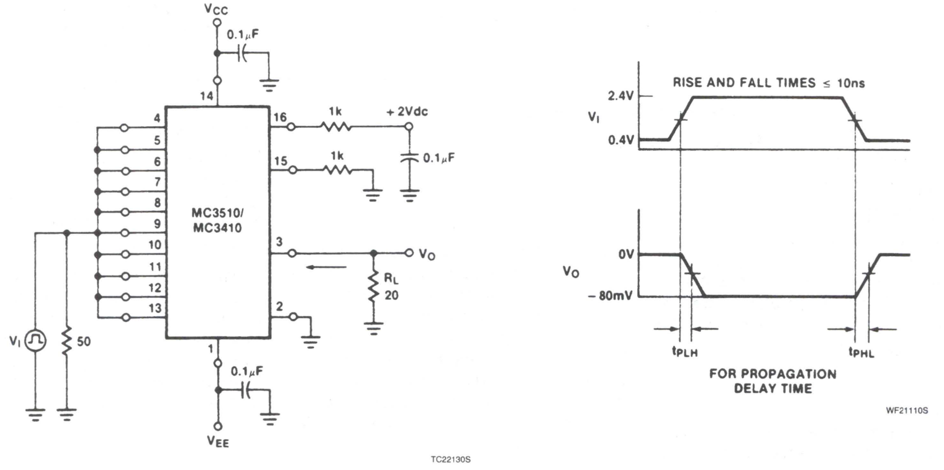

VCC
0.1μF
14
16
1k
+2Vdc
15
1k
0.1μF
MC3510/
MC3410
4
5
6
7
8
9
10
11
12
13
3
VO
RL
20
2
VI
50
1
0.1μF
VEE
TC22130S
RISE AND FALL TIMES ≤ 10ns
2.4V
VI
0.4V
0V
VO
−80mV
tPLH
tPHL
FOR PROPAGATION
DELAY TIME
WF21110S

Figure 8. Propagation Delay Time

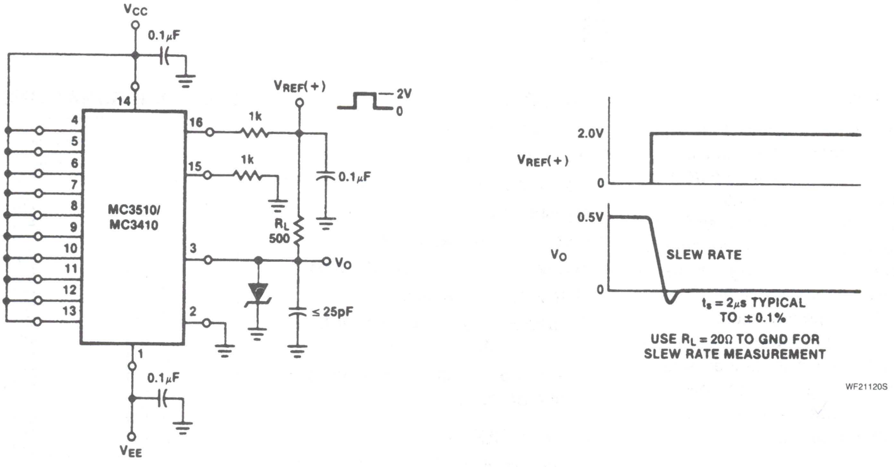
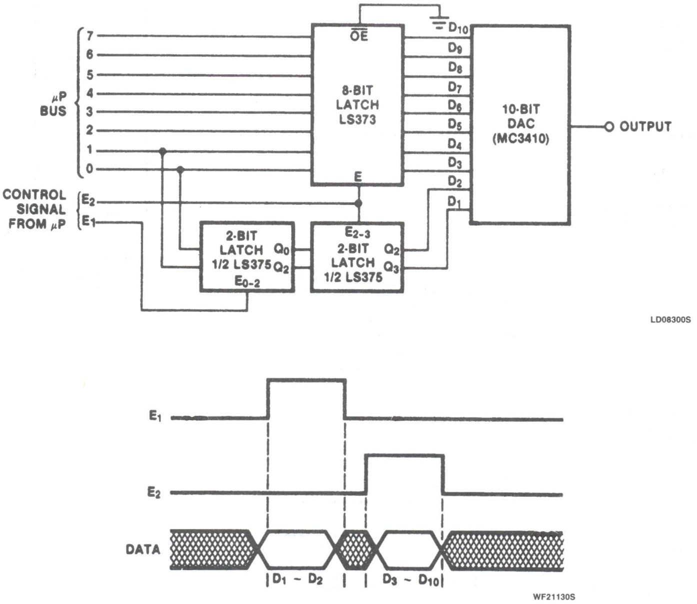

V_{CC}
0.1µF
14
4
5
6
7
8
9
10
11
12
13
MC3510/ MC3410
16
15
3
2
1
1k
1k
$V_{REF}(+)$
2V
0
0.1µF
R_L 500
V_O
≤ 25pF
0.1µF
V_{EE}
TC22140S
2.0V
0
0.5V
0
$V_{REF}(+)$
V_O
SLEW RATE
$t_s = 2\mu s$ TYPICAL TO ±0.1%
USE $R_L = 20\Omega$ TO GND FOR SLEW RATE MEASUREMENT
WF21120S

Figure 9. Reference Amplifier Settling Time and Slew Rate

TYPICAL APPLICATIONS


µP BUS
7
6
5
4
3
2
1
0
CONTROL SIGNAL FROM µP
E_2
E_1
$\overline{OE}$
8-BIT LATCH LS373
E
D_{10}
D_9
D_8
D_7
D_6
D_5
D_4
D_3
D_2
D_1
10-BIT DAC (MC3410)
OUTPUT
2-BIT LATCH 1/2 LS375
Q_0
Q_2
E_{0-2}
E_{2-3}
2-BIT LATCH 1/2 LS375
Q_2
Q_3
LD08300S
E_1
E_2
DATA
$D_1 \sim D_2$
$D_3 \sim D_{10}$
WF21130S

THE VALID DATA WILL BE LATCHED TO THE DAC UNTIL UPDATED WITH E_2 PULSE.
TIMING WILL DEPEND ON THE PROCESSOR USED.

Figure 10. Interfacing 10-Bit DAC With 8-Bit Microprocessor

Signetics

NE/SE5018

8-Bit μP-Compatible D/A Converter

Product Specification

Linear Products

DESCRIPTION

The NE5018 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches which are controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{\text{LE}}$ input is in the low state. When $\overline{\text{LE}}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{\text{LE}}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

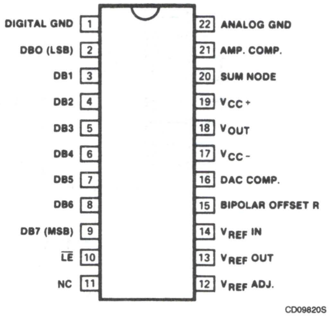
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± ½ LSB (0.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μPs**

APPLICATIONS

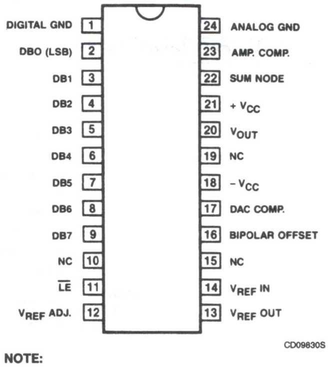
- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog – digital multiplication**

PIN CONFIGURATIONS

F, N Packages

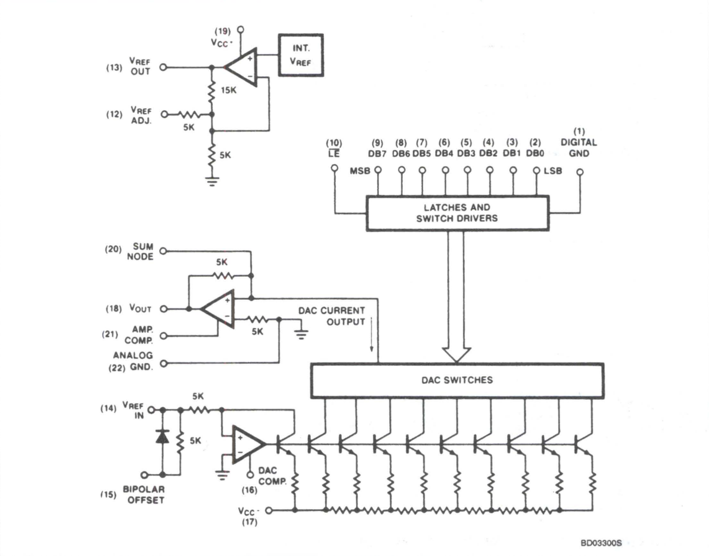

DIGITAL GND 1
DBO (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{\text{LE}}$ 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 $V_{CC}+$
18 V_{OUT}
17 $V_{CC}-$
16 DAC COMP.
15 BIPOLAR OFFSET R
14 V_{REF} IN
13 V_{REF} OUT
12 V_{REF} ADJ.
CD09820S

D Package[1]


DIGITAL GND 1
DBO (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 9
NC 10
$\overline{\text{LE}}$ 11
V_{REF} ADJ. 12
24 ANALOG GND
23 AMP. COMP.
22 SUM NODE
21 $+V_{CC}$
20 V_{OUT}
19 NC
18 $-V_{CC}$
17 DAC COMP.
16 BIPOLAR OFFSET
15 NC
14 V_{REF} IN
13 V_{REF} OUT
CD09830S

NOTE:
1. SOL and non-standard pinout.

BLOCK DIAGRAM


(19) $V_{CC}-$
INT. V_{REF}
(13) V_{REF} OUT
15K
(12) V_{REF} ADJ.
5K
5K
(10) $\overline{\text{LE}}$
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
(1) DIGITAL GND
MSB
LSB
LATCHES AND SWITCH DRIVERS
(20) SUM NODE
5K
(18) V_{OUT}
5K
DAC CURRENT OUTPUT
(21) AMP. COMP.
ANALOG (22) GND.
DAC SWITCHES
5K
(14) V_{REF} IN
5K
DAC COMP. (16)
(15) BIPOLAR OFFSET
$V_{CC}-$ (17)
BD03300S

8-Bit µP-Compatible D/A Converter

NE/SE5018

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Cerdip	0 to +70°C	NE5018F
22-Pin Cerdip	−55°C to +125°C	SE5018F
22-Pin Plastic DIP	0 to +70°C	NE5018N
22-Pin Plastic DIP	−55°C to +125°C	SE5018N
24-Pin SO Package	0 to +70°C	NE5018D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 1740 2190 1600	 mW mW mW
T_A	Operating temperature range SE5018 NE5018	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.
   D package at 12.8mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC}+$ = +15V, $V_{CC}-$ = −15V, SE5018. −55°C ≤ T_A ≤ 125°C, NE5018. 0°C ≤ T_A ≤ 70°C, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, 2V < V_{IN} < 18V		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, −5V < V_{IN} < 0.8V		−2.0	−10		−2.0	−10	μA
V_{FS}	Full-scale output	Unipolar mode, V_{REF} = 5.000V, all bits high, T_A = 25°C	9.50		10.5	9.50		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, V_{REF} = 5.000V all bits high, T_A = 25°C	4.75		5.25	4.75		5.25	V
$-V_{FS}$	Negative full scale	Bipolar mode, V_{REF} = 5.000V, all bits low, T_A = 25°C	−5.25		−4.75	−5.25		−4.75	V
V_{ZS}	Zero-scale Output	Unipolar mode, V_{REF} = 5.000V all bits low, T_A = 25°C	−30		+30	−30		+30	mV
I_{OS}	Output short circuit current	T_A = 25°C V_{OUT} = 0V		15	40		15	40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V− = −15V, 13.5V ≤ V+ ≤ 16.5V, external $V_{REF\ IN}$ = 5.000V		0.001	0.01		0.001	0.01	%FS %VS
$PSR-_{(OUT)}$	Output power supply rejection (−)	V+ = −15V, −13.5V ≤ V− ≤ −16.5V, external $V_{REF\ IN}$ = 5.000V		0.001	0.01		0.001	0.01	%FS %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN}$ = 5.000V		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C
I_{REF}	Reference output current				3			3	mA
I_{REFSC}	Reference short circuit current	T_A = 25°C[8] $V_{REF\ OUT}$ = 0V		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	V− = −15V, 13.5V ≤ V+ ≤ 16.5V, I_{REF} = 1.0mA		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	V+ = −15V, −13.5V ≤ V− ≤ 16.5V,		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	I_{REF} = 1.0mA T_A = 25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	I_{REF} = 1.0mA		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF} = 1.0mA, T_A = 25°C	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+$ = 15V		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}-$ = −15V		−10	−15		−10	−15	mA
P_D	Power dissipation	I_{REF} = 1.0mA, V_{CC} = ±15V		255	435		255	435	mW

NOTE:

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[1] $V_{CC} = \pm 15V$, $T_A = 25°C$.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5018			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits low-to-high[2]		1.8		μs
t_{SHL}	Settling time	± ½ LSB	Input	All bits high-to-low[3]		2.3		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2, 3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Setup time	$\overline{LE}$	Input	[1, 6]	100			ns
t_H	Hold time	Input	$\overline{LE}$	[1, 6]	50			ns
t_{PW}	Latch enable pulse width			[1, 6]	150			ns

NOTES:

1. Refer to Figure 3.
2. See Figure 6.
3. See Figure 7.
4. See Figure 8.
5. See Figure 9.
6. See Figure 10.
7. For reference currents > 3mA, use of an external buffer is required.

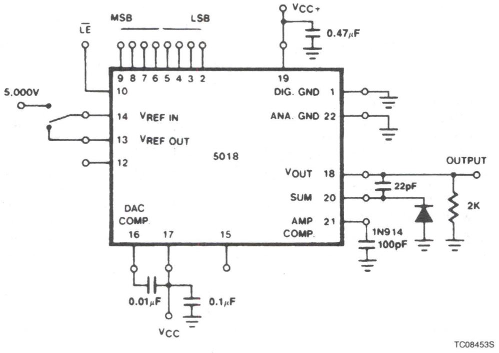

LE
MSB
LSB
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
5.000V
14 VREF IN
ANA. GND 22
13 VREF OUT
12
5018
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP
16 17 15
AMP COMP. 21
1N914
100pF
0.01µF
0.1µF
VCC
TC08453S

Figure 2. DC Parametric Test Configuration

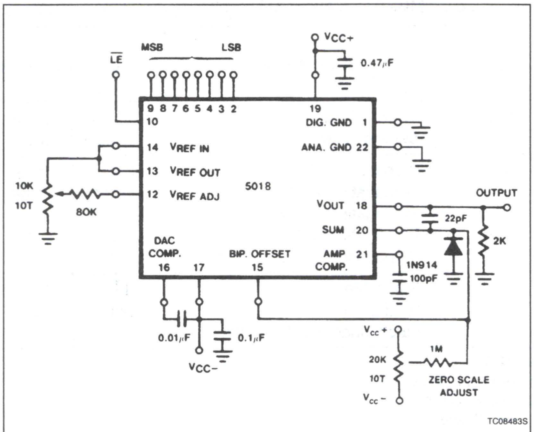

LE
MSB
LSB
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
80K
12 VREF ADJ
5018
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP.
16 17
BIP. OFFSET 15
AMP COMP. 21
1N914
100pF
0.01µF
0.1µF
VCC−
Vcc +
1M
20K
10T
ZERO SCALE ADJUST
Vcc −
TC08483S

Figure 5. Bipolar Output Operation (−5 to +5V)

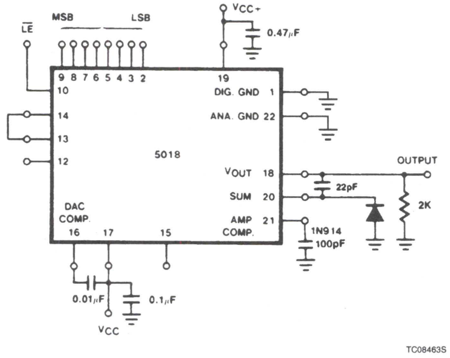

LE
MSB
LSB
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14
ANA. GND 22
13
12
5018
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP.
16 17 15
AMP COMP. 21
1N914
100pF
0.01µF
0.1µF
VCC
TC08463S

Figure 3. AC Parametric Test Configuration

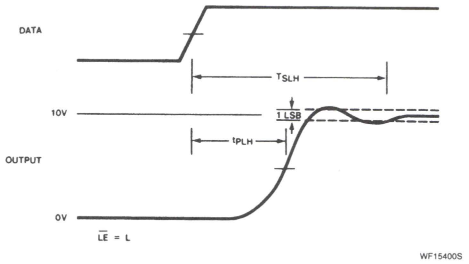


Figure 6. Settling Time and Propagation Delay, Low-to-High Data

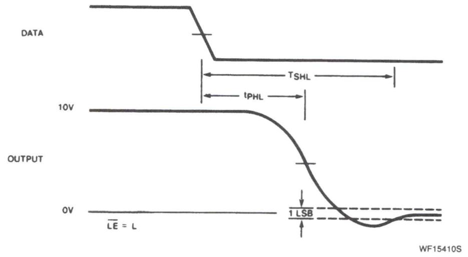


Figure 7. Settling Time And Propagation Delay, High-to-Low Data

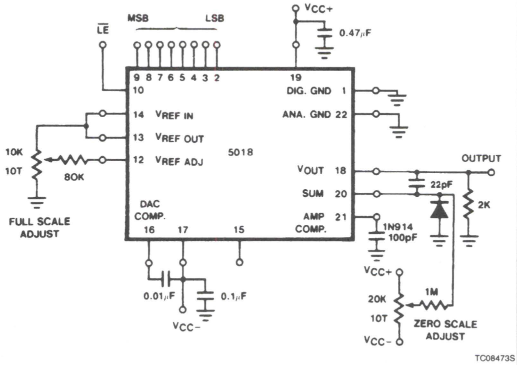

LE
MSB
LSB
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
80K
12 VREF ADJ
5018
FULL SCALE ADJUST
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP.
16 17 15
AMP COMP. 21
1N914
100pF
0.01µF
0.1µF
VCC−
VCC+
1M
20K
10T
ZERO SCALE ADJUST
VCC−
TC08473S

Figure 4. Full-/Zero-Scale Adjust — Unipolar Output (0 – 10V)

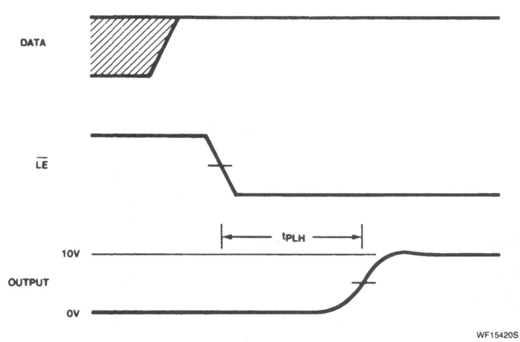

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V
WF15420S

Figure 8. Propagation Delay, Latch Enable to Output

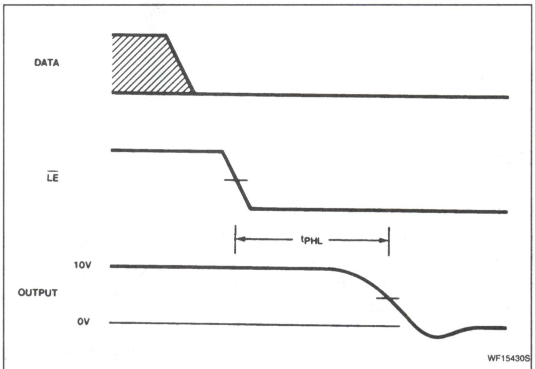

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V
WF15430S

Figure 9. Propagation Delay, Latch Enable to Output

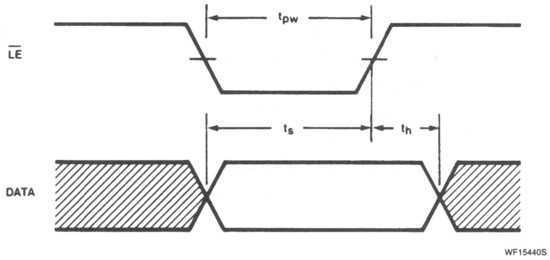

t_{pw}
$\overline{LE}$
t_s
t_h
DATA
WF15440S

Figure 10. Latch Enable Pulse Width, Setup And Hold Times

Signetics

NE/SE5019
8-Bit µP-Compatible D/A Converter

Product Specification

Linear Products

DESCRIPTION

The NE5019 is a complete 8-bit digital-to-analog converter sub-system on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale, while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

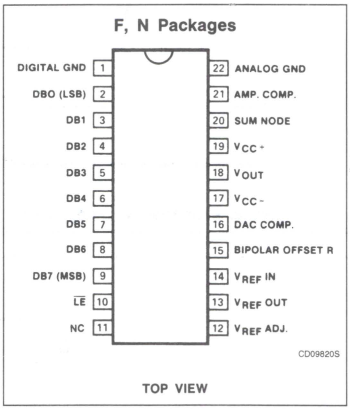
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± ¼ LSB (0.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other µPs**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog – digital multiplication**

PIN CONFIGURATION

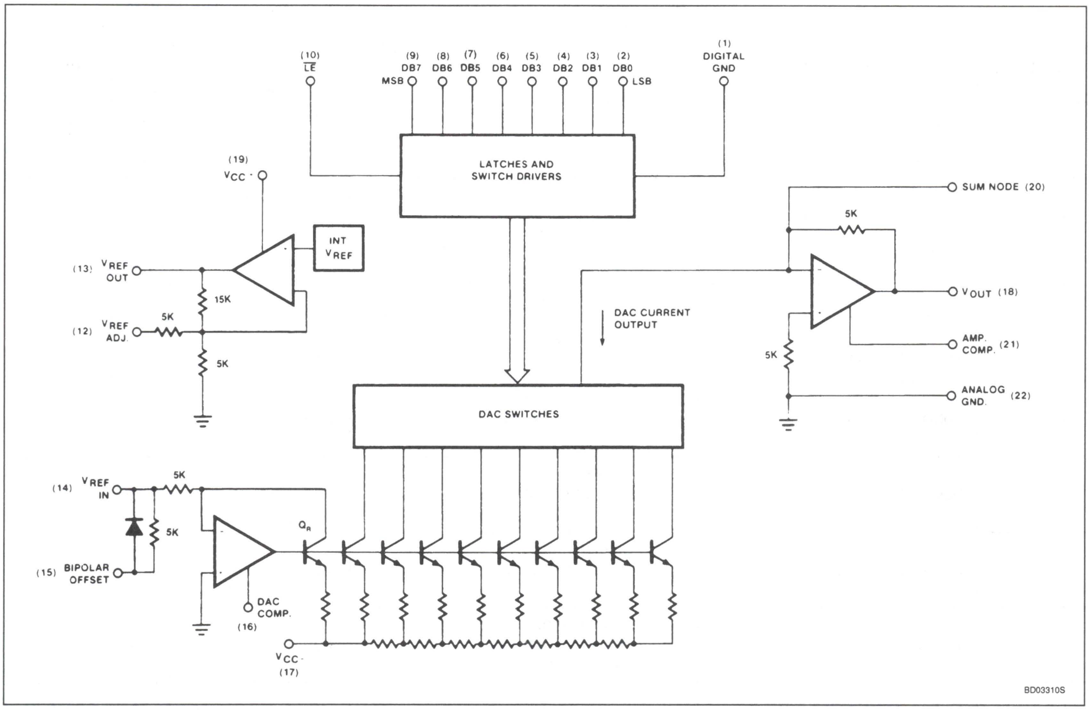

F, N Packages
DIGITAL GND 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{LE}$ 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 V_{CC+}
18 V_{OUT}
17 V_{CC-}
16 DAC COMP.
15 BIPOLAR OFFSET R
14 V_{REF} IN
13 V_{REF} OUT
12 V_{REF} ADJ.
CD09820S
TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Cerdip	−55°C to +125°C	SE5019F
22-Pin Cerdip	0 to +70°C	NE5019F
22-Pin Plastic DIP	0 to +70°C	NE5019N

8-Bit µP-Compatible D/A Converter NE/SE5019

BLOCK DIAGRAM


(10) LE
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(1) DIGITAL GND
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT VREF
(13) VREF OUT
15K
5K
(12) VREF ADJ.
5K
SUM NODE (20)
5K
VOUT (18)
DAC CURRENT OUTPUT
5K
AMP. COMP. (21)
ANALOG GND. (22)
DAC SWITCHES
(14) VREF IN
5K
5K
(15) BIPOLAR OFFSET
QR
DAC COMP. (16)
VCC- (17)
BD03310S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	-18	V
V_I	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	mA
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] F package N package	 1740 2190	 mW mW
T_A	Operating temperature range SE5019 NE5019	 -55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE:

1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leqslant T_A \leqslant 125°C$, NE5019. $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	9.5		10.5	9.5		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	4.75		5.25	4.75		5.25	V
$-V_{FS}$	Negative full-scale	Bipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−5.25		−4.75	−5.25		−4.75	V
V_{ZS}	Zero-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−30		+30	−30		+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leqslant V- \leqslant -16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/%VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C

NOTE:

Refer to Figure 1.

DC ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leqslant T_A \leqslant 125°C$, NE5019. $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leqslant V- \leqslant 16.5V$		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE:
Refer to Figure 1.

AC ELECTRICAL CHARACTERISTICS[1]

$V_{CC} = \pm 15V$, $T_A = 25°C^2$.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5019			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits low-to-high^2		1.8		μs
t_{SHL}	Settling time	± ½ LSB	Input	All bits high-to-low^3		2.3		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high^2		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low^3		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change$^{2,\ 3}$		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition^4		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition^5		150		ns
t_S	Setup time	$\overline{LE}$	Input	1, 6	100			ns
t_H	Hold time	Input	$\overline{LE}$	1, 6	50			ns
t_{PW}	Latch enable pulse width			1, 6	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. For reference current > 3mA, use of an external buffer is required.

8-Bit μP-Compatible D/A Converter NE/SE5019

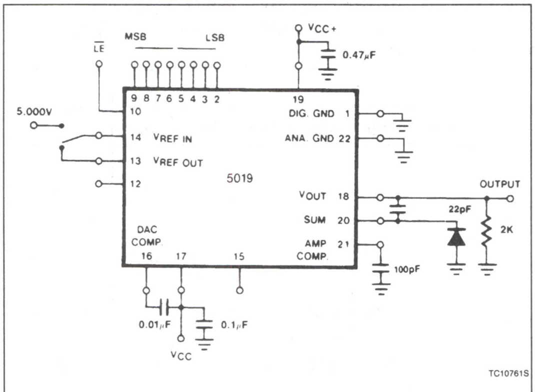

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
5.000V
14 VREF IN
13 VREF OUT
12
5019
VOUT 18
SUM 20
AMP 21
COMP.
DAC
COMP.
16
17
15
OUTPUT
22pF
2K
100pF
0.01µF
0.1µF
VCC
TC10761S

Figure 1. DC Parametric Test Configuration

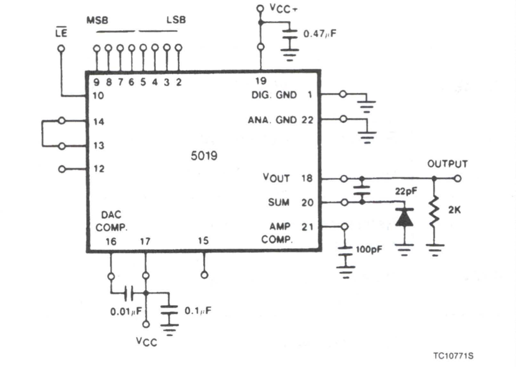

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
14
13
12
5019
VOUT 18
SUM 20
AMP 21
COMP.
DAC
COMP.
16
17
15
OUTPUT
22pF
2K
100pF
0.01µF
0.1µF
VCC
TC10771S

Figure 2. AC Parametric Test Configuration

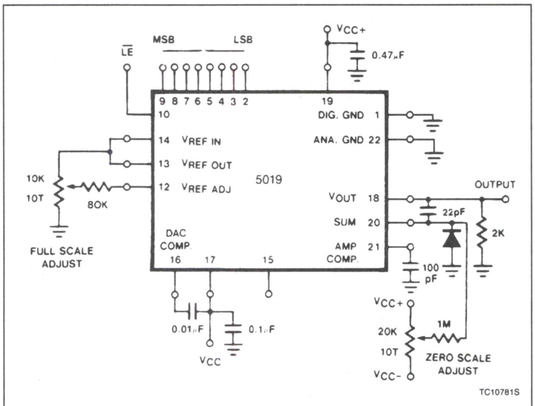

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
14 VREF IN
13 VREF OUT
12 VREF ADJ
5019
10K
10T
80K
FULL SCALE ADJUST
VOUT 18
SUM 20
AMP 21
COMP.
DAC
COMP.
16
17
15
OUTPUT
22pF
2K
100 pF
0.01µF
0.1µF
VCC
VCC+
20K
10T
VCC−
1M
ZERO SCALE ADJUST
TC10781S

Figure 3. Full-/Zero-Scale Adjust-Unipolar Output (0 – 10V)

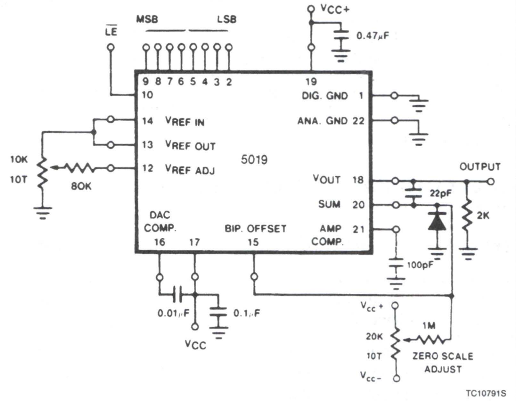

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
14 VREF IN
13 VREF OUT
12 VREF ADJ
5019
10K
10T
80K
VOUT 18
SUM 20
AMP 21
COMP.
DAC
COMP.
BIP. OFFSET
16
17
15
OUTPUT
22pF
2K
100pF
0.01µF
0.1µF
VCC
Vcc+
20K
10T
Vcc−
1M
ZERO SCALE ADJUST
TC10791S

Figure 4. Bipolar Output Operation (−5 to +5V)

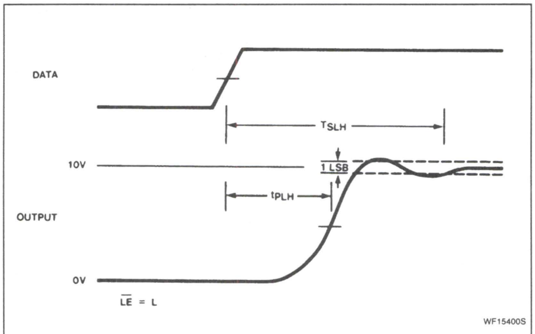


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

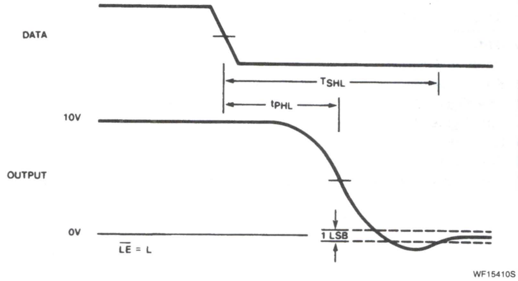


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

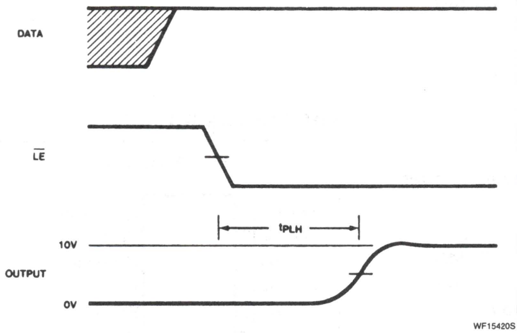

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V
WF15420S

Figure 7. Propagation Delay, Latch Enable to Output

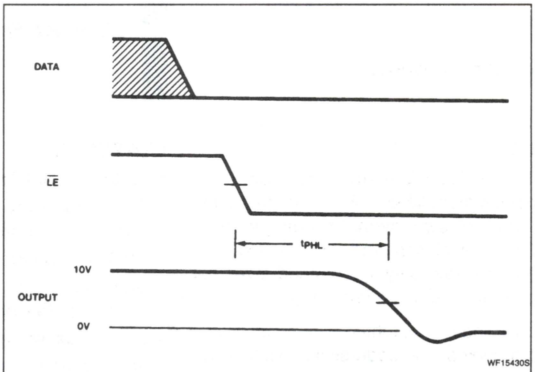

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V
WF15430S

Figure 8. Propagation Delay, Latch Enable to Output

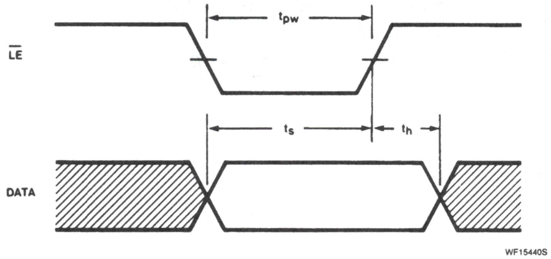

$\overline{LE}$
t_{pw}
t_s
t_h
DATA
WF15440S

Figure 9. Latch Enable Pulse Width, Setup and Hold Times

Signetics

NE5020

10-Bit µP-Compatible D/A Converter

Product Specification

Linear Products

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital-to-analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds, and addressing capability allow the NE5020 to directly interface with most microprocessor- and logic-controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

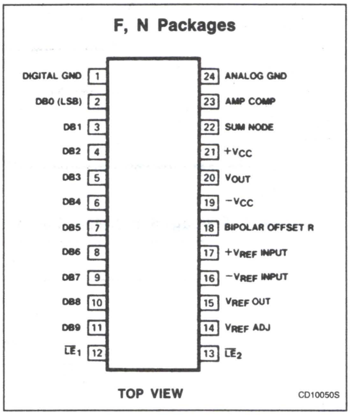
FEATURES

- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and bipolar (±5V) output range**
- **Logic bus compatible**
- **5µs settling time**

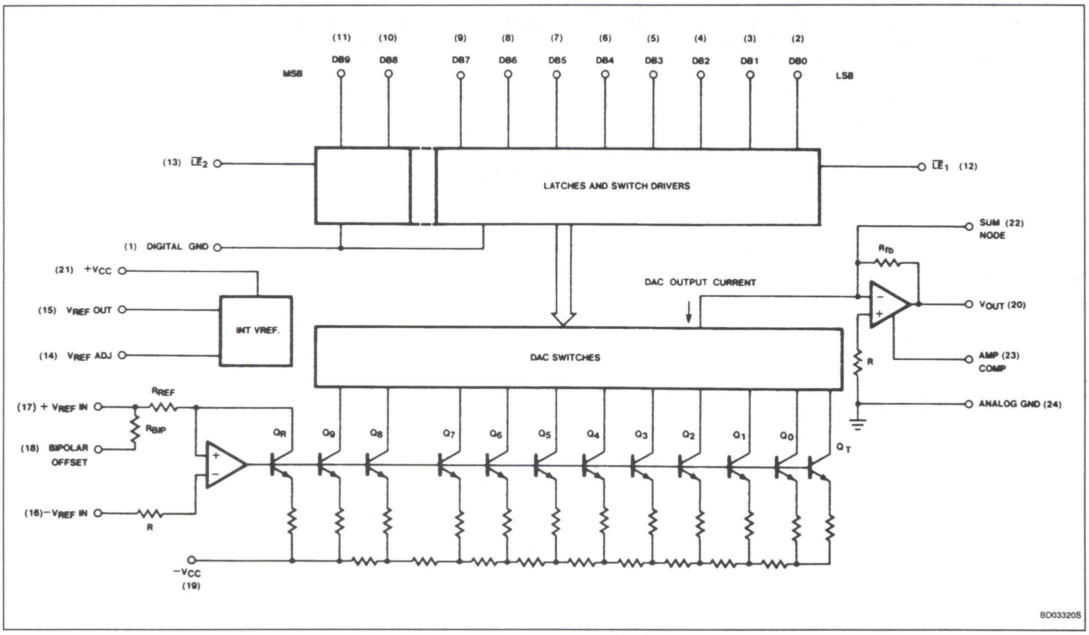
APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit analog-to-digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

PIN CONFIGURATION


F, N Packages
DIGITAL GND 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 9
DB8 10
DB9 11
LE1 12
24 ANALOG GND
23 AMP COMP
22 SUM NODE
21 +VCC
20 VOUT
19 −VCC
18 BIPOLAR OFFSET R
17 +VREF INPUT
16 −VREF INPUT
15 VREF OUT
14 VREF ADJ
13 LE2
TOP VIEW
CD10050S

BLOCK DIAGRAM


(11) DB9
(10) DB8
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(13) LE2
LE1 (12)
LATCHES AND SWITCH DRIVERS
(1) DIGITAL GND
(21) +VCC
(15) VREF OUT
(14) VREF ADJ
INT VREF.
DAC SWITCHES
DAC OUTPUT CURRENT
SUM (22) NODE
Rfb
VOUT (20)
AMP (23) COMP
R
ANALOG GND (24)
(17) + VREF IN
RREF
RBIP
(18) BIPOLAR OFFSET
(16)−VREF IN
R
QR
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
QT
−VCC (19)
BD03320S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Cerdip	0 to 70°C	NE5020F
24-Pin Plastic DIP	0 t0 70°C	NE5020N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at $+V_{REF}$ input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation $T_A = 25°C$, (still-air)[1] F package N package	 2150 2150	 mW mW
T_A	Operating temperature range NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 17.2mW/°C.
   N package at 17.2mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0 \leqslant T_A \leqslant 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution Monotonicity Relative accuracy				10 10 ±0.1	Bits Bits %FS
$V_{CC}+$ $V_{CC}-$	Positive supply voltage Negative supply voltage		11.4 −11.4	15 −15	16.5 −16.5	V V
$V_{IN(1)}$ $V_{IN(0)}$	Logic "1" input voltage Logic "0" input voltage	Pin 1 = 0V Pin 1 = 0V	2.0		 0.8	V V
$I_{IN(1)}$ $I_{IN(0)}$	Logic "1" input current Logic "0" input current	Pin 1 = 0V, $2 < V_{IN} < 18V$ Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		0.1 −2.0	10 −10	µA µA
V_{FS}	Full-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	9.5		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	4.75		5.25	V
$-V_{FS}$	Negative full-scale	Bipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−5.25		−4.75	V

NOTE:

1. Refer to Figure 1.

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0 \leqslant T_A \leqslant 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{ZS}	Zero-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−30		+30	mV
I_{OS}	Output short-circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		±15	±40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01	%FS/ %VS
$PSR-_{(OUT)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leqslant V- \leqslant -16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01	%FS/ %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20		ppmFS /°C
TC_{ZS}	Zero-scale temperature coefficient			5		ppmFS /°C
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$, $I_{REF} = 1.0mA$		.003	.01	%VR/ %VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leqslant V- \leqslant 16.5V$,		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	$I_{REF} = 1.0mA$		5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435	mW

NOTE:

1. Refer to Figure 1.
2. For $I_{REF\ OUT}$ greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[1] $V_{CC} = \pm 15V$, $T_A = 25°C$.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	±½ LSB	Input	All bits low-to-high[2]		5		μs
t_{SHL}	Settling time	±½ LSB	Input	All bits high-to-low[3]		5		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		30		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2,3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Set-up time	$\overline{LE}$	Input	[1,6]	100			ns
t_H	Hold time	Input	$\overline{LE}$	[1,6]	50			ns
t_{PW}	Latch enable pulse width			[1,6]	150			ns

NOTES:

1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.

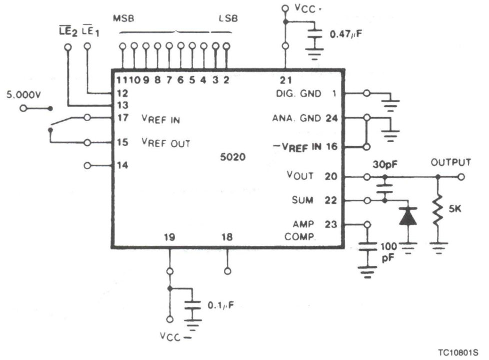

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
5.000V
11 10 9 8 7 6 5 4 3 2
21
12
13
17 VREF IN
15 VREF OUT
14
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP 23
19
18
30pF
OUTPUT
5K
100 pF
0.1μF
VCC−
TC10801S

Figure 1. DC Parametric Test Configuration

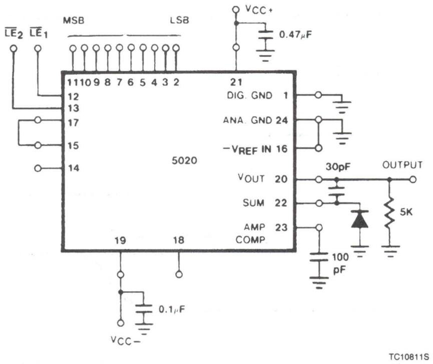

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
11 10 9 8 7 6 5 4 3 2
21
12
13
17
15
14
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP 23
19
18
30pF
OUTPUT
5K
100 pF
0.1μF
VCC−
TC10811S

Figure 2. AC Parametric Test Configuration

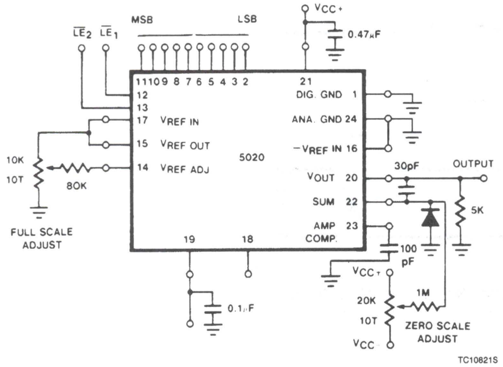

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
11 10 9 8 7 6 5 4 3 2
21
12
13
17 VREF IN
15 VREF OUT
14 VREF ADJ
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP 23
19
18
10K
10T
80K
FULL SCALE ADJUST
30pF
OUTPUT
5K
100 pF
0.1μF
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−
TC10821S

Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0 – 10V)

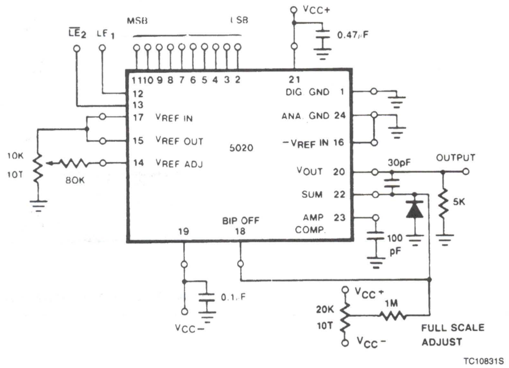

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
11 10 9 8 7 6 5 4 3 2
21
12
13
17 VREF IN
15 VREF OUT
14 VREF ADJ
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP 23
19
BIP OFF 18
10K
10T
80K
30pF
OUTPUT
5K
100 pF
0.1μF
VCC−
VCC+
20K
10T
1M
VCC−
FULL SCALE ADJUST
TC10831S

Figure 4. Bipolar Output Operation (–5 to +5V)

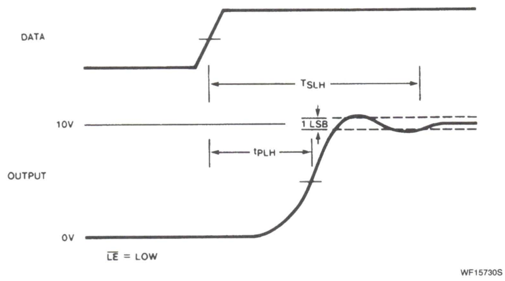

DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
$\overline{LE}$ = LOW
WF15730S

Figure 5. Settling Time and Propagation Delay, Low-to-High Data

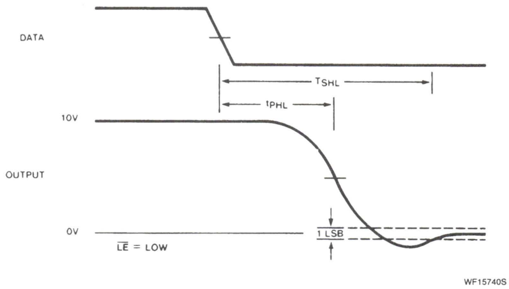

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
$\overline{LE}$ = LOW
WF15740S

Figure 6. Settling Time and Propagation Delay, High-to-Low Data

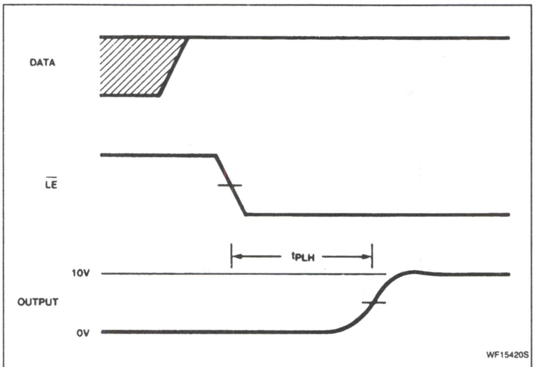

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V
WF15420S

Figure 7. Propagation Delay, Latch Enable to Output

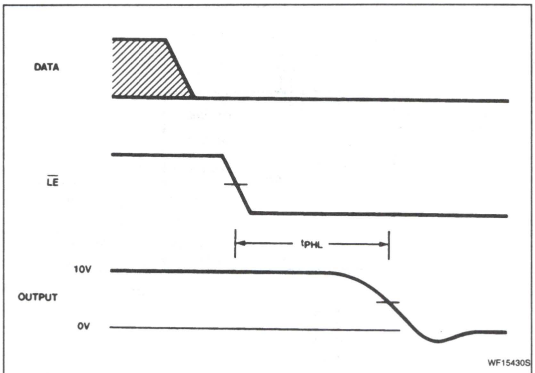

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V
WF15430S

Figure 8. Propagation Delay, Latch Enable to Output

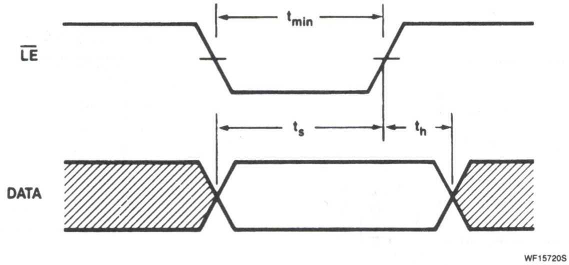

t_{min}
$\overline{LE}$
t_s
t_h
DATA
WF15720S

Figure 9. Latch Enable Pulse Width, Setup and Hold Times

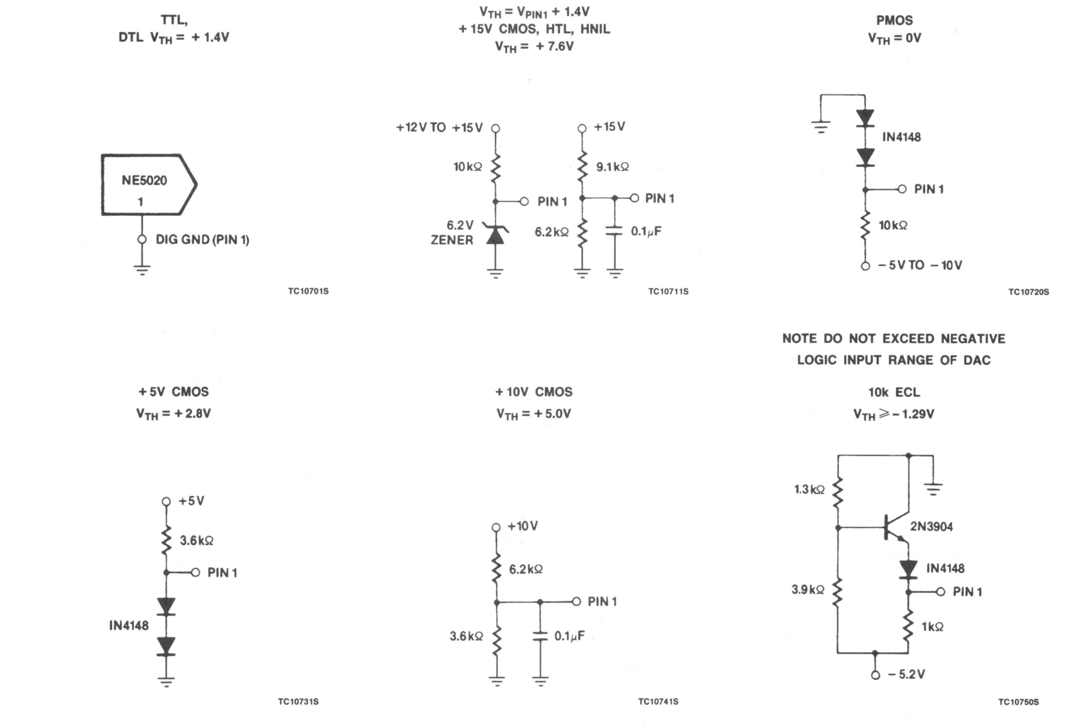

TTL,
DTL V_{TH} = +1.4V
NE5020
1
DIG GND (PIN 1)
TC10701S
$V_{TH} = V_{PIN1}$ + 1.4V
+15V CMOS, HTL, HNIL
V_{TH} = +7.6V
+12V TO +15V
10kΩ
PIN 1
6.2V
ZENER
+15V
9.1kΩ
PIN 1
6.2kΩ
0.1μF
TC10711S
PMOS
V_{TH} = 0V
IN4148
PIN 1
10kΩ
−5V TO −10V
TC10720S
NOTE DO NOT EXCEED NEGATIVE
LOGIC INPUT RANGE OF DAC
+5V CMOS
V_{TH} = +2.8V
+5V
3.6kΩ
PIN 1
IN4148
TC10731S
+10V CMOS
V_{TH} = +5.0V
+10V
6.2kΩ
PIN 1
3.6kΩ
0.1μF
TC10741S
10k ECL
$V_{TH} \geqslant -1.29$V
1.3kΩ
2N3904
IN4148
PIN 1
3.9kΩ
1kΩ
−5.2V
TC10750S

Figure 10

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage in addition to the basic DAC components (see Block Diagram).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_ϕ). Both the latch enable ports ($\overline{LE}$) and the data inputs are static- and threshold-sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low static (Logic '0'), the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on

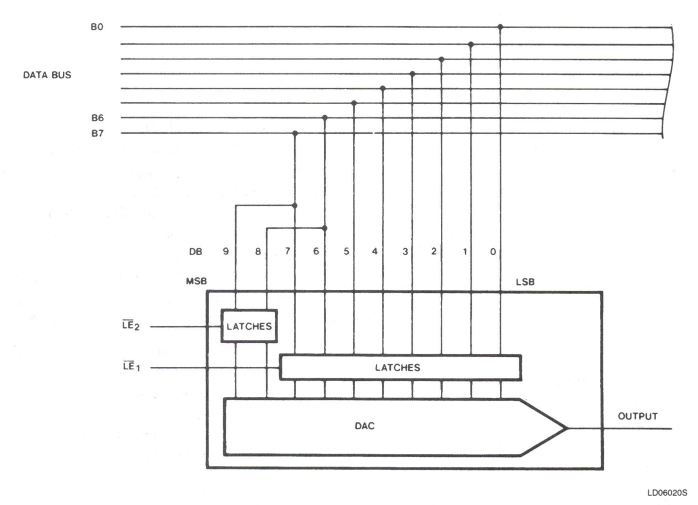

B0
DATA BUS
B6
B7
DB 9 8 7 6 5 4 3 2 1 0
MSB
LSB
$\overline{LE}_2$
LATCHES
$\overline{LE}_1$
LATCHES
DAC
OUTPUT
LD06020S

Figure 11. NE5020 μP Interface 8-Bit Data Bus Example

which $\overline{LE}$ goes high) 'memorizes' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (0.8V max) or $0.1\mu A$ for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). Figure 10 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus-oriented system, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 9 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50ns after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8-bit data bus (see Figure 11). Data for the two MSBs is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSBs of data are transferred into the DAC. With $\overline{LE}_1$ returning high, the loading of 10-bit data word from an 8-bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16-bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8-bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 12 shows the circuit configuration.

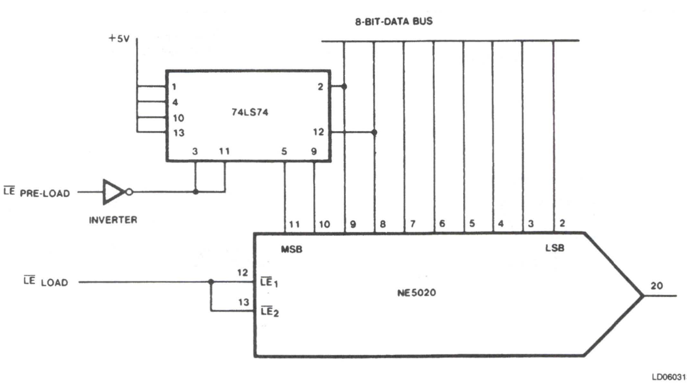


Figure 12. Preloading the 2 MSBs to Provide a Single-Step Output

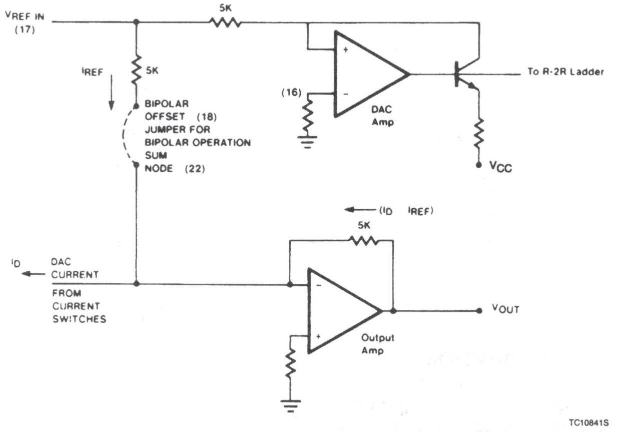


Figure 13. Bipolar Output

After preloading (via $\overline{LE}$ preload) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSBs and the two MSBs are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in Figure 15 performs not only V_{REF} adjustment, but also full-scale output adjust. Notice that the $V_{REF\ ADJ}$ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the $V_{REF\ ADJ}$ pin and observing good layout practices.

The $V_{REF\ OUT}$ node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier be used.

Input Amplifier

The DAC reference amplifier is a high gain internally-compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

The Block Diagram details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5V V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA, and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}}\left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024}\right).$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μs and source impedances at the $V_{REF\ INPUT}$ greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$. The $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on-chip output op amp to eliminate the need for additional external active circuits. Its two-stage design with feed-forward compensation allows it to slew at 15V/μs and settle to within ± ½LSB in 5μs. These times are typical when driving the rated loads of $R_L \geqslant 5k$ and $C_L \leqslant 50pF$ with recommended values of $C_{FF} = 1nF$ and $C_{FB} = 30pF$. Typical input offset voltages of 5mV and 50kΩ open-loop gain insure that an accurate current-to-voltage conversion is performed when using the on-chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ± 15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short-circuit and die temperature stabilization.

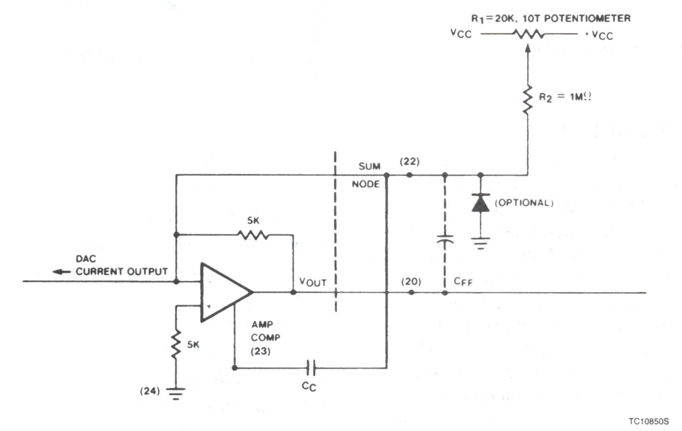


Figure 14. Zero-Scale Adjustment

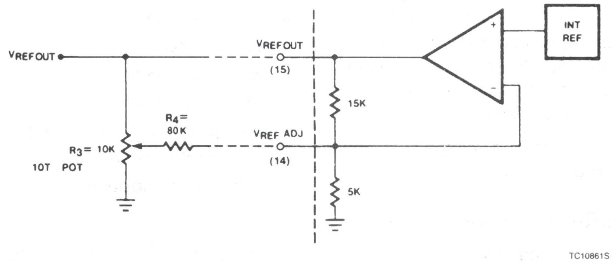


Figure 15. Reference Adjust Circuit

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5V to obtain −5V to +5V output voltage range operation. This is accomplished by shorting Pins 18 and 22 (see Figure 13). This connection produces a current equal to $(V_{REFIN} - _{SUM\ NODE}) \div R_{BIP}$ (1mA nominal), which is injected into the sum node. Since full-scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5kΩ = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum node and $V_{OUT} = -(5k\Omega)(1mA) = -5V$. Zero-scale adjust and full-scale adjust are performed as described below, noting that full-scale voltage is now approximately +5V. Zero-scale adjust may be used to trim $V_{OUT} = 0.00$ with the MSB high or $V_{OUT} = -5.0V$ with all bits off.

Zero-Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in Figure 14. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000V in the unipolar mode or −5.000V in the bipolar mode (see bipolar section) accomplishes this trim.

Full-Scale Adjustment

A recommended full-scale adjustment circuit, when using the internal voltage reference, is shown in Figure 15. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accuracy of full-scale is of low importance when compared to the other system accuracy factors this adjustment circuit is optional.

As resistors R_{REF}, R_{FB}, and R_{BIP} shown in the Block Diagram are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ± 0.3% which implies that typical full-scale (or gain) error is less than ± 0.3% of ideal full-scale value.

Signetics

Linear Products

NE/SE5118

8-Bit Microprocessor-Compatible D/A Converter — Current Output

Product Specification

DESCRIPTION

The NE5118 is a high-speed 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the Low state. When $\overline{LE}$ goes High, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes Low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance, increasing versatility.

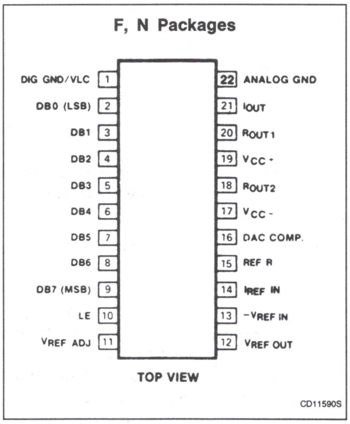
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Fast settling output current — 200ns
- Accurate to ± ½ LSB (0.19%)
- Monotonic to 8 bits
- Reference short-circuit protected
- Compatible with 8086, 6800 and many other microprocessors

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication
- CRT display drivers
- High-speed modems

PIN CONFIGURATION


F, N Packages
DIG GND/VLC 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
LE 10
VREF ADJ 11
22 ANALOG GND
21 IOUT
20 ROUT1
19 VCC+
18 ROUT2
17 VCC-
16 DAC COMP.
15 REF R
14 IREF IN
13 -VREF IN
12 VREF OUT
TOP VIEW
CD11590S

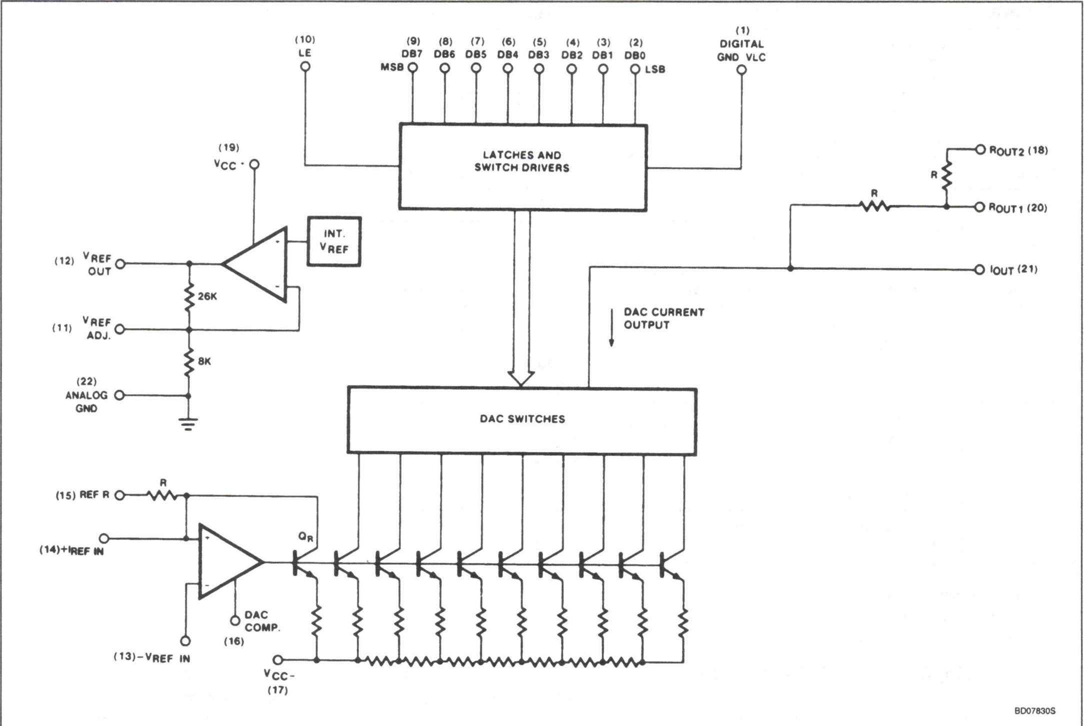
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Plastic DIP	0 to +70°C	NE5118N
22-Pin Ceramic DIP	0 to +70°C	NE5118F
22-Pin Ceramic DIP	-55°C to +125°C	SE5118F

8-Bit Microprocessor-Compatible D/A Converter — Current Output

NE/SE5118

BLOCK DIAGRAM


(10) LE
(9) DB7 MSB
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0 LSB
(1) DIGITAL GND VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
26K
(11) VREF ADJ.
8K
(22) ANALOG GND
ROUT2 (18)
R
R
ROUT1 (20)
IOUT (21)
DAC CURRENT OUTPUT
DAC SWITCHES
(15) REF R
R
(14)+IREF IN
QR
DAC COMP.
(16)
(13)−VREF IN
VCC−
(17)
BD07830S

NOTE:
All R values equal 5kΩ and are thermally matched.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at R_{REF} input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
$I_{REF\ IN}$	Reference input current (Pin 14)	3	mA
	Maximum power dissipation $T_A = 25°C$ (still-air)[1] F package N package	 1740 2190	 mW mW
T_A	Operating ambient temperature range SE5118 NE5118	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$; SE5118; $-55°C \leqslant T_A \leqslant 125°C$; NE5118; $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	µA
I_{FS}	Full-scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero-scale current		−6	1	+6	−6	1	+6	µA

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC}+ = +15V$, $V_{CC}- = -15V$; SE5118; $-55°C \leqslant T_A \leqslant 125°C$; NE5118; $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{REF}	Reference voltage	$I_{REF} = 1mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
$PSR+_{(OUT)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/ %VS
$PSR-_{(OUT)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leqslant V- \leqslant -16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/ %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$ (Pin 15)		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient	$I_{REF\ IN} = 1.00mA$ (Pin 14)		5			5		ppm/°C
I_{REF}	Reference output current	$T_A = 25°C$			3			3	mA
I_{REFSC}	Reference short circuit current[1]	$V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/ %VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V, -13.5V \leqslant V- \leqslant 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/ %VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF\ IN}$ input impedance			5.0			5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

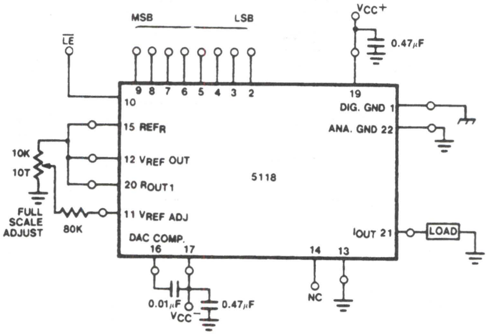
NOTES:

1. For reference currents > 3mA, use of an external buffer is required.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

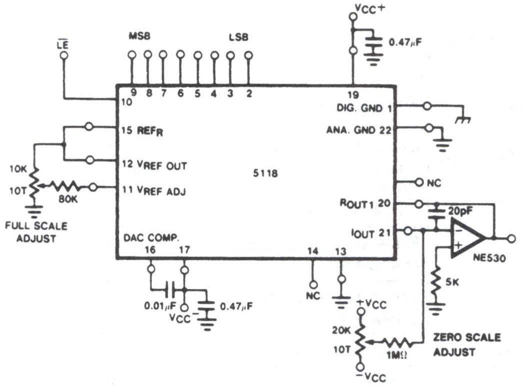
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5118			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-High		200		ns
t_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-Low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-High		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-Low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-High transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-Low transition		60		ns
t_S	Setup time	$\overline{LE}$	Input		100			ns
t_H	Hold time	Input	$\overline{LE}$		50			ns
t_{PW}	Latch enable pulse width				150			ns

TYPICAL APPLICATIONS


MSB
LSB
VCC+
0.47μF
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
20 ROUT1
11 VREF ADJ
5118
10K
10T
FULL SCALE ADJUST
80K
DAC COMP.
16 17
14 13
IOUT 21
LOAD
0.01μF
0.47μF
VCC−
NC

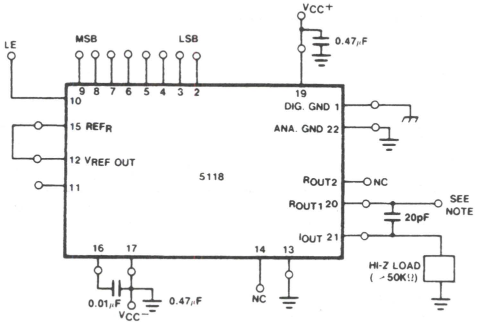
TC14680S

Bipolar Output Operation (−1mA to +1mA)


VCC+
0.47μF
MSB
LSB
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118
10K
10T
80K
FULL SCALE ADJUST
NC
ROUT1 20
20pF
IOUT 21
NE530
DAC COMP.
16 17
14 13
0.01μF
0.47μF
VCC
NC
5K
+VCC
20K
10T
1MΩ
ZERO SCALE ADJUST
−VCC

TC14710S

Unipolar Voltage Output (0 to +10V)

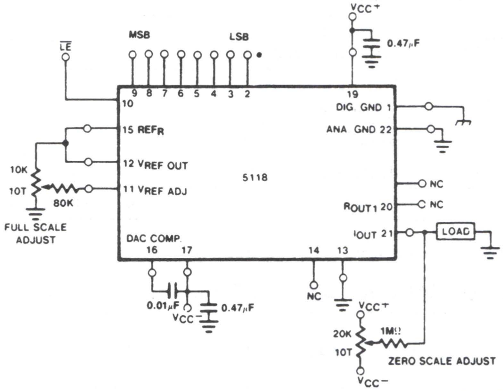

VCC+
0.47μF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11
5118
ROUT2
NC
ROUT1 20
SEE NOTE
20pF
IOUT 21
HI-Z LOAD (>50KΩ)
16 17
14 13
0.01μF
0.47μF
VCC−
NC

TC14660S

NOTE:

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

Fast Voltage Output


VCC+
0.47μF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118
10K
10T
80K
FULL SCALE ADJUST
NC
ROUT1 20
NC
IOUT 21
LOAD
DAC COMP.
16 17
14 13
0.01μF
0.47μF
VCC−
NC
VCC+
20K
1MΩ
10T
ZERO SCALE ADJUST
VCC−

TC14690S

Basic Unipolar Current Output (0 to −2mA)

Signetics

Linear Products

NE/SE5119
8-Bit Microprocessor-Compatible D/A Converter — Current Output

Product Specification

DESCRIPTION

The NE/SE5119 is a high-speed 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultralow loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale, while maintaining a low temperature coefficient.

The output has high voltage compliance, increasing versatility.

FEATURES

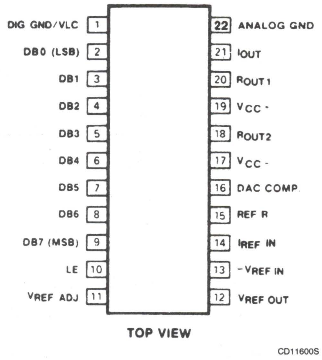
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current — 200ns**
- **Accurate to ± ¼LSB (0.1%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 8086, 6800 and many other microprocessors**

APPLICATIONS

- **Precision 8-BIT D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION

F, N Packages


DIG GND/VLC
1
DB0 (LSB)
2
DB1
3
DB2
4
DB3
5
DB4
6
DB5
7
DB6
8
DB7 (MSB)
9
LE
10
VREF ADJ
11
22
ANALOG GND
21
IOUT
20
ROUT1
19
VCC+
18
ROUT2
17
VCC-
16
DAC COMP.
15
REF R
14
IREF IN
13
-VREF IN
12
VREF OUT
TOP VIEW
CD11600S

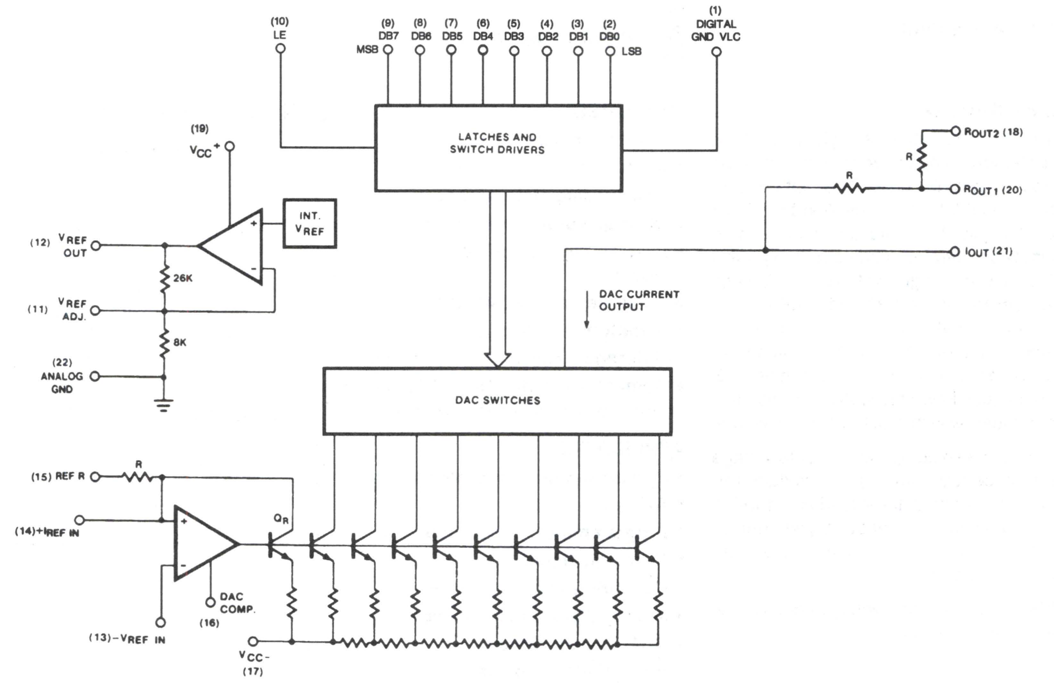
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Plastic DIP	0 to +70°C	NE5119N
22-Pin Ceramic DIP	0 to +70°C	NE5119F
22-Pin Ceramic DIP	-55°C to +125°C	SE5119F

8-Bit Microprocessor-Compatible D/A Converter — Current Output

NE/SE5119

BLOCK DIAGRAM


(10) LE
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(1) DIGITAL GND VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
26K
(11) VREF ADJ.
8K
(22) ANALOG GND
DAC CURRENT OUTPUT
DAC SWITCHES
R
ROUT2 (18)
ROUT1 (20)
IOUT (21)
(15) REF R
(14)+IREF IN
QR
DAC COMP. (16)
(13)−VREF IN
VCC− (17)
BD07831S

NOTE:
All R values equal 5kΩ and are thermally matched.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
$I_{REF\ IN}$	Reference input current (Pin 14)	3	mA
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1] F package N package	 1740 2190	 mW mW
T_A	Operating ambient temperature range SE5119 NE5119	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leqslant T_A \leqslant 125°C$, NE5119. $0°C \leqslant T_A \leqslant 70°C$ unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
I_{FS}	Full-scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero-scale current			1			1		μA
V_{REF}	Reference voltage	$I_{REF} = 1mA$, $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
$PSR+_{(OUT)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$ external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/ %VS

DC ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leqslant T_A \leqslant 125°C$, NE5119. $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
$RSR-_{(OUT)}$	Output power supply rejection (–)	$V+ = 15V$, $-13.5V \leqslant V- \leqslant -16.5V$ external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/ %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$ (Pin 15)		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient	$I_{REF\ IN} = 1.00mA$ (Pin 14)		5			5		ppm/°C
I_{REF}	Reference output current	$T_A = 25°C$			3			3	mA
I_{REFSC}	Reference short circuit current[1]	$V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leqslant V+ \leqslant 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/ %VS
$PSR-_{(REF)}$	Reference power supply rejection (–)	$V+ = 15V$, $-13.5V \leqslant V- \leqslant 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/ %VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF\ IN}$ input impedance			5.0			5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		–10	–15		–10	–15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE:

1. For reference currents > 3mA, use of an external buffer is required.

AC ELECTRICAL CHARACTERISTICS

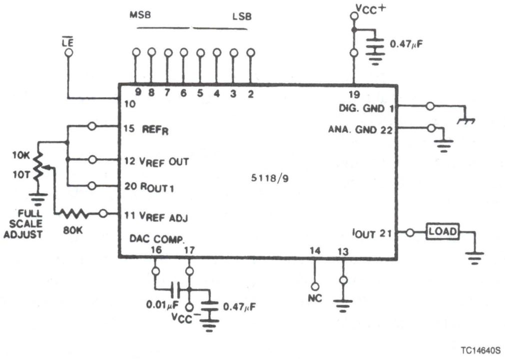
$V_{CC} = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5119			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-High		200		ns
t_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-Low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-High		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-Low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-High transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-Low transition		60		ns
t_S	Setup time	$\overline{LE}$	Input		100			ns
t_H	Hold time	Input	$\overline{LE}$		50			ns
t_{PW}	Latch enable pulse width				150			ns

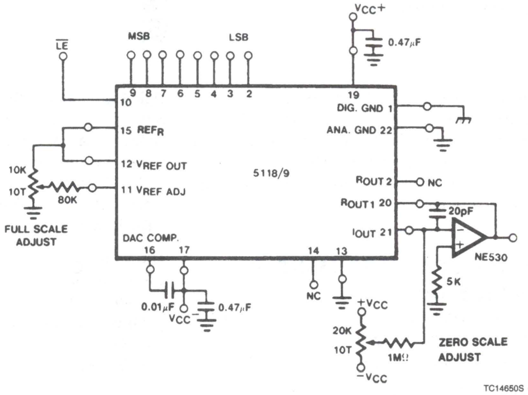
8-Bit Microprocessor-Compatible D/A Converter — Current Output

NE/SE5119

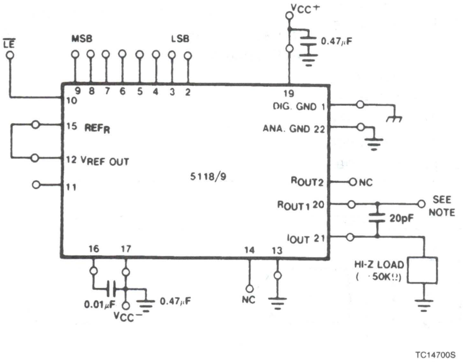
TYPICAL APPLICATIONS


MSB
LSB
LE
VCC+
0.47μF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
20 ROUT1
11 VREF ADJ
5118/9
10K
10T
FULL SCALE ADJUST
80K
DAC COMP.
16 17
14 13
IOUT 21
LOAD
0.01μF
VCC−
0.47μF
NC
TC14640S

Bipolar Output Operation (−1mA to+1mA)


VCC+
0.47μF
MSB
LSB
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118/9
10K
10T
80K
FULL SCALE ADJUST
ROUT 2
NC
ROUT1 20
20pF
IOUT 21
NE530
5K
DAC COMP.
16 17
14 13
0.01μF
VCC−
0.47μF
NC
+VCC
20K
10T
1MΩ
ZERO SCALE ADJUST
−VCC
TC14650S

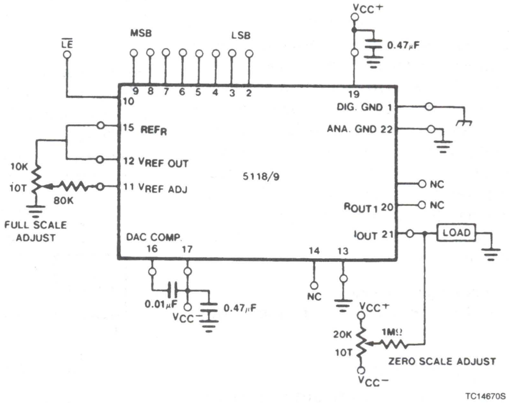
Unipolar Voltage Output (0 to+10V)


VCC+
0.47μF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11
5118/9
ROUT2
NC
ROUT1 20
SEE NOTE
20pF
IOUT 21
HI-Z LOAD (≥50KΩ)
16 17
14 13
0.01μF
VCC−
0.47μF
NC
TC14700S

NOTE:

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

Fast Voltage Output


VCC+
0.47μF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118/9
10K
10T
80K
FULL SCALE ADJUST
NC
ROUT1 20
NC
IOUT 21
LOAD
DAC COMP.
16 17
14 13
0.01μF
VCC−
0.47μF
NC
VCC+
20K
10T
1MΩ
ZERO SCALE ADJUST
VCC−
TC14670S

Basic Unipolar Current Output (0 to −2mA)

Signetics

AN109
Microprocessor-Compatible DACs

Application Note

Linear Products

DAC products are designed to convert a digital code to an analog signal. Since a common source of digital signals is the data bus of a microprocessor, DAC circuits that are bus compatible ease the design engineer's interface problems.

WHAT FEATURES MAKE A DEVICE BUS-COMPATIBLE?

The five conditions which determine processor bus compatibility are:

- Inputs must present low bus load
- Addressing must be provided
- Inputs must be latched
- Logic thresholds must be compatible
- Timing requirements should be adequate ($< 1\mu s$)

Signetics' microprocessor-compatible DACs, the NE5018 series, meet these requirements. In addition, they provide an internal reference source. The NE5018 provides a scaled voltage output, eliminating the need for an external op amp. The NE5118 is identical to the NE5018, except it provides the user with a current output. Figure 1 shows a typical microprocessor system with analog output using the NE5018 to provide a programmable voltage and an NE5118 to provide a programmable current.

The following discussions detail the operation of the NE5018 and NE5118 series DACs.

LATCH CIRCUIT

The latch circuits of the NE5018 and NE5118 are identical. Both the data inputs and latch enable ($\overline{\text{LE}}$) input feature ultra-low loading for ease of interfacing. The 8-bit data latch, controlled by the latch enable input, is static and level sensitive. When ($\overline{\text{LE}}$) is low, all the latches become transparent and the output changes as the bit pattern changes on the data bus. When the latch enable returns to its high state, the last set of inputs are held by the latch and a unique output corresponding to the binary word in the latch is produced. While the latch enable is high, the latch inputs represent a high impedance load on the data bus and changes on the data bus have no effect on the DAC output.

The digital logic input for the NE5018 and NE5118 series DACs utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). To be compatible with microprocessors, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor and I/O data bus lines. Figure 2 gives the typical timing requirements of the latch circuits in the NE5018 and NE5118.

The voltage levels on the data bus should be stable for approximately 150ns before latch enable returns to high level. The timing diagram shows 100ns is required for setup time and the information on the data lines should remain valid for another 50ns.

REFERENCE INTERFACE

The NE5018 and NE5118 contain an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 12) allows easy trimming of the reference output (Pin 13). Use of a 10k pot and series resistor, as shown in Figure 3, adjusts the gain of the buffer amplifier, therefore varying the output reference voltage level.

This network can then be used as a full-scale output adjust. A variation in the $V_{REF\ OUT}$ of ~0.8V, results in a corresponding 1.6V variation in the full-scale output. This is more than adequate since the untrimmed $V_{REF\ OUT}$ is typically within 200mV of the nominal 5V. The $V_{REF\ OUT}$ will provide a maximum of 5mA drive and can be used as a reference voltage for other system components, if required.

Since a potential need exists to use the NE5018 and NE5118 as multiplying DACs, the V_{REF} is not connected internally, allowing the use of external reference sources. To utilize the internal reference, the $V_{REF\ OUT}$ (Pin 13) must be jumper-connected to the $V_{REF\ IN}$ (Pin 14). This also makes it possible to use a common reference for other D/A or A/D circuits in a system.

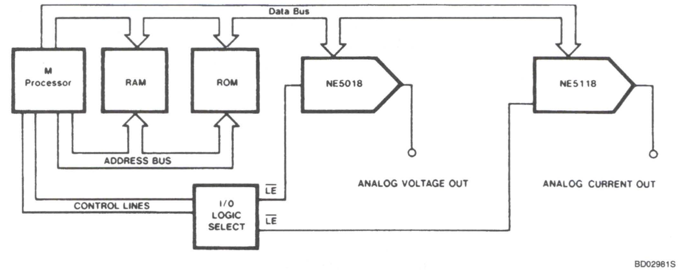


Figure 1. Interfacing to a Microprocessor

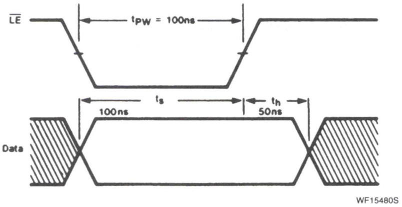


Figure 2. Latch Enable ($\overline{\text{LE}}$) Timing Diagram for the NE5018 and NE5118

INPUT AMPLIFIER OF THE NE5018

The DAC reference amplifier has been designed to eliminate the need for compensation when operating from the internal reference or from an external reference which is buffered by an op amp or low impedance source. Compensation is required, however, when operating from a high impedance source. The addition of an external resistance reduces the phase margin of the amplifier making it less stable. Compensation, when required, is a single capacitor from Pin 16 to ground.

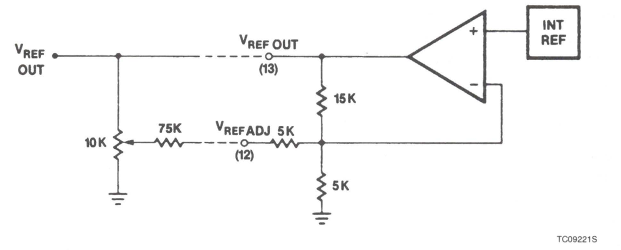


Figure 3. Reference Adjust Circuit

Figure 4 details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5V V_{REF}. This current sets the input bias to the ladder network. Data bit 7 (DB_7) Q_7, when turned on, will mirror this current and will contribute 1mA to the output. DB_6 (Q_6) will contribute ½ of that value or 0.5mA, and so on. If all bits are on, the output current will be 2mA − 1 LSB. The full-scale V_{OUT} will be ($I_{OUT}R_F$) or 2mA − 1 LSB × 5k) = (10V − 1 LSB) = 9.961V. The overall input/output expression for the NE5018 is:

$$V_{OUT} = 2V_{REF} \times \left(\frac{DB7}{2} + \frac{DB6}{4} + \frac{DB5}{8} + \frac{DB4}{16} + \frac{DB3}{32} + \frac{DB2}{64} + \frac{DB1}{128} + \frac{DB0}{256}\right)$$

The minimum current for the ladder network to be operative in the linear region is 500μA. Therefore, the minimum V_{REF} input is 2.5V. The slew rate of the reference amplifier is typically 0.7V/μs without compensation. The input structure of the NE5118 is slightly different and will be discussed in greater detail later. Q_T provides a termination for the R-2R ladder network and does not contribute to I_{OUT}.

OUTPUT INTERFACE OF THE NE5018

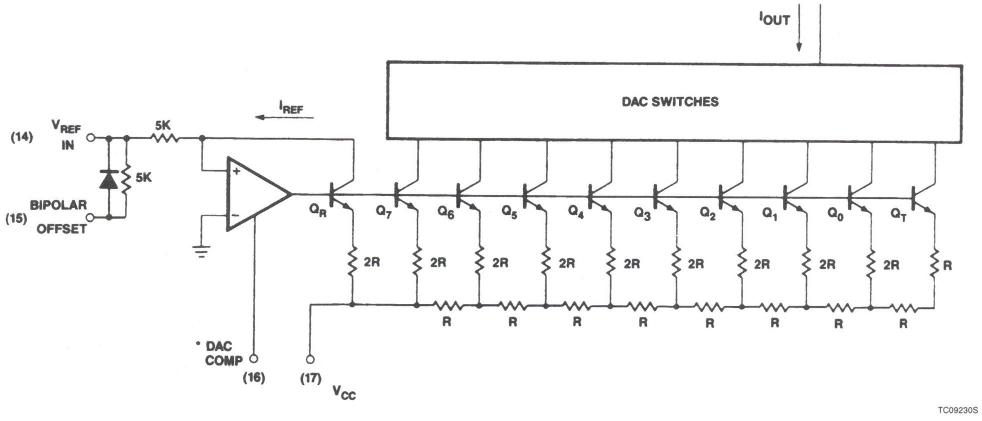
The NE5018 has an internal op amp which provides a voltage output, while the NE5118 is a current output device. The NE5018 output op amp is a two-stage design with feedforward compensation. Having a slew rate of 10V/μs, it provides a voltage output from 0 to 10V (±0.2%) typically within 2μs (the time allowed for the output voltage to settle to within ½ LSB). Compensation must be provided externally as shown in Figure 5.

The addition of the optional diode between the summing node (Pin 20) and ground prevents the DAC current switches from driving the op amp into saturation during large-signal transitions which would increase the settling time.

Zero adjust circuits, such as the one shown in Figure 5, may also be connected to the summing node to provide a means to zero the output when all zeros are present on the input. Not all applications require a zero adjust circuit since the untrimmed zero-scale is typically less than 5mV. Excess stray capacitance at the sum node of the output op amp may necessitate the use of a feedback capacitor from V_{OUT} to the sum node (C_{FF}) to insure stability of the op amp. Typical values of C_{FF} range from 15 to 22pF. The rated load of the op amp is ~2kΩ. For stability, the load capacitance should be minimized (50pF max).

MODES OF OPERATION OF THE NE5018

The NE5018 has two basic modes of operation: unipolar and bipolar. When operating in



NOTE:
DAC compensation may be required if V_{REF} resistance exceeds 10kΩ.

Figure 4. R-2R Ladder Network Develops a Scaled Reference Current Value Into the DAC Switching Network

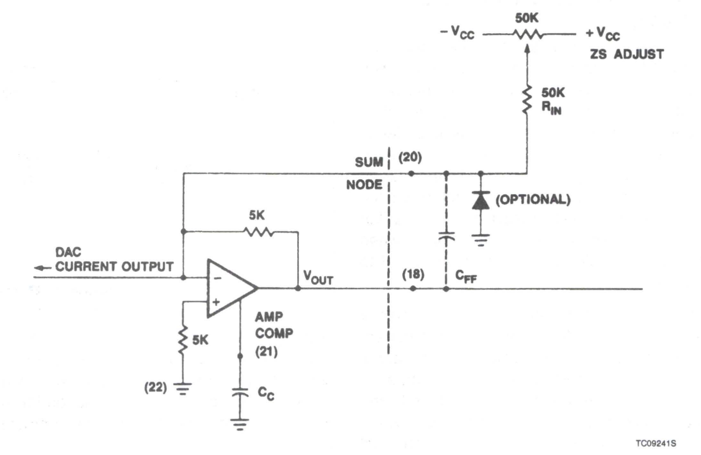


Figure 5. Zero-Scale Adjust

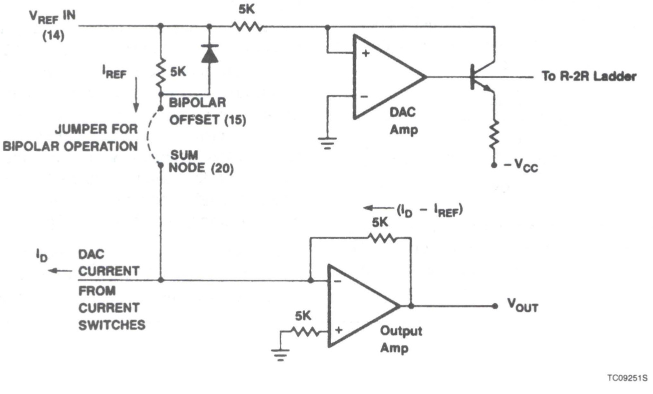


Figure 6. Bipolar Output

the unipolar mode, the output range is 0 to +10V. To change from unipolar to bipolar operation, the bipolar offset pin is connected to the summing node. This provides the 5V offset required for this mode of operation. The output now will have a range from −5 to +5V. Figure 6 details the connection of the NE5018 in the bipolar mode of operation.

With the bipolar offset, Pin 15, connected to the sum node, Pin 20, it forms a unity gain inverter with an input of $+V_{REF}$. The bipolar offset develops an I_{REF} current through the internal 5k resistor. This current is then fed to the sum node of the output amplifier where it is summed with the current output of the DAC ladder network. Assume for the moment that the current output of the ladder network is 0mA. With a V_{REF} equal to +5V, I_{REF} is 1mA and the output of the op amp is converted to −5V. If the DAC switches are now set to full-scale, the current from the DAC ladder is 2mA. This is summed against the 1mA I_{REF} and causes the output of the op amp to swing from −5V to +5V.

$$(I_{DAC} - I_{REF})5k = (2mA - 1mA)5k = +5V$$

Since the bipolar offset resistor is monolithic, tracking with the 5k feedback resistor of the output amplifier is excellent.

Note that the bipolar offset pin could not be used when using the DAC in a multiplier application since the V_{OUT} would reflect an inverted input signal.

NOTES ON THE NE5118 CURRENT OUTPUT DAC

The basic operation of the NE5118 current output DAC is the same as the NE5018. The current output structure allows the user to provide a programmable current sink (I_{OUT} max of 2mA). Several jumper options provide a variety of operational modes. Figure 7 is a block diagram of the NE5118. The input logic and V_{REF} portions are identical to the NE5018.

REFERENCE INPUT AMPLIFIER

The characteristics of the reference input amplifier are identical to the NE5018; however, extended versatility of the input structure allows for both current (via Pin 14) or voltage (via Pin 15) reference inputs.

The maximum DAC output current is 2mA. The DAC has an internal gain of 2, limiting the maximum usable input current to 1mA.

NOTE:

The absolute maximum input current should be limited to 5mA to prevent damage to the input reference amplifier.

Figure 8 shows the basic operating mode of the NE5118 using an external current reference resistor (R_1) and a positive reference voltage.

This voltage can be provided by either an internal or external reference voltage. Figure 9 shows a typical connection using a voltage input directly via Pin 15.

Besides a reduced parts count, use of the internal R_{REF} provides excellent tracking characteristics with the R_{OUT} resistor (Pin 20) when developing a high slew rate voltage output. The negative V_{REF} input must be returned to ground directly or through R_2. R_2 is optional and is used to cancel minor errors developed by the input bias currents of the reference amplifier ($R_2 = R_1$ in Figure 8). A negative voltage can be the reference by using the $-V_{REF}$ input pin as shown in Figure 10.

The positive V_{REF} is returned to ground via R_{IN} (Pin 15). As with the NE5018, a compensation capacitor on Pin 16 is not required if the V_{REF} is supplied by a low impedance source.

OUTPUT STRUCTURE

The output of the NE5118 is a current sink with a capacity of 2mA (full-scale) capable of settling to 0.2% in 200ns. Internal bias and feedback resistors are also made available to ease the designer's task of interfacing.

Figure 11 shows the NE5118 using a current-to-voltage converter at the output to provide a high slew rate voltage output. Using the NE538 as shown can provide 60V/μs slew rate output. The diode at the inverting node of the op amp improves the response time by

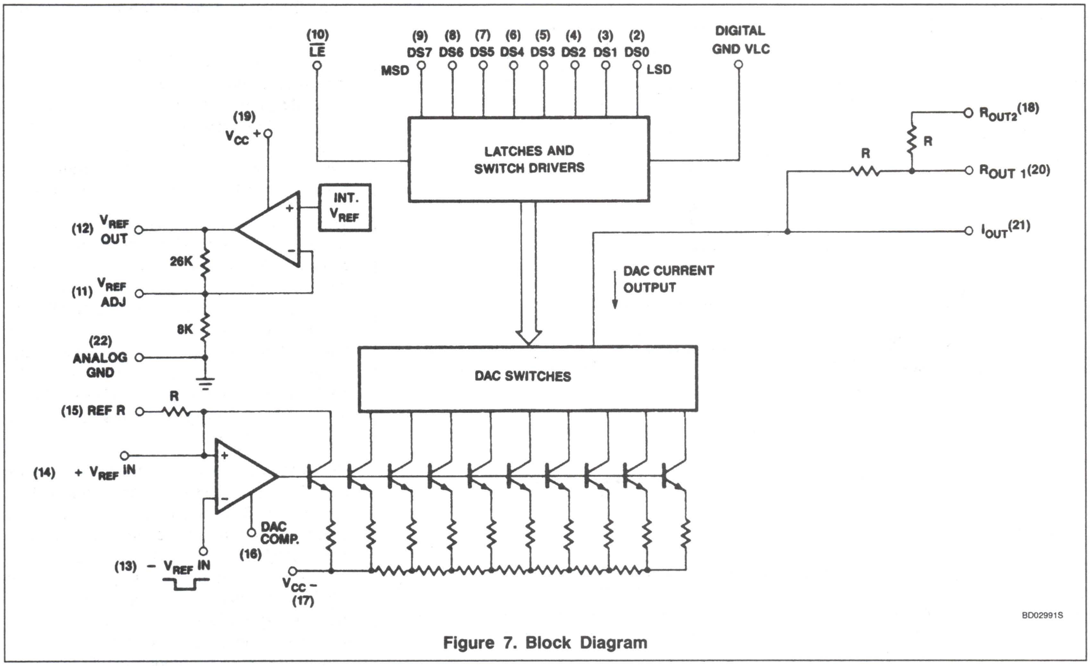

(10)
LE
(9) (8) (7) (6) (5) (4) (3) (2)
DS7 DS6 DS5 DS4 DS3 DS2 DS1 DS0
MSD
LSD
DIGITAL
GND VLC
(19)
V_{CC} +
LATCHES AND
SWITCH DRIVERS
INT.
V_{REF}
(12) V_{REF} OUT
26K
(11) V_{REF} ADJ
8K
(22)
ANALOG
GND
R
(15) REF R
(14) + V_{REF} IN
DAC
COMP.
(16)
(13) − V_{REF} IN
V_{CC} −
(17)
DAC SWITCHES
DAC CURRENT
OUTPUT
R
R
R_{OUT2}(18)
R_{OUT} 1(20)
I_{OUT}(21)
BD02991S

Figure 7. Block Diagram

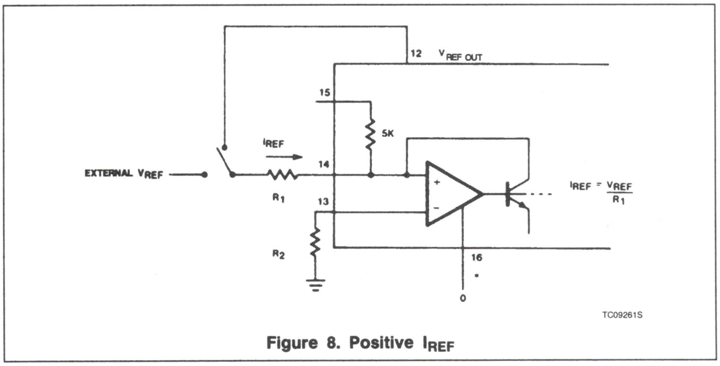

12 $V_{REF\ OUT}$
15
5K
I_{REF}
EXTERNAL V_{REF}
14
R_1
13
R_2
+
−
$I_{REF} = \frac{V_{REF}}{R_1}$
16
0
TC09261S

Figure 8. Positive I_{REF}

preventing saturation of the op amp during large signal transitions. The feedback resistor R_{OUT1} (Pin 20) is provided internally, providing excellent thermal tracking characteristics with the R_{REF} at the input.

Bipolar operation can be accomplished by connecting the V_{REFOUT} (Pin 12) to the R_{OUT} resistor (Pin 20) (Figure 12). The principal is the same as the NE5018 bipolar operation. The internal resistors exhibit excellent thermal tracking characteristics.

An alternate method of bipolar output operation is shown in Figure 12. The R_{REF} and R_{OUT} set up a current-to-voltage converter while two (2) external resistors provide a bipolar offset. R_{EXT_1} and R_{EXT_2} should have similar thermal tracking characteristics.

The NE5118 can provide a voltage output directly when driving a high impedance load as shown in Figure 13. With a full-scale current of 2mA, Pin 20 tied to +10V and a digital input of zero, the high impedance load will see +10V. For a full-scale digital input, the load will see 0V. Since the load and the internal resistor form a voltage divider, their ratio determines full-scale accuracy.

By connecting the R_{OUT} resistor (Pin 20) to ground (Figure 13), the output voltage seen by the load ranges from 0V as zero-scale to −10V as full-scale. Only a few of the many possible output configurations have been shown to demonstrate the NE5118 flexibility.

CIRCUIT EXAMPLES

Now that the basics of the NE5018 and the NE5118 have been discussed, let's examine some specific circuits. Figure 14 is a microprocessor-controlled programmable gain amplifier, using the NE5018. The V_{REF} output is fed to the non-inverting input to a differential amplifier. $R_1 + R_2$ places $2.5V_{DC}$ bias on the V_{REF} input. R_2 can be made adjustable to precisely control the DC reference input. The analog input is fed to the inverting input of the differential amplifier with a gain of unity. An input range of 0 to 2.5V will produce an output of 10V to 5V full-scale. $V_{REF\ IN}$ will vary from 5V to 2.5V. The current ladder is always kept in the linear operating range and the output will not become distorted.

No compensation is required for the DAC reference amplifier since the $V_{REF\ IN}$ is fed from a low impedance source. With a compensation cap of 33pF on the output amplifier, the frequency response of the output is linear to at least 20kHz with less than 0.1% distortion with an input amplitude of $1V_{P\text{-}P}$.

Microprocessor-Compatible DACs AN109

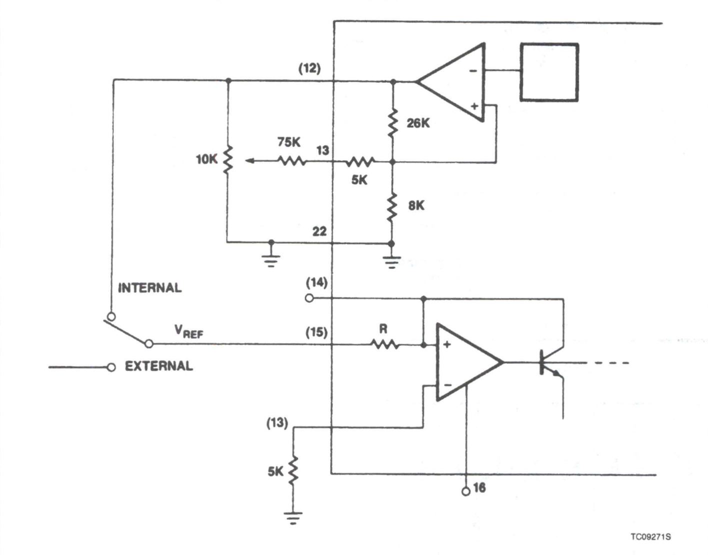

(12)
26K
75K
13
10K
5K
8K
22
INTERNAL
(14)
V_{REF}
(15)
R
EXTERNAL
(13)
5K
16
TC09271S

Figure 9. Positive V_{REF}

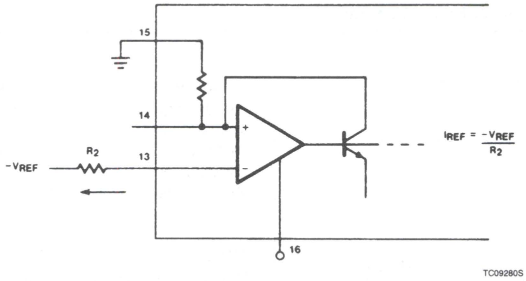

15
14
13
R_2
$-V_{REF}$
16
$I_{REF} = \frac{-V_{REF}}{R_2}$
TC09280S

Figure 10. Using a Negative I_{REF}

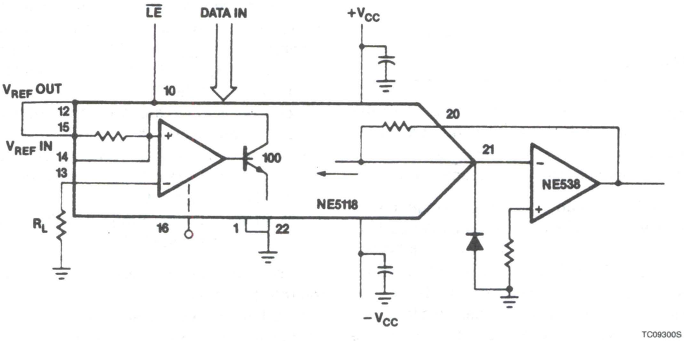

$\overline{LE}$
DATA IN
$+V_{CC}$
V_{REF} OUT
10
12
15
V_{REF} IN
14
13
100
20
21
NE538
NE5118
R_L
16
1
22
$-V_{CC}$
TC09300S

Figure 11. High Slew Rate Voltage Outputs

The NE5018 is seen by the microprocessor as an I/O device.

In Figure 15, the N5018 and NE5118 provide a method of summing two digital words and generating a voltage output. The latch enable feature of both devices direct connection to a data bus, using address decoding. These devices greatly reduced the total component count required to perform this operation.

The reference voltage is common to both DACs, being provided by the NE5018. The bipolar offset resistor of the NE5018 provides the 1mA current reference for the NE5118. Using the internal resistor of the NE5018 to develop the reference current enhances the thermal tracking since the current-to-voltage resistor of the output op amp is also in the NE5018. Both DACs can be addressed by a microprocessor using an address decoder to select DAC A or DAC B.

Figure 16 is a schematic of the NE5118 and a NE527 as a high-speed programmable limit sensor (or A/D converter). A 4.8V zener diode is used on the comparator input to insure the input voltage range of the comparator is not exceeded. The outputs of the NE527 comparator are complementary, easing the logic interface requirement. If the strobe function is not used, the strobe inputs should be tied high, through a 10kΩ resistor.

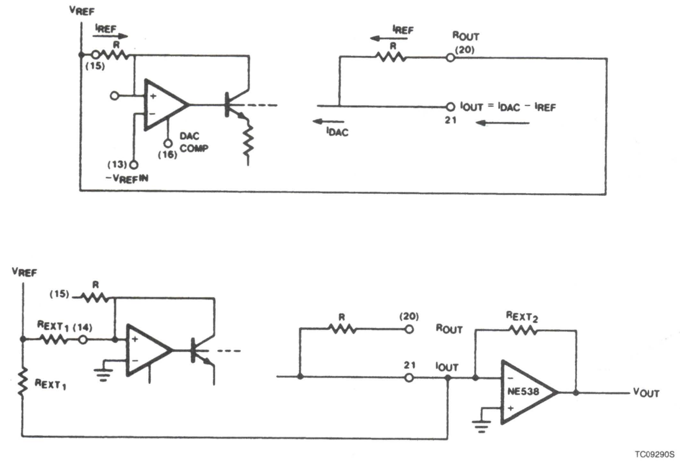
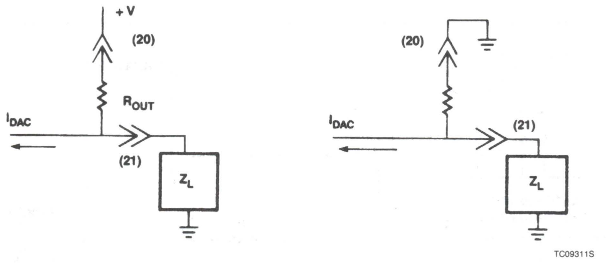

VREF
IREF
R
(15)
DAC COMP
(16)
(13)
−VREF IN
IREF
R
ROUT
(20)
IOUT = IDAC − IREF
21
IDAC
VREF
(15)
R
REXT1 (14)
REXT1
R
(20)
ROUT
21
IOUT
REXT2
NE538
VOUT
TC09290S

Figure 12. Bipolar Options of the NE5118


+V
(20)
ROUT
IDAC
(21)
ZL
(20)
IDAC
(21)
ZL
TC09311S

a. +10 to 0V

b. 0 to −10V

Figure 13

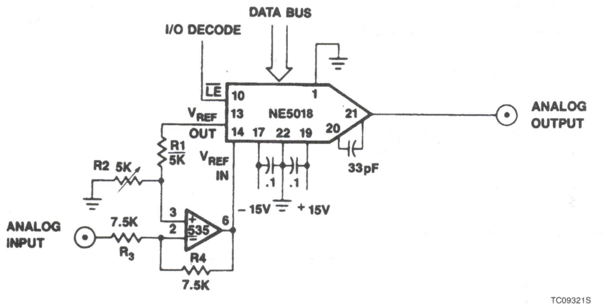

DATA BUS
I/O DECODE
LE
10
1
VREF
13
NE5018
21
OUT
14 17 22 19
20
ANALOG OUTPUT
R1 5K
VREF IN
R2 5K
33pF
.1
.1
−15V
+15V
3
2
535
6
7.5K
R3
R4
7.5K
ANALOG INPUT
TC09321S

Figure 14. Programmable Gain Amplifier

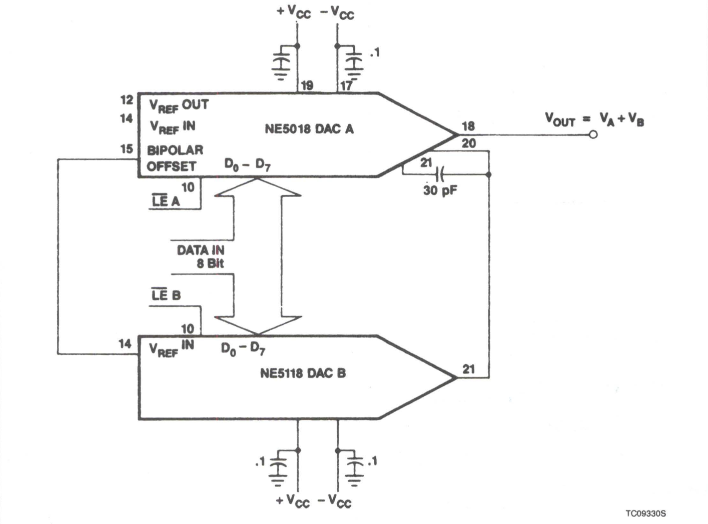

+VCC
−VCC
.1
19
17
12
14
15
VREF OUT
VREF IN
BIPOLAR OFFSET
NE5018 DAC A
D0 − D7
18
20
21
30 pF
VOUT = VA + VB
10
LE A
DATA IN 8 Bit
LE B
10
14
VREF IN
D0 − D7
NE5118 DAC B
21
.1
.1
+VCC
−VCC
TC09330S

Figure 15. Analog Summation With Digital Inputs

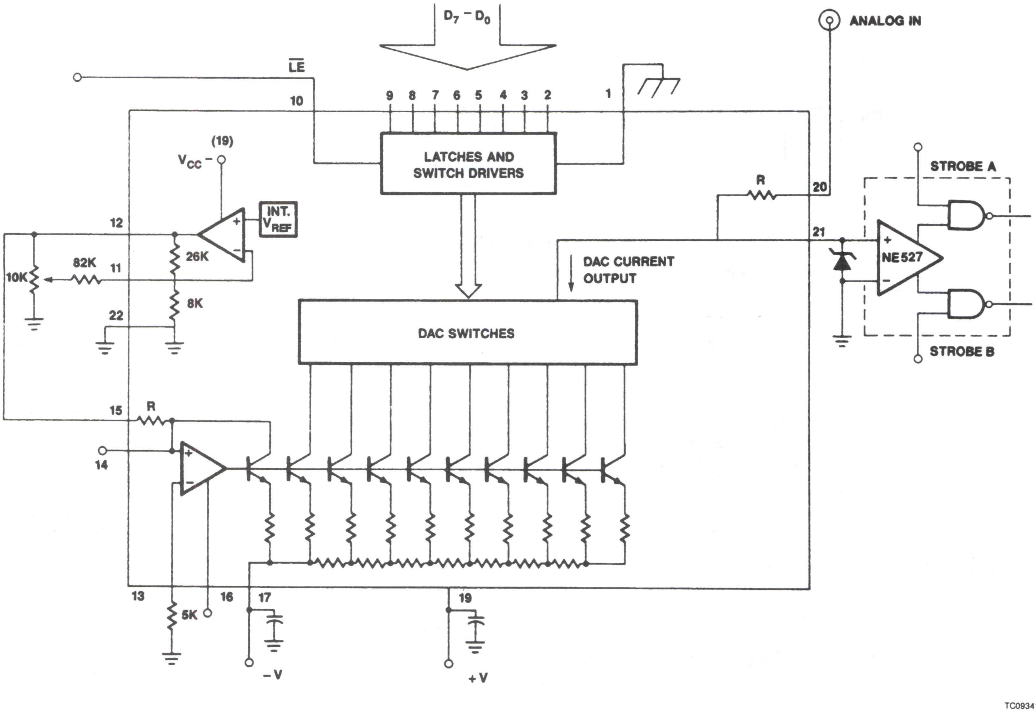

D7 − D0
ANALOG IN
LE
10
9 8 7 6 5 4 3 2
1
(19)
VCC −
LATCHES AND SWITCH DRIVERS
STROBE A
R
20
12
INT. VREF
21
26K
NE527
82K
11
DAC CURRENT OUTPUT
10K
8K
22
DAC SWITCHES
STROBE B
15
R
14
13
5K
16
17
19
−V
+V
TC09341S

Figure 16. Programmable Limit Comparator

Signetics

NE5150/5151/5152
Triple 4-Bit RGB D/A Converter With and Without Memory

Preliminary Specification

Linear Products

DESCRIPTION

The NE5150/5151/5152 are triple 4-bit DACs intended for use in graphic display systems. They are a high performance — yet cost effective — means of interfacing digital memory and a CRT. The NE5150/5152 are single integrated circuit chips containing special input buffers, an ECL static RAM, high-speed latches, and three 4-bit DACs. The input buffers are user-selectable as either ECL or TTL compatible for the NE5150. The NE5152 is similar to the NE5150, but is TTL compatible only, and operates off of a single +5V supply. The RAM is organized as 16 × 12, so that 16 "color words" can be down-loaded from the pixel memory into the chip memory. Each 12-bit word represents 4 bits of red, 4 bits of green and 4 bits of blue information. This system gives 4096 possible colors. The RAM is fast enough to completely reload during the horizontal retrace time. The latches resynchronize the digital data to the DACs to prevent glitches. The DACs include all the composite video functions to make the output waveforms meet RS-170 and RS-343 standards, and produce 1V_{P-P} into 75Ω. The composite functions (reference white, bright, blank, and sync) are latched to prevent screen-edge distortions generally found on "video DACs." External components are kept to an absolute minimum (bypass capacitors only as needed) by including all reference generation circuitry and termination resistors on-chip, by building in high-frequency PSRR (eliminating separate V_{EE}s and costly power supplies and filtering), and by using a single-ended clock. The guaranteed maximum operating frequency for the NE5150/5152 is 110MHz over the commercial termperature range. The devices are housed in a standard 24-pin package and consume less than 1W of power.

The NE5151 is a simplified version of the NE5150, including all functions except the memory. Maximum operating frequency is 150MHz.

FEATURES

- **Single-chip**
- **On-board ECL static RAM**
- **4096 colors**
- **ECL and TTL compatible**
- **110MHz update rate (NE5150, 5152)**
- **150MHz update rate (NE5151)**
- **Low power and cost**
- **Drives 75Ω cable directly**
- **Internal reference**
- **40dB PSRR**
- **No external components necessary**

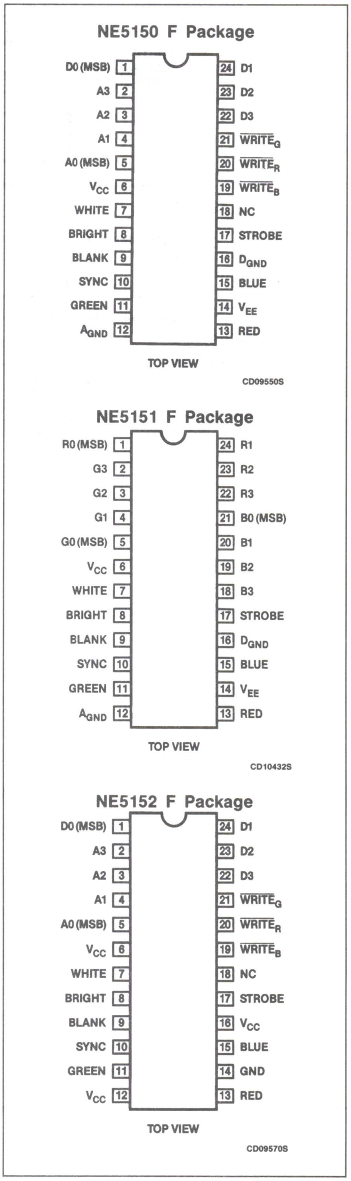
APPLICATIONS

- **Bit-mapped graphics**
- **Super high-speed DAC**
- **Home computers**
- **Raster-scan displays**

ORDERING INFORMATION

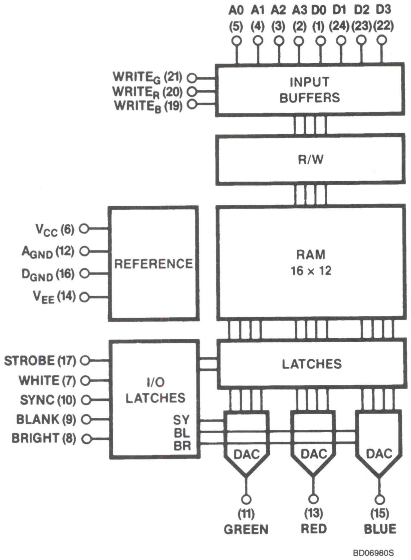
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Ceramic DIP	0°C to +70°C	NE5150F
24-Pin Ceramic DIP	0°C to +70°C	NE5151F
24-Pin Ceramic DIP	0°C to +70°C	NE5152F

PIN CONFIGURATIONS

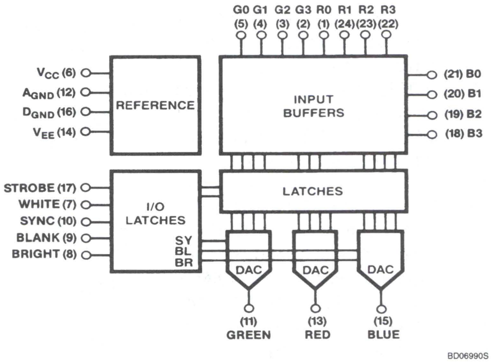

NE5150 F Package
D0 (MSB) 1
A3 2
A2 3
A1 4
A0 (MSB) 5
VCC 6
WHITE 7
BRIGHT 8
BLANK 9
SYNC 10
GREEN 11
AGND 12
24 D1
23 D2
22 D3
21 WRITEG
20 WRITER
19 WRITEB
18 NC
17 STROBE
16 DGND
15 BLUE
14 VEE
13 RED
TOP VIEW
CD09550S
NE5151 F Package
R0 (MSB) 1
G3 2
G2 3
G1 4
G0 (MSB) 5
VCC 6
WHITE 7
BRIGHT 8
BLANK 9
SYNC 10
GREEN 11
AGND 12
24 R1
23 R2
22 R3
21 B0 (MSB)
20 B1
19 B2
18 B3
17 STROBE
16 DGND
15 BLUE
14 VEE
13 RED
TOP VIEW
CD10432S
NE5152 F Package
D0 (MSB) 1
A3 2
A2 3
A1 4
A0 (MSB) 5
VCC 6
WHITE 7
BRIGHT 8
BLANK 9
SYNC 10
GREEN 11
VCC 12
24 D1
23 D2
22 D3
21 WRITEG
20 WRITER
19 WRITEB
18 NC
17 STROBE
16 VCC
15 BLUE
14 GND
13 RED
TOP VIEW
CD09570S

BLOCK DIAGRAMS

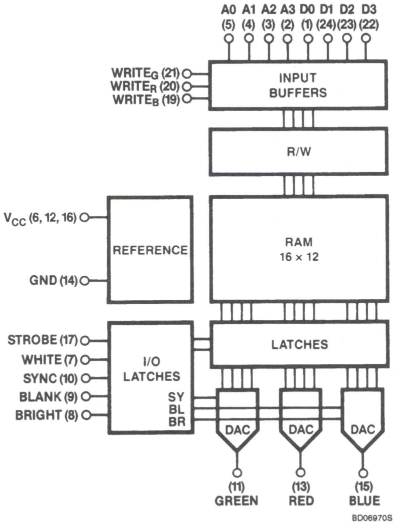
NE5150


A0 A1 A2 A3 D0 D1 D2 D3
(5) (4) (3) (2) (1) (24) (23) (22)
WRITE$_G$ (21)
WRITE$_R$ (20)
WRITE$_B$ (19)
INPUT BUFFERS
R/W
V$_{CC}$ (6)
A$_{GND}$ (12)
D$_{GND}$ (16)
V$_{EE}$ (14)
REFERENCE
RAM 16 × 12
STROBE (17)
WHITE (7)
SYNC (10)
BLANK (9)
BRIGHT (8)
I/O LATCHES
SY
BL
BR
LATCHES
DAC
DAC
DAC
(11) GREEN
(13) RED
(15) BLUE
BD06980S

NE5151


G0 G1 G2 G3 R0 R1 R2 R3
(5) (4) (3) (2) (1) (24) (23) (22)
V$_{CC}$ (6)
A$_{GND}$ (12)
D$_{GND}$ (16)
V$_{EE}$ (14)
REFERENCE
INPUT BUFFERS
(21) B0
(20) B1
(19) B2
(18) B3
STROBE (17)
WHITE (7)
SYNC (10)
BLANK (9)
BRIGHT (8)
I/O LATCHES
SY
BL
BR
LATCHES
DAC
DAC
DAC
(11) GREEN
(13) RED
(15) BLUE
BD06990S

NE5152


A0 A1 A2 A3 D0 D1 D2 D3
(5) (4) (3) (2) (1) (24) (23) (22)
WRITE$_G$ (21)
WRITE$_R$ (20)
WRITE$_B$ (19)
INPUT BUFFERS
R/W
V$_{CC}$ (6, 12, 16)
GND (14)
REFERENCE
RAM 16 × 12
STROBE (17)
WHITE (7)
SYNC (10)
BLANK (9)
BRIGHT (8)
I/O LATCHES
SY
BL
BR
LATCHES
DAC
DAC
DAC
(11) GREEN
(13) RED
(15) BLUE
BD06970S

Triple 4-Bit RGB D/A Converter With and Without Memory

NE5150/5151/5152

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Temperature range		
T_A	Operating	0 to +70	°C
T_{STG}	Storage	-65 to +150	°C
V_{CC} V_{EE}	Power supply	7.0 −7.0	V V
	Logic levels		
	TTL-high	5.5	V
	TTL-low	−0.5	V
	ECL-high	0.0	V
	ECL-low	0 to V_{EE}	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < +70°C, for NE5150/5151; V_{CC} = +5V (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Resolution	4			bits
	Monotonicity	4			bits
NL	Non-linearity		± 1/16	± 1/2	LSB
DNL	Differential non-linearity		± 1/8	± 1	LSB
	Offset error (25°C) [1111] (BRT = 1)		− 1/5	± 1	LSB
	Gain error (25°C) [0000] (BRT = 1)		± 1/2	± 1	LSB
V_{CC}	Positive power supply (TTL mode) (NE5150) (TTL mode) (NE5151) (ECL mode)	4.5 4.75 −0.1	5.0 5.0 0.0	5.5 5.5 0.1	V V V
V_{EE}	Negative power supply (TTL or ECL mode) (NE5150/5151)	−4.75	−5.0	-5.5	V
I_{CC}	Positive supply current (NE5150/5151) (NE5152)		15 175	25 210	mA mA
I_{EE}	Negative supply current (NE5150) (NE5151)		175 145	210 175	mA mA
	Analog voltage range (ZS to FS)		603		mV
	Gain tracking (any two channels)			± 1/4	LSB
LSB	Least significant bit		40.2		mV
EWH	Enhanced white level (25°C)^2		0		mV
BS	Bright shift (25°C)(0 to 1)		71.4		mV
EBL	Enhanced blanking level (25°C)^2		−674		mV
ESY	Enhanced sync level (25°C)^2		−960		mV
R_O	Output resistance (25°C)	67.5	75.0	82.5	Ω
V_{IH}	TTL logic input high	2.0			V
V_{IL}	TTL logic input low			0.8	V
I_{IH}	TTL logic high input current (V_{IN} = 2.4V)			20	µA
I_{IL}	TTL logic low input current (V_{IN} = 0.4V)			−1.6	mA
V_{IH}	ECL logic input high	−1.045			V
V_{IL}	ECL logic input low			−1.48	V
I_{IH}	ECL logic high input current (V_{IN} = −0.8V)			−1.0	mA
I_{IL}	ECL logic low input current (V_{IN} = −1.8V)			−1.0	mA

TEMPERATURE CHARACTERISTICS $V_{CC} = +5V$ (TTL), 0V (ECL), $V_{EE} = -5V$, $0°C < T_A < +70°C$, for NE5150/5151;
$V_{CC} = +5V$ (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Offset TC[1]		±50	±100	ppm/°C
	Gain TC[1]		±70	±200	ppm/°C
	Gain Tracking TC (any two channels)		±20	±50	ppm/°C
	Enhanced white level TC[1]		±50	±100	ppm/°C
	Bright shift TC		±70	±200	ppm/°C
	Enhanced blanking level TC		±100	±300	ppm/°C
	Enhanced sync level TC		±100	±300	ppm/°C
	Output resistance TC		+1000	+2000	ppm/°C

NOTES:
1. Normalized to full-scale (603mV).
2. With respect to [1111] (BRT = 1).

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$ (TTL), 0V (ECL), $V_{EE} = -5V$, $0°C < T_A < +70°C$, for NE5150/5151;
$V_{CC} = +5V$ (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{MAX}	Maximum operating frequency (NE5150/5152)	110			MHz
t_{WAS}	Write address setup (NE5150/5152)	0			ns
t_{WAH}	Write address hold (NE5150/5152)	0			ns
t_{WDS}	Write data setup (NE5150/5152)	4			ns
t_{WDH}	Write data hold (NE5150/5152)	2			ns
t_{WEW}	Write enable pulse width (NE5150/5152)	3			ns
t_{RCS}	Read composite[1] setup (NE5150/5152)	3			ns
t_{RCH}	Read composite[1] hold (NE5150/5152)	2			ns
t_{RAS}	Read address setup (NE5150/5152)	3			ns
t_{RAH}	Read address hold (NE5150/5152)	2			ns
t_{RSW}	Read strobe pulse width (NE5150/5152)	3			ns
t_{RDD}	Read DAC delay (NE5150/5152)		8		ns
f_{MAX}	Maximum operating frequency (NE5151)	150			MHz
t_{CS}	Composite[1] setup (NE5151)	3			ns
t_{CH}	Composite[1] hold (NE5151)	2			ns
t_{DS}	Data-bits setup (NE5151)	1			ns
t_{DH}	Data-bits hold (NE5151)	5			ns
t_{SW}	Strobe pulse width (NE5151)	3			ns
t_{DD}	DAC delay (NE5151)		8		ns
t_R	DAC rise time (10 – 90%)		3		ns
t_S	DAC full-scale settling time[2]		10		ns
C_{OUT}	Output capacitance (each DAC)		10		pF
SR	Slew rate		200		V/μs

Triple 4-Bit RGB D/A Converter With and Without Memory

NE5150/5151/5152

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
GE	Glitch energy			30	pV-s
PSRR[3]	Power supply rejection ratio (to red, green or blue outputs)				
	V_{EE} at 1kHz		43		dB
	V_{EE} at 10MHz		28		dB
	V_{EE} at 50MHz		14		dB
	V_{CC} at 1kHz		80		dB
	V_{CC} at 10MHz		50		dB
	V_{CC} at 50MHz		36		dB

NOTES:
1. Composite implies any of the WHITE, BRIGHT, BLANK or SYNC signals.
2. Setting to ± ½ LSB, measured from STROBE 50% point (rising edge). This time includes the delay throught the strobe input buffer and latch.
3. Listed PSRR is for the NE5150/51. The NE5152 PSRR specs are identical to the V_{EE} numbers in the table.

NE5150 PIN DESCRIPTION

Write enable inputs use negative-true logic while all other inputs are positive-true. All inputs operate synchronously with the positive edge-triggered strobe input. When V_{CC} is taken high (5V), all inputs are TTL compatible. When V_{CC} is grounded, all inputs are ECL compatible. All DACs are complementary, so that all ones is the highest absolute voltage and all zeroes is the lowest. All ones is called zero-scale (ZS) and all zeroes is called full-scale (FS). The analog output voltage is approximately 0V (ZS) to −1V (SYNC).

Pins 1, 24, 23, 22: **DATA** bits D0 (MSB) through D3, used to input digital information to the memory during the write phase. During this phase, the data bits are presented to the internal latches (noninverted) and the DACs will output the analog equivalent of the stored word, unless overridden by WHITE, BLANK or SYNC.

Pins 5, 4, 3, 2: **ADDRESS** lines A0 (MSB) through A3, used for selecting a memory address to write to or read from.

Pin 7: **WHITE** command. Presets the latches to all ones [1111] and outputs 0V absolute on all DACs. Can be modified to −71mV absolute when BRIGHT is taken low. Will be overridden by either a BLANK or SYNC command.

Pin 8: **BRIGHT** command. A low input here turns on an additional −71mV (10 IRE unit) switch, shifting all other levels downward. Not overridden by any other input.

Pin 9: **BLANK** command. Presets the latches to all zeroes [0000] and turns on an additional −71mV (10 IRE unit) switch. Absolute output is −671mV. Can be modified another −71mV to −742mV absolute when BRIGHT is taken low. Will override WHITE, and will be overridden by SYNC.

Pin 10: **SYNC** command. Presets the latches to all zeroes [0000] and turns on the BLANK switch. Additionally turns on a −286mV (40 IRE unit) switch in the green channel only. Absolute output is −671mV for the red and blue channels, and −957mV for the green channel. All levels can be shifted −71mV by taking BRIGHT low. Overrides WHITE and BLANK.

Pins 11, 13, 15: **GREEN, RED, BLUE.** Analog outputs with 75Ω internal termination resistors. Can directly drive 75Ω cable and should be terminated at the display end of the line with 75Ω. Output voltage range is approximately 0V to −1V, independent of whether the digital inputs are ECL or TTL compatible. All outputs are simultaneously affected by the WHITE, BLANK or BRIGHT commands. Only the GREEN channel carries SYNC information.

NOTE:
There are 100 IRE units from WHITE to BLANK. One IRE unit is approximately 7.1mV. Full-scale is 90 IRE units and 10 IRE units is ⅑ of full-scale (e.g., BRIGHT function).

Pins 19, 20, 21: $\overline{\textbf{WRITE}_B}$, $\overline{\textbf{WRITE}_R}$, $\overline{\textbf{WRITE}_G}$. Write enable commands for each of the three 16 × 4 memories. When all write commands are high, then the READ operation is selected. This is the normal display mode. To write data into memory, the write enable pin is taken low. Data D0 − D3 will be written into address A0 − A3 of each memory when its corresponding write enable pin goes low.

Pin 17: **STROBE.** The strobe signal is the main system clock and is used for resynchronizing digital signals to the DACs. Preventing data skew eliminates glitches which would otherwise become visible color distortions on a CRT display. The strobe command has no special drive requirements and is TTL or ECL compatible.

Pins 12, 16: **A_{GND}, D_{GND}.** Both **A**nalog and **D**igital ground carry a maximum of approximately 100mA of DC current. For proper operation, the difference voltage between A_{GND} and D_{GND} should be no greater than 50mV, preferably less.

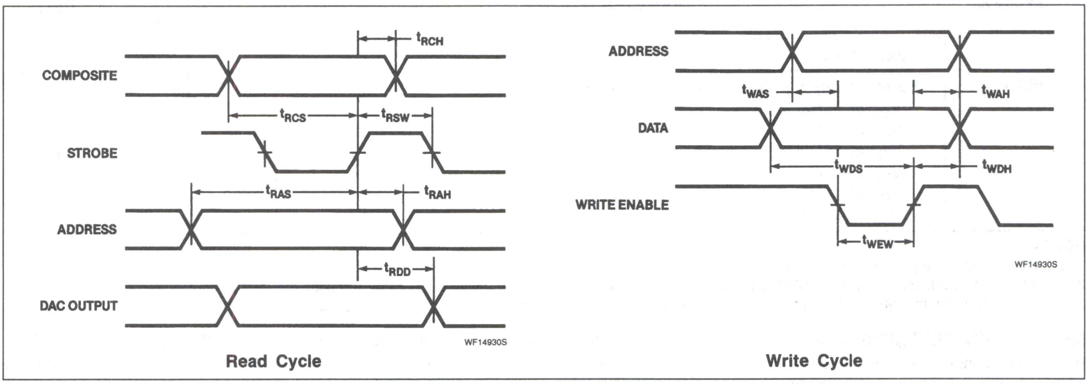
Pin 14: **V_{EE}.** The negative power supply is the main chip power source. V_{CC} is only used for TTL input buffers. As is usual, good bypassing techniques should be used. The chip itself has a good deal of power supply rejection — well up into the VHF frequency range — so no elaborate power supply filtering is necessary.

Pin 18: **NC.** This unused pin should be tied high or low.

Triple 4-Bit RGB D/A Converter With and Without Memory

NE5150/5151/5152

NE5150/5152 TIMING DIAGRAMS


COMPOSITE
STROBE
ADDRESS
DAC OUTPUT
t_{RCH}
t_{RCS}
t_{RSW}
t_{RAS}
t_{RAH}
t_{RDD}
WF14930S
ADDRESS
DATA
WRITE ENABLE
t_{WAS}
t_{WAH}
t_{WDS}
t_{WDH}
t_{WEW}
WF14930S

Read Cycle

Write Cycle

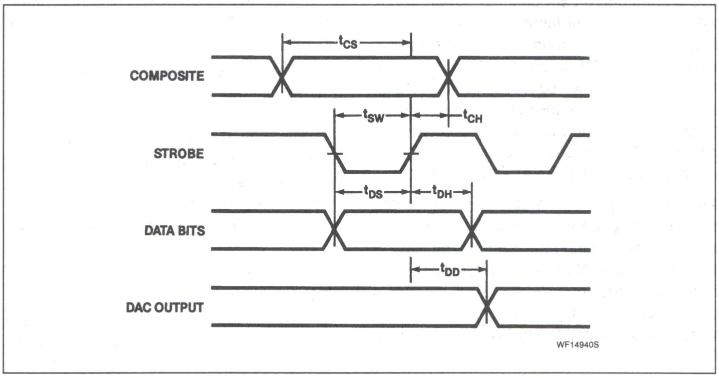
NE5151 PIN DESCRIPTION AND TIMING DIAGRAM

The eleven digital inputs D0 – D3, A0 – A3, $\overline{\text{WRITE}}_{G/R/B}$, and the unused Pin 18 of the NE5150 are replaced in the NE5151 with the three 4-bit DAC digital inputs G0 – G3, R0 – R3, and B0 – B3. All other pin functions (e.g., composite functions, power supplies, strobe, etc.) are identical to the NE5150.

NE5152 PIN DESCRIPTION

The NE5152 is a TTL-compatible-only version of the NE5150, operating off of a single +5V supply. V_{CC} Pins 6, 12 and 16 should be connected to +5V and Pin 14 to 0V. DAC output is referenced to V_{CC}.

NE5151 TIMING DIAGRAM


COMPOSITE
STROBE
DATA BITS
DAC OUTPUT
t_{CS}
t_{SW}
t_{CH}
t_{DS}
t_{DH}
t_{DD}
WF14940S

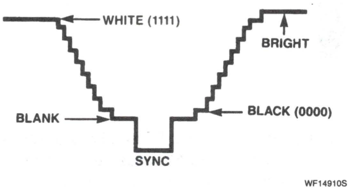
NE5150/NE5151/NE5152 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT[3]	CONDITION
1	X	X	0	X	X	-1031mV	SYNC[1]
1	X	X	1	X	X	-960mV	Enhanced SYNC[1]
0	1	X	0	X	X	-746mV	BLANK
0	1	X	1	X	X	-674mV	Enhanced BLANK
0	0	1	0	X	X	-71mV	WHITE
0	0	1	1	X	X	0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	-674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	-603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	-71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	0mV	Enhanced WHITE (EZS)

NOTES:

1. Green channel output only. RED and BLUE will output BLANK or Enhanced BLANK under these conditions.
2. For the NE5150/5152 the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.
3. Note output voltages in Logic Table are referenced to V_{CC} for the NE5152 only.

COMPOSITE VIDEO WAVEFORM


WHITE (1111)
BRIGHT
BLANK
BLACK (0000)
SYNC
WF14910S

AN1081
NE5150/51/52 Family of Video Digital-to-Analog Converters

Application Note

Author: Michael J. Sedayao

INTRODUCTION

Raster-scan systems and bit-mapped graphics are here to stay. For a computer to be of use, it needs an interactive means of communicating with the user. So for every computer, whether it is a 10MFLOP (millions of floating-point operations per second) supercomputer or a home computer for playing video games, some type of terminal or graphics display device is needed. Not long ago, inputs to the computer were made using stacks of Hollerith cards pushed into a hopper and then read into the computer. Results would then come from a printer. The hardcopy results were exactly what they looked like: final judgment from the computer. In order to respond, it was back to the punch-card machine. Needless to say, debugging programs became quite laborious. This problem led to the interactive display, allowing the user to enter information and see the results immediately. A new age in computing had arrived.

The areas of word processing, on-screen circuit simulation, and computer graphics developed with great rapidity. As technology improved, so did the ability to make larger displays having more colors and better resolution. As software developed, so did techniques such as windowing, the use of icons, and the ability to use graphic input devices such as mouses, light pens, and joysticks. Three-dimensional images and photographic quality reproduction soon followed.

Of the different technologies, how did raster scanning predominate over other forms? What differentiates bit-mapped graphics systems from character or vector-map systems? In the following sections it will become clear how technology and economics drove the market and, consequently, product development.

Displays: Raster, Vector Refresh, Storage Tube

A *raster* is technically a display of horizontal lines. How the display is created is what makes it unique. An electron beam generated by a CRT (Cathode Ray Tube) and containing video information, starts at the top left of the screen and traces a path to the right part of the screen (see Figure 1). It makes a slight angle as it travels across. The gun is then turned off as the beam rapidly returns to the left. It then repeats this zig-zag path until it reaches the bottom of the screen. The gun is again turned off as the beam travels back to the top of the screen. This entire process is repeated from 30 to 60 times per second so flicker is decreased (motion pictures or film typically display 24 images per second). What the electron beam has done is *scanned* its information onto the screen. This process is called *raster scanning.*

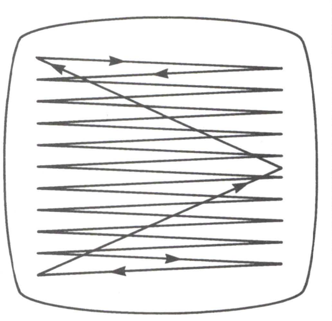


Figure 1. Raster-Scanned Display

All television sets display information in this manner. For television sets in the United States, the screen is redrawn 30 times per second. Additionally, the screen is *interlaced*, meaning that every other line is scanned and then the lines in between are scanned. This gives the illusion that the image is continuous. Since the television sets have 525 lines, 262.5 lines are scanned first (the odd field) and then the other 262.5 (the even field) are scanned. To visualize this, consider a 21-line system (see Figure 2). Scanning occurs at the above-mentioned 30Hz rate which is also known as the *frame rate*. Two fields (odd and even) equal one frame. Scanning 525 lines 30 times a second equals 15,750 horizontal lines scanned in a second. This is called the *horizontal scan frequency*. These are standard in the U.S., coming under the standard known as NTSC (National Television Standards Committee). In Europe, television has 625 lines and has a frame rate of 25Hz, or half the power line frequency, 50Hz.

Vector refresh displays, or stroke-writers, work on the principle that one line is the base unit of information. Each line then corresponds to a vector. Instead of scanning continuously, information is drawn line-by-line, hence the name stroke-writer. These systems off-load the refreshing tasks to special hardware, making the system slightly more cost-effective. Still, during the 1960's making them proved too expensive for everyday applications.

In 1971, Tektronix introduced the Direct View Storage Tube (DVST) for displaying and interfacing graphic data. It was based on oscilloscope techniques, storing information in a special, long-persistence phosphor which coats the inside of the screen. The display resolution is limited only by the phosphor grain size and the quality of the deflection circuitry. Although inexpensive, these devices were fine for oscilloscopes in the lab, but too cumbersome for fully interactive work. When the screen would redraw itself after the entry of new information, the sudden disappearance and reappearance was almost like looking at the light of a camera flashbulb. Another problem with the storage refresh screen was that when new information entered, it would write directly over the existing information. Only upon refreshing the screen would the new information be clear and readable. In many cases, the annoyance did not justify the low cost.

Bit-Mapped Graphics

In a bit-mapped graphics system, the screen is divided into individual elements called pixels, short for picture elements. When they say "bit-mapped", each pixel corresponds to a bit, or, in most cases, an address or memory location. This is what differentiates television from bit-mapped computer displays. Although both systems use raster scanning techniques, the information transmitted on television is continuous — a stream of analog information between horizontal sync pulses (the pulses used to denote the beginning and end of a horizontal line) — whereas in bit-mapped systems, each line is divided into discrete elements (the aforementioned pixels). The approximation of analog images would then be determined by the pixel density or screen resolution. As an example, Figure 3 shows a line approximated by a finite number of pixels.

The lines seem to staircase rather than flow because of the enlargement of the pixels. The effect is known in some computer graphics circles as "jaggies", short for jagged edges.

So, with more pixels, better resolution is possible. This is not without a price, though. Since each pixel corresponds to a memory location, memory cost rises dramatically as pixel resolution increases. Drawing speed

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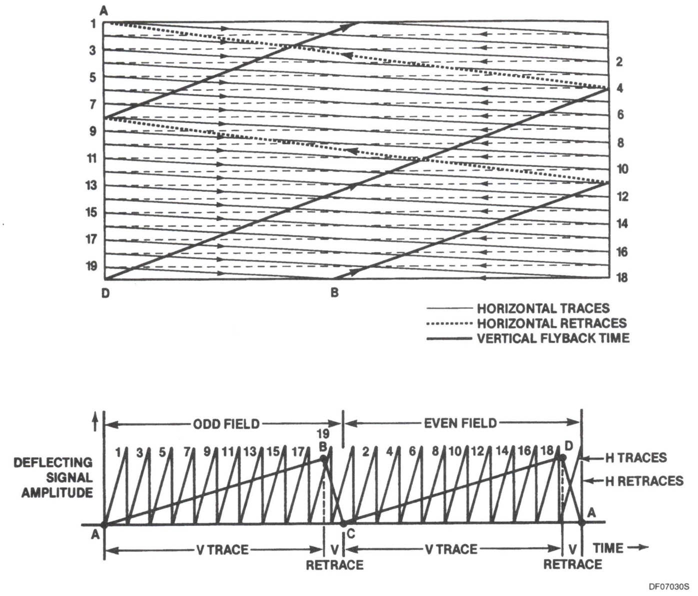

NOTES:

A sample scanning pattern for 21 interlaced lines per frame and 10½ lines per field. The corresponding H and V sawtooth deflection waveforms are shown below pattern. Starting at point A, the scanning motion continues through B, C, and D, and back to A again.

Figure 2. Interlaced Raster for 21-Line System

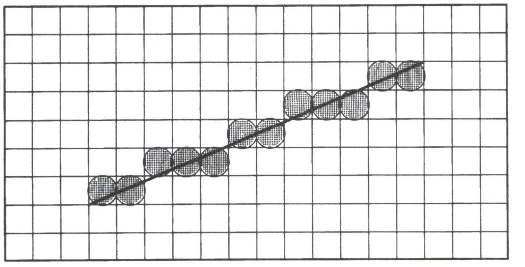

Figure 3. Ideal Line and Its Discrete Pixel Representation

must also increase since more pixels have to be drawn to maintain the ⩾30Hz frame rate needed to avoid flicker. Clearly then, the increase in bit-mapped graphics systems can be tied to the continuing price reductions in memory, specifically, the Dynamic Random Access Memory (DRAM). Fortunately, as the price has dropped, the memory size has not stood still. The last 14 years have seen size increases from 4k to 16k, 16k to 64k, 64k to 256k, and now, 256k to 1M bits of memory. One might expect to see DRAMs on the order of 4Mb within 2 to 3 years. Additionally, the continuing development of video RAMs cannot be ignored.

A bit-mapped system might be described in one of three ways. First, assume the display is monochrome and that each pixel can be represented by a certain number, for instance, 4 bits of information. This means that there are $2^4 = 16$ possible values of shading. Each bit of information can be represented by a "plane" of information. The plane would correspond to the area that was mapped by the pixels, namely the drawing area or display. Imagine an 8 × 8 pixel display. This means that there are 4 bit-planes and each pixel would have to pierce all four planes to give the proper information (see Figure 4). This is a fairly quick way to draw the screen since the data goes directly from the bit-map to the DAC (Digital/Analog Converter; DAC is singular here since the display is monochrome).

A direct conversion system for color is the second step. This is just an upgrade of the first case. Instead of 4 bit-planes, there are 12: three sets of the 4 planes for the three primary colors red, green, and blue. The advantage here is that there are now $2^{12} = 4096$ different colors, but the corresponding disadvantage is that the memory requirement has tripled. For more bit resolution per pixel, the associated memory demands increase by 3 times the pixel size times n, where n is the additional bit of resolution per pixel.

The third type of bit-map system uses a color look-up table (CLUT) as the driver for the display. The operation is straightforward. As the controller scans the bit-map each time it comes upon a pixel, it retrieves the bits which are then decoded into an address. This address is a pointer to the look-up table where sixteen 12-bit words (colors) are stored (see Figure 5). Once selected, that word is then sent to the color DACs and, from there, to the screen. The idea is similar to that of having cache memory in a computer, a fast memory used when the information in the memory is frequently accessed. Note that the bit-planes grow as n for 2^n additional colors while memory grows for 3n in the direct conversion case, a definite savings in memory.

The limitation in this case is that only 16 colors can be displayed at a time. In some systems, however, the CLUT is fast enough to be reloaded during the horizontal retrace time (CLUT size is sometimes referred to as the maximum number of colors that can be displayed on one horizontal line). This is especially important if the image is to simulate a smooth motion such as the rotation of a merry-go-round or the movement of an object with mirrored surfaces. In most cases, 16 colors is sufficient for any single display. 64 colors (6 bit-planes) is extremely good. 256 colors (8 bit-planes) is definitely a luxury.

It's clear that the memory speed and memory density, which are direct functions of the color and screen resolution, play a large part in the feasibility of a bit-mapped system. For that reason, the enormous gains and technological advancements in the field of memory design have made bit-mapped raster-scan graphic systems the best choice for both cost and performance.

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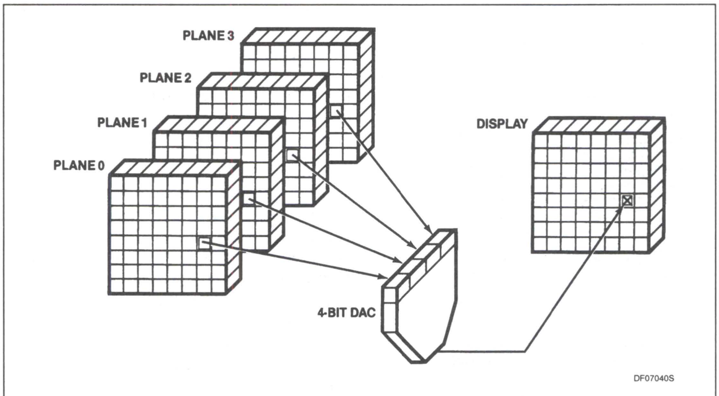

Figure 4. Monochrome Bit-Map With Direct Conversion to Display

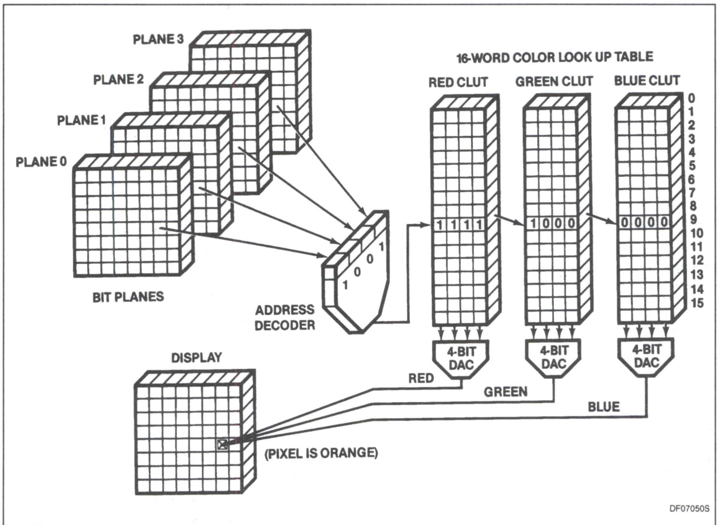

Figure 5. Color Bit-Map With 16-Word Color Look-Up Table

ISSUES FOR GRAPHIC DISPLAY SYSTEMS

Making the DAC Fit the Application

When designing graphic display systems, there are many decisions to be made in specifying the hardware and software needed for a system. What kind of speed is necessary in a given application? What kind of resolution will the users of the system require? Is color needed or will monochrome be adequate? If color, how many colors? Will images be viewed in two or three dimensions? How much memory is needed? How should the microprocessor/CRT controller/video DAC/frame buffer be matched with the rest of the system? What's the best type of software for a particular application? and on and on...

These questions could form the subject of an entire book and so will not be discussed in detail. This section will, however, discuss the few issues needed in the selection of the proper video DAC for a system.

Display Resolution vs Bit Resolution

When the quality of a display terminal is being evaluated, one primary consideration is the kind of resolution it has. There are two different types of resolution: display resolution, which is determined by the monitor and cannot be changed by the design; and bit resolution, which is dependent on the design of the video DAC used.

Display resolution determines how many pixels can be projected onto the monitor at any one time. (Actually, only one pixel is displayed on the screen at a time, in rapid succession). Table 1 shows commonly-used screen resolutions corresponding to various applications.

However, since each pixel must correspond to a memory element, the more pixels per screen the faster the DAC and video RAM must be in order to write the information to the screen fast enough to avoid flicker. This imposes speed requirements that have to be satisfied.

The other type of resolution, bit resolution, depends on the type of DAC used. The number of bits converted also determines the size of the color palette which is the number of possible colors that can be displayed. This should not be confused with the number of colors displayed at once (see Section on Color Look-Up Tables). Assuming that the monitor is an RGB-type, the bit resolution, n, must be multiplied by 3 to get the total bit resolution, 3n. Taking this number as 2^{3n} gives the size of our color palette. Table 2 shows common bit sizes for video DACs with their corresponding palettes.

It should be clear that, if imaging is the goal, a higher bit resolution gives access to the assorted tones and mixtures of colors that make color graphics as realistic as possible. The major problems associated with higher-resolution DACs are that they are larger and more complex than lower-resolution DACs and tend to take longer for their signals to settle. This has a direct effect on selection of the proper DAC for a particular system because of the DAC's bandwidth and because of the need to weigh advantages and disadvantages of higher and lower bit resolutions.

For a low-end personal computer graphics screen on which the pixels can actually be seen at arm's length, it makes little sense to have a bit resolution that shows flesh tones because the benefit of the large palette is defeated by a screen that shows jagged edges. On the other hand, having a high screen resolution with a limited amount of colors does not defeat the purpose in the same way — if many colors aren't needed.

Integrated circuit layout, for instance, may not require thousands of colors — only enough to distinguish 12 – 15 masks; but sharply defined edges and zooming ability are needed to examine the circuit. The need for this user could be a bit resolution of 2 (64 colors) and a display resolution of 1024 × 1280.

For all this talk of colors and bit resolution, monochrome should not be totally ignored. After all, people got along fine with black and white TV for years before color came along. For applications such as word processing or

Table 1. Display Resolutions With Applications

DISPLAY RESOLUTION	APPLICATION
250 × 500	Low-end personal computers (home computers)
640 × 480	High-end personal computers
600 × 800	Next-generation personal computers
768 × 576	Next-generation personal computers
1024 × 800	Workstations
1024 × 1024	High-end workstations
1024 × 1280	High-end graphics terminals (CAE/CAD)
1024 × 1500	High-end graphics terminals (3-D Imaging)
1500 × 1500	High-end graphics terminals
2048 × 2048	High-end graphics terminals (photo quality)

Table 2. Bit Resolution With Palette Size

BITS/DAC	RGB	PALETTE SIZE	APPLICATION
1	3	8	Digital RGB, "rainbow colors"
2	6	64	Some home and personal computers
4	12	4096	Color workstations, CAD/CAE
6	18	262,144	High-end CAD/CAE, medical imaging
8	24	16,777,216	Photographic quality reproduction

Table 3. Display Resolution With Minimum DAC Speed

DISPLAY RESOLUTION	# PIXELS	MINIMUM DAC SPEED
250 × 500	125,000	10MHz
640 × 480	308,000	25MHz
600 × 800	480,000	38MHz
768 × 576	443,000	35MHz
1024 × 800	820,000	65MHz
1024 × 1024	1,049,000	85MHz
1024 × 1280	1,311,000	105MHz
1024 × 1500	1,536,000	125MHz
1500 × 1500	2,250,000	180MHz
2048 × 2048	4,195,000	330MHz

circuit design, monochrome is fine. To achieve different shades of black and white, no chrominance operation is necessary. All of the bit resolution can be done with one DAC to operate on the luminance, or brightness signal. In this case, the brightness resolution can be said to be 2^n. Remember, the decision to go with color or monochrome does not rest upon the designers of the graphics board. A monitor is either color or monochrome to begin with. Adding a color video DAC won't change that.

DAC Speed

The DAC's update rate or bandwidth is a crucial consideration in choosing a DAC if the type of monitor has already been specified. For raster-scan systems, a few calculations can be made to determine the minimum speed required for the DAC.

First of all, assume that the screen needs to be refreshed at 60Hz to avoid flicker. To account for the electron beam going back to the top to start the next frame, assume that the retrace time is 30% of the drawing time. Multiply the frame rate by 1.3 to account for the retrace. Thus, the minimum bandwidth for the DAC would be determined by the following formula:

$$\text{Speed (Hz)} = 1.3 \text{ (retrace factor)} \times \# \text{ pixels} \times 60\text{Hz (frame rate)}$$

For the screen resolutions noted earlier, a new table can be generated for the minimum DAC speed required (see Figure 8).

For the 60Hz frame rate, the screen is probably not interlaced. Interlacing the screen at 30Hz would give the same effect because interlacing gives the *illusion* that the screen is being refreshed at a faster rate. The DAC would only have to operate at a quarter of the speed of the 60Hz non-interlaced rate because only half of the lines are being drawn at a speed that's half the 60Hz frame rate. This is how scanning operates under the NTSC television standard. The FCC says that televisions can't refresh the screen faster than 30Hz, so interlacing was developed to get around it. There are no such restrictions in graphics monitors. In fact, there are monitors that have horizontal scan rates as much as 4 times faster (65kHz) than that for television (15.75kHz).

Color Look-Up Tables: Yes or No?

As mentioned in the Bit-Mapped Graphics section, graphic systems may have direct conversion from a bit-map or they can use color look-up tables (CLUTs). It should be pointed out that one is not necessarily faster than the other. Speed depends primarily on the system. A fast CLUT is of no use if the external frame buffer can't load a new set of colors into the CLUT during the retrace time (horizontal or vertical). A video DAC without the CLUT may be faster since it can bypass the memory accesses needed for the CLUT, but, as seen in the Bit-Mapped Graphics section, the extra cost of the bit-planes (1 million additional bits for a 1024 × 1024 display) may be excessive, and accessing the additional planes may produce some design problems.

If a CLUT is needed, the size of the CLUT should also be a major consideration. Each bit-plane added requires 2^n more memory cells. Constraints on die-size and power requirements become apparent. Also, one must ask whether one needs 16, 32, 64, 128, or 256 colors on every line. This depends on the color resolution desired *for the entire screen*. An easy way to determine the system needs is to picture the most common scene that would be displayed. The general rule is that the more complex and three-dimensional the images that are required, the more variations and shading are needed to truly represent them. Conversely, if the image is simple and two-dimensional, fewer colors would be needed. An example of the former would be geological formations. For the latter, consider the colors of flags of the world's nations. Almost all of them can be displayed with a CLUT of 16 colors. Remember, this refers to the number of colors needed at any one time.

No flag has more than 16 colors. The range of colors available for display after CLUT refresh depends on the color resolution or the number of data bits for each pixel.

Gamma Correction

A problem encountered in both television systems and in display monitors in general is the gamma effect. This is due to the nonlinear relationship between light output and the signal voltage applied to a cathode-ray tube. Although it would be desirable to have the luminous output of the phosphors on the display to vary directly with the changes in the signal applied to it, they usually do not. Each monitor has its own characteristic, but the international convention is to assume that the fractional value of the luminous output can be approximated by raising the percentage of display signal input to the 2.2 power. For example, a 60% of full-scale input signal will result in 33% of the full-scale luminous output ($0.6^{2.2} = 0.33$).

In Figure 6, the monitor does not respond linearly for a linear input signal. Adding a gamma correction circuit can take care of this problem.

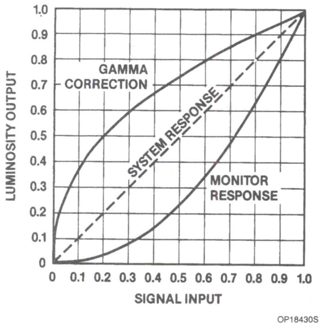

Figure 6. Monitor and System Response With Gamma Correction

In the television industry, correction for this non-linearity takes place at the camera as the image is recorded. The camera takes the 2.2 root of its full-scale fractional value. This cancels the gamma effect and produces a linear system response.

In graphics systems for which the image is generated from digital information, DACs convert the digital information into a voltage that drives the guns of the CRT. Basically, the systems designer has three choices:

1. Correct for gamma in the software. This can be done by using the 2.2 power/root compensation to pixel values before they are stored into the frame buffer. This could be an expensive addition to the software and might slow the overall system because of the added computation time.
2. Apply analog gamma correction in the hardware. The correction factor could be done with additional circuitry to the output of the DAC before it drives the monitor. As mentioned before, this presents an additional hardware overhead. This is not done, however, without some risks. Since every monitor has individual characteristics, the resulting correction would not look the same on every monitor.
3. Ignore the whole subject and accept the non-linearity of the luminous output as a characteristic of the system. Since most graphics applications are for the generation of images for specific problems and not for the lifelike reproduction of scenes (although it would be desirable), a gamma correction mechanism is unnecessary.

This last approach seems to be the most prevalent solution since few, if any, DACs contain gamma correction circuitry. When graphics software designers select their colors, they do so for the best visual performance. This fine-tuning for colors and shading is really software gamma correction because they can select the digital information needed for colors and intensity and see the results from the other side of the monitor.

CIRCUIT FEATURES AND OPERATION

This section covers the basic features and operation of the NE5150/51/52. The first two sections briefly discuss RS-170 and RS-343A, the standards for color and monochrome video systems. The next section covers the composite video signal (CVS) that is specified in the two previous standards.

RS-343A and RS-170

RS-170, the Electrical Performance Standards for Monochrome Television Studio Facilities, and RS-343A, the Electrical Performance Standards for High Resolution Monochrome Closed Circuit Television Cameras, were issued in November 1957 and September 1969, respectively, by the EIA (Electronic Industries Association). The specifications outlined in RS-343A determine the voltage levels required for the part.

Composite Video Signal

Shown in Figure 7 is a section of a composite video signal. With the exception of the BRIGHT function, the levels and tolerances are specified by RS-343A.

Sync, Blank, and Setup

The sync signal is situated 286mV (40 IRE) below the blanking level which lies 714mV (100 IRE) below the reference white level (next section). The sync signal synchronizes the monitor horizontal and vertical scanning. This, and the rest of the composite video signal, is not to be confused with the composite sync signal which is often used for a combined horizontal *and* vertical sync signal.

The blank level lies just below the reference black level, separated by an amount known as the setup. The difference between reference white and the blanking level is defined as 100 IRE. Applying the blanking level voltage to the monitor input will reduce the CRT electron beam current so that there will be no visible trace of the electron gun on the phosphor.

For television, the setup is defined as the *ratio* between the reference white and the reference black level measured from the blanking level. It is usually expressed as a percentage. Basically, it's the difference between the reference black level and the composite blanking level. RS-343A has set the limits of the setup as 7.5 ±5 IRE. Any value between 2.5 to 12.5% of the blanked picture signal can be designated as the setup (2.5 – 12.5 IRE or 17.85 – 89.25mV). Since the full-scale range of the video signal represents 100 IRE, a percentage of the signal is synonymous with its IRE value. For the NE5150, the setup is 71mV or 10 IRE.

Reference Black and White

Reference black and white correspond to the signal levels for a maximum limit of black and white peaks. White corresponds to having all color guns on and black to having all guns off. The gray scale, which refers to the rest of the color values and contains a majority of the signal information, is defined by the amplitude between reference white and reference black. Since the reference white to blanking level is fixed at 100 IRE, the reference black level is determined by the setup. Since the setup can be between 2.5 and 12.5 IRE, the gray scale range must reflect those tolerances and so has a range of 92.5 ±5 IRE (660.5mV ±35.7mV).

To allow for a BRIGHT function, the NE5150/51/52 family of video DACs were designed for a full-scale range (blank to reference white) of 675mV (about 94 IRE) and a gray-scale range of 643mV (about 90 IRE). Using the BRIGHT function adds 71mV (10 IRE) to the reference white value.

For instance, in a 12-bit system like the NE5150/51/52, using 4 bits/DAC would enable us to resolve the gray scale range into 16 parts. For the NE5150, that would be about 40.1mV (5.6 IRE) = 1 LSB. For 6 bits, 64 parts could be resolved, and for 8 bits, 256 parts.

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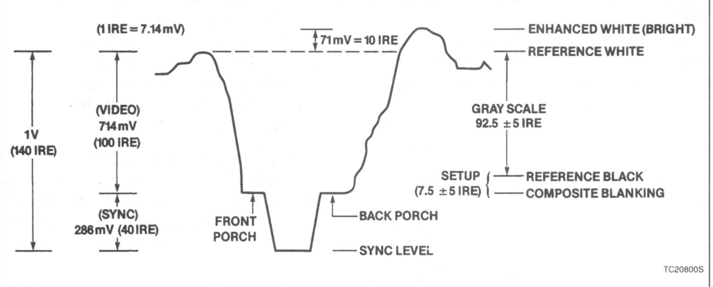

Figure 7. RS-343A Video and Sync Levels

NE5150/NE5151/NE5152 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT[3]	CONDITION
1	X	X	0	X	X	−1031mV	SYNC[1]
1	X	X	1	X	X	−960mV	Enhanced SYNC[1]
0	1	X	0	X	X	−746mV	BLANK
0	1	X	1	X	X	−674mV	Enhanced BLANK
0	0	1	0	X	X	−71mV	WHITE
0	0	1	1	X	X	0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	−674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	−603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	−71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	0mV	Enhanced WHITE (EZS)

NOTES:

1. Green channel output only. RED and BLUE will output BLANK or ENHANCED BLANK (BRIGHT ON) under these conditions.
2. For the NE5150/5152, the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.
3. Note output voltages in Logic Table are referenced to V_{CC} for the NE5152 only.

Device Description and Operation

Corresponding to the RS-343A requirements outlined in the previous section, the logic table indicates the output voltages given the digital inputs shown. Although the output voltages for the DACs are shown, the user should also know what is happening to the circuit and how the priority given to each function influences the output. [All ones (1111) is called zero-scale (ZS) and all zeroes (0000) is called full-scale (FS).]

The BLANK command presets all the latches to all zeroes (0000) and sends the output to its blanking level of 100 ± 5 IRE below reference white (−71mV) or about −746mV. When BRIGHT is on (a '1'), the output is raised 10 IRE (71mV or ¹⁄₉th of full-scale) to −674mV. BLANK overrides WHITE and is overridden by SYNC.

The WHITE command presets the latches to all ones (1111) and outputs −71mV to all DACs. When the BRIGHT command is on, this value is raised to 0V. WHITE will be overridden by both SYNC and BLANK.

The SYNC command presets all of the latches to zeroes and turns on the BLANK switch. In addition, it turns on a 40 IRE switch (drops voltage 286mV) in the GREEN channel only. So the GREEN channel sits at 140 IRE down and the RED and BLUE channels will be 100 IRE below ground.

The BRIGHT command turns off one current switch within the circuit and adds 10 IRE (71mV) to the output levels of all three guns. This comes in handy if using a cursor (optional blinking) to brighten other parts of the screen. This switch cannot be overridden by any other switch.

Referring to the pinouts of both the NE5150/52 and the NE5151 (see Figure 8), there are additional considerations.

The $\overline{\text{WRITE}}_G$, $\overline{\text{WRITE}}_R$, and $\overline{\text{WRITE}}_B$ pins are the write enable pins for each of the 16 × 4 memories in the CLUT. When these pins are pulled High, the memory is then in the READ mode. This is the normal mode of operation. To write to the memory, **one** of the pins must be pulled Low. The data on D0 – D3 will then be written to the memory location A0 – A3 of the corresponding WRITE pin.

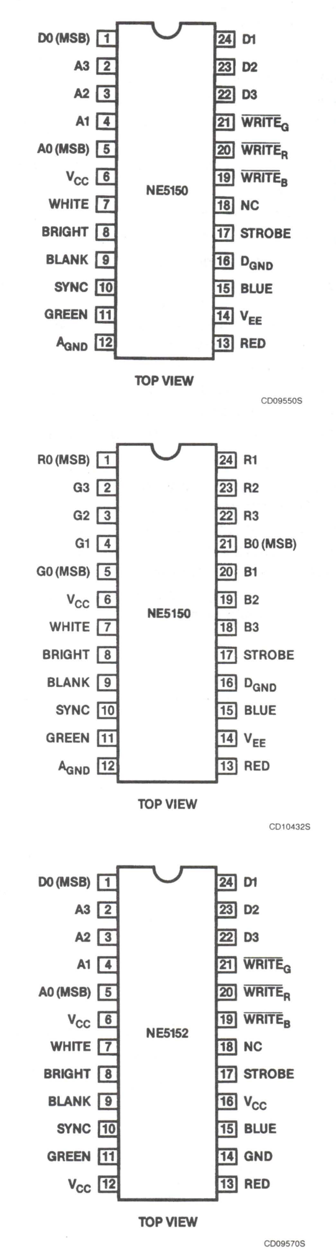
D0 (MSB) 1
A3 2
A2 3
A1 4
A0 (MSB) 5
VCC 6
WHITE 7
BRIGHT 8
BLANK 9
SYNC 10
GREEN 11
AGND 12
24 D1
23 D2
22 D3
21 WRITEG
20 WRITER
19 WRITEB
18 NC
17 STROBE
16 DGND
15 BLUE
14 VEE
13 RED
NE5150
TOP VIEW
CD09550S
R0 (MSB) 1
G3 2
G2 3
G1 4
G0 (MSB) 5
VCC 6
WHITE 7
BRIGHT 8
BLANK 9
SYNC 10
GREEN 11
AGND 12
24 R1
23 R2
22 R3
21 B0 (MSB)
20 B1
19 B2
18 B3
17 STROBE
16 DGND
15 BLUE
14 VEE
13 RED
NE5150
TOP VIEW
CD10432S
D0 (MSB) 1
A3 2
A2 3
A1 4
A0 (MSB) 5
VCC 6
WHITE 7
BRIGHT 8
BLANK 9
SYNC 10
GREEN 11
VCC 12
24 D1
23 D2
22 D3
21 WRITEG
20 WRITER
19 WRITEB
18 NC
17 STROBE
16 VCC
15 BLUE
14 GND
13 RED
NE5152
TOP VIEW
CD09570S

Figure 8. Pinouts of NE5150/52 and NE5151

STROBE is the main system clock and synchronizes all digital operations on the DAC.

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The strobe is ECL and TTL compatible and demands no special drive requirements. The positive edge of STROBE clocks the latches.

The GREEN, RED, and BLUE pins are the analog outputs of the DACs. The DACs are voltage output and need no external components (75Ω resistors are on-chip). The output voltage range is approximately 0 to −1V and is independent of the input logic (either TTL or ECL).

The DATA and ADDRESS bits are designated so that D0 and A0 represent the most significant data and address bits (MSB), respectively. Similarly, D3 and A3 correspond to the least significant data and address bits (LSB). Since the NE5151 has no CLUT, there is no need for the address pins (4) or the write enable pins (3). Adding the NC (no connection) pin (1) gives the eight additional input pins for two 4-bit DACs. The original data bus now carries the logic for the RED gun.

Analog and digital ground (A_{GND} and D_{GND}) should always be connected together in any configuration and should not have more than 50mV of potential between them to insure proper operation of the device. The next section will cover connection of V_{CC} and V_{EE}, in addition to A_{GND} and D_{GND}, on different system configurations.

Using Different Logic and Supply Voltages

Different users have different needs. Some have access to dual supplies, other only to single-ended supplies. Signal logic may be TTL or ECL. In any case or configuration, the NE5150/51/52 family can be used. The following configurations cover most cases.

Explanation of the configurations are as follows:

A. Case A shows a basic ECL configuration for the NE5150 and NE5151. The signal voltage is basic ECL with a −1.3V threshold and is powered from ground and −5V (or −5.2V). Since the TTL buffers are no longer needed, V_{CC} is tied to analog and digital ground (A_{GND} and D_{GND}), excluding the buffers from the circuit.

B. In some cases, people use ECL logic but run it off a single supply, +5V and ground. In this case, operation is the same except that the supplies are shifted up 5V. In this new ECL mode, the threshold −1.3V is moved up by 5V to +3.7V. ECL operation is not available for the NE5152.

C. For TTL operation in the NE5150 and NE5151, dual supplies are normally needed. If available, standard TTL-level signals with a +1.4V threshold (between a logic '1' Low of 2.0V and a logic '0' High of 0.8V) can be connected directly.

D. In some situations, a dual supply is not available. Single-supply TTL operation is made possible by making similar connections and by pulling up the inputs of each pin with a 10kΩ resistor connected to V_{CC} = +5V. This is necessary because the threshold is now 3.7V.

E. Case (D) necessitated the construction of the NE5152, which has only one mode using a single 5V supply and accepts TTL inputs. A_{GND} and D_{GND} become V_{CCA} and V_{CCD} and are tied to V_{CC}.

   In some cases, a single supply is used and the internal ECL mode has been shifted up to the positive supply; the output voltage will be swinging from 0V to −1V, but, referenced from V_{CC} = +5V, it will swing from 5V to 4V. If the monitor accepts only positive sync pulses or video information, DC-offsetting the outputs or AC-coupling them with 1μF capacitors would make the signal acceptable to the monitor.

Since the outputs have internal 75Ω resistors, the monitor should have a 75Ω resistor to ground in order to doubly-terminate the cable and to prevent reflections.

Unused Inputs

For ECL mode (NE5150), any unused inputs, regardless of desired permanent stage, should be tied to a fixed-level output of an unused gate.

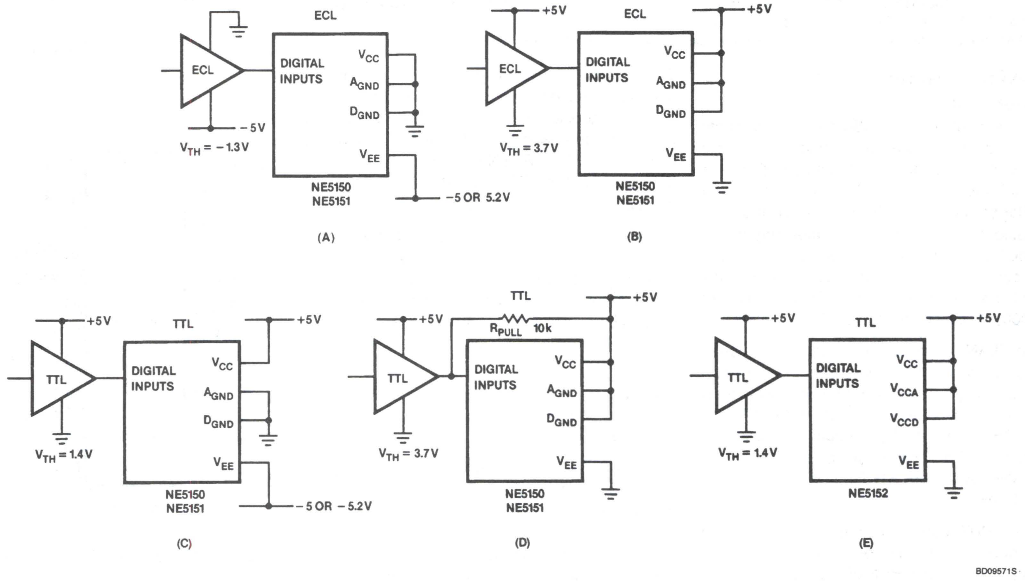

Figure 9. Video DAC Modes of Operation

BLOCK DIAGRAMS

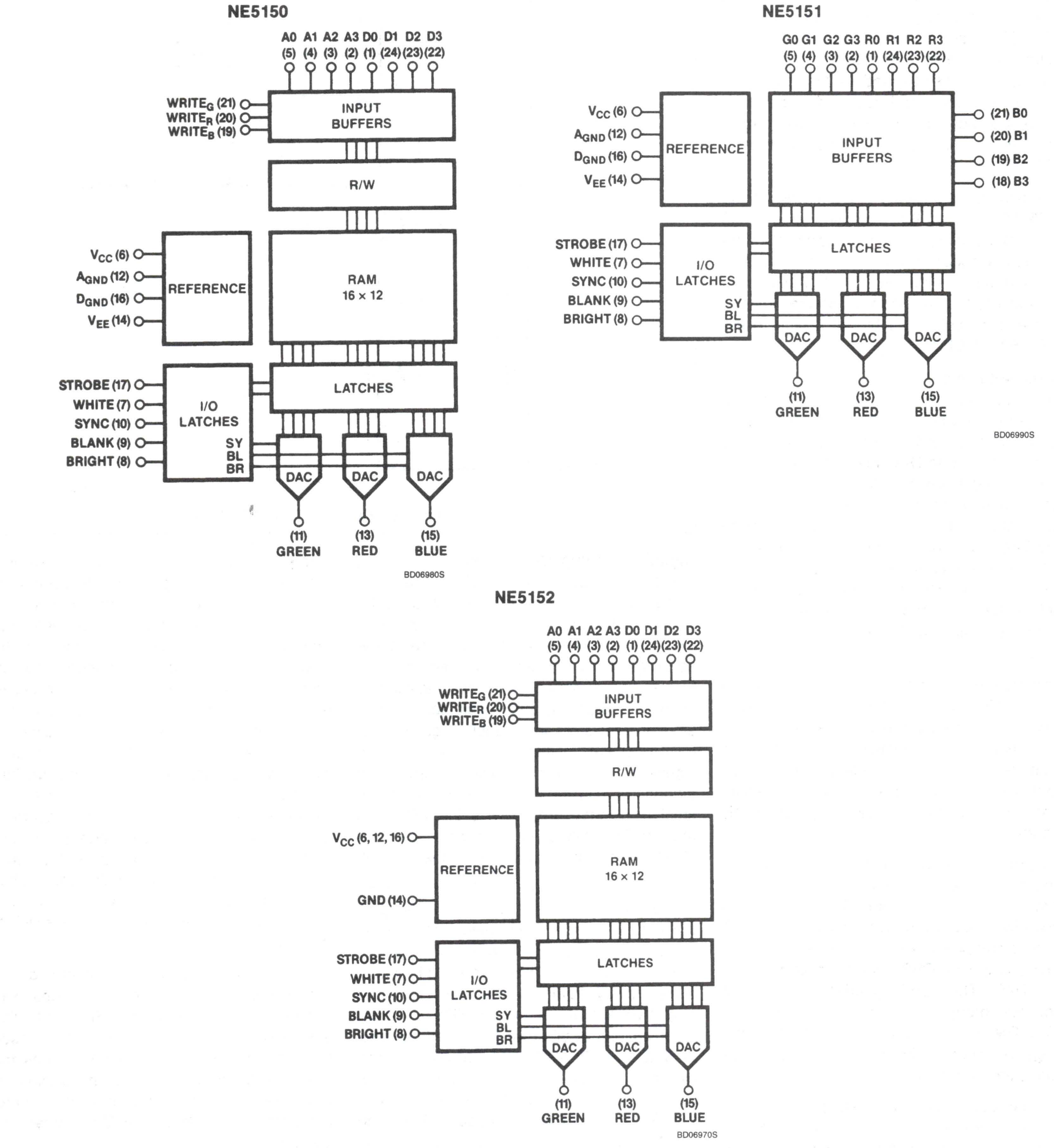
NE5150
A0 A1 A2 A3 D0 D1 D2 D3
(5) (4) (3) (2) (1) (24) (23) (22)
WRITE$_G$ (21)
WRITE$_R$ (20)
WRITE$_B$ (19)
INPUT BUFFERS
R/W
V$_{CC}$ (6)
A$_{GND}$ (12)
D$_{GND}$ (16)
V$_{EE}$ (14)
REFERENCE
RAM 16 × 12
STROBE (17)
WHITE (7)
SYNC (10)
BLANK (9)
BRIGHT (8)
I/O LATCHES
SY
BL
BR
LATCHES
DAC
DAC
DAC
(11) GREEN
(13) RED
(15) BLUE
BD06980S
NE5151
G0 G1 G2 G3 R0 R1 R2 R3
(5) (4) (3) (2) (1) (24) (23) (22)
V$_{CC}$ (6)
A$_{GND}$ (12)
D$_{GND}$ (16)
V$_{EE}$ (14)
REFERENCE
INPUT BUFFERS
(21) B0
(20) B1
(19) B2
(18) B3
STROBE (17)
WHITE (7)
SYNC (10)
BLANK (9)
BRIGHT (8)
I/O LATCHES
SY
BL
BR
LATCHES
DAC
DAC
DAC
(11) GREEN
(13) RED
(15) BLUE
BD06990S
NE5152
A0 A1 A2 A3 D0 D1 D2 D3
(5) (4) (3) (2) (1) (24) (23) (22)
WRITE$_G$ (21)
WRITE$_R$ (20)
WRITE$_B$ (19)
INPUT BUFFERS
R/W
V$_{CC}$ (6, 12, 16)
GND (14)
REFERENCE
RAM 16 × 12
STROBE (17)
WHITE (7)
SYNC (10)
BLANK (9)
BRIGHT (8)
I/O LATCHES
SY
BL
BR
LATCHES
DAC
DAC
DAC
(11) GREEN
(13) RED
(15) BLUE
BD06970S

Figure 10. NE5150/51/52 Block Diagrams

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Circuit Description

As can be seen from the block diagrams in Figure 13, the only difference between the NE5150/52 and the NE5151 is the lack of a color look-up table on the NE5151. Bypassing the CLUT with its assorted address decoding, sense amplifiers, and read/write logic enables it to not only use 200mW less power, but also to increase its update rate to 150MHz.

The NE5151 is basically the same die as the NE5150/52, with the exception of a metal mask option that permits it to bypass all of the circuitry associated with the CLUT. It is also bonded differently to enable all 12 bits to be loaded into the DAC at any one time instead of being multiplexed 4 bits at a time to the NE5150/52 CLUT.

DAC Reference

The need for separate references for the DACs resulted from the problems associated with glitching and crosstalk between the DACs. When one DAC maintains a constant value through pixel updates, while another undergoes major transitions such as the 1111 to 0000 on/off switching of currents through the DAC, feedthrough can be expected if all 3 DACs derive their reference voltage from the same source. Having separate references solves this problem. It also isolates the DACs from each other and the other parts of the circuit.

The reasons for choosing the DAC shown in Figure 12 are its simplicity, the bandgap's insensitivity to temperature variations, and its excellent supply rejection (PSRR) through high frequencies. It consists of a PTAT current source supplying a bandgap reference. The output of the bandgap is approximately −1.2V.

To provide the bias for the different current sources on each of the DAC stages, the circuit uses a control amplifier that provides negative feedback to maintain its stability. BIT and its complement drive the differential pair that (along with QS2) makes up one part of the DAC. The bandgap drives the current sources through the control amplifier. If the bias line voltage should rise or fall, the negative feedback in the QS1 and QS3 current path would correct for it.

The control amplifier consists of a transconductance stage driving an emitter-follower. The output of the emitter-follower provides a low-output impedance line that drives QS4. The inclusion of QS4 prevents switching transients from degrading settling time. The control amplifier has a 60MHz unity-gain bandwidth, providing power supply rejection up into the VHF range.

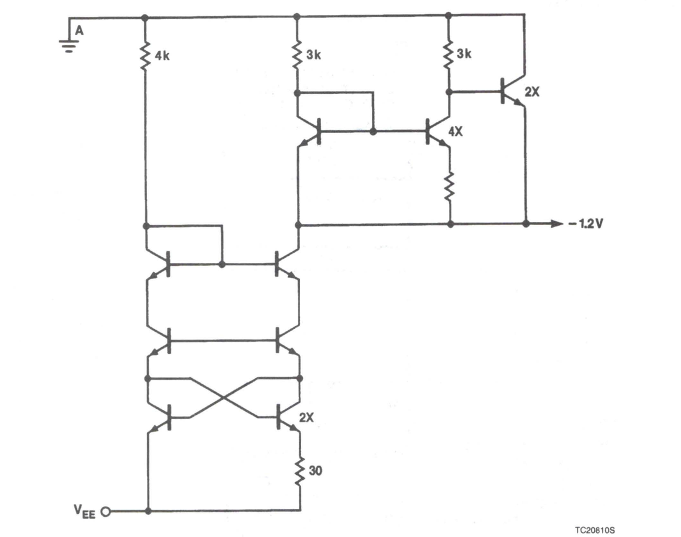

Figure 11. Bandgap Reference for DAC (1 of 3)

Digital-to-Analog Converters

The three DACs consist of differential pairs that are switched on or off depending on the value of the bits. Each of the transistors switches a different amount of current depending on the significance of each bit (see Figure 13). Although only one transistor is shown for each bit, the circuit actually has several transistors in parallel to get the required current. In this case, B3 is the least significant bit since it switches the least amount of current and would produce the smallest voltage drop across the 75Ω load resistor. The reverse is true for B0, the most significant bit, since it draws the most current.

So for all bits low, 0000, all of the current would go through the load resistor, bringing the output voltage to its lowest point. If all three DACs are low, this would correspond to reference BLACK. All bits high, or 1111, shunt current away from the load and leave the output voltage at reference WHITE. Different combinations of bits give 16 values between WHITE and BLACK. One additional 2mA switch is turned on by the input value of BRIGHT, which level-shifts the output by 1/9th the full-scale value, or about 10%. The BLANK and SYNC pins work in a similar manner. Refer to the Logic Table beside Figure 8 for the output voltages for each of these functions.

Some of the problems associated with DACs can be attributed to switching glitches, usually measured in terms of glitch energy. Glitching occurs when digital switching of the transistors causes spikes onto the collectors of the current sources to each of the differential pairs. These current spikes charge the collector-base capacitance, C_{JC}, of the collector transistor, and result in a slower settling time. The asymmetrical turn-on/off behavior of bipolar transistors and mismatched load bit-wiring capacitances also contribute to glitches. This can also be seen as an overshoot of the waveform, a "glitch" on the rising or falling edge of what should look like a square wave. Signals that overshoot the desired analog output level consequently take longer to settle to their final value. The measure of this overshoot is the glitch energy, usually given in pV-sec. The units do not actually work out as units of energy or Joules, which is C-V (Coulomb-Volts), but result from measuring the area of the glitch [Area = Height (V) × Width (psec)].

The NE5150/51/52 resolves this problem by putting the current sources in series with another set of transistors (see Figure 14). The stage below the differential pair is then biased by a low-impedance line which reduces the effect of the current spiking. The biasing for the lower transistor comes from the control amplifier mentioned in the DAC Reference Section.

Video DAC Timing

For the NE5150 and NE5152, the presence of the memory dictates both a READ and a WRITE cycle, whereas the NE5151 needs only one diagram. The explanation of each of the waveforms can be found in the timing glossary. For the guaranteed specifications, the user is referred to the data sheet.

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NE5150/52 (With CLUT)

In the NE5150/52 READ cycle, the COMPOSITE signal refers to either the WHITE, BRIGHT, BLANK, or SYNC signals. The read composite hold time, t_{RCH}, is defined from the rising edge of the strobe to the end of the composite pulse. This is the required time the composite signal must remain on the bus for latching. The time between the end of the composite pulse to the next rising edge of the strobe defines the read composite setup time, t_{RCS}. This is the same as the read address setup time, t_{RAS}. The read DAC delay time, t_{RDD}, is the propagation time of the signal through the device clocked from the strobe to the 50% change of the DAC output.

In the WRITE cycle, t_{WAS}, the write address setup time is defined by the start of address to the falling edge of the write enable strobe. At the end of this time, data can be written to the CLUT. Both ADDRESS and DATA must remain latched until they reach the rising edge of the WRITE ENABLE. This defines the WRITE ENABLE pulse width, t_{WEW}. The data should also be latched at the same time as the address. The start of the data (and address) to the end of the write enable pulse is defined as t_{WDS}, or the write data setup time. After the write pulse finishes, an address and data hold time is also specified.

NE5151 (No CLUT)

Since the NE5151 has no memory for the signal to propagate through, it typically has a faster conversion time. As can be seen from the pinouts, the three 4-bit words enter the DAC simultaneously as opposed to the sequential 4-bit loading scheme used in the NE5150/52. With no memory, there's no need for READ or WRITE cycles and so there is only one standard timing diagram. (See Figure 16).

This timing diagram is similar to the READ cycle of the NE5150/52 with the exception that addresses are not clocked to the CLUT; instead, data bits are sent directly to the DACs. In this case, t_{DH} is analogous to the address hold time in the NE5150/52. All other definitions are analogous to the earlier READ case.

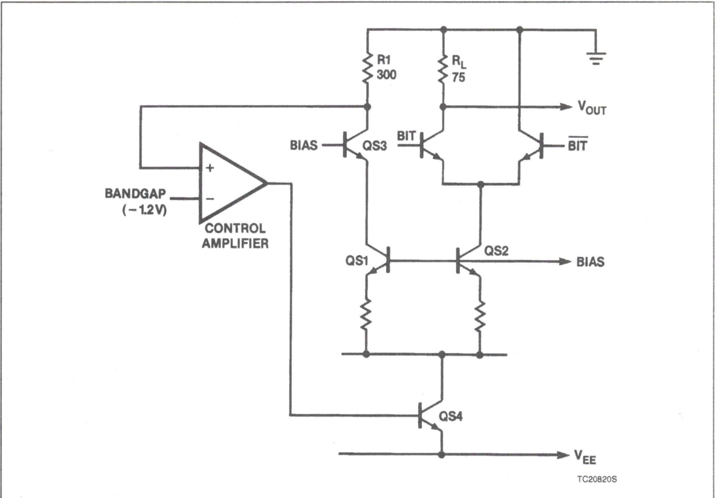

Figure 12. Negative Feedback Referenced to Bandgap

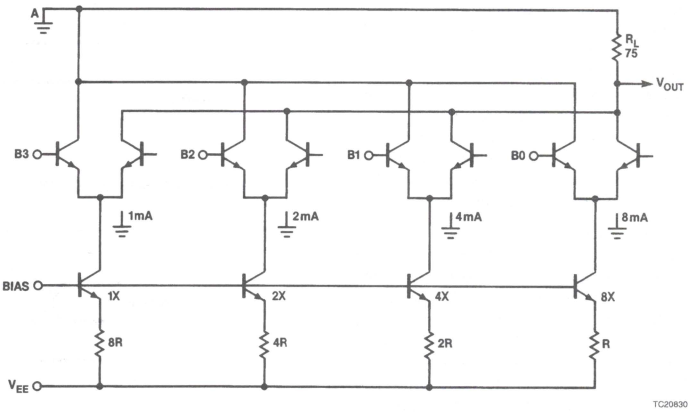

Figure 13. Simplified Schematic of DAC (1 of 3)

WORKSTATION APPLICATION

Introduction

This section describes the design of a color graphics interface for the Modula, Inc. Lilith Workstation. The workstation initially loads 16 colors (it only requires 16) into the NE5150's color look-up table. After the colors are loaded, the workstation then generates addresses to the look-up table. The entire color range (4096) is not required in this application.

The LILITH Workstation

The Lilith Workstation is a 16-bit workstation manufactured by Modula, Inc. It was originally designed by Niklaus Wirth and his students at the Swiss Federal Institute of Technology (ETH). The Lilith is a Modula-2 computing engine. In its original package, the Lilith includes 256kB of memory, a 15MB Winchester disk drive, a floppy disk, a mouse, and an 832 × 640 monochrome graphics tube.

The Signetics Logic Design Group in Orem, Utah, has modified the Lilith by adding 2MB of memory and a high-resolution 1024 × 1024 color monitor. The changes made to the Lilith graphics section comprise the bulk of this application description. Benchmarks of the modified workstation have shown that its performance on applications ranging from matrix multiplications to complete circuit analysis is approximately half as fast as a VAX 11/780 minicomputer. In addition to the circuit simulator used, the Signetics-modified Lilith also supports a layout editor, SLED, that uses about 10,000 lines of Modula-2 source code. More detailed information on the Lilith can be obtained from the manufacturer and from the articles listed in the reference section.

For the purposes of this application, it is sufficient to know that the Lilith contains a 16-bit data bus for interaction with the SCC63484 Advanced CRT Controller and a

14-bit bus that is used to initialize the color look-up table in the NE5150 video DAC. Read/write, I/O lines, CLOCK, data acknowledge, and chip select signals are also sent to the SCC63484 for data and control purposes.

Software Aspects (Pascal and Modula-2) Modula-2 is a superset of Pascal. Anyone with a working knowledge of Pascal should have no trouble programming a Lilith workstation or in understanding the initialization program outlined in this section. Some noteworthy features about Modula-2 and its influence on the architecture of the Lilith (the M-machine) is the fact that the Lilith instruction set (M-code) has only 256 carefully chosen instructions. This limits any instruction to a 1B length and increases the speed of operation. The Modula-2 language constructs map neatly to M-code. There are no excess instructions to add extra baggage. For additional details, the reader is referred to the August 1984 issue of BYTE magazine that contains several good articles on Modula-2.

Considering each '1' as ON and each '0' as OFF, the binary values for each color can be specified for each of the respective guns. Starting from the top, all guns OFF = BLACK. Similarly, all guns ON corresponds to word 7, WHITE. In the software definition module used to load the values, two constants were declared: black = 0 and white = 15. These correspond to the addresses shown in the table and were predefined because of their frequent use. Single guns completely ON give 1, 2, and 4 — the primary colors RED, GREEN, and BLUE, respectively.

System Hardware

The basic system configuration for the color graphics interface is shown below. The Lilith workstation sends data to the SCC63484 and the NE5150. The information sent to the NE5150 is the data for the CLUT initialization. Control signals are sent to the ACRTC. The ACRTC in turn controls the video DAC. The frame buffer sends and receives data (via an address/data buffer stage) to and from the ACRTC for video DAC addressing. The ACRTC also provides horizontal and vertical sync to the CRT while the video DAC supplies the video information. One stage not shown is the address and data buffering for the frame buffer and the pixel stage. This stage, in addition to assorted logic and timing chips, merely facilitates functionality between the major blocks shown in Figure 21.

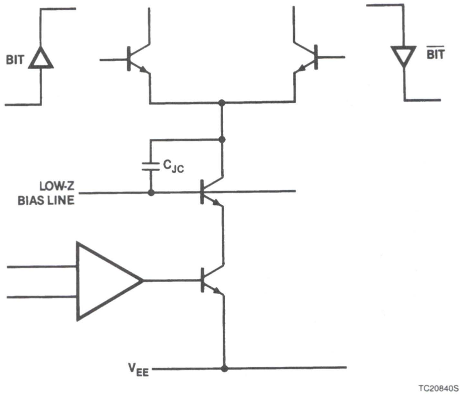

Figure 14. Low-Z Bias Line to Improve Settling Time of DAC

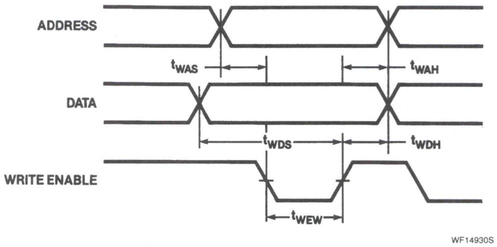

Figure 15. NE5150/52 READ and WRITE Cycle Timing Diagrams

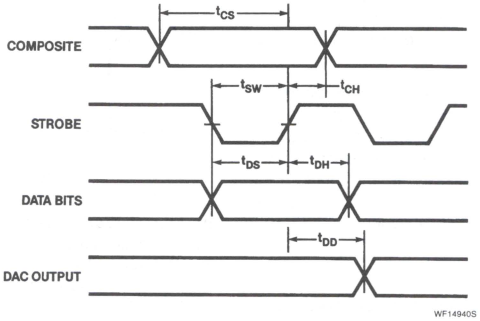

Figure 16. NE5151 Timing Diagram

The host microprocessor, system memory, and DMA control are local to the workstation and will not be described. The horizontal and vertical deflection sections are local to the CRT and will also be omitted. The rest of this section supplies an overall parts list and then describes each of the graphics blocks in somewhat greater detail. Although the actual pin numbers have been omitted, the functionality of each pin is shown for understanding. For actual pinouts and more detailed information, refer to the appropriate data sheet.

Parts List

The following parts were used in the design of the color graphics interface (the actual quantity of each part is not listed). The "F" designation stands for Signetics FAST-type logic.

- NE5150 Video DAC
- SCC63484 Advanced CRT Controller
- MB85103-10 64k × 8 Dynamic RAM modules (Fujitsu)
- 7404 Hex Inverter
- 7432 2-Input NAND Gate

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- 7474 Dual D-Type Flip-Flop
- 74123 Dual Retriggerable Monostable Multivibrator
- 74138 1-of-8 Decoder/Demultiplexer
- 74F139 Dual 1-of-4 Decoder/Multiplexer
- 74F157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
- 74F161 4-Bit Binary Counter
- 74F164 8-Bit Serial-In/Parallel-Out Shift Register
- 74F166 8-Bit Serial/Parallel-In, Serial-Out Shift Register
- 74F245 Octal Transceiver (3-State)
- 74F373 Octal Transparent Latch
- 7905 5V Voltage Regulator
- M1001 40MHz Crystal (MF Electronics)

PC Board Layout Considerations

Whenever dealing with high-frequency systems, analog or digital, care must be taken with PC board layout in order to insure good, reliable operation. Video DACs are hybrid devices in the sense that they are both analog and digital. They are also run at frequencies well into the RF range. This makes them especially susceptible to RF interference and different types of radiation. Signal traces should be kept as short as possible and 90° turns should be avoided. Power supplies should have adequate decoupling.

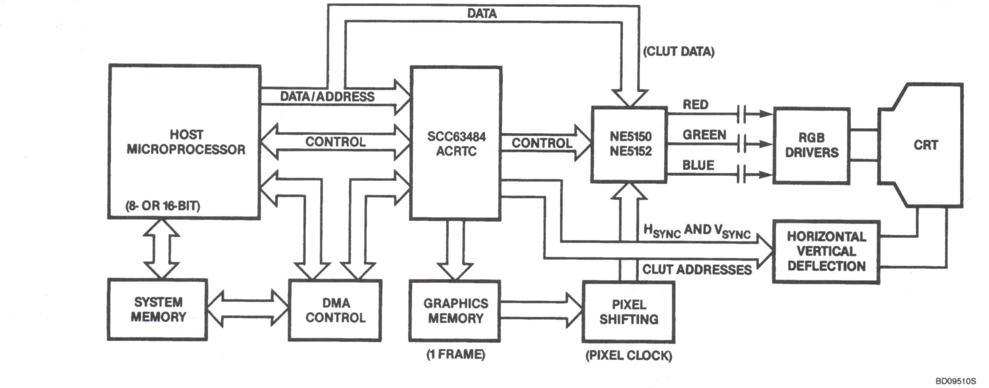


Figure 17. Block Diagram of Color Graphics Interface

More details are provided in the reference section under Reference Number 4, "Getting the Best Performance From Your Video Digital-to-Analog Converter".

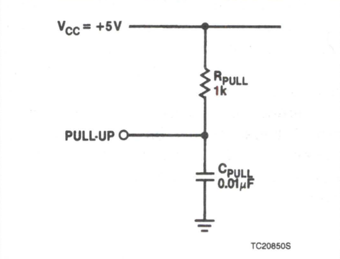
Functional Description

The interface is designed to drive a Mitsubishi C-6919 or 6920 19-inch monitor. The monitor has 1024 × 1024 display resolution. Of these, 1024 × 768 pixels are actually drawn, giving us about 790,000 pixels, and, according to our earlier formulas, requiring a DAC with a conversion frequency of about 62MHz. That, however, assumes a non-interlaced display with a frame rate of 60Hz. This application uses a 30Hz interlaced display and so it needs only one-fourth that speed since it is drawing half as many lines at half of the frame rate. The pixel clock is derived from a 40MHz crystal. Other timing signals are also derived from the same crystal.

Table 4. Colors with Corresponding Bit Values

WORD #	COLOR	BLUE	GREEN	RED
0	BLACK	0000	0000	0000
1	RED	0000	0000	1111
2	GREEN	0000	1111	0000
3	YELLOW	0000	1111	1111
4	BLUE	1111	0000	0000
5	VIOLET	1111	0000	1111
6	TURQUOISE	1111	1111	0000
7	WHITE	1111	1111	1111
8	GREY	1010	1010	1010
9	ORANGE	0000	1000	1111
10	AVOCADO	0000	1010	1000
11	LIME	0101	1111	1111
12	NAVY	1111	1000	1000
13	ROUGE	1000	0000	1111
14	LAVENDER	1111	1111	1000
15	PEA	1000	1111	1000

NOTE:
The colors listed are for an application example only. The colors were randomly ordered and their gun and bit values in no way represent the de facto standard values or colors.



V_{CC} = +5V
R_{PULL}
1k
PULL-UP
C_{PULL}
0.01µF
TC20850S

Figure 18. Circuit for Pull-Up to V_{CC}

The interface uses a 512kByte frame buffer that is organized as 64k by 64-bit words. Within each 16-bit block of memory (1 of 4 per word), there are 4 pixels of 4 bits each. Each bit supplies an address to the Color Look-Up Table in the Video DAC. The interface shifts out 64-bits or 16 pixels of information during each display cycle.

In each of the following schematics certain pins have been pulled up to V_{CC}, indicated by an arrow. For each arrow pointing to PULL-UP, the connection goes into the pull-up circuit shown below.

C_{PULL} is used for decoupling any power line ripple. Each point has a similar circuit.

ADVANCED CRT CONTROLLER

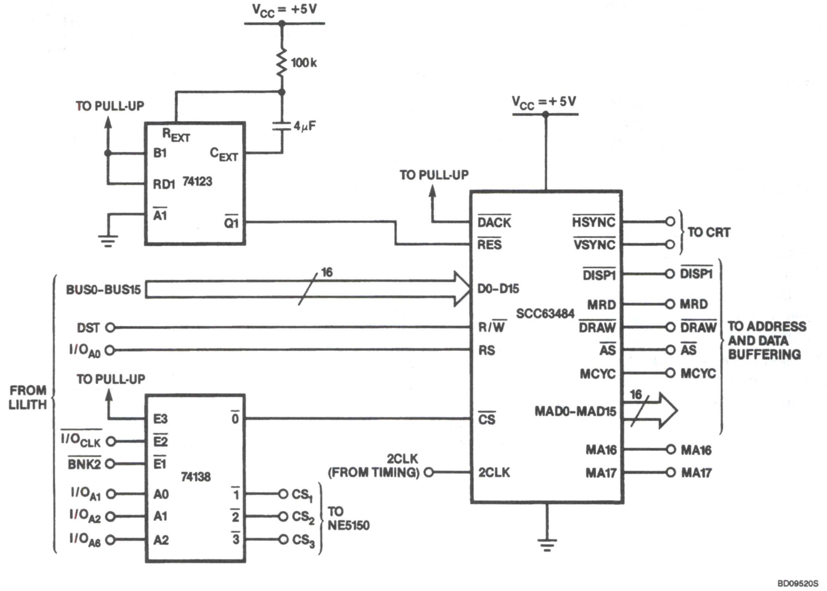
The Signetics SCC63484 is a state-of-the-art device ideal for controlling raster-scan-type CRTs. It is a CMOS VLSI system that can control both text and graphics. One of the advantages of this part is its ability to do on-board graphic processing in its Drawing and Display Processor, relieving some of the computational overhead from the Lilith.

Another attractive feature of the part is its flexibility. It has three different operating modes: character only, graphic only, and multiplexed character/graphic mode. In addition, it offers three scanning modes: non-interlace, interlace sync (this application), and interlace sync and video modes. With 2MB of graphic memory and a maximum drawing speed of 2 million pixels/second, it can supply the information to almost any type of high-resolution display (4096 × 4096 pixels maximum).

For additional information on the command set and a full listing of features, please refer to the data sheet and user's manual. This application note will concentrate on only the interconnections relevant to this application.

In this configuration (Figure 19), the SCC63484 Graphics Controller provides the horizontal and vertical sync pulses to the CRT and important timing pulses to the address and data buffers. It supplies timing to the frame buffer, the pixel-shifting stage, and to the frame buffer through direct and logical modifications made to the following system outputs:

1. MRD — Memory Read or the Bus Direction Control Line. This determines the bus direction for the Frame Buffer Data Bus.
2. $\overline{\text{DRAW}}$ — the Drawing/Refresh Cycle pin. This differentiates between drawing cycles and CRT display refresh cycles.
3. $\overline{\text{AS}}$ — Address Strobe. This provides the address strobe for demultiplexing the frame buffer/data bus (MAD0/MAD15).
4. MCYC — Memory Clock. Provides the frame buffer memory access timing. Equal to one-half the frequency of 2CLK signal.
5. $\overline{\text{DISP1}}$ — Display Enable Timing. This is a programmable display enable timing signal used to selectively enable, disable, and blank logical screens.
6. MAD0 - MAD15 — Address and Data Bus. Multiplexed frame buffer address/data bus.
7. MA16, MA17 — Address Bits/Raster Address Outputs. Gives the higher-order address bits for graphic screens and the raster address outputs for character screens. (lower 2 bits of MA16 - MA19).



V_{CC} = +5V
100k
4µF
TO PULL-UP
R_{EXT}
B1
C_{EXT}
RD1
74123
$\overline{A1}$
$\overline{Q1}$
V_{CC} = +5V
TO PULL-UP
$\overline{DACK}$
$\overline{RES}$
$\overline{HSYNC}$
$\overline{VSYNC}$
TO CRT
BUS0-BUS15
16
D0-D15
$\overline{DISP1}$
$\overline{DISP1}$
SCC63484
MRD
MRD
DST
R/$\overline{W}$
$\overline{DRAW}$
$\overline{DRAW}$
TO ADDRESS AND DATA BUFFERING
I/O_{A0}
RS
$\overline{AS}$
$\overline{AS}$
MCYC
MCYC
FROM LILITH
TO PULL-UP
16
E3
$\overline{0}$
$\overline{CS}$
MAD0-MAD15
$\overline{I/O_{CLK}}$
$\overline{E2}$
$\overline{BNK2}$
$\overline{E1}$
74138
2CLK (FROM TIMING)
2CLK
MA16
MA16
MA17
MA17
I/O_{A1}
A0
$\overline{1}$
CS_1
I/O_{A2}
A1
$\overline{2}$
CS_2
TO NE5150
I/O_{A6}
A2
$\overline{3}$
CS_3
BD09520S

Figure 19. SCC63484 Advanced CRT Controller

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The 2CLK signal provides the main clock input to the SCC63484 and is derived from the pixel clock (see System Timing).

The ACRTC also provides horizontal and vertical sync pulses directly to the CRT via the $\overline{HSYNC}$ and $\overline{VSYNC}$ outputs.

In Figure 19, the 16-bit bus of the Lilith is connected directly to the data inputs. The Lilith also provides a write signal (DST) to the R/$\overline{W}$ input. The first I/O line (I/OA0) is connected to the RS (Register Select) input. In addition, there is a high-order I/O bank select, three lower-order address lines, and a negative true I/O clock that, used with the 74138 Decoder, selects one of 4 devices: the ACRTC or 3 areas in the NE5150's color look-up table.

On the ACRTC, a 74123 one-shot produces a reset pulse ($\overline{RES}$) on power-up. The Data Acknowledge pin is not used and is pulled up to V_{CC}.

ADDRESS AND DATA BUFFERING

The address and data buffer stage provides an interface between the SCC63484 and the rest of the circuit. This stage takes the address/data lines MAD0 – MAD15 and separates them into two blocks. The 74F373 latches the upper bank for the addresses; this is the first bank. The second bank consists of 74F245 transceivers in the lower bank for the data.

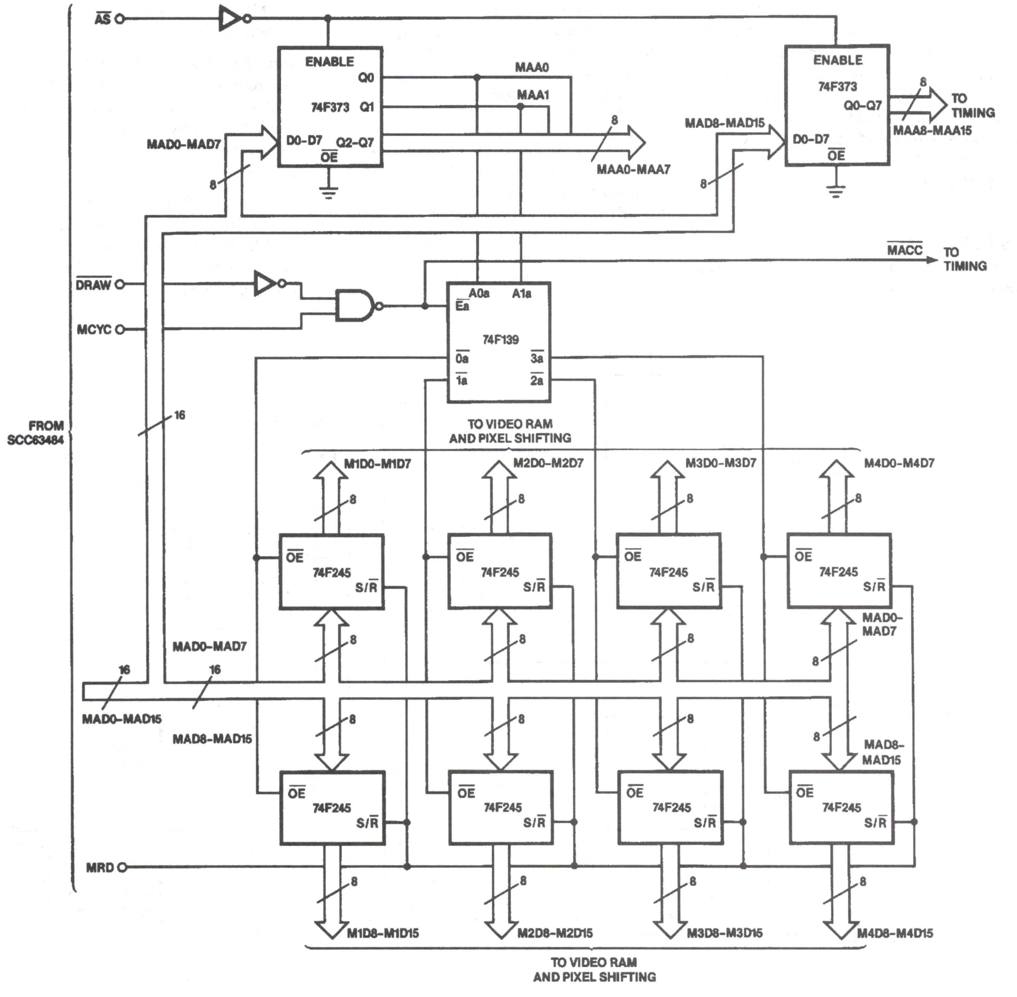

AS
ENABLE
Q0
74F373 Q1
D0-D7 Q2-Q7
OE
MAA0
MAA1
8
MAA0-MAA7
MAD0-MAD7
8
ENABLE
74F373
Q0-Q7
D0-D7
OE
MAD8-MAD15
8
TO TIMING
MAA8-MAA15
MACC
TO TIMING
DRAW
MCYC
A0a A1a
Ea
74F139
0a 3a
1a 2a
TO VIDEO RAM AND PIXEL SHIFTING
FROM SCC63484
16
M1D0-M1D7
M2D0-M2D7
M3D0-M3D7
M4D0-M4D7
OE
74F245
S/R
MAD0-MAD7
MAD0-MAD15
MAD8-MAD15
16
MAD0-MAD7
MAD8-MAD15
MRD
M1D8-M1D15
M2D8-M2D15
M3D8-M3D15
M4D8-M4D15
TO VIDEO RAM AND PIXEL SHIFTING
BD09531S

Figure 20. Address and Data Buffering

The 74F373s are used to latch the addresses at the beginning of every memory cycle. The latches are enabled by the $\overline{\text{AS}}$ signal coming from the ACRTC. Since the ACRTC is configured to increment its display addresses by four between display cycles, 4 words or 64 bits are shifted out every cycle. For modifying memory cycles, the two lower address lines are used to enable one of four sets of 74F245 transceivers (2 per set). Enabling is performed by the 74F139 Decoder. The signal that clocks the decoder is a combination of MCYC (Memory Cycle) and $\overline{\text{DRAW}}$, that results in a new signal, $\overline{\text{MACC}}$. This signal is also used in the timing block.

The transceiver outputs are now written into the frame buffer. From there, they will be sent to the pixel-shifting stage and then to the DAC. Each set of four 4-bit pixels in a serial string of displayed pixels is contained in a different block of memory. This is the reason the two lower-order address signals are used to select one of the four banks in the Video RAM (frame buffer).

SYSTEM TIMING

In a system as complicated as a graphics display board, the timing of the various elements grows exceedingly complicated as the number of components grows. It becomes even more apparent when the components are individual systems with their own set of timing considerations. In our case, this means the Lilith, the ACRTC, and the frame buffer.

Figure 21 shows the many elements it takes to generate the timing signals for the system. In the middle of the diagram, there are two 74F164 8-bit serial-in/parallel-out shift registers that count the timing states for the rest of the interface. The Address Strobe ($\overline{\text{AS}}$) signal, coming from the ACRTC, starts and ends this timing train. Because of the pulse width of $\overline{\text{AS}}$, many states at the end of the train are unusable. The video RAM $\overline{\text{RAS}}$ signal (Row Address Strobe) starts at the beginning of State 1, and terminates as $\overline{\text{AS}}$ goes Low, activating the register's MR (Master Reset). The precharge requirement of $\overline{\text{RAS}}$ is met by the $\overline{\text{AS}}$ pulse width.

The 74F157 Multiplexers are connected in such a way that the lower-order addresses are used for the video RAM row addresses (the 157 on top). At the beginning of State 3, the higher-order addresses are presented at the Video RAM address inputs as the column address. At State 5 the $\overline{\text{CAS}}$ signal becomes valid. Because of changes in the data hold (WRITE cycle) and data setup (READ cycle) of the ACRTC, the timing edge of $\overline{\text{CAS}}$ might have to be changed to insure proper operation.

MRD (Memory Read) along with a combination of MCYC and $\overline{\text{DRAW}}$ from the Address and Data Buffer called $\overline{\text{MACC}}$, are used with the two lowest-order address lines from the 74F373s (MAA0 and MAA1) to write-select one of the four memory planes (this memory plane runs orthogonal to the bit-planes discussed earlier). Because this signal comes well before the $\overline{\text{CAS}}$ signal, this qualifies as an early WRITE cycle, allowing the use of DRAMs with Data-In and Data Out signals connected together.

Using two flip-flops, the output of the lower shift register generates the PE (Parallel Enable) signal for the pixel-shifting stage. Because it is clocked from the fifth point in the shifter, this pulse occurs between States 10 and 11.

The upper left-hand corner of Figure 21 shows the creation of the 2CLK signal derived from the 40MHz pixel clock by using a 74F161 Counter that performs a divide-by-eight operation.

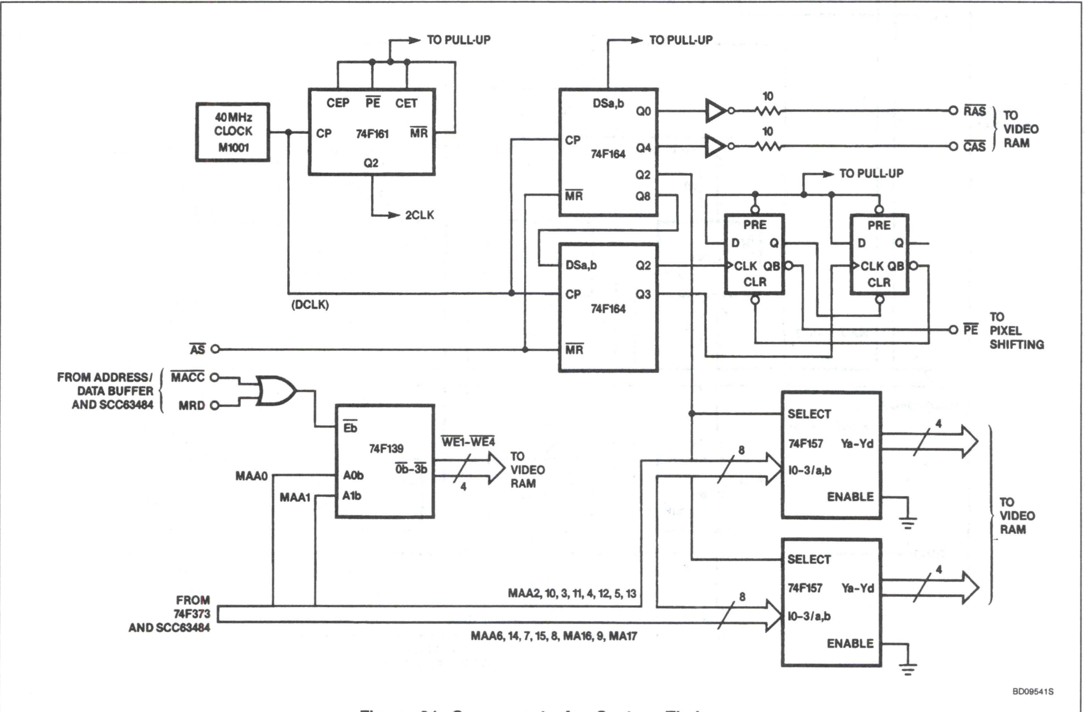

TO PULL-UP
TO PULL-UP
40MHz CLOCK M1001
CEP
PE
CET
CP
74F161
MR
Q2
2CLK
DSa,b
Q0
CP
74F164
Q4
Q2
MR
Q8
10
10
RAS
CAS
TO VIDEO RAM
TO PULL-UP
PRE
D
Q
CLK
QB
CLR
PRE
D
Q
CLK
QB
CLR
DSa,b
Q2
CP
Q3
74F164
MR
(DCLK)
AS
TO PIXEL SHIFTING
PE
FROM ADDRESS/ DATA BUFFER AND SCC63484
MACC
MRD
Eb
74F139
WE1-WE4
0b-3b
4
TO VIDEO RAM
MAA0
A0b
MAA1
A1b
SELECT
74F157
Ya-Yd
I0-3/a,b
ENABLE
8
4
TO VIDEO RAM
SELECT
74F157
Ya-Yd
I0-3/a,b
ENABLE
8
4
FROM 74F373 AND SCC63484
MAA2, 10, 3, 11, 4, 12, 5, 13
MAA6, 14, 7, 15, 8, MA16, 9, MA17
BD09541S

Figure 21. Components for System Timing

PIXEL SHIFTING

The pixel-shifting stage consists of 8 very fast 74F166 Shift Registers divided into 4 banks, one for each address bit. These shift registers have maximum operating frequencies of 120MHz.

The data comes from the address and data buffering and the video RAM. The $\overline{PE}$ (Parallel Enable Input) signal from the system timing block activates the register, while the pixel clock, DCLK, strobes each of the registers. All chips are permanently enabled by grounding their chip enable ($\overline{CE}$) pins. The master reset ($\overline{MR}$) is permanently disabled by tying it to a pull-up.

The connection between the registers and the memory is such that all the bits of each pixel are shifted out simultaneously before going to the 74F157 multiplexer. From there, they address the colors of the CLUT on the Video DAC.

VIDEO RAM

The phrase "Video RAM" refers to a set of dynamic RAMs used as the memory section in this application. It is not meant to be confused with the Video RAM which is a dedicated device for video applications.

The Video RAM or frame buffer section consists of 8 Fujitsu MB85103-10 modules. The 10 suffix signals a 100ns row access time. The cycle time is about 200ns, or about 5MHz. This is fine because only the pixel clock has to travel at the high screen draw speeds. These modules are SIPs (single in-line packages) and were used because of space considerations. Each module consists of eight 64k × 1-bit DRAMs, giving eight modules of 64k × 8 or a 64k × 64 buffer. This buffer is divided into four sections (64k × 16) that represent the four bits of address that are shifted out to the NE5150's CLUT.

One can see how the frame buffer is set up to shift out data to the pixel shifter. The memory is divided into 4 banks that are write-selected by the $\overline{WE1}$ – $\overline{WE4}$ pulses. Two modules (64k × 16 bits) make up one bank. This makes up the four 16-bit words that are shifted out. But where is the information for each pixel? Taking the 1st bank as an example, it can be divided into 4 quadrants:

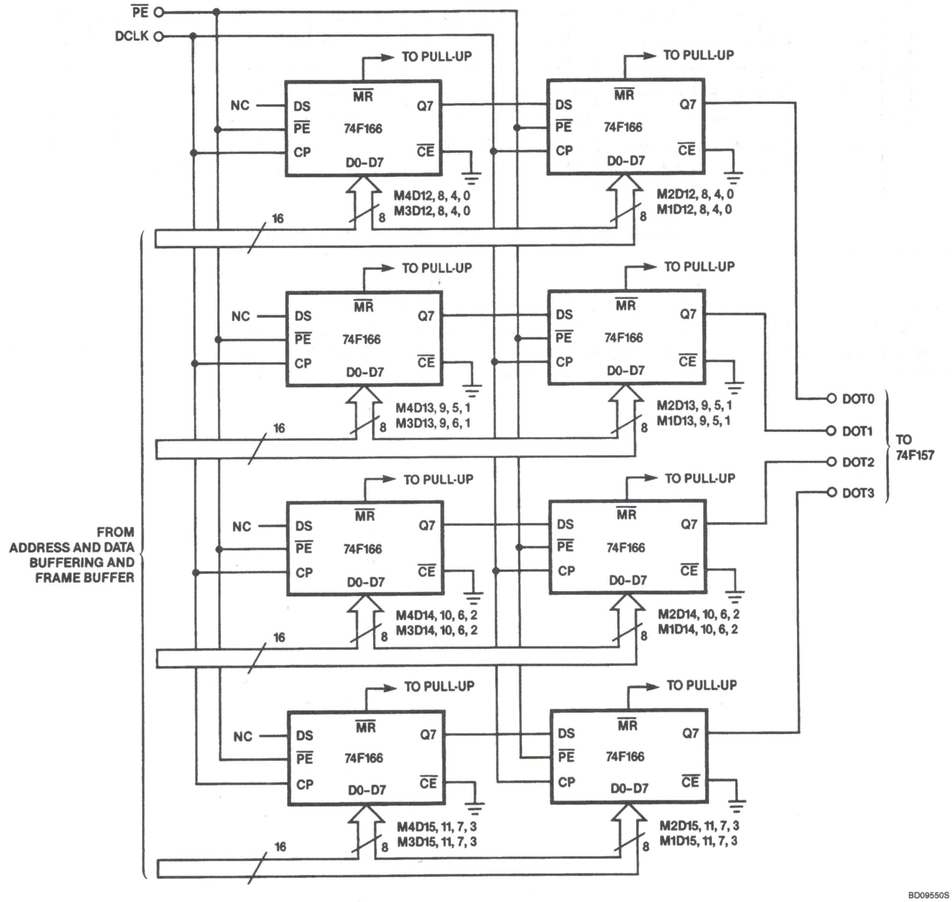

$\overline{PE}$
DCLK
TO PULL-UP
NC
DS
$\overline{MR}$
Q7
$\overline{PE}$
74F166
CP
D0-D7
$\overline{CE}$
M4D12, 8, 4, 0
M3D12, 8, 4, 0
M2D12, 8, 4, 0
M1D12, 8, 4, 0
M4D13, 9, 5, 1
M3D13, 9, 6, 1
M2D13, 9, 5, 1
M1D13, 9, 5, 1
M4D14, 10, 6, 2
M3D14, 10, 6, 2
M2D14, 10, 6, 2
M1D14, 10, 6, 2
M4D15, 11, 7, 3
M3D15, 11, 7, 3
M2D15, 11, 7, 3
M1D15, 11, 7, 3
16
8
DOT0
DOT1
DOT2
DOT3
TO 74F157
FROM ADDRESS AND DATA BUFFERING AND FRAME BUFFER
BD09550S

Figure 22. Shift Registers for Pixel-Shifting

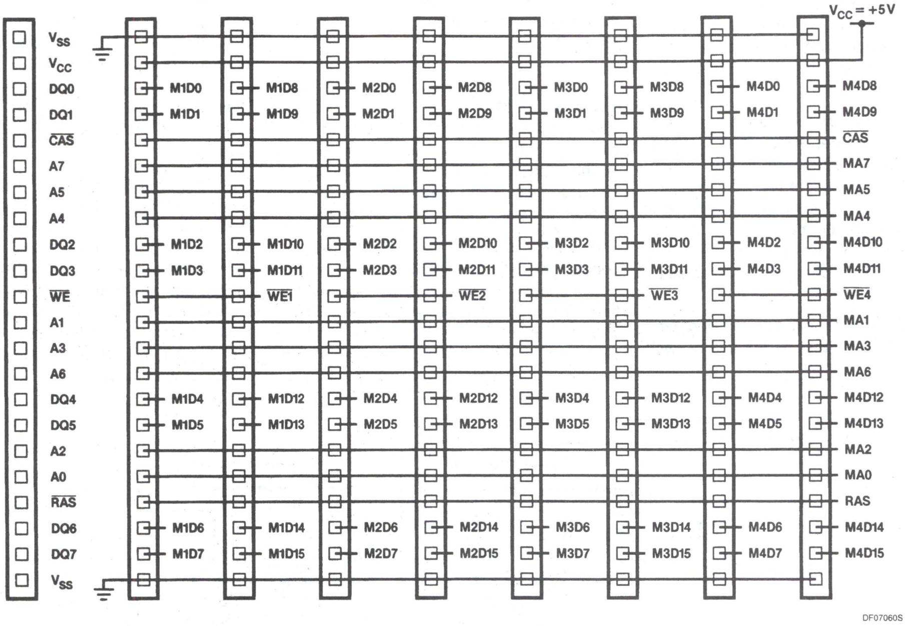

V_{CC} = +5V
V_{SS}
V_{CC}
DQ0
DQ1
$\overline{CAS}$
A7
A5
A4
DQ2
DQ3
$\overline{WE}$
A1
A3
A6
DQ4
DQ5
A2
A0
$\overline{RAS}$
DQ6
DQ7
V_{SS}
M1D0
M1D8
M2D0
M2D8
M3D0
M3D8
M4D0
M4D8
M1D1
M1D9
M2D1
M2D9
M3D1
M3D9
M4D1
M4D9
$\overline{CAS}$
MA7
MA5
MA4
M1D2
M1D10
M2D2
M2D10
M3D2
M3D10
M4D2
M4D10
M1D3
M1D11
M2D3
M2D11
M3D3
M3D11
M4D3
M4D11
$\overline{WE1}$
$\overline{WE2}$
$\overline{WE3}$
$\overline{WE4}$
MA1
MA3
MA6
M1D4
M1D12
M2D4
M2D12
M3D4
M3D12
M4D4
M4D12
M1D5
M1D13
M2D5
M2D13
M3D5
M3D13
M4D5
M4D13
MA2
MA0
RAS
M1D6
M1D14
M2D6
M2D14
M3D6
M3D14
M4D6
M4D14
M1D7
M1D15
M2D7
M2D15
M3D7
M3D15
M4D7
M4D15
DF07060S

Figure 23. Memory Configuration to Store Pixels

M1D0 – M1D3, M1D4 – M1D7, M1D8 – M1D11, and M1D12 – M1D15. Each of these quadrants represents a dot. By tracking each dot in parallel back to the shift register in the pixel-shifting stage, they turn out to be each of the four quadrants in parallel. Comparing diagrams reveals the same to be true for each of the quadrants in each of the four banks of memory. Each quadrant, then, corresponds to one pixel, and all of the pixels for one bank are written out to the shift register during a write cycle.

VIDEO DAC INTERFACE

The interface to the NE5150 is shown in Figure 24. The 8-bit data bus comes from the lower 8 bits of the Lilith. The low 4 bits are connected directly to the Video DAC data inputs. Bits 4 – 7 are tied to the 74F157 Multiplexer. This provides the address to the CLUT when it is initialized.

The other set of inputs to the multiplexer comes from the pixel-shifting stage. After the first CLUT initialization, all of the addresses come from the pixel-shifter. The inverters, NAND gates, and OR gates are used to delay the write pulses $\overline{\text{WRR}}$, $\overline{\text{WRG}}$, and $\overline{\text{WRB}}$ so that they fit into the address setup window. The chip select pulses come from the 74F138 which are selected by the Lilith. $\overline{\text{I/OCLK}}$ clocks the 74138 and the OR gates for the chip select.

DCLK drives the STROBE of the DAC and clocks the two D-type flip-flops which provide the BLANKing signal. Both of these signals come from the ACRTC and the system timing section. The WHITE, BRIGHT, and SYNC inputs are not utilized and are connected to ground. V_{EE} is run off a 7905 voltage regulator powered by a –12V power supply.

The capacitors to the monitor and voltage regulator are polarized with the positive end to the monitor for the RGB outputs and to ground for the regulator. The regulator uses Tantalum capacitors.

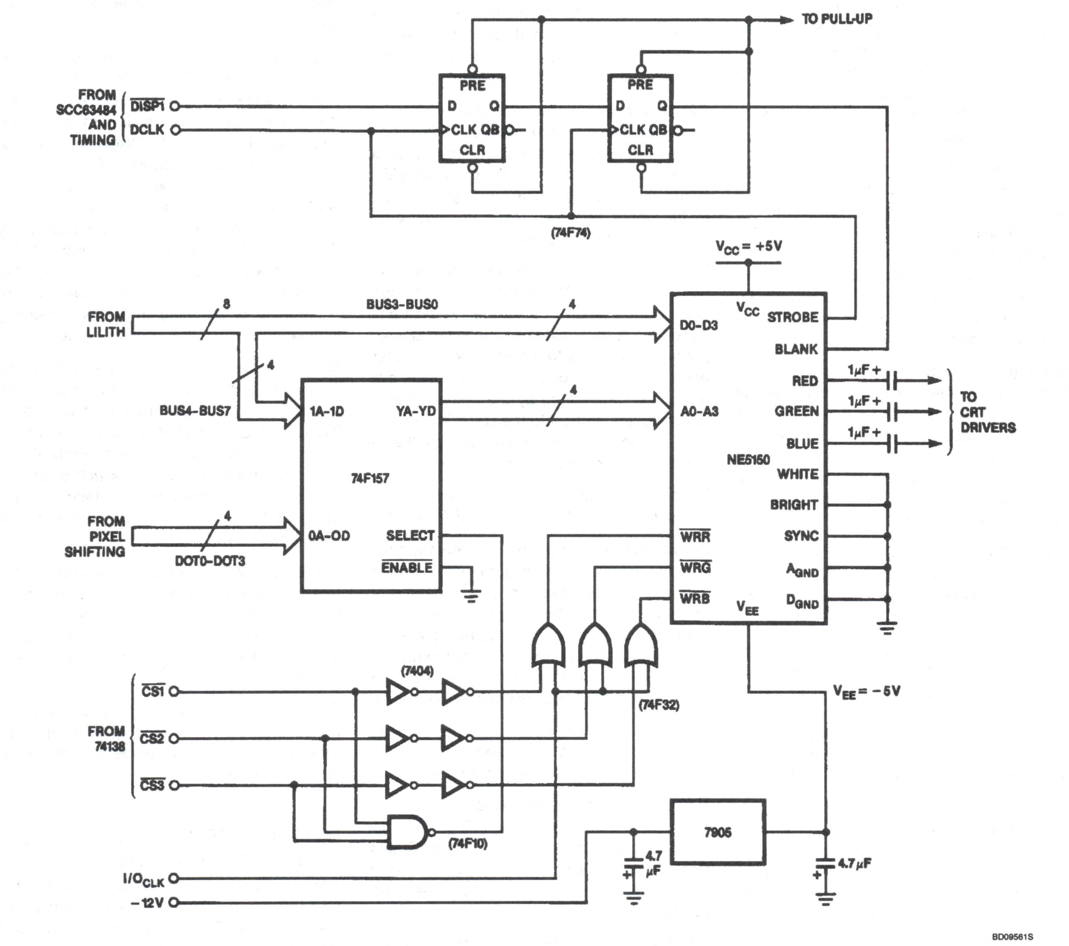

TO PULL-UP
FROM SCC63484 AND TIMING
$\overline{\text{DISP1}}$
DCLK
PRE
D
Q
CLK
QB
CLR
(74F74)
V_{CC} = +5V
FROM LILITH
8
BUS3-BUS0
4
4
BUS4-BUS7
1A-1D
YA-YD
74F157
FROM PIXEL SHIFTING
DOT0-DOT3
0A-0D
SELECT
$\overline{\text{ENABLE}}$
D0-D3
A0-A3
V_{CC}
STROBE
BLANK
RED
GREEN
BLUE
NE5150
WHITE
BRIGHT
SYNC
A_{GND}
D_{GND}
$\overline{\text{WRR}}$
$\overline{\text{WRG}}$
$\overline{\text{WRB}}$
V_{EE}
1μF +
1μF +
1μF +
TO CRT DRIVERS
(7404)
(74F32)
V_{EE} = –5V
FROM 74138
$\overline{\text{CS1}}$
$\overline{\text{CS2}}$
$\overline{\text{CS3}}$
(74F10)
7905
4.7 μF
4.7μF
I/O_{CLK}
–12V
BD09561S

Figure 24. NE5150 Video DAC Interface

NE5150/51/52 Family of Video Digital-to-Analog Converters AN1081

GLOSSARY

This glossary consists of three parts: a section for graphics terminology, one for the timing of the NE5150 used in the Lilith workstation application, and a list of references. For the glossary section, many analogies are made with television to clarify some terminology.

GRAPHICS TERMINOLOGY

ACRTC — Short for Advanced CRT Controller. A device that helps to interface a microprocessor or microcomputer with a monitor. Advanced refers to the Signetics ACRTC, the SCC63484, called advanced because of its ability to do most of its graphics computations on-board, thus relieving some of the workload from the microprocessor and increasing its overall efficiency.

Bit-Map, Bit-Plane — A memory representation in which one or more bits correspond to a pixel. For each bit used in the representation of a pixel, there is a plane on which it can be mapped. To represent each pixel by 4 bits, 4 bit planes are needed. This is the case whether the bits store the actual data for the pixel or hold the address of the memory location containing the data.

Blanking — The process of turning off an electron gun so that it leaves no trace on the screen as it returns to the left or top of the screen in a raster-scan system. Applies to both television sets and monitors. The period for the blanking is defined as the horizontal blanking and the vertical blanking interval for their respective cases.

CRT — Short for Cathode Ray Tube, a type of electron tube that produces an electron beam that strikes the phosphor-coated screen, causing that screen to emit light.

Chrominance — The color information supplied in a signal. While this information has to be extracted by color decoders in television (via phase differencing with a fixed-frequency subcarrier), in computer monitors and bit-mapped systems it is supplied digitally and then converted to analog to directly drive color guns.

Color Look-up Table — Sometimes referred to as the CLUT, it is associated with a Video DAC and speeds system access of often-used colors. The time savings results because a color can be generated by sending a CLUT address to the DAC instead of loading a word from external memory. Current CLUTs range in size from 16 to 256 words. Word length depends on the bit resolution of the DAC.

DAC — Short for Digital-to-Analog Converter. Most DACs have a single output. Some have as many as eight. RGB Video DACs have three — one for each of the primary colors. Video DACs typically operate at very high speeds since they have to supply a new piece of information for each pixel on the screen at rates of 30 to 80 times per second.

ECL — Short for Emitter-Coupled-Logic. A fast, non-saturating form of bipolar logic that usually operates from 0 to −5.2V. It has a threshold of −1.3V.

Frame Buffer — Sometimes used interchangeably with video RAM. A frame buffer is a large, fast-access store of memory that contains the digital information necessary to display part or all of a display. It is used in conjunction with bit-mapped graphic systems. It actually "stores" the bit-plane.

Glitch Energy — The area displaced by an analog signal as it overshoots or undershoots its ideal value. This is a problem usually found in DACs. Units are usually given in pV-s. When glitch energy is high, settling times tend to be longer and may result in visual color aberrations on the screen.

Hue — The actual color(s) on a monitor. The hue depends on the frequency of the light striking the human eye. For television transmission, it is determined by the video signal's phase difference with a color subcarrier reference frequency. For computer graphics systems, it is determined by the combination of binary values applied to the DAC. The resolution of hue/colors is determined by the bit length of each word of information.

Lilith — The brand name of the workstation manufactured by Modulo, Inc. of Provo, UT.

Luminance — The brightness information in a video signal. A black and white (monochrome) monitor displays only variations in brightness. Only a luminance signal is being manipulated. The same holds true for television. Although chrominance information is also present in a television signal, B/W TV sets do not have the necessary decoders.

Modula-2 — A language that is the superset of Pascal. This was also invented by Niklaus Wirth of the Swiss Technological Institute.

NTSC — Short for the National Television Standards Committee, the ruling body for television standards in the United States. Other countries also use this standard as is, or with a different frequency for the color subcarrier.

Orthogonal — Defined as being mutually perpendicular. The product of two orthogonal vectors is zero. In bit-mapped systems, the bit length of a word lies orthogonal to the plane itself. Hence, each plane supplies only one bit of information for each pixel.

Pixel — Short for "picture element". The smallest resolvable element on a graphics display. Each pixel usually corresponds to at least one bit. The entire display is made up of a map of pixels. The term bit-map comes from the bit association. There is no equivalent in television. What is seen is the true analog representation of what is being recorded by a camera and then retraced on horizontal lines.

Raster-Scan — The form of visual display transmission used in all television sets and in most monitors. It consists of an electron beam tracing a path from left-to-right while going top-to-bottom.

Saturation — The "deepness" of a color. Usually depends on the amplitude of the color signal in television systems. Red and pink are the same hue, but red is actually more saturated than pink. In graphics systems, there is no true equivalent. Changing bit-values changes the color itself. The closest analogy would be to raise or lower the voltages on all three color guns simultaneously (the BRIGHT function on the NE5150/51/52). This would, however, depending on the amplitude change, give the impression of brightening or dimming the color (changing luminance) rather than saturating it.

Sync — The voltage level specified in RS-343A as being 140 IRE (1V) below the enhanced white level (ground). It is also 40 IRE (286mV) below the blanking level. Generically it is also used to refer to vertical and horizontal sync pulses that synchronize the timing and movement of the electron beam on a CRT. It should not be confused with "composite sync".

Teletext — A form of data transmission via television signals. In many cases, digital information is sent during the vertical blanking interval (VBI). In some cases, it is sent during every retrace. This is known as full-field teletext.

TTL — Short for Transistor-Transistor Logic. It has a threshold voltage of approximately 1.4V and is the most widely-used form of logic in the world today.

DEFINITIONS FOR NE5150/51/52 TIMING DIAGRAMS

This section contains explanations for the NE5150/51/52 Video DAC's timing diagram specifications. For the typical, minimum, and maximum values, please refer to Signetics' data sheet.

t_{WAS} — Write Address Setup (NE5150/52)

t_{WAH} — Write Address Hold (NE5150/52)

t_{WDS} — Write Data Setup (NE5150/52)

NE5150/51/52 Family of Video Digital-to-Analog Converters AN1081

t_{WDH} — Write Data Hold (NE5150/52)

t_{WEW} — Write Enable Pulse Width (NE5150/52)

t_{RCS} — Read Composite Setup (NE5150/52)

t_{RCH} — Read Composite Hold (NE5150/52)

t_{RAS} — Read Address Setup (NE5150/52)

t_{RAH} — Read Address Hold (NE5150/52)

t_{RSW} — Read Strobe Pulse Width (NE5150/52)

t_{RDD} — Read DAC Delay (NE5150/52)

t_{CS} — Composite Setup (NE5151)

t_{CH} — Composite Hold (NE5151)

t_{DS} — Data bits Setup (NE5151)

t_{DH} — Data bits Hold (NE5151)

t_{SW} — Strobe Pulse Width (NE5151)

t_{DD} — DAC Delay (NE5151)

t_R — DAC Rise Time (NE5151)

t_S — DAC Full-Scale Settling Time (NE5151)

REFERENCES

The following books, articles, notes, and correspondences were used in the preparation of this application note.

1. *Raster Graphics Handbook*, 2nd edition, by the Conrac Corporation
2. "Trends in Graphics Hardware", paper by Randall R. Bird, Genisco Computers Corporation; presented at WESCON '85
3. *Basic Television and Video Systems*, 5th edition, by Bernard Grob, McGraw-Hill
4. *Getting the Best Performance from Video Digital-to-Analog Converters*, (AN-1) by Dennis Packard, Brooktree Corporation, San Diego
5. "A Cost-Effective Custom CAD System", paper by R.C. Burton, D.G. Brewer, R.E. Penman, and R. Schilimoeller, Computer Science Department, Brigham Young University and Signetics Corporation
6. "Lilith and Modula-2", by Richard Ohran, *Byte Magazine*, pgs. 181 – 192; August 1984
7. "Monolithic Color Palette Fills in the Picture for High-Speed Graphics", by Steven Sidman and John C. Kuklewicz, *Electronic Design*; November 29, 1984
8. *EIA Standard RS-343A: Electrical Performance Standards for High-Resolution Monochrome Closed-Circuit Television Camera*, by the Video Engineering Department of the Electronic Industries Association; September, 1969
9. "A Single-Chip RGB Digital-to-Analog Converter with High-Speed Color-Map Memory", by W. Mack and M. Horowitz, *Digest of the International Conference on Consumer Electronics*, p. 90; 1985

Signetics

Linear Products

NE/SE5410
10-Bit High-Speed Multiplying D/A Converter

Product Specification

DESCRIPTION

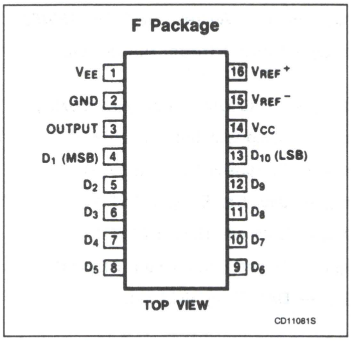
The NE5410/SE5410 are 10-bit Multiplying Digital-to-Analog Converters pin- and function-compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost effective D/A systems.

The NE/SE5410 provides complete 10-bit accuracy and differential non-linearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC, provide the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

- **Pin- and function-compatible with MC3410**
- **10-bit resolution and accuracy (±0.05%)**
- **Guaranteed differential non-linearity over temperature**
- **Wide compliance voltage range — −2.5 to +2.5V**
- **Fast settling time — 250ns typical**
- **Digital inputs are TTL- and CMOS-compatible**
- **High-speed multiplying input slew rate — 20mA/µs**
- **Reference amplifier internally-compensated**
- **Standard supply voltages +5V and −15V**

PIN CONFIGURATION



F Package
VEE 1
GND 2
OUTPUT 3
D1 (MSB) 4
D2 5
D3 6
D4 7
D5 8
16 VREF+
15 VREF−
14 VCC
13 D10 (LSB)
12 D9
11 D8
10 D7
9 D6
TOP VIEW
CD11081S

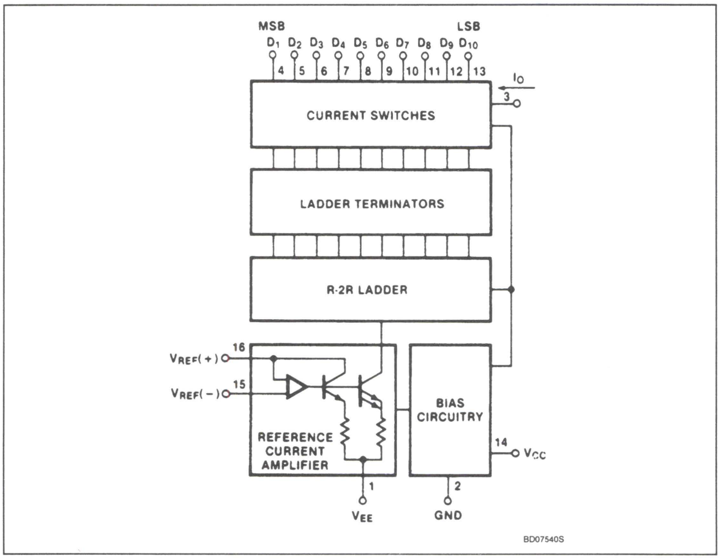
APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE5410F
16-Pin Cerdip	−55 to +125°C	SE5410F

BLOCK DIAGRAM



MSB
LSB
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10
4 5 6 7 8 9 10 11 12 13
IO
3
CURRENT SWITCHES
LADDER TERMINATORS
R-2R LADDER
16
VREF(+)
15
VREF(−)
REFERENCE CURRENT AMPLIFIER
BIAS CIRCUITRY
14
VCC
1
VEE
2
GND
BD07540S

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+7.0	V_{DC}
V_{EE}		−18	V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	+4, −5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating temperature range SE5410 NE5410	 −55 to +125 0 to +70	 °C °C
T_J	Junction temperature Ceramic package	 +150	 °C
T_{STG}	Storage temperature	−65 to +150	°C
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1]	1190	mW

NOTE:

1. Derate above 25°C at the following rate:
   F package at 9.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $I_{REF} = 2.0mA$, all digital inputs at high logic level. SE5410: $T_A = -55°C$ to $+125°C$, NE5410 Series: $T_A = 0°C$ to $+70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ϵ_R	Relative accuracy (Error relative to full scale I_O)	Over temperature		±0.025	±0.05	%
				±¼	±½	LSB
	Differential non-linearity	Over temperature		±0.025	±0.05	%
				±¼	±½	LSB
t_S	Settling time to within ±½ LSB (all bits low to high)	$T_A = 25°C$		250		ns
t_{PLH} t_{PHL}	Propagation delay time	$T_A = 25°C$		35 20		ns
TCI_O	Output full-scale current drift			20	40	ppm/°C
V_{IH}	Digital input logic levels (all bits) High level, Logic "1" Low level, Logic "0"		 2.0 		 0.8	V_{DC}
 I_{IH} I_{IL}	Digital input current (all bits) High level, $V_{IH} = 5.5V$ Low level, $V_{IL} = 0.8V$				 20 −20	μA
$I_{REF(15)}$	Reference input bias current (Pin 15)			−1.0	−5.0	μA
I_{OH}	Output current (all bits high)	$V_{REF} = 2.000V$, $R_{16} = 1000\Omega$	3.937	3.996	4.054	mA
I_{OL}	Output current (all bits low)	$T_A = 25°C$		0	0.4	μA
V_O	Output voltage compliance	$T_A = 25°C$ $\epsilon_R < 0.050\%$ relative to full-scale			−2.5 +2.5	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20		mA/μs

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $I_{REF} = 2.0mA$, all digital inputs at high logic level. SE5410: $T_A = -55°C$ to $+125°C$, NE5410 Series: $T_A = 0°C$ to $+70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0		µs
PSRR(−)	Output current power supply sensitivity			0.003	0.01	%/%
C_O	Output capacitance	$V_O = 0$		25		pF
C_I	Digital input capacitance (all bits high)			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			+2 −12	+4 −18	mA
V_{CC} V_{EE}	Power supply voltage range	$T_A = 25°C$ $V_O = 0$	+4.75 −14.25	+5.0 −15	+5.25 −15.75	V_{DC}
	Power consumption			190	300	mW

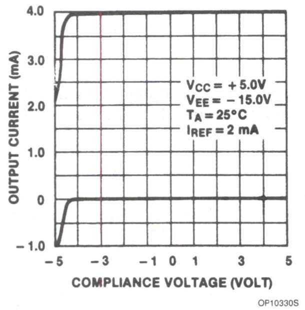


Figure 1. Output Current vs Output Compliance Voltage

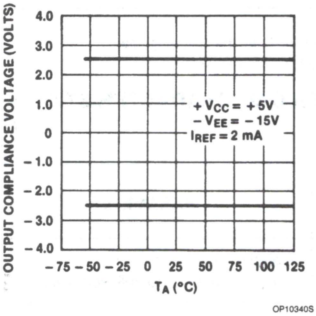


Figure 2. Maximum Output Compliance Voltage vs Temperature

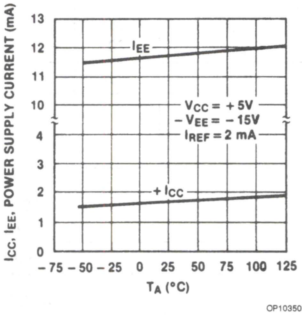


Figure 3. Power Supply Currents vs Temperature

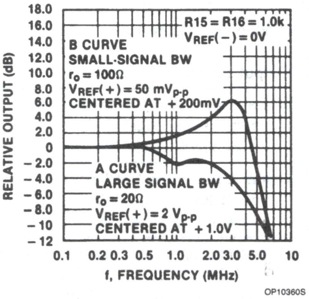


Figure 4. Reference Amplifier Frequency Response

CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion-implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs) (see Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully-differential current switches. The switches use current steering for speed.

An on-chip high slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a $1k\Omega$ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a $0.1\mu F$ capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of $1.0M\Omega$, the bandwidth of the reference amplifier is approximately half what it is in the case of $R16 = 1.0k\Omega$, and settling time is $\approx 10\mu s$. The reference amplifier phase margin decreases as the current souce value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

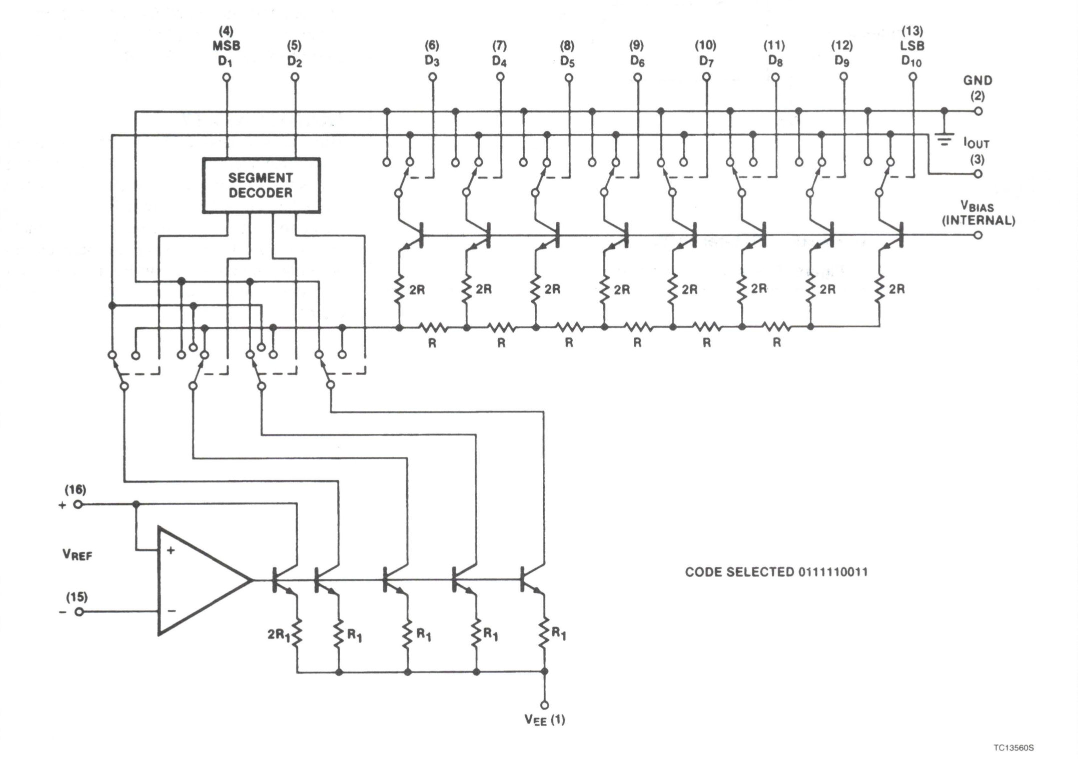
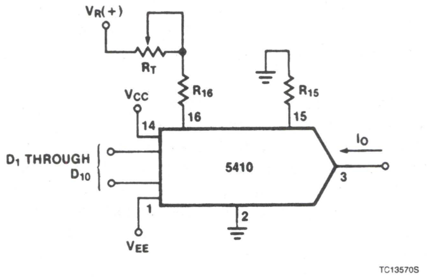
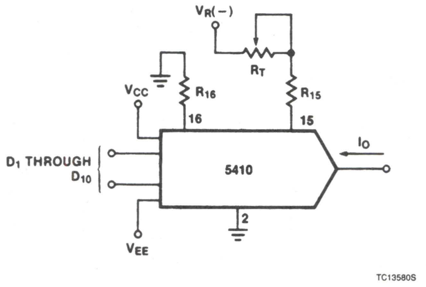


Figure 5. NE5410 Equivalent Circuit



NOTES:
$R_{16}+R_T = R_{15} = R_{REF}$
$R_T < \; < R_{16}$
I_O F.S. = 2 I_R = V_{REF}/R_{REF}

a. Positive Reference Voltabe



NOTES:
$R_{15}+R_T = R_{16}$
$R_T < \; < R_{15}$
$IV_{REF} \geqslant R_{VEE}+3V$

b. Negative Reference Voltage

Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +2.5V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full-scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ± ½ LSB at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for the output to settle to within ± ½ LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (< 0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to −2.5V, the settling time increases to 1.5µs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100µF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

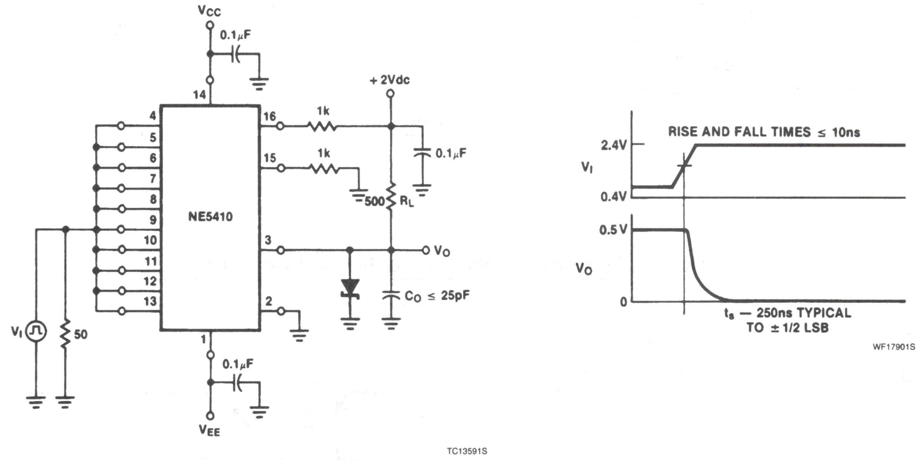

VCC
0.1µF
14
4
5
6
7
8
9
10
11
12
13
NE5410
16
15
1k
1k
+2Vdc
0.1µF
500
RL
3
VO
2
CO ≤ 25pF
1
0.1µF
VEE
VI
50
TC13591S
RISE AND FALL TIMES ≤ 10ns
2.4V
VI
0.4V
0.5V
VO
0
ts — 250ns TYPICAL TO ± 1/2 LSB
WF17901S

Figure 7. Settling Time

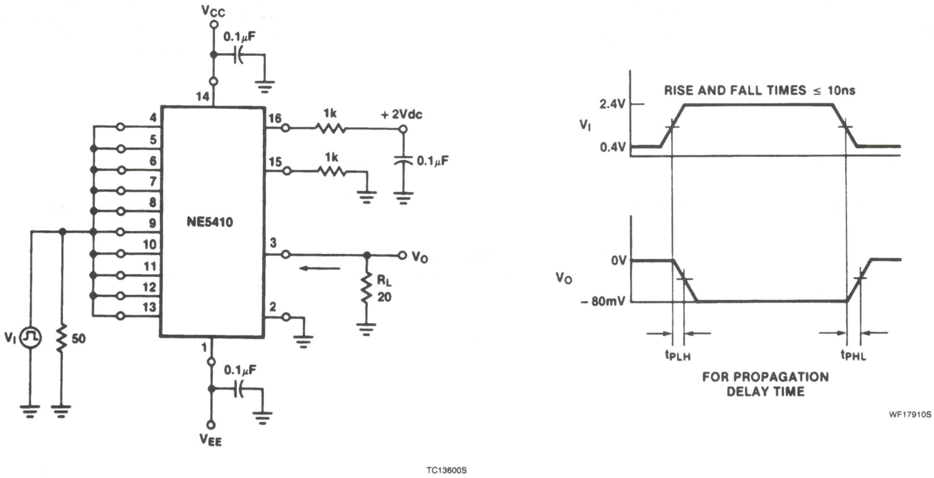
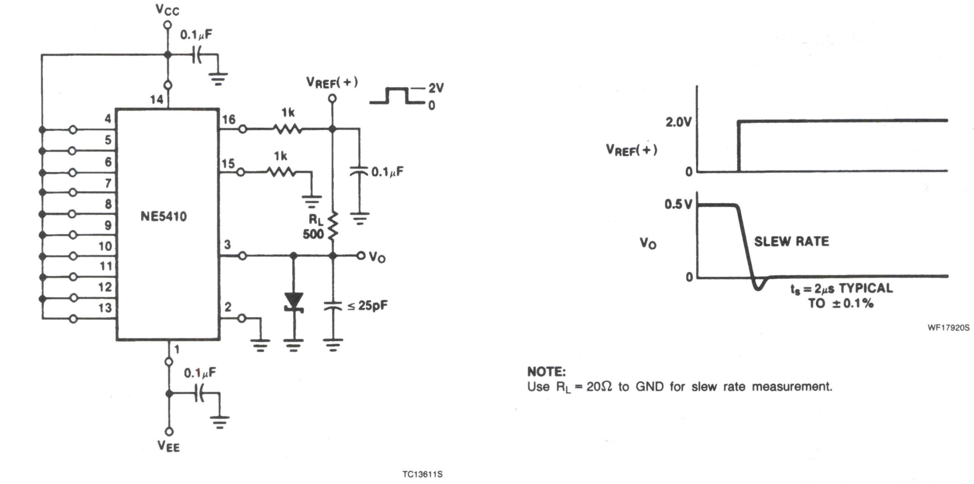
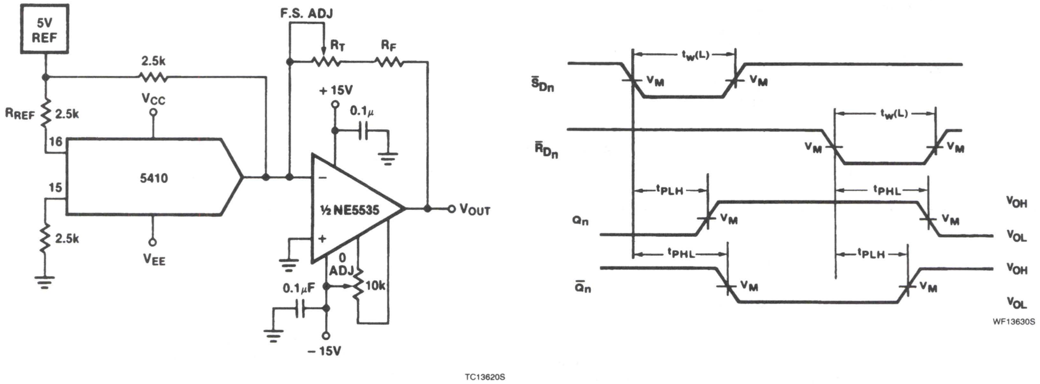

VCC
0.1µF
14
4
5
6
7
8
9
10
11
12
13
NE5410
16
15
1k
1k
+2Vdc
0.1µF
3
VO
RL
20
2
1
0.1µF
VEE
VI
50
TC13600S
RISE AND FALL TIMES ≤ 10ns
2.4V
VI
0.4V
0V
VO
−80mV
tPLH
tPHL
FOR PROPAGATION DELAY TIME
WF17910S

Figure 8. Propagation Delay Time


VCC
0.1μF
14
VREF(+)
2V
0
16
1k
15
1k
0.1μF
4
5
6
7
8
9
10
11
12
13
NE5410
RL
500
3
VO
2
≤ 25pF
1
0.1μF
VEE
TC13611S
2.0V
VREF(+)
0
0.5V
VO
SLEW RATE
0
ts = 2μs TYPICAL
TO ±0.1%
WF17920S

NOTE:
Use $R_L = 20\Omega$ to GND for slew rate measurement.

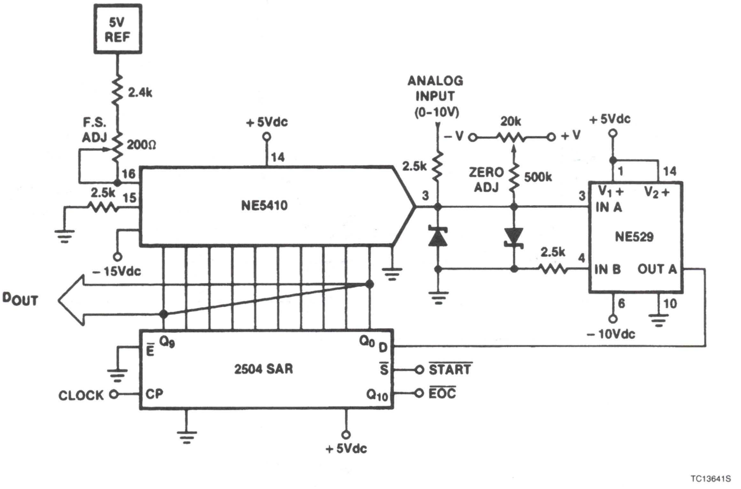
Figure 9. Reference Amplifier Settling Time and Slew Rate


5V
REF
RREF
2.5k
2.5k
VCC
16
5410
15
2.5k
VEE
F.S. ADJ
RT
RF
+15V
0.1μ
½ NE5535
VOUT
0
ADJ
10k
0.1μF
−15V
TC13620S
tw(L)
S̄Dn
VM
VM
tw(L)
R̄Dn
VM
VM
tPLH
tPHL
Qn
VM
VM
VOH
VOL
tPHL
tPLH
Q̄n
VM
VM
VOH
VOL
WF13630S

a. Bipolar Output (−10 to +10V)

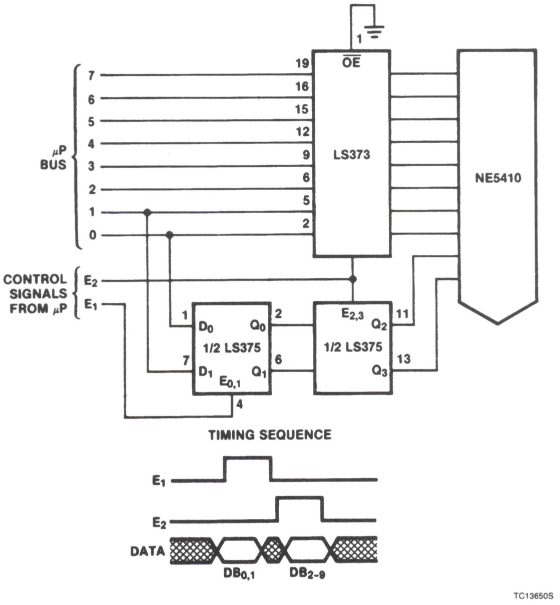
b. Unipolar Positive Output (0 − 10V)

Figure 10. Voltage Output Circuits


5V REF
2.4k
F.S. ADJ
200Ω
2.5k
16
15
+5Vdc
14
NE5410
3
−15Vdc
ANALOG INPUT (0-10V)
2.5k
−V
20k
+V
ZERO ADJ
500k
2.5k
+5Vdc
1
14
V1+
V2+
IN A
NE529
4
IN B
OUT A
6
10
−10Vdc
DOUT
Q9
Q0
D
E
2504 SAR
S
START
CLOCK
CP
Q10
EOC
+5Vdc
TC13641S

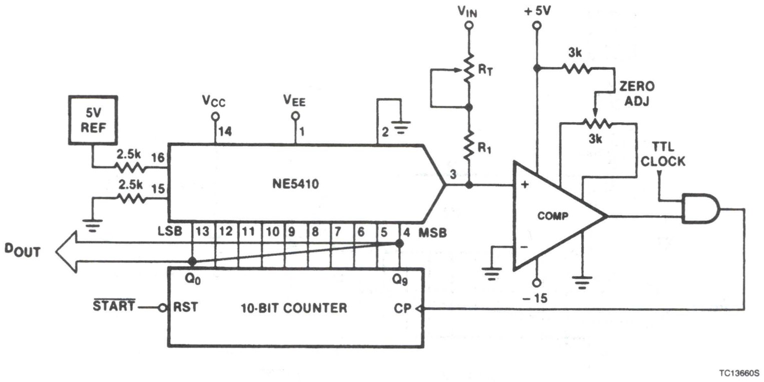
NOTES:
10-bit conversion time = 3.3μs with 3MHz clock.
This converter uses a 2504 12-bit successive approximation register in the short cycle operating mode where the end of conversion signal is taken from the first unused bit of the SAR (Q_{10}).

Figure 11. Successive Approximation A/D Converter


1
OE
19
16
15
12
9
6
5
2
7
6
5
4
3
2
1
0
μP BUS
LS373
NE5410
CONTROL SIGNALS FROM μP
E2
E1
1
D0
Q0
2
1/2 LS375
7
D1
E0,1
Q1
6
4
E2,3
Q2
11
1/2 LS375
Q3
13
TIMING SEQUENCE
E1
E2
DATA
DB0,1
DB2-9
TC13650S

NOTE:
With this double latch technique, valid data will be latched to the DAC until updated with the E_2 pulse. Timing will depend on the processor used.

Figure 12. 8-Bit μP Bus Interface


VIN
+5V
RT
3k
ZERO ADJ
3k
R1
TTL CLOCK
5V REF
VCC
VEE
14
1
2
2.5k
16
2.5k
15
NE5410
3
COMP
LSB
13
12
11
10
9
8
7
6
5
4
MSB
DOUT
Q0
Q9
START
RST
10-BIT COUNTER
CP
−15
TC13660S

NOTE:

V_{IN} FULL SCALE = 4mA $(R_1 + R_T)\left(\frac{1023}{1024}\right)$

Figure 13. Staircase A/D

Signetics

PNA7518

8-Bit Multiplying DAC

Product Specification

Linear Products

DESCRIPTION

The PNA7518 is an NMOS 8-bit multiplying digital-to-analog converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analog output at a sampling rate of 30MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analog signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive edge-triggered. The output impedance is approximately 0.5kΩ, depending upon the applied digital code. An additional operational amplifier is required for the full bandwidth. Two's complement is selected when STC (Pin 11) is HIGH or is not connected.

FEATURES

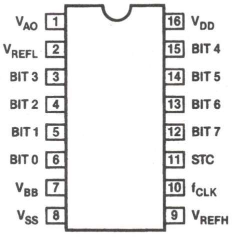
- **TTL input levels**
- **Positive edge-triggered**
- **Analog voltage output at 30MHz sampling rate**
- **Binary or two's complement input**
- **Output voltage accuracy to within ± ½ of the input LSB**

APPLICATIONS

- **Video data conversion**
- **CRT displays**
- **Waveform/test signal generation**
- **Color/black-and-white graphics**

PIN CONFIGURATION

N Package



TOP VIEW

CD10200S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{AO}	Analog output voltage
2	V_{refL}	Reference voltage LOW
3	bit 3	Digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	Least-significant bit (LSB)
7	V_{BB}	Back bias
8	V_{SS}	Ground
9	V_{refH}	Reference voltage HIGH
10	f_{CLK}	Clock input
11	STC	Select two's complement
12	bit 7	Most-significant bit (MSB)
13	bit 6	Digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	Positive supply voltage

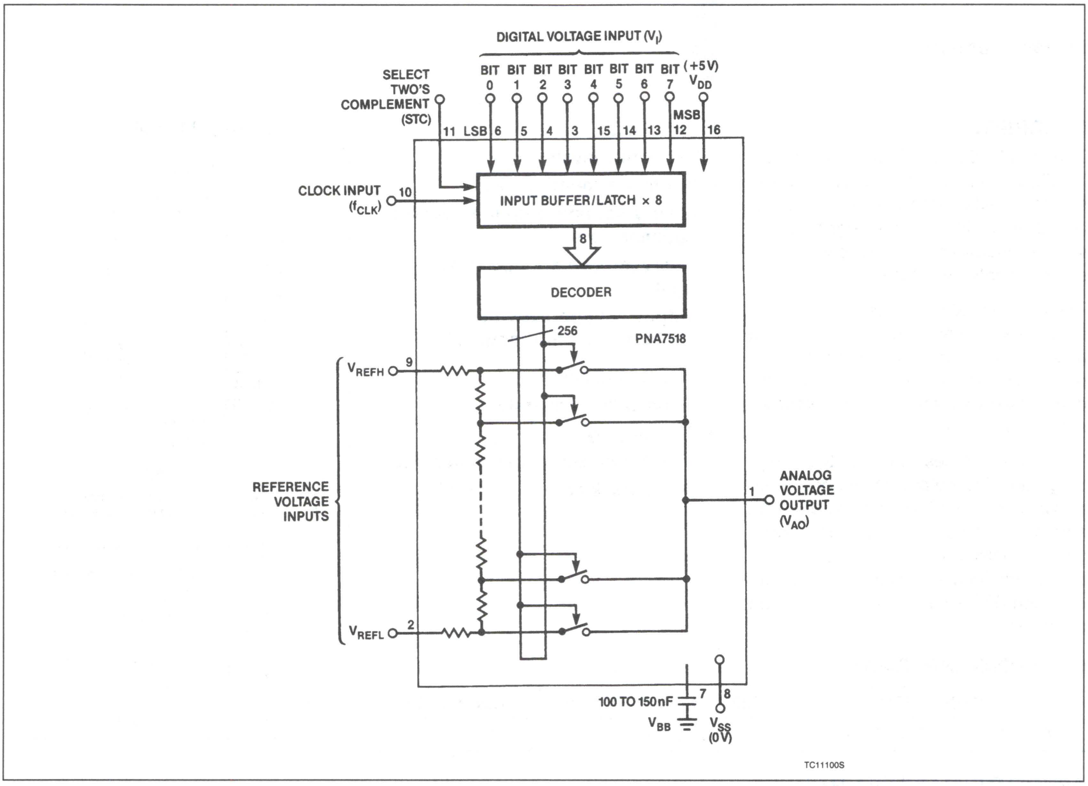
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38WE-1)	0 to +70°C	PNA7518N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 16)	−0.5 to +7	V
V_I	Input voltage range (Pins 3, 4, 5, 6, 11, 12, 13, 14 and 15)	−0.5 to +7	V
V_{AO}	Output voltage range (Pin 1)	−0.5 to +7	V
P_{TOT}	Total power dissipation	400	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

BLOCK DIAGRAM


DIGITAL VOLTAGE INPUT (V_I)
SELECT TWO'S COMPLEMENT (STC)
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
(+5V) V_DD
11 LSB 6 5 4 3 15 14 13 MSB 12 16
CLOCK INPUT (f_CLK) 10
INPUT BUFFER/LATCH × 8
8
DECODER
256
PNA7518
V_REFH 9
REFERENCE VOLTAGE INPUTS
V_REFL 2
1
ANALOG VOLTAGE OUTPUT (V_AO)
100 TO 150nF
7
8
V_BB
V_SS (0V)
TC11100S

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

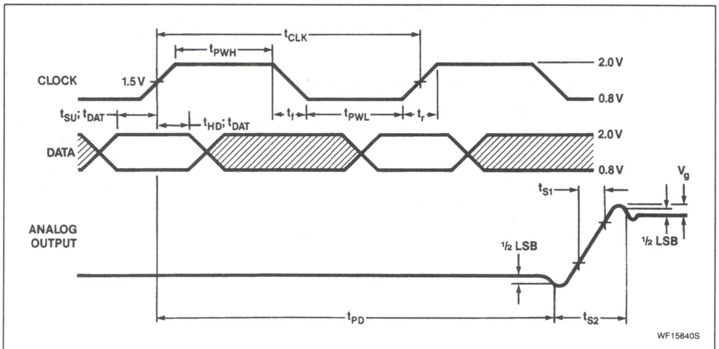

CLOCK
1.5V
t_CLK
t_PWH
2.0V
0.8V
t_SU; t_DAT
t_HD; t_DAT
t_f
t_PWL
t_r
DATA
2.0V
0.8V
ANALOG OUTPUT
V_g
t_S1
½ LSB
½ LSB
t_PD
t_S2
WF15840S

Figure 1. Switching Characteristics

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 to 5.5; V_{SS} = 0V; C_{BB} = 100nF; T_A = 0 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 16)					
V_{DD}	Supply voltage	4.5	5	5.5	V
I_{DD}	Supply current		50	80	mA
Reference voltages					
V_{REFL}	Reference voltage LOW (Pin 2)	−0.1		+2.1	V
V_{REFH}	Reference voltage HIGH (Pin 9)	−0.1		+2.1	V
R_{REF}	Reference ladder	150	230	300	Ω
Inputs					
	Digital input levels (TTL)[1]				
V_{IL}	input voltage LOW	0		0.8	V
V_{IH}	input voltage HIGH	2.0		5.25	V
I_{LI}	input leakage current			10	μA
	Clock input (Pin 10)				
V_{IL}	input voltage LOW	0		0.8	V
V_{IH}	input voltage HIGH	2.0		5.25	V
I_{LI}	input leakage current			10	μA
Output					
V_{AO}	Analog voltage output (Pin 1) at R_L = 200 kΩ)	0		2	V
BW	Bandwidth (−3 dB) at C_L = 6 pF		12		MHz
Output transients (glitches)[2]					
V_G	Glitch occurring at step 7F-80 (HEX): maximum amplitude for 1 LSB change area		3 23		LSB LSB ns
V_G	Glitch occurring at step 00-AA (HEX): maximum amplitude for 1 LSB change area		5 41		LSB LSB ns
P_{TOT}	Total power dissipation		300		mW

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = 4.5$ to 5.5; $V_{SS} = 0V$; $C_{BB} = 100nF$; $T_A = 0$ to $+70°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Clock input (Pin 10)				
f_{CLK}	frequency	1		30	MHz
t_{PWH}	pulse width HIGH	10			ns
t_{PWL}	pulse width LOW	10			ns
t_R	input rise time at $f_{CLK} = 30MHz$			3	ns
t_F	input fall time at $f_{CLK} = 30MHz$			3	ns
Switching characteristics (Figure 1)					
t_{SU}, t_{DAT}	Data setup time	3			ns
t_{HD}, t_{DAT}	Data hold time	4			ns
t_{PD}	Propagation delay time, input to output	$t_{CLK} + 15$	$t_{CLK} + 22$	$t_{CLK} + 30$	ns
t_{S1}	Settling time; 10 to 90% full-scale change; $C_L = 6pF$; $R_L = 200k\Omega$		13	20	ns
t_{S2}	Settling time to ±1 LSB; $C_L = 6pF$; $R_L = 200k\Omega$		40		ns
	Linearity at $R_L = 200k\Omega$; $V_O = 2V_{P-P}$			±½	LSB
Influence of clock frequency[2]					
	Cross-talk at 2 × f_{CLK}				
	amplitude		2		LSB
	area		8		LSB ns

NOTES:

1. Inputs Bit 0 to Bit 7 are positive edge-triggered and STC.
2. Measured at $V_{REFH} - V_{REFL} = 2.0$ V; 1 × LSB = 7.8mV. The energy equivalent of output transients is given as the area contained by the graph of output amplitude (LSB) against time (ns). The glitch area is independent of the value of V_{REF}. Glitch amplitudes and clock cross-talk can be reduced by using a shielded printed circuit board (see Pin Configuration).

Signetics

Linear Products

TDA1540TD, PN

14-Bit DAC (Serial Output)

Product Specification

DESCRIPTION

The TDA1540 is a monolithic integrated 14-bit digital-to-analog converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85dB in the audio band.

FEATURES

- **Clock frequency 12MHz**
- **Signal-to-noise ratio 85dB**
- **TTL compatible input**
- **On-chip current reference**
- **Inherent monotonicity from −25°C to 70°C**
- **Serial data input**

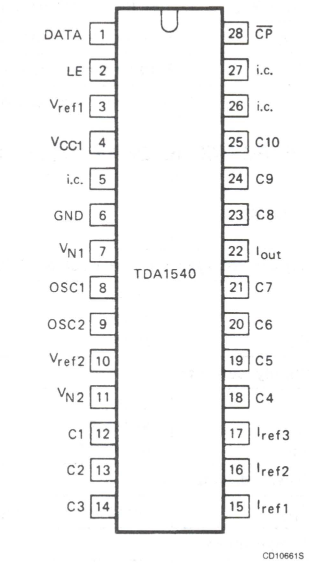
APPLICATIONS

- **Sound reproduction**
- **Recording systems**
- **Graphic display systems**
- **Electron-beam recording**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117BE)	0 to +70°C	TDA1540PN
28-Pin Plastic SO (SOT-117BE)	0 to +70°C	TDA1540D

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	DATA	Data input
2	LE	Latch enable input
3	V_{REF1}	Voltage reference
4	V_{CC1}	Positive supply
5	IC*	Frequency compensation on-chip operational amplifier
6	GND	Ground
7	V_{N1}	Negative supply
8	OSC1	Oscillator capacitor
9	OSC2	
10	V_{REF2}	Voltage reference
11	V_{N2}	Negative supply
12	C1	Doubling binary
13	C2	Weighted current
14	C3	Sources
15	I_{REF1}	Current reference sources
16	I_{REF2}	
17	I_{REF3}	
18	C4	
19	C5	Decoupling binary weighted
20	C6	Current sources
21	C7	
22	I_{OUT}	Analogue output
23	C8	Decoupling binary
24	C9	Weighted current
25	C10	Sources
26	IC*	Voltage reference
27	IC*	Voltage reference
28	$\overline{CP}$	Clock pulse input

ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	RATING	UNIT
	Supply voltages with respect to GND (Pin 6)		
V_{CC1}	at Pin 4	MAX. 12	V
V_{N1}	at Pin 7	MAX. −12	V
V_{N2}	at Pin 11	MAX. −20	V
$V_{P1} - V_{N2}$	at Pin 4 with respect to Pin 11	MAX. 32	V
$V_{N1} - V_{N2}$	at Pin 7 with respect to Pin 11	−1 to +20	V
P_{TOT}	Total power dissipation	Max. 600	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +80	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ at typical supply voltages unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply voltages with respect to GND (Pin 6)					
V_{CC1}	at Pin 4	3	5	7	V
V_{N1}	at Pin 7	−4.7	−5	−7	V
V_{N2}	at Pin 11	−16.5	−17	−18	V
Supply currents					
I_{CC1}	at Pin 4[1]		12	14	mA
I_{N1}	at Pin 7		−20	−24	mA
I_{N2}	at Pin 11		−11	−13	mA
Power dissipation					
P_{TOT}	Total power dissipation		350	410	mW
Temperature					
T_A	Operating ambient temperature range	−20		+70	°C
Data input DATA (Pin 1)					
V_{IH}	Input voltage HIGH	2.0		7.0	V
V_{IL}	Input voltage LOW	0		0.8	V
I_{IH}	Input current HIGH at V_{IH}			50	μA
$-I_{IL}$	Input current LOW at V_{IL}			0.2	mA
BR_{MAX}	Maximum input bit rate	12			Mbits/s
Latch enable input LE (Pin 2) **Clock input $\overline{CP}$ (Pin 28)**					
V_{IH}	Input voltage HIGH	2.0		7.0	V
V_{IL}	Input voltage LOW	0		0.8	V
I_{IH}	Input current HIGH at V_{IH}			50	μA
$-I_{IL}$	Input current LOW at V_{IL}			0.2	mA
f_{CPMAX}	Maximum clock frequency	12			MHz
Oscillator (Pins 8 and 9)					
f_{OSC}	Oscillator frequency at $C_{8-9} = 820pF$	100	160	200	kHz

14-Bit DAC (Serial Output) TDA1540TD, PN

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ at typical supply voltages unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Analog output I_{OUT} (Pin 22)					
V_{OC}	Output voltage compliance	−10		+10	mV
I_{FS}	Full-scale current	3.8	4.0	4.2	mA
$\pm I_{ZS}$	Zero-scale current			100	nA
TC_{FS}	Full-scale temperature coefficient $T_A = -20$ to $+70°C$		$\pm 30 \times 10^{-6}$		$°C^{-1}$
t_{CS}	Settling time to ± ½ LSB all bits on or off		0.5		μs
S/N	Signal-to-noise ratio^2	80	85		dB

NOTES:
1. When the output current is $\frac{1}{2}I_{FS}$ (½ full-scale output current).
2. Signal-to-noise ratio within 20Hz and 20kHz full-scale sinewave, generated at a sample rate of 44kHz.

FUNCTIONAL DESCRIPTION

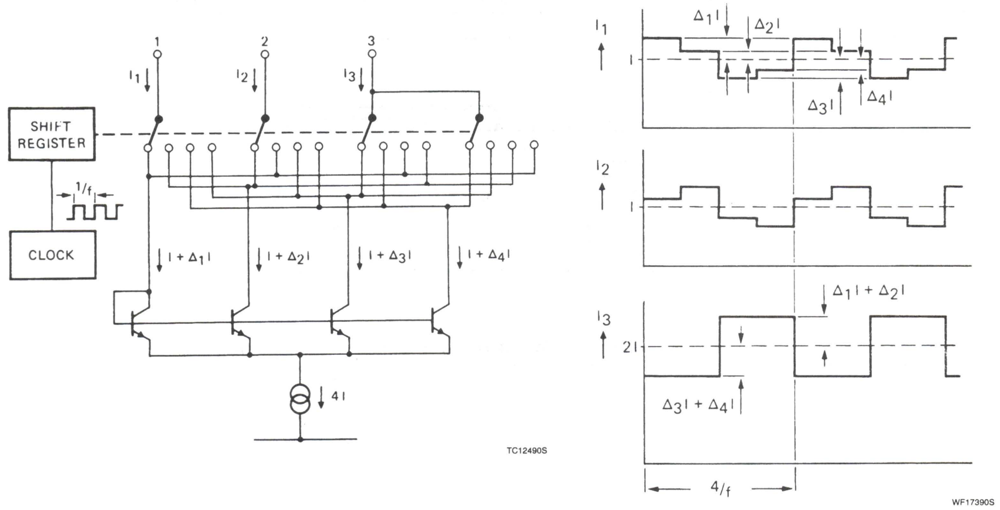
The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current 4 I of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an AC low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents I ($\bar{I}_1$), I($\bar{I}_2$) and 2I ($\bar{I}_3$) (see Figure 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Figure 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (Pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be 0V ± 10mV. The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Figure 4.



a. **Circuit Diagram of One Divider Stage**

b. **Waveforms Showing Output Currents I_1, I_2 and I_3 of Figure 1a**

Figure 1

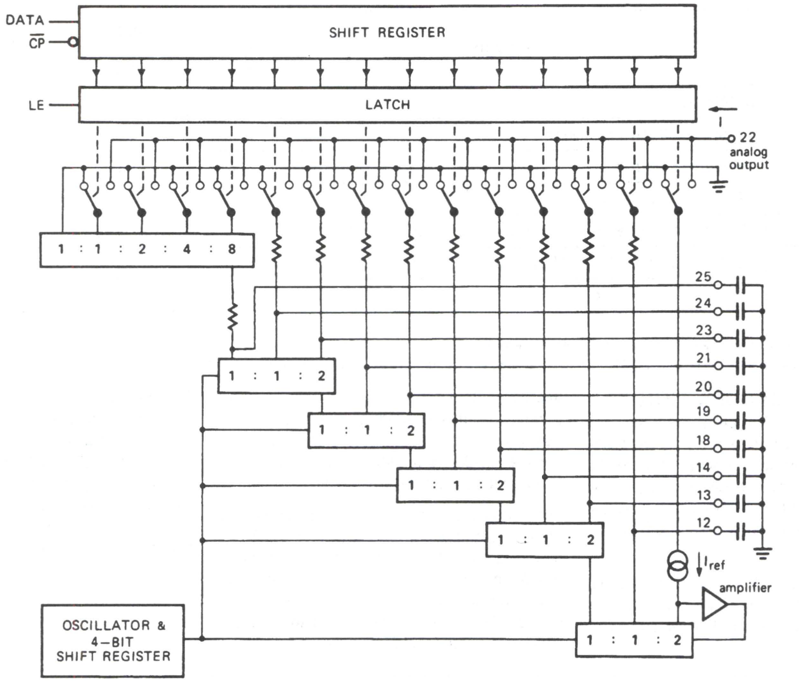

DATA
CP
SHIFT REGISTER
LE
LATCH
I
22
analog
output
1 : 1 : 2 : 4 : 8
25
24
23
21
20
19
18
14
13
12
1 : 1 : 2
I ref
amplifier
OSCILLATOR &
4-BIT
SHIFT REGISTER
TC12501S

Figure 2. Functional Diagram Showing Cascading of Current Division Stages

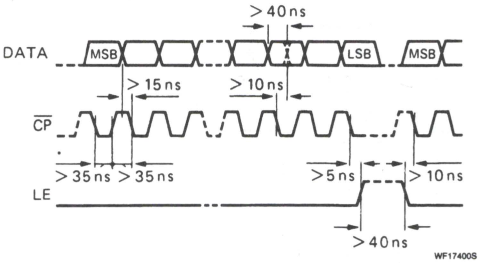

> 40 ns
DATA
MSB
LSB
MSB
> 15 ns
> 10 ns
CP
> 35 ns
> 35 ns
> 5 ns
> 10 ns
LE
> 40 ns
WF17400S

Figure 3. Format of Input Signals

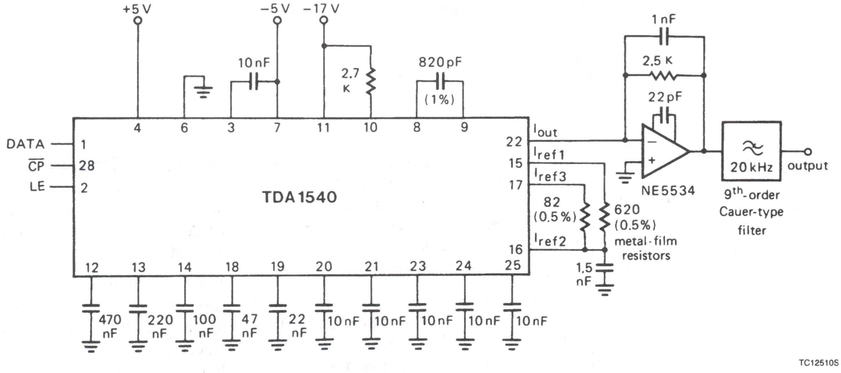

+5 V
−5 V
−17 V
10 nF
2.7 K
820 pF
(1%)
1 nF
2.5 K
22 pF
DATA
CP
LE
TDA1540
4
6
3
7
11
10
8
9
1
28
2
22
15
17
16
25
12
13
14
18
19
20
21
23
24
Iout
Iref1
Iref3
Iref2
82 (0.5%)
620 (0.5%)
metal-film resistors
1.5 nF
NE5534
20 kHz
output
9th-order Cauer-type filter
470 nF
220 nF
100 nF
47 nF
22 nF
10 nF
10 nF
10 nF
10 nF
10 nF
TC12510S

Figure 4. Application Circuit

Signetics

AN110
Monolithic 14-Bit DAC With 85dB Signal-to-Noise Ratio

Application Note

Linear Products

Author: R. J. v. d. Plassche

The introduction of digital signal processing in sound recording and reproduction systems imposes stringent requirements on the performance of digital-to-analog converters (DACs). Many of these systems demand converters with up to 16-bit resolution to obtain sufficiently high signal-to-noise ratio and good linearity.

The TDA1540 is the first monolithic bipolar 14-bit DAC with a signal-to-noise ratio of 85dB (typ) for audio signals, sampled at 44kHz. It uses a new method of current division, called dynamic element matching, to achieve high-accuracy binary-weighted currents with long-term stability. Dynamic element matching combines passive division with a time division concept which eliminates resistor trimming.

In addition, the TDA1540 features:

- **On-chip serial-to-parallel shift register and data latches**
- **On-chip current reference**
- **Inherent monotonicity from −25 to +70°C**
- **TTL-compatible input**
- **Serial data input (offset binary) which reduces feedthrough and correlated noise**
- **Improved bit switching — no deglitching circuit required.**

Table 1 gives further data on the TDA1540.

STANDARD DIGITAL-TO-ANALOG CONVERSION TECHNIQUES

Monolithic DACs widely use an R-2R resistive ladder network with multiple-emitter terminating transistors to generate binary-weighted currents. These currents are switched by digitally-controlled switches (bit switches) to a summing point; thereby digital-to-analog signal conversion is performed. Figure 1 shows a DAC of this type.

There are two problems in the design of an R-2R DAC: the weighting accuracy of the binary currents which is set by the tolerance of the resistors and transistors, and the switching of the accurately-weighted binary currents without glitches which determines the dynamic performance. Regarding the problem of accuracy, Table 2 shows that it is straightforward to integrate DACs having up to 10 bits; a 10-bit converter requires a 512:1 current division, i.e., requires resistor tolerance better than 0.05%. 12-bit converters usually need laser-trimming of thin-film resistors, or trimming of the binary-weighted currents using Zener zapping to achieve 12-bit accuracy.

It is questionable how successfully trimming can be applied to 14- or 16-bit converters. Mounting the chip after trimming can change the resistances; trimming after mounting can be expensive. Long-term stability may be a problem too. Furthermore, the cost of laser-trimming in large-volume production can be significant.

In the TDA1540 trimming has been eliminated by dynamic element matching.

DYNAMIC ELEMENT MATCHING

Basic Current Divider

Figure 2a shows the block diagram of the divider. It consists of a passive current divider and a set of switches driven at a frequency, f, by a clock pulse generator.

The input current 2I is divided into two nearly equal parts: $I_1 = I + \Delta I$ and $I_2 = I - \Delta I$. Then, I_1 and I_2 are interchanged with respect to the output terminals 3 and 4 *for equal times* by means of the switches. The average current at each output terminal is then exactly equal and has a value I, see Figure 2b.

There is a small ripple current $2\Delta I_{P\text{-}P}$ of frequency f on the output currents. This ripple is proportional to the accuracy of current division by the passive divider. By using a simple low-pass filter to suppress the ripple, an exact current ratio of 2:1 (input-to-output) is obtained.

If the time that I_1 and I_2 are switched to each output differs by Δt (see Figure 2b) there will be an error in their 1:1 current ratio of $(\Delta t/t)(\Delta I/I)$. For $\Delta I/I \approx 1\%$ and $\Delta t/t \approx 0.1\%$, this error is $\approx 0.001\%$.

By cascading divider stages, an accurate binary-weighted current network is formed. However, in a practical circuit, each stage requires a minimum supply voltage of ≈2V. This leads to an impractically large supply voltage for a 14-bit current network. Therefore, an improved divider is used which gives more weighted currents in one current interchange.

Improved Divider

In the improved divider, a current, 4I, is divided into four nearly equal parts: $I + \Delta_1 I$, $I + \Delta_2 I$, $I + \Delta_3 I$ and $I + \Delta_4 I$, (see Figure 3a). Note that $\Delta_1 + \Delta_2 + \Delta_3 + \Delta_4 = 0$.

These currents are fed into a switching network which interchanges all the currents with respect to the output terminals for equal times. The switches are controlled by signals from a 4-bit shift register.

At the output of the switching network, two currents are combined. Thus, the output currents have average values of 2I, I and I, Figure 3b. All currents have a ripple of frequency f/4 (the time for one complete interchange of the four currents being 4/f). Timing errors in the current switching have the same effect on accuracy as for the basic divider.

Figure 4 shows the circuit diagram of a practical current divider. Transistors TR1, TR2, TR3 and TR4, with the resistors, R, divide the current 4I into four nearly equal currents. These currents are fed into the switching network which consists of Darlington transistor switches to minimize base current loss. Two currents are summed directly, giving an output current of 21 (avg). A 4-bit shift register controls the transistor switches which for accurate current division must have high current gain.

BINARY-WEIGHTED CURRENT NETWORK

By cascading divider stages, a binary-weighted current network is formed (see Figure 5). In the first stage the on-chip reference current source, I_{REF}, and a current amplifier form an accurate current mirror. The reference current is used as the most significant bit current, which eliminates filtering.

To obtain 14-bit accuracy, a choice can be made between the number of switched and unswitched current dividers. The minimum supply voltage decreases as the number of unswitched dividers increases. However, the number of unswitched dividers is limited by circuit yield. Five switched dividers followed by a 4-bit passive divider using emitter scaling represents the best compromise between supply voltage and circuit yield.

Monolithic 14-Bit DAC With 85dB Signal-to-Noise Ratio AN110

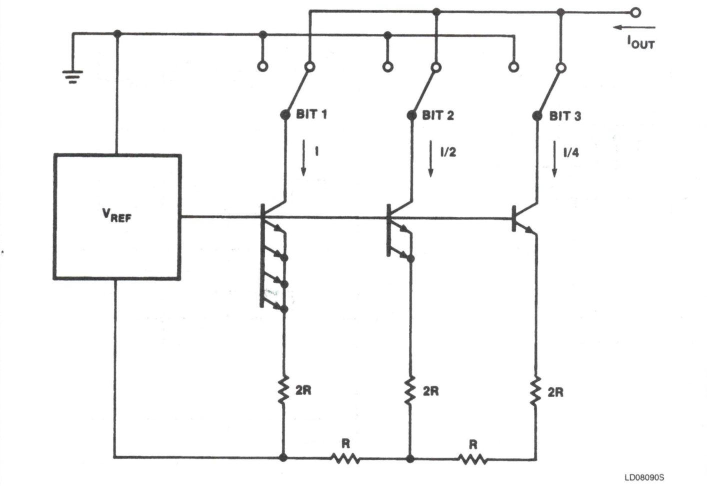


Figure 1. 3-Bit Binary-Weighted R-2R Digital-to-Analog Converter

Table 1. TDA1540 Data

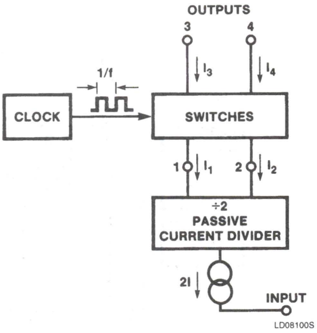
Resolution	14 bits
Signal-to-noise ratio (typ.)	85dB
Linearity (typ.)	± ¼LSB at $T_A = 25°C$ ± ½LSB $-20°C < T_A < +70°C$
Full-scale current (typ.)	4mA
Settling time to ± ½LSB (for a full-scale change)	typ. 1µs
Maximum input bit rate	12 Mbit/s
Power dissipation	350mW
Supply voltages	+5V, −5V and −17V
Encapsulation	28-pin ceramic DIP

NOTE:
1. Measured between 31.5Hz and 20kHz at a sampling frequency of 44kHz.

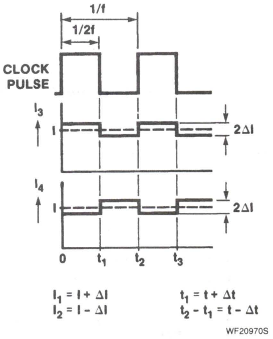
Table 2. Matching Tolerance of Different Types of Resistor

Fabrication Process	MATCHING TOLERANCE			
	σ(%)		Mean (%)	
	10µm	40µm	10µm	50µm
Diffusion	0.44	0.23	−0.1	0.07
Thin-film	0.24	0.11	−0.1	−0.06
Ion implantation	0.34	0.12	−0.04	0.05

Resistor linewidth 10µm and 40µm



a. Basic Current Divider Using Dynamic Element Matching



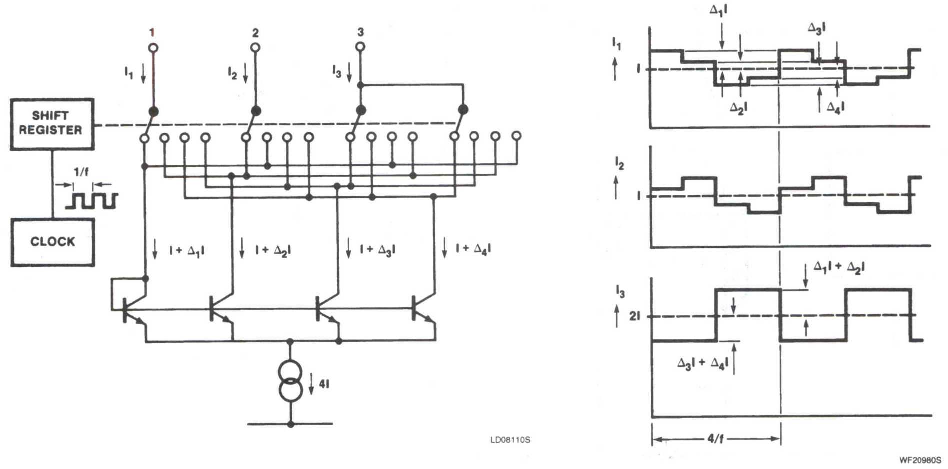
b. Output Currents I_3 and I_4

Figure 2

FILTERS AND BIT SWITCHES

Figure 6 shows how the output currents of a switched divider stage are filtered and switched to the output. R1C1 and R2C2 form first-order filters (the capacitors are connected externally). Darlington transistors TR3, TR4 and TR5, TR6 isolate the filters from the switching of the binary-weighted currents to the output (bit switching). Bit switching is performed with a diode-transistor configuration TR1, D1 and TR2, D2, enabling fast and accurate switching with no loss of base currents.

Individual filtering of bit currents minimizes the noise of the TDA1540 output current, and makes the conversion time solely dependent upon the speed of the bit switches.


1
2
3
I_1
I_2
I_3
SHIFT REGISTER
1/f
CLOCK
$I + \Delta_1 I$
$I + \Delta_2 I$
$I + \Delta_3 I$
$I + \Delta_4 I$
4I
LD08110S
$\Delta_1 I$
$\Delta_3 I$
$\Delta_2 I$
$\Delta_4 I$
I
$\Delta_1 I + \Delta_2 I$
2I
$\Delta_3 I + \Delta_4 I$
4/f
WF20980S

a. Improved Current Divider

b. Output Currents I_1, I_2 and I_3

Figure 3

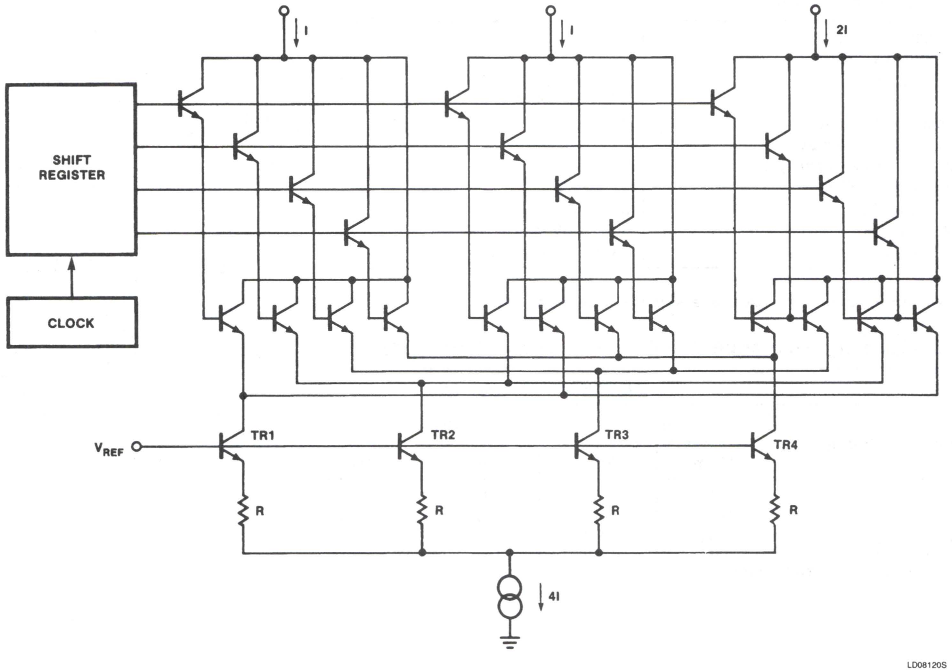

I
I
2I
SHIFT REGISTER
CLOCK
TR1
TR2
TR3
TR4
V_{REF}
R
R
R
R
4I
LD08120S

Figure 4. Circuit Diagram of the Practical Current Divider

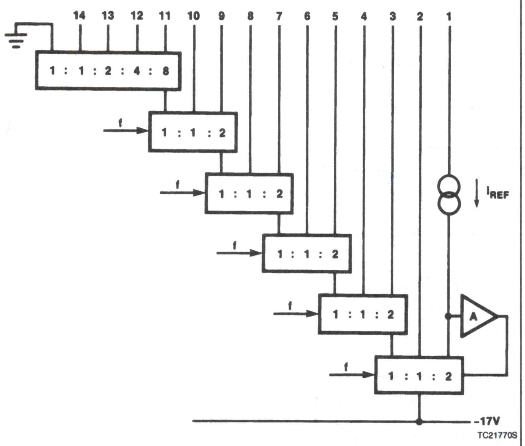

14 13 12 11 10 9 8 7 6 5 4 3 2 1
1 : 1 : 2 : 4 : 8
f
1 : 1 : 2
I_REF
A
-17V
TC21770S

Figure 5. Binary-Weighted Current Network

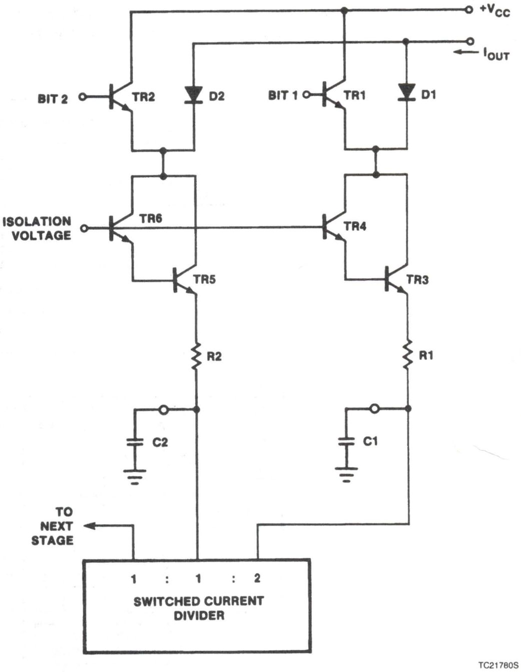

+VCC
IOUT
BIT 2
TR2
D2
BIT 1
TR1
D1
ISOLATION VOLTAGE
TR6
TR4
TR5
TR3
R2
R1
C2
C1
TO NEXT STAGE
1 : 1 : 2
SWITCHED CURRENT DIVIDER
TC21780S

Figure 6. Filtering and Switching the Binary-Weighted Currents to the Output

COMPLETE 14-BIT DAC

Figure 7 is the block diagram of the complete DAC. It shows the 14-bit binary-weighted current network, the reference current source, individual bit-current filters and the bit switches. The shift register that controls the Darlington transistor switches is at the bottom of the figure.

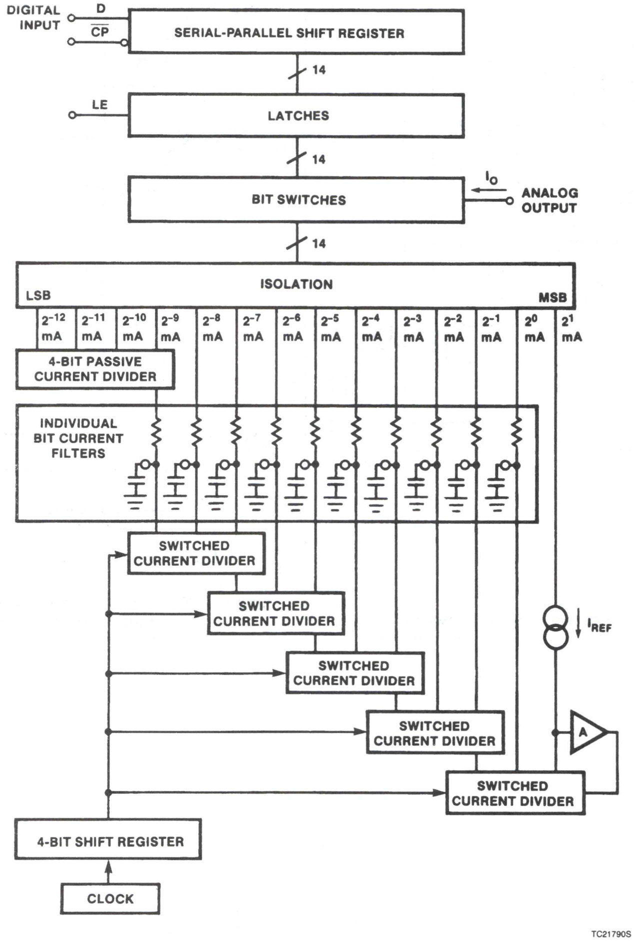

DIGITAL INPUT
D
CP
SERIAL-PARALLEL SHIFT REGISTER
14
LE
LATCHES
14
BIT SWITCHES
I_O
ANALOG OUTPUT
14
ISOLATION
LSB
MSB
2^{-12} mA
2^{-11} mA
2^{-10} mA
2^{-9} mA
2^{-8} mA
2^{-7} mA
2^{-6} mA
2^{-5} mA
2^{-4} mA
2^{-3} mA
2^{-2} mA
2^{-1} mA
2^{0} mA
2^{1} mA
4-BIT PASSIVE CURRENT DIVIDER
INDIVIDUAL BIT CURRENT FILTERS
SWITCHED CURRENT DIVIDER
SWITCHED CURRENT DIVIDER
SWITCHED CURRENT DIVIDER
SWITCHED CURRENT DIVIDER
SWITCHED CURRENT DIVIDER
I_{REF}
A
4-BIT SHIFT REGISTER
CLOCK
TC21790S

Figure 7. Block Diagram of the TDA1540

Monolithic 14-Bit DAC With 85dB Signal-to-Noise Ratio AN110

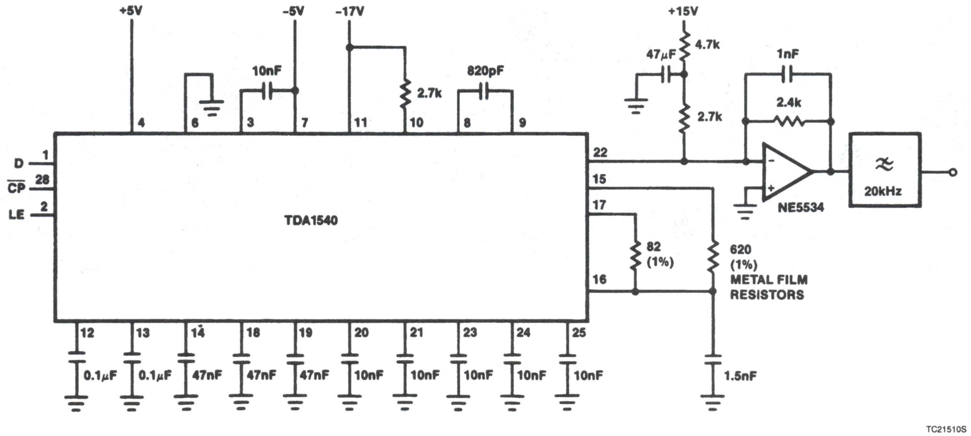

+5V
-5V
-17V
+15V
10nF
2.7k
820pF
47µF
4.7k
2.7k
1nF
2.4k
4
6
3
7
11
10
8
9
D 1
CP 28
LE 2
TDA1540
22
15
17
16
NE5534
20kHz
82 (1%)
620 (1%) METAL FILM RESISTORS
12
13
14
18
19
20
21
23
24
25
0.1µF
0.1µF
47nF
47nF
47nF
10nF
10nF
10nF
10nF
10nF
1.5nF
TC21510S

Figure 8. Circuit Diagram of a Voltage Output Digital-to-Analog Converter Using the TDA1540

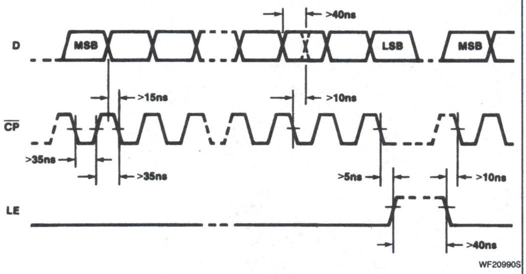

D
CP
LE
MSB
LSB
MSB
>40ns
>15ns
>10ns
>35ns
>35ns
>5ns
>10ns
>40ns
WF20990S

Figure 9. TDA1540 Timing Diagram

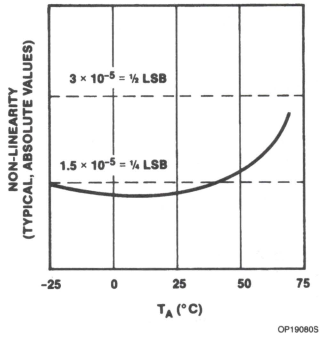


Figure 10. Non-Linearity of the TDA1540 as a Function of Temperature

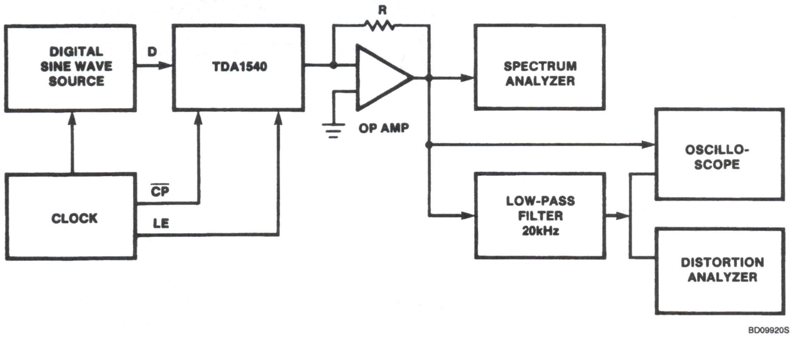
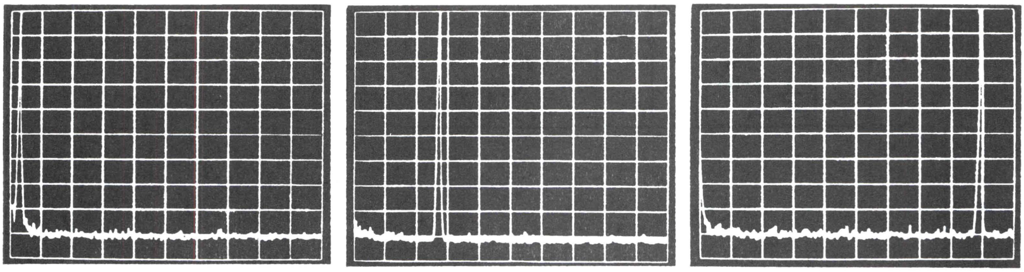

DIGITAL SINE WAVE SOURCE
D
TDA1540
R
OP AMP
SPECTRUM ANALYZER
OSCILLO-SCOPE
CLOCK
CP
LE
LOW-PASS FILTER 20kHz
DISTORTION ANALYZER
BD09920S

Figure 11. Arrangement for Measuring Dynamic Performance

Monolithic 14-Bit DAC With 85dB Signal-to-Noise Ratio AN110



NOTE:
Vertical Scale 10dB/div., Horizontal Scale 2kHz/div. Bandwidth 30Hz.

Figure 12. Distortion of an Output Sine Wave of Frequency 600Hz, 5.5kHz and 18kHz, Respectively

Figure 8 shows how to obtain a voltage output using the TDA1540 with an operational amplifier.

Figure 9 shows the input data format D, and the corresponding timing signals $\overline{CP}$ (clock input) and LE (latch enable).

PERFORMANCE

Linearity

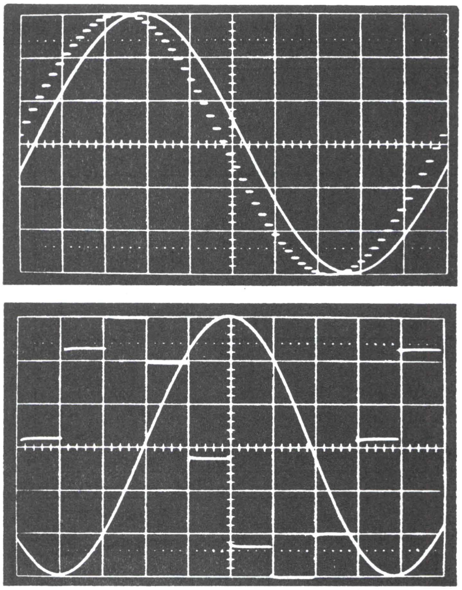
A DAC is monotonic if the non-linearity is less than ± ½ LSB. Figure 10 shows that the non-linearity of the TDA1540 is typically less than ½LSB (3×10^{-5}) over the temperature range −20 to +70°C.

Dynamic Performance

Figure 11 shows the arrangement used to measure dynamic performance. A digital sine wave source produces 14-bit words which are latched at 44kHz. The outputs of the latches drive directly the bit switches of the converter. A high-speed operational amplifier with feedback resistor R converts the output current of the converter into a voltage suitable for examination by spectrum analyzer and oscilloscope, or distortion analyzer.

Figure 12 shows the results of spectrum analysis. For sine waves of 600Hz, 5.5kHz and 18kHz, distortion is about −90dB with respect to the maximum sine wave output. Note, −90dB is the limit of resolution of the spectrum analyzer.

Figure 13 shows oscillograms of the filtered and unfiltered output signals. The low-pass filter introduces a delay in the output signal.



NOTE:
Vertical Scale 0.33 Volt/Div.

Figure 13. Filtered and Unfiltered Output Signals: Above, 1kHz; Below, 6.3kHz

APPLICATIONS

Dynamic element matching is a simple, accurate, and reliable method of current division for high-accuracy monolithic DACs; the resulting dynamic performance of the TDA1540 makes it ideal for sound reproduction and recording systems.

Its 15-bit linearity also makes it suitable for applications that do not require 14-bit resolution, but demand high linearity to improve relative accuracy. Such applications include graphic display systems, electron-beam recording and nuclear instrumentation.

The TDA1540 easily fulfills the requirements of a 12-bit DAC for telephony. For instrument manufacturers, the TDA1540 can extend present limits of performance of distortion meters, spectrum analyzers, sine wave and other signal generators.

The use of over-sampling techniques with the TDA1540 further improves the S/N ratio in audio applications and simplifies output analog filters.

Signetics

TDA1541

Dual 16-Bit Digital-to-Analog Converter

Product Specification

Linear Products

DESCRIPTION

The TDA1541 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed for use in hi-fi digital audio equipment such as compact disc players, digital tape, or cassette recorders.

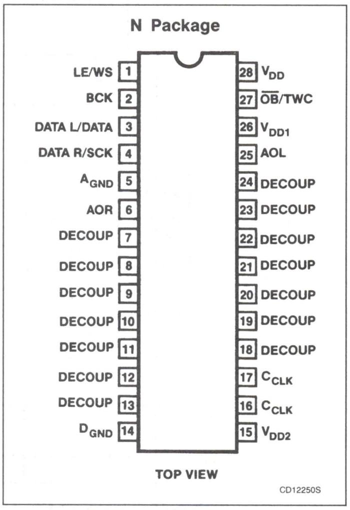
FEATURES

- **Selectable input format: offset binary or two's complement**
- **Internal timing and control circuit**
- **TTL-compatible digital inputs**
- **High maximum input bit rate and fast settling time**
- **6Mbits/s data rate**
- **Low linearity error (½ LSB typ.)**
- **Fast settling (1μs typ.)**

APPLICATIONS

- **Compact disc players**
- **Digital audio tape, and cassette recorders and players**
- **Waveform generation**

PIN CONFIGURATION


N Package
LE/WS 1
BCK 2
DATA L/DATA 3
DATA R/SCK 4
AGND 5
AOR 6
DECOUP 7
DECOUP 8
DECOUP 9
DECOUP 10
DECOUP 11
DECOUP 12
DECOUP 13
DGND 14
28 VDD
27 OB/TWC
26 VDD1
25 AOL
24 DECOUP
23 DECOUP
22 DECOUP
21 DECOUP
20 DECOUP
19 DECOUP
18 DECOUP
17 CCLK
16 CCLK
15 VDD2
TOP VIEW
CD12250S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	−20°C to +70°C	TDA1541N

ABSOLUTE MAXIMUM RATINGS

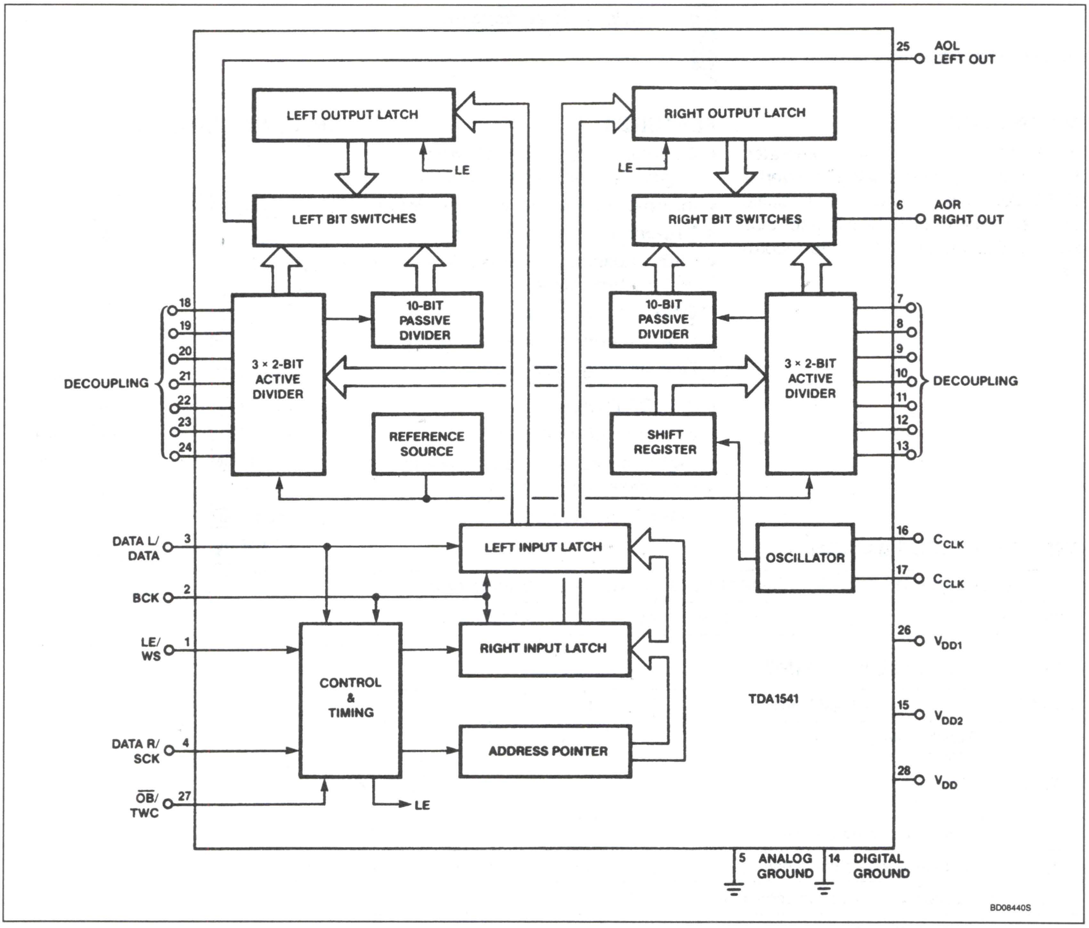
SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage ranges		
V_{DD}	Pin 28	+7	V
V_{DD1}	Pin 26	−7	V
V_{DD2}	Pin 15	−17	V
T_J	Junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C
V_{ES}	Electrostatic handling[1]	−1000 to +1000	V

NOTE:

1. Discharging a 250pF capacitor through a 1kΩ series resistor.

Dual 16-Bit Digital-to-Analog Converter TDA1541

BLOCK DIAGRAM


25 AOL LEFT OUT
LEFT OUTPUT LATCH
LE
LEFT BIT SWITCHES
RIGHT OUTPUT LATCH
LE
RIGHT BIT SWITCHES
6 AOR RIGHT OUT
10-BIT PASSIVE DIVIDER
3 × 2-BIT ACTIVE DIVIDER
DECOUPLING
18
19
20
21
22
23
24
REFERENCE SOURCE
10-BIT PASSIVE DIVIDER
3 × 2-BIT ACTIVE DIVIDER
SHIFT REGISTER
7
8
9
10
11
12
13
DECOUPLING
DATA L/ DATA 3
BCK 2
LE/ WS 1
DATA R/ SCK 4
OB/ TWC 27
LEFT INPUT LATCH
RIGHT INPUT LATCH
CONTROL & TIMING
ADDRESS POINTER
LE
OSCILLATOR
16 C_{CLK}
17 C_{CLK}
26 V_{DD1}
15 V_{DD2}
28 V_{DD}
TDA1541
5 ANALOG GROUND
14 DIGITAL GROUND
BD08440S

DC AND AC ELECTRICAL CHARACTERISTICS $V_{DD} = +5V$; $V_{DD1} = -5V$; $V_{DD2} = -15V$; $T_A = +25°C$; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
	Supply voltage ranges				
V_{DD}	Pin 28	4.0	5.0	6.0	V
$-V_{DD1}$	Pin 26	4.5	5.0	6.0	V
$-V_{DD2}$	Pin 15	14	15	16	V
	Supply currents				
I_{DD}	Pin 28		45	60	mA
$-I_{DD1}$	Pin 26		45	75	mA
$-I_{DD2}$	Pin 15		25	60	mA
	Resolution		16		bits
Inputs					
	Input current (Pin 3 and Pin 4)				
I_{IL}	digital inputs LOW ($< 0.8V$)			TBD	mA
I_{IH}	digital inputs HIGH ($> 2.0V$)			TBD	μA
	Input frequency				
f_{SCK}	at clock input (Pin 4)			12	MHz
f_{BCK}	at clock input (Pin 2)			6	MHz
f_{DAT}	at data inputs (Pin 3 and Pin 4)			6	MHz
f_{WS}	at word select input (Pin 1)			200	kHz
C_I	Input capacitance of digital inputs		12		pF
Oscillator					
f_{OSC}	Oscillator frequency	150	200	250	kHz
Analog outputs (AOL; AOR)					
V_{OC}	Output voltage compliance	TBD		TBD	mV
I_{FS}	Full-scale current	3.4	4.0	4.6	mA
$\pm I_{ZS}$	Zero-scale current		TBD		nA
TC_{FS}	Full-scale temperature coefficient $T_A = -20$ to $+70°C$		± 200		ppm/°C
	Linearity error integral				
E_1	at $T_A = 25°C$		0.5		LSB
E_1	at $T_A = -20$ to $+70°C$		TBD		LSB
	Linearity error differential				
E_{D1}	at $T_A = 25°C$		0.5	1	LSB
E_{D1}	at $T_A = -20$ to $+70°C$		TBD		LSB
S/N	Signal-to-noise ratio + THD[1]	90	95		dB
t_{CS}	Settling time to ± 1 LSB		1		μs
∝	Channel separation	80	TBD		dB
ΔI_{FS}	Unbalance between outputs		0.1	0.2	dB
t_D	Time delay between outputs			1	μs
	Power supply ripple rejection[2]				
RR	$V_{DD} = +5V$		TBD		dB
RR	$V_{DD1} = -5V$		TBD		dB
RR	$V_{DD2} = -15V$		TBD		dB
S/N	Signal-to-noise ratio at bipolar zero		−100		dB

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{DD} = +5V$; $V_{DD1} = -5V$; $V_{DD2} = -12V$; $T_A = +25°C$; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Timing (see Figures 2, 3, and 4)					
t_R	Rise time			35	ns
t_F	Fall time			35	ns
t_{CY}	Bit clock cycle time	160			ns
t_{HB}	Bit clock High time	48			ns
t_{LB}	Bit clock Low time	48			ns
t_{FBRL}	Bit clock fall time to latch rise time	0			ns
t_{RBFL}	Bit clock rise time to latch fall time	0			ns
t_{SDB}	Data setup time to bit clock	32			ns
t_{HDB}	Data hold time to bit clock	0			ns
t_{SDS}	Data setup time to system clock	32			ns
t_{HWS}	Word select hold time to system clock	0			ns
t_{SWS}	Word select setup time to system clock	32			ns
t_{FBRS}	Bit clock fall time to system clock rise time	32			ns
t_{RSFB}	System clock rise time to bit clock fall time	32			ns
t_{FSRB}	System clock fall time to bit clock rise time	50			ns
t_{RBFS}	Bit clock rise time to system clock fall time	0			ns
t_{LLE}	Latch enable Low time	20			ns
t_{HLE}	Latch enable High time	32			ns

NOTES:
1. Signal-to-noise ratio + THD with 1kHz full-scale sine wave generated at a sampling rate of 176.4kHz.
2. V_{RIPPLE} = 1% of supply voltage and f_{RIPPLE} = 100Hz.

FUNCTIONAL DESCRIPTION

The TDA1541 accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit rate and fast settling time facilitates application in 4× oversampling systems (44.1kHz to 176.4kHz) with the associated simple analog filtering function (low-order, linear phase filter).

Input Data Selection

(See also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analog outputs AOL and AOR.

With $\overline{OB}$/TWC connected to V_{DD}, the mode is the same, but data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to (V_{DD1}) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied by BCK and a latch-enable input (LE). With this mode selected, the data must be in offset binary.

The format of data input signals is shown in Figures 2, 3, and 4.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL-compatible.

Dual 16-Bit Digital-to-Analog Converter TDA1541

Table 1. Input Data Selection

$\overline{\text{OB}}$/TWC	MODE	PIN 1	PIN 2	PIN 3	PIN 4
−5V	Simultaneous	LE	BCK	DATA L	DATA R
0V	Time MUX OB	WS	BCK	DATA OB	SCK
+5V	Time MUX TWC	WS	BCK	DATA TWC	SCK

Where:
LE = Latch enable
WS = Word select
BCK = Bit clock
DATA L = Data left
DATA R = Data right
DATA OB = Data offset binary
DATA TWC = Data two's complement
MUX OB = Multiplexed offset binary
MUX TWC = Multiplexed two's complement

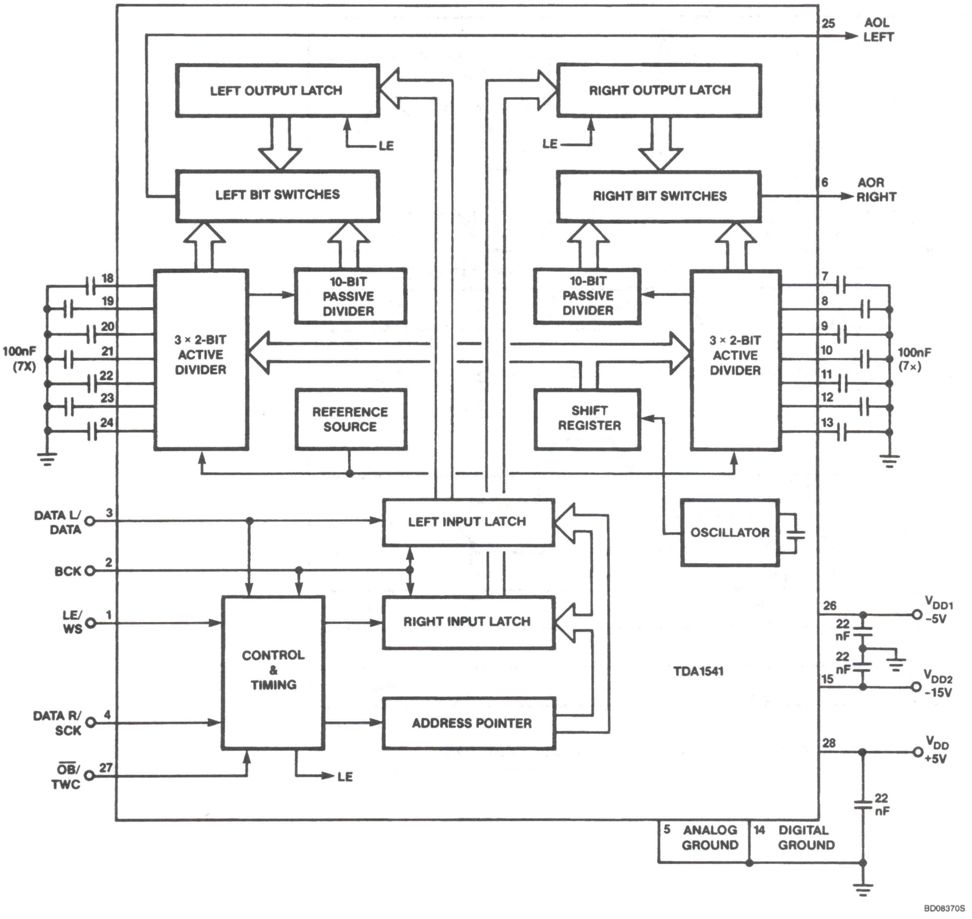

25 AOL LEFT
LEFT OUTPUT LATCH
RIGHT OUTPUT LATCH
LE
LE
LEFT BIT SWITCHES
RIGHT BIT SWITCHES
6 AOR RIGHT
10-BIT PASSIVE DIVIDER
10-BIT PASSIVE DIVIDER
3 × 2-BIT ACTIVE DIVIDER
3 × 2-BIT ACTIVE DIVIDER
18
19
20
21
22
23
24
100nF (7X)
7
8
9
10
11
12
13
100nF (7×)
REFERENCE SOURCE
SHIFT REGISTER
DATA L/ DATA 3
BCK 2
LE/ WS 1
DATA R/ SCK 4
OB/ TWC 27
LEFT INPUT LATCH
RIGHT INPUT LATCH
OSCILLATOR
CONTROL & TIMING
ADDRESS POINTER
LE
TDA1541
26
22 nF
22 nF
15
VDD1 −5V
VDD2 −15V
28
VDD +5V
22 nF
5 ANALOG GROUND
14 DIGITAL GROUND
BD08370S

Figure 1. Typical Application

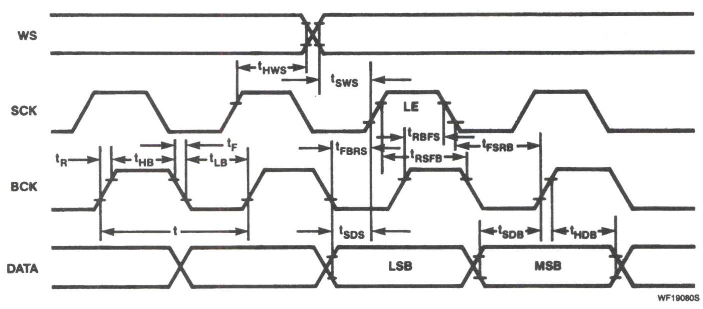

WS
SCK
BCK
DATA
t_{HWS}
t_{SWS}
LE
t_R
t_{HB}
t_F
t_{LB}
t_{FBRS}
t_{RBFS}
t_{RSFB}
t_{FSRB}
t
t_{SDS}
t_{SDB}
t_{HDB}
LSB
MSB
WF19080S

Figure 2. Format of Input Signals; Time Multiplexed at $f_{SCK} = f_{BCK}$ (I^2S Format)

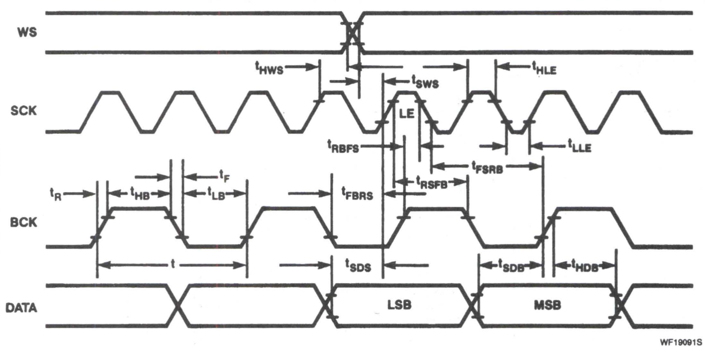

WS
SCK
BCK
DATA
t_{HWS}
t_{SWS}
t_{HLE}
LE
t_{RBFS}
t_{LLE}
t_{FSRB}
t_{RSFB}
t_R
t_{HB}
t_F
t_{LB}
t_{FBRS}
t
t_{SDS}
t_{SDB}
t_{HDB}
LSB
MSB
WF19091S

Figure 3. Format of Input Signals; Time Multiplexed at $f_{SCK} = 2 \times f_{BCK}$

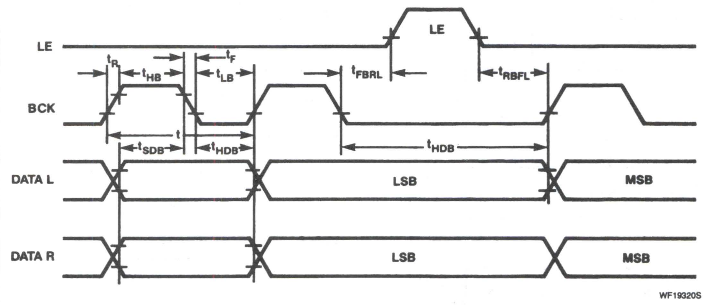

LE
BCK
DATA L
DATA R
LE
t_R
t_{HB}
t_F
t_{LB}
t_{FBRL}
t_{RBFL}
t
t_{SDB}
t_{HDB}
t_{HDB}
LSB
MSB
LSB
MSB
WF19320S

Figure 4. Format of Input Signals; Simultaneous Data

Signetics

Linear Products

TDA1721

8-Bit Multiplying DAC

Objective Specification

DESCRIPTION

The TDA1721 is an 8-bit multiplying DAC manufactured in the LOCMOS technology. Apart from the reference voltage, the device uses only one supply voltage, which may range from 5 up to 15V.

The digital bit inputs can be switched from CMOS to TTL compatibility over total supply voltage range by means of an extra pin ($TTL/\overline{CMOS}$), which may be connected to V_{DD} or V_{SS}.

These inputs are also provided with transparent latches, controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) signals, so the device can be used in microprocessor environments.

The reference inputs (Ref Voltage as well as Ref Common) may have any voltage between V_{SS} and V_{DD} −3V. A resistor (typical 35kΩ) is connected between these two terminals.

The binary input value is translated into an output voltage with a relative accuracy of ±½LSB. The output is internally buffered.

FEATURES

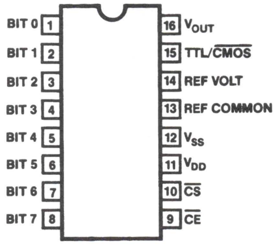
- **Single supply operation**
- **Variable output range**
- **½ LSB accuracy**
- **Fully monotonic**
- **Fast settling (3μs typ)**
- **Low power consumption (15mW at 10V)**

APPLICATIONS

- **Waveform generators**
- **Modems**
- **Analog meter drivers**
- **Tracking A-D converters**
- **Programmable power supplies**

PIN CONFIGURATION

N Package



TOP VIEW

CD12220S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38DIZ)	0 to +70°C	TDA1721N

DC AND AC ELECTRICAL CHARACTERISTICS $V_{DD} = 10V$, $V_{SS} = V_{RCOM} = 0V$, $V_{REF} = 5V$, $T_A = 25°C$, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution			19.5		mV
E_O	Offset error			5		mV
E_{FS}	Full-scale error			2		%
D_{NL}	Differential linearity			¼	½	LSB
	Monotonicity	Guaranteed for $T_A = -40°C$ to $+85°C$				
	Feedthrough	Input code 00000000 $V_{REF} = 6V_{P\text{-}P}$, 200kHz sine wave		0.01		LSB
t_S	Settling time to 1/2 LSB	5V step 10pF load		3		µs
d_V/d_T	Slew rate			4		V/µs
	Temp. coefficients:					
TC_{FS}	Full-scale error	ppm		15		FS/°C
TC_{2S}	Offset error	ppm		2		FS/°C
TC_{ONL}	Linearity	ppm		2		FS/°C
PSRR	Power supply rejection ratio			0.4		mV/V
C_L	Maximum load capacitance		TBD	TBD	TBD	pF
R_{REF}	Resistance between Ref Voltage and Ref Common			35		kΩ
	Output:					
	range[1]	Not loaded	0		7	V
$I_{OUT}+$	current source				3	mA
$I_{OUT}-$	sink	$0.5V < V_{OUT} < (V_{DD} - 3V)$			−1.2	mA
	Latching time			150		ns
V_{DD}	Supply voltage		4.75		15	V
I_{DD}	Supply current	$V_{DD} = 10V$ analog output not loaded		1.5		mA
	Reference voltage:					
V_{REF}	Ref Voltage		0		V_{DD} −3.0	V
V_{RCOM}	Ref Common		0		V_{DD} −3.0	V
	Digital input levels:					
V_{IL}	Input voltage low	TTL/$\overline{\text{CMOS}} \geq 4.0V$			0.8	V
		TTL/$\overline{\text{CMOS}} \leq 0.8V$			$0.3 \times V_{DD}$	V
V_{IH}	Input voltage high	TTL/$\overline{\text{CMOS}} \geq 4.0V$	2.0			V
		TTL/$\overline{\text{CMOS}} \geq 2.0V$	$0.7 \times V_{DD}$			V
V_{IL}	TTL/$\overline{\text{CMOS}}$				0.3 V_{DD}	
V_{IH}			0.7 V_{DD}			

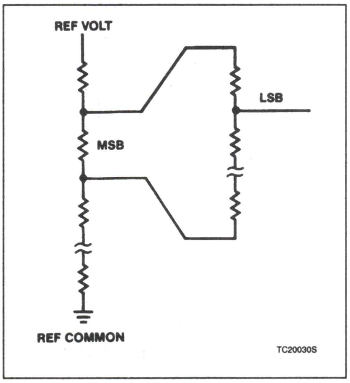
NOTE:

1. Provided V_{REF} and the input code are adapted to this output voltage.

PRINCIPLE OF OPERATION

The resistor connected to the two reference terminals can be divided into two parts:

1. Main string of 16 equal resistors connected to Ref Volt and Ref Common.
2. Second string of 16 equal resistors (resistance is not the same as the resistance of the 16 resistors in the main string), which a string is connected in parallel with one of the resistors of the main string.



The four MSBs determine the resistor to which the second resistor string is connected in parallel. The four LSBs determine the tap of the second resistor string.

The tap of the second resistor string is connected to an internal voltage follower. The output of this voltage follower is connected to V_{OUT}. The offset is trimmed with zener zapping to a value smaller then ± 7mV.

The digital inputs first pass a level convertor, which adapts the input switching levels to standard TTL or standard CMOS levels, depending on the position of the TTL/$\overline{CMOS}$ pin. The output of these convertors is connected to transparent latches, which are controlled by the pins Chip Select and Chip Enable.

DESCRIPTION OF INPUTS AND OUTPUTS

Inputs

A: Analog

A1 Ref Volt: This pin connected to one side of the main resistor string. The typical resistance of this string is 35kΩ.

A2 Ref Common: This pin is connected to the other side of the main resistor string.

The input voltage of both A1 and A2 may vary from V_{SS} to V_{DD} −3V.

B: Digital

B1 8 input bits (from LSB to MSB). These bits determine the output voltage via an ordinary binary code. The output voltage is obtained by choosing the place of the second resistor string in the main string, and the tap of the second resistor string. The inputs are TTL and CMOS compatible, controlled by the TTL/CMOS pin, over the total supply voltage range. Further on, the inputs are provided with latches, controlled by CS and CE pins, so the device can be used in microprocessor environments.

B2 TTL/$\overline{CMOS}$. This input (CMOS levels) controls the levels of all other digital input pins. If the pin is low the inputs are CMOS compatible; if the pin is high the inputs are TTL compatible.

B3 $\overline{CS}$ Chip Select pin

B4 $\overline{CE}$ Chip Enable pin; it controls the transparent latches at the inputs of the 8 bits. The following table gives the possible input combinations:

$\overline{CE}$	$\overline{CS}$	Latch condition
L	L	Transparent
_┌	L	"latching"
L	_┌	"
H	X	previous data latched
X	H	" " "

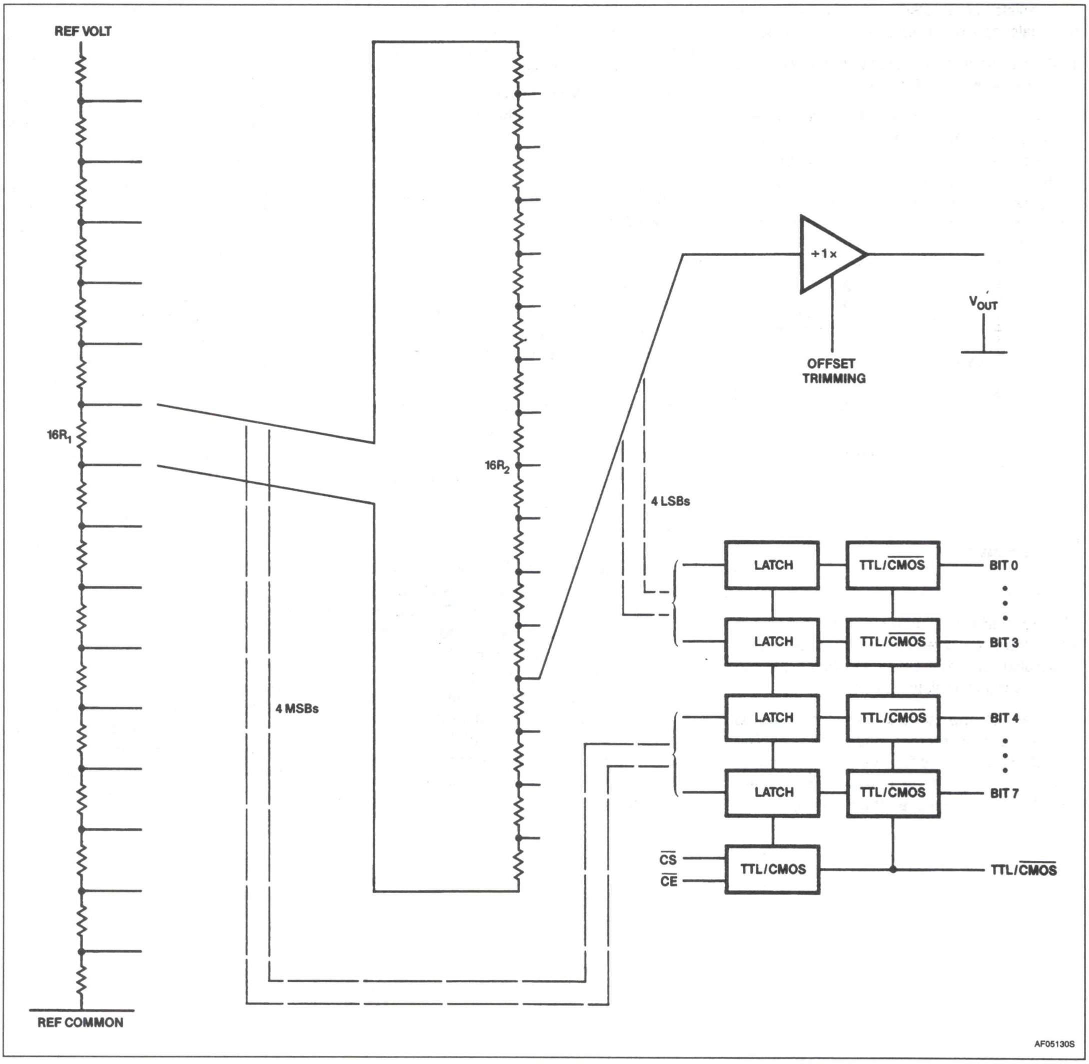
NOTE:
_┌ = Positive-going transition
X = State is immaterial
H = High state (the more positive voltage)
L = Low state (the less positive voltage)

Output

C: Analog

C1 Analog output: This is the buffered voltage output of the DAC. The output ranges from V_{SS} to V_{DD} −3V, when proper reference voltage and input code are applied. The output can be loaded with a maximum capacitance of 75pF. The slew rate of the internal buffer is typical 3V/μs.

BLOCK DIAGRAM


REF VOLT
16R$_1$
REF COMMON
16R$_2$
4 MSBs
4 LSBs
÷1×
OFFSET TRIMMING
V$_{OUT}$
LATCH
TTL/$\overline{CMOS}$
BIT 0
BIT 3
BIT 4
BIT 7
$\overline{CS}$
$\overline{CE}$
TTL/CMOS
TTL/$\overline{CMOS}$
AF05130S

Signetics

TDA5702

8-Bit Digital-to-Analog Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA5702 is an 8-bit digital-to-analog converter (DAC) designed for video and professional applications. The TDA5702 converts the 8-bit binary-coded digital words into an analog output signal at a sampling rate of 25MHz. The design of the TDA5702 has eliminated the need for an operational amplifier, buffer and deglitching circuit at the analog output.

FEATURES

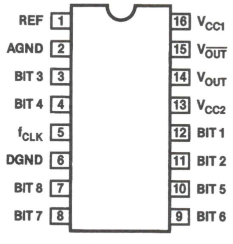
- **8-bit accuracy**
- **Internal input register**
- **TTL compatible digital signals**
- **Two voltage supply connections:**
  - **analog +5V**
  - **digital +5V**
- **Two complementary outputs (V_{OUT}, $\overline{V_{OUT}}$)**
- **No deglitching circuit required**
- **Low power consumption; typically 300mW**
- **16-lead plastic DIP**

APPLICATIONS

- **Video data conversion**
- **Color/black-and-white graphics**
- **CRT displays**
- **Waveform/test signal generation**

PIN CONFIGURATION

N Package



TOP VIEW

CD10840S

PIN NO.	SYMBOL	DESCRIPTION
1	REF	Current reference loop decoupling
2	AGND	Analog ground
3	Bit 3	
4	Bit 4	
5	f_{CLK}	25MHz clock input
6	DGND	Sigital ground
7	Bit 8	Most significant bit (MSB)
8	Bit 7	
9	Bit 6	
10	Bit 5	
11	Bit 2	
12	Bit 1	Least significant bit (LSB)
13	V_{CC2}	Digital supply voltage
14	V_{OUT}	Analog voltage output
15	$\overline{V_{OUT}}$	Complementary analog voltage output
16	V_{CC1}	Analog supply voltage

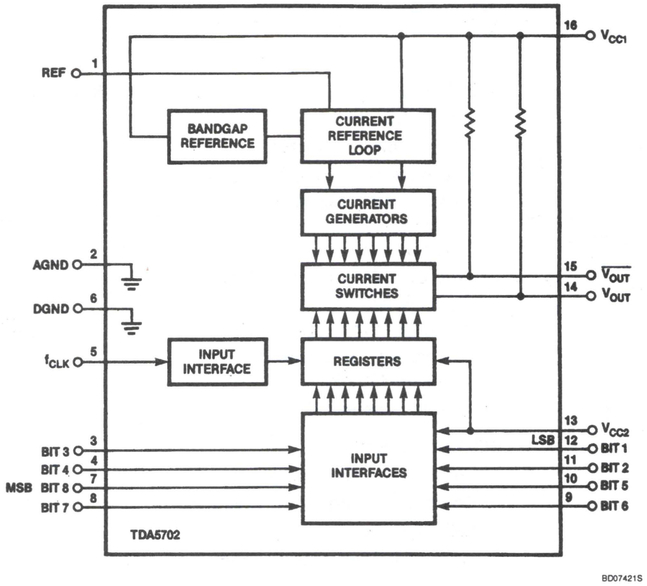
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	0 to +70°C	TDA5702N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
V_{CC2}	at Pin 13	8	V
V_{CC1}	at Pin 16	8	V
	Input voltage		
V_{IN}	at Pins 3, 4, 5, 7, 8, 9, 10, 11 and 12	8	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Junction temperature	+125	°C
T_A	Operating ambient temperature range	0 to +70	°C

BLOCK DIAGRAM


16
V_{CC1}
REF
1
BANDGAP REFERENCE
CURRENT REFERENCE LOOP
CURRENT GENERATORS
AGND
2
DGND
6
CURRENT SWITCHES
15
$\overline{V_{OUT}}$
14
V_{OUT}
f_{CLK}
5
INPUT INTERFACE
REGISTERS
13
V_{CC2}
LSB
12
BIT 1
11
BIT 2
10
BIT 5
9
BIT 6
BIT 3
3
BIT 4
4
MSB
BIT 8
7
BIT 7
8
INPUT INTERFACES
TDA5702
BD07421S

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V, $T_A = 0$ to +70°C, unless otherwise specified.

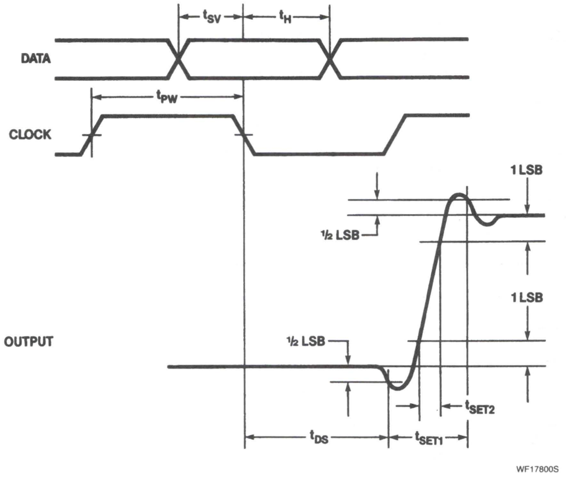
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{CC2}	Digital supply voltage	Pin 13	4.75	5.0	5.25	V
V_{CC1}	Analog supply voltage	Pin 16	4.75	5.0	5.25	V
I_{CC2}	Digital supply current	Pin 13	25	34	43	mA
I_{CC1}	Analog supply current	Pin 16	20	27	34	mA
Res	Resolution			8		bits
Digital input levels						
V_{IH}	Input voltage HIGH		2.2			V
V_{IL}	Input voltage LOW				0.8	V
I_{IH}	Input current HIGH				10	μA
I_{IL}	Input current LOW		−1.5			mA
I_{IL}	Clock input current LOW		−1.0			mA
Outputs[2]						
V_{FS}	Full-scale voltage	with respect to V_{CC}	1.43	1.6	1.75	V
V_{ZS}	Zero offset voltage	with respect to V_{CC}		10	25	mV
	Absolute linearity	V_{14}, V_{15}	−0.5		+0.5	LSB
	Differential linearity	V_{14}, V_{15}	−0.5		+0.5	LSB
R_{16-14}	Output resistance			75		Ω
C_1	External capacitance			100		nF

NOTES:
1. See Figure 3.
2. See Figure 2.
3. See Figure 1.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V, $T_A = 0$ to +70°C, unless otherwise specified.

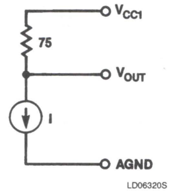
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Timing						
f_C	Maximum conversion rate		25			MHz
t_{DS}	Data turn-on delay[1]			10		ns
t_{SET1}	Transient settling time	½ LSB		30		ns
t_{SET2}	Transient settling time	1 LSB		20		ns
t_O	Transient output (glitch) energy				+50	LSB ns
t_{PW}	Pulse width[3]		10			ns
t_{SU}	Data setup time		4			ns
t_H	Data hold time		6			ns

NOTE:
1. See Figure 1.



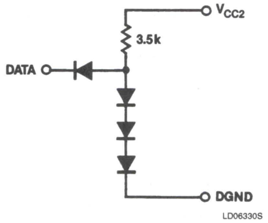
t_{SV}
t_H
DATA
t_{PW}
CLOCK
1 LSB
½ LSB
1 LSB
OUTPUT
½ LSB
t_{SET2}
t_{DS}
t_{SET1}
WF17800S

Figure 1. Timing Diagram



V_{CC1}
75
V_{OUT}
I
AGND
LD06320S

Figure 2. Equivalent Analog Output Circuit



V_{CC2}
3.5k
DATA
DGND
LD06330S

Figure 3. Equivalent Digital Input Circuit

Signetics

Linear Products

TDA8444

Octal 6-Bit DAC With I^{2}C Bus

Objective Specification

DESCRIPTION

The TDA8444 is a bipolar integrated circuit in a 16-pin dual in-line package made with an I^{2}L-compatible, 18V process. It features 8 programmable 6-bit DAC outputs, an I^{2}C bus slave receiver with 3 programmable address bits, and one input (V_{MAX}) to set the maximum output voltage.

Each DAC can be programmed separately by a 6-bit word to 64 steps, but V_{MAX} determines the maximum output voltage for all DACs. The resolution will be approximately $V_{MAX}/64$. At power-on, all DACs are set to their lowest value.

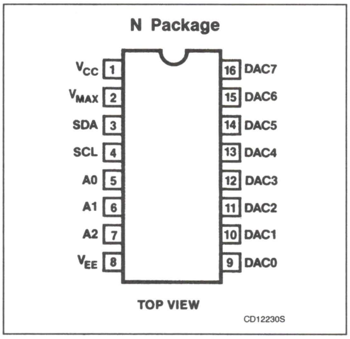
FEATURES

- **I^{2}C compatible**
- **Serial input**
- **Single supply operation**
- **Low power consumption (150mW typ.)**
- **8 DACs in single package**

APPLICATIONS

- **Television**
- **Radio**
- **Instrumentation**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38WE1)	0 to 70°C	TDA8444N

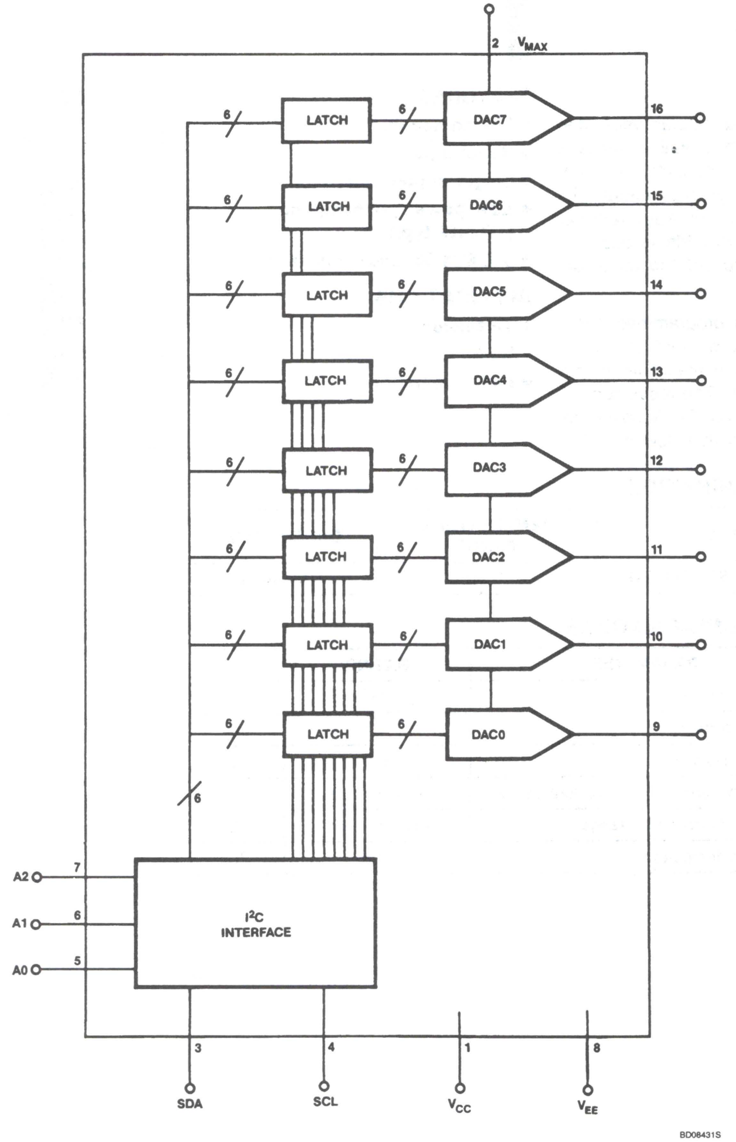
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
I_{CC}	Supply current	10	mA
P_{DMAX}	Power dissipation	500	mW
T_A	Operating ambient temperature range	−20 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	+125	°C

Octal 6-Bit DAC With I^{2}C Bus

TDA8444

BLOCK DIAGRAM


2
VMAX
LATCH
DAC7
DAC6
DAC5
DAC4
DAC3
DAC2
DAC1
DAC0
6
16
15
14
13
12
11
10
9
I²C
INTERFACE
A2
7
A1
6
A0
5
3
SDA
4
SCL
1
VCC
8
VEE
BD08431S

Octal 6-Bit DAC With I^{2}C Bus TDA8444

DC ELECTRICAL CHARACTERISTICS Voltages with respect to V_{EE}, $V_{CC} = 12V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	10.8	12	13.2	V
I_{CC}	Supply current (no loads, $V_{MAX} = V_{CC}$, all data = 00)	8	11	15	mA
P_D	Power dissipation		130		mW
	V_{MAX} input effective voltage range V_2 ($V_{CC} = 12V$)	1		10.5	V
	V_{MAX} input current $-I_2$			10	μA
	SDA, SCL input voltage V_3, V_4	0		5.5	V
	SDA, SCL input logic LOW level $V_{IL3,\ 4}$			1.5	V
	SDA, SCL input logic HIGH level $V_{IH3,\ 4}$	3.0			V
	SDA, SCL input current LOW (Pins 3, 4) HIGH (Pins 3, 4)			10 10	μA μA
	SDA output logic LOW level V_{OL}			0.4	V
	SDA output sink current I_3	3	5		mA
	Address input voltage	0		V_{CC}	V
	Address logic LOW level $V_{IL5,\ 6,\ 7}$			1.4	V
	Address logic HIGH level $V_{IH\ 5,\ 6,\ 7}$	2.1			V
$-I_{IL}$	Address input current LOW (Pins 5, 6, 7)		5	10	μA
	Address input current HIGH (Pins 5, 6, 7)			1	μA
	DAC output voltage $V_9 - V_{16}$	0.1		$V_{CC} - 0.5$	V
	DAC output low (data = 00, $I_L = 0$)	0.1	0.4	0.8	V
	DAC output high (data = 3F, $I_L = 0$, VCC = 12V)				
	$V_{MAX} = V_{CC}$	10.0	10.5	11.5	V
	$1 < V_{MAX} < 10.5V$	$V_{OMAX} = 0.95V_{MAX} + V_{OMIN} + 0.5V$			V
I_O	DAC output sink current $I_9 - I_{16}$	2	8	15	mA
$-I_O$	DAC output source current $-I_9 - -I_{16}$	2		6.0	mA
Z_O	DAC output impedance ($-2 \leqslant I_L \leqslant +2mA$) Z_O		2	70	Ω
V_{LSB}	Step value of 1LSB ($V_{MAX} = V_{CC}$)	100	160	250	mV
	Deviation from linearity			0.50	V
	Power reset range	1		4.6	V

FUNCTIONAL DESCRIPTION

I^{2}C Bus

The I^{2}C bus interface is a receive-only slave which accepts data according to the following formats:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	address byte		instruction byte		first data byte		

S = Start condition
P = Stop condition
A = Acknowledge
I3 – I0 = Instruction bits
SD – SA = Sub-address bits
A2,A1,A0 = Programmable address bits
X = Don't care
D5 – D0 = Data bits

Valid addresses (hexadecimal) are: 40, 42, 44, 46, 48, 4A, 4C, 4E

All other addresses cannot be acknowledged by the circuit. The actual address depends on the program address bits A2, A1, A0. In this way up to 8 circuits can be used on one I^{2}C bus.

Valid instructions (hexadecimal) are: 00 – 0F; F0 – FF.

The circuit will not respond to combinations of the 4 instruction bits I3 – I0 other than 0 or F. The difference between instructions 0 and F is only important when more than one data byte is sent within one transmission. Instruction 0 causes the data bytes to be written into the DAC latches with consecutive sub-addresses, starting with the sub-address given in the instruction byte (auto-increment of sub-address), while instruction F will cause a consecutive writing of the data bytes into the same DAC latch whose sub-address was given in the instruction byte. In case of only one data byte, the DAC latch with the sub-address equal to the sub-address in the instruction byte will receive the data.

Valid sub-addresses (hexadecimal) are: 0 – 7.

The sub-addresses correspond to DAC0 – DAC7.

The auto-increment (AI) function of instruction byte 0, however, works on all possible sub-addresses 0 – F in such a way that next to sub-address F, sub-address 0 will follow, and so on.

The data will be latched into the DAC latch on the positive-going edge of the acknowledge-related clock pulse.

The specification of the SCL and SDA I/O meets the I^{2}C bus specification. For protection against positive voltage pulses on Pins 3 and 4, zeners are connected between these pins and V_{EE}. This means that normal bus line voltage should not exceed 5.9V.

The address inputs A0, A1, A2 can be easily programmed by either a connection to V_{EE} (AX = 0) or V_{CC} (AX = 1). If the inputs are left floating, AX = 1 will result.

V_{MAX}

The V_{MAX} input (Pin 2) provides a means of compressing the DAC output voltage swing. The maximum DAC output voltage will be approximately equal to V_{MAX}, while the 6-bit resolution is maintained. This enables a higher voltage resolution for smaller output swings.

DACs

Each DAC consists of a 6-bit data latch, current switches, and an op amp. The current sources connected to the switches have values with weights $2^0 - 2^5$. The sum of the switched-on currents is converted by the op amp into a voltage between approximately 0.5V and 10.5V if $V_{MAX} = V_{CC}$.

The DAC outputs are short circuit protected against V_{CC} and V_{EE}.

Comparator Selector Guide

Comparator Selector Guide

DEVICE	COM-PLEXITY	TEMP RANGE*	MAX. INP. OFFSET VOLT (mV)	MAX. INPUT CURRENT BIAS (μA)	MAX. INPUT CURRENT OFFSET (μA)	SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP) (ns)	COMMON-MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE $V_{OL\ MAX}$ (V)	OUTPUT VOLTAGE $V_{OH\ MIN}$ (V)	OUTPUT STRUCTURE	VOLTAGE GAIN (TYP) (V/mV)	TTL FANOUT	MAX DIFF INPUT VOLTAGE (V)
LM111[1]	Single	M	3.0	0.10	0.01	±15	200	−14.5/+13	0.4		OC	200	5	±30
LM211	Single	I	3.0	0.10	0.01	to	200	−14.5/+13	0.4		OC	200	5	±30
LM311	Single	C	7.5	0.25	0.05	+5 and GND	200	−14.5/+13	0.4		OC	200	5	±30
NE527[2]	Single	C	10.0	4.00	1.0	±10	16	±5	0.5	2.7	TTL		5	±5
SE527	Single	M	6.00	4.00	1.00	+5	16	±5	0.5	2.5	TTL		5	±5
NE529[3]	Single	C	10.0	50.0	15.0	±10	12	±5	0.5	2.7	TTL		5	±5
SE529	Single	M	6.00	36.0	9.00	and +5	12	±5	0.5	2.5	TTL		5	±5
NE5105A	Single	A/C/M	0.25	1.2	0.02	±5	36	±3	0.4	2.4	TTL	26	10	±5
NE5105	Single	A/C/M	0.60	1.4	0.04	±5	36	±3	0.4	2.4	TTL	26	10	±5
LM119[3]	Dual	M	7.00	1.00	0.10	±15	80	±13	0.4		OC	40	2	±5
LM219	Dual	I	7.00	1.00	0.10	to	80	±13	0.4		OC	40	2	±5
LM319	Dual	C	10.0	1.20	0.30	+5 and GND	80	±13	0.4		OC	40	2	±5
LM193[3]/193A	Dual	M	9.00/4.0	0.30	0.10	±1 to ±18	1300	0 to V_S-2	0.7		OC	200	2	36
LM293/293A	Dual	I	9.00/4.0	0.40	0.15	or	1300	0 to V_S-2	0.7		OC	200	2	36
LM393/393A	Dual	C	9.00/4.0	0.40	0.15	+2 to +36 GND	1300	0 to V_S-2	0.7		OC	200	2	36
LM2903	Dual	I	15.0	0.50	0.20		1300	0 to V_S-2	0.7		OC	100	2	36
NE/SE521[4]	Dual	M/C	15/10.0	40.0	12.0	+5 −5 GND	8	±3	0.5	2.5/2.7	TTL		12	±6
NE/SE522	Dual	M/C	15/10.0	40.0	12.0	+5 −5 GND	10	±3	0.5		OC		12	±6
LM139[3]/139A	Quad	M	9.00/4.0	0.30	0.10		1300	0 to V_S-2	0.7		OC	200	2	36
LM239/239A	Quad	I	9.00/4.0	0.40	0.15	±1 to ±18 or	1300	0 to V_S-2	0.7		OC	200	2	36
LM339/339A	Quad	C	9.00/4.0	0.40	0.15	+2 to +36	1300	0 to V_S-2	0.7		OC	200	2	36
LM2901	Quad	I	15.0	0.50	0.20		1300	0 to V_S-2	0.7		OC	100	2	36
MC3302[3]	Quad	I	40.0	1.00	0.30	+2 to +28 GND	1300	0 to V_S-2	0.7		OC	100	2	36

NOTES:

1. With strobe, will work from single supply
2. Complementary output gates with individual strobes
3. Will operate from single or dual supplies
4. Ultra-high speed

*Temperature Range

I = Industrial −25°C to +85°C
C = Commercial 0°C to +70°C
M = Military −55°C to +125°C
A = Automotive −40°C to +85°C

Signetics

Symbols and Definitions for Comparators

Linear Products

Common-Mode Rejection Ratio (CMRR)

The ratio of the change in input common-mode voltage (over a specified input common-mode range) to the corresponding change in V_{OS} (see definition below). CMRR is expressed in dB where CMRR (dB) = $20\log(\Delta CMV/\Delta V_{OS})$.

Differential Input Resistance (R_{IN})

The small-signal resistance looking into either input terminal with the other input terminal connected to a specified voltage.

Input Bias Current (I_{BIAS})

The current into either input terminal with both inputs connected to a common specified voltage.

Input Common-Mode Voltage Range (CMVR)

The range of input common-mode voltage for which operation within the specifications is guaranteed.

Input Offset Current (I_{OS})

The difference between the two input bias currents with both inputs connected to a common specified voltage.

Input Offset Current Drift (TCI_{OS})

The ratio of the change in I_{OS} to the corresponding change in temperature as that temperature deviates from 25°C.

Input Offset Voltage (V_{OS})

The minimum potential difference required between the input terminals to force the output to a specified voltage.

Input Offset Voltage Drift (TCV_{OS})

The ratio of the change in V_{OS} to the corresponding change in temperature as that temperature deviates from 25°C.

Input to Output Propagation Delay (t_{PD})

The propagation delay measured from the time the differential input signal equals V_{OS} to the 50% point of the output transition with the comparator in the compare mode. The propagation delay is specified for a given initial input voltage ($-V_{IN}$) and overdrive (V_{OD}, see definition below) and can also be specified for both positive-(t_{PD+}) and negative-(t_{PD-}) going input signals.

Latch Disable Propagation Delay (t_{LPD})

The propagation delay measured between the 50% point of the latch-to-compare transition of the latch enable signal and the 50% point of the output transition. This propagation delay can be specified for both positive-(t_{lPD+}) and negative-(t_{lPD-}) going output transitions and is specified for a particular value of V_{OD} (see definition below).

Latch Hold Time (t_H)

The minimum time after the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output. Hold time is measured from the 50% transition point of the latch enable signal to the point at which the differential input signal equals V_{OS} and is specified for a particular value of V_{OD} (see definition below).

Latch Pulse Width (t_W)

The minimum time that the latch enable signal must be in the compare mode in order to acquire and subsequently hold an input signal change. Pulse width is measured between the 50% transition points of the latch enable pulse and is specified for a particular value of V_{OD} (see definition below).

Latch Setup Time (t_S)

The minimum time before the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output. Setup time is measured from the point at which the differential input voltage equals V_{OS} to the 50% transition point of the latch enable signal and is specified for a particular value of V_{OD} (see definition below).

Output High Current (I_{OH})

The current that can be sourced at the output terminal at a specified output voltage.

Output High Voltage (V_{OH})

The high output voltage at a specified output source current and differential input voltage.

Output Low Current (I_{OL})

The current that can be sunk at the output terminal at a specified output voltage.

Output Low Voltage (V_{OL})

The low output voltage at a specified output sink current and differential input voltage.

Overdrive (V_{OD})

The input overdrive (V_{OD}) is the applied differential input voltage (V_{IN}) in excess of the comparator input offset voltage (V_{OS}); i.e., $V_{OD} = V_{IN} - V_{OS}$. The dynamic response of a comparator depends on the input overdrive and, for this reason, such parameters as propagation delay and latch setup time, hold time, and pulse width are specified for a particular value of V_{OD}.

Power Supply Rejection Ratio (PSRR)

The ratio of the change in power supply voltage (over a specified power supply voltage range) to the corresponding change in V_{OS}. PSRR is expressed in dB where PSRR(dB) = $20\log(\Delta PSV/\Delta V_{OS})$.

Voltage Gain (A_V)

The ratio of the change in output voltage (over a specified output voltage range) to the change in differential input voltage.

Signetics

LM111/211/311
Voltage Comparator

Product Specification

Linear Products

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

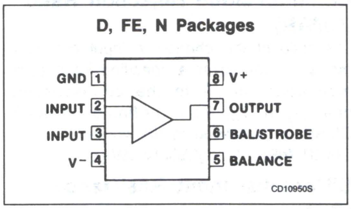
Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply, or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire-ORed.

Although slower than the μA710 (200ns response time vs 40ns), the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

FEATURES

- **Operates from single 5V supply**
- **Maximum input bias current: 150nA (LM311 — 250nA)**
- **Maximum offset current: 20nA (LM311 — 50nA)**
- **Differential input voltage range: ±30V**
- **Power consumption: 135mW at ±15V**
- **High sensitivity — 200V/mV**

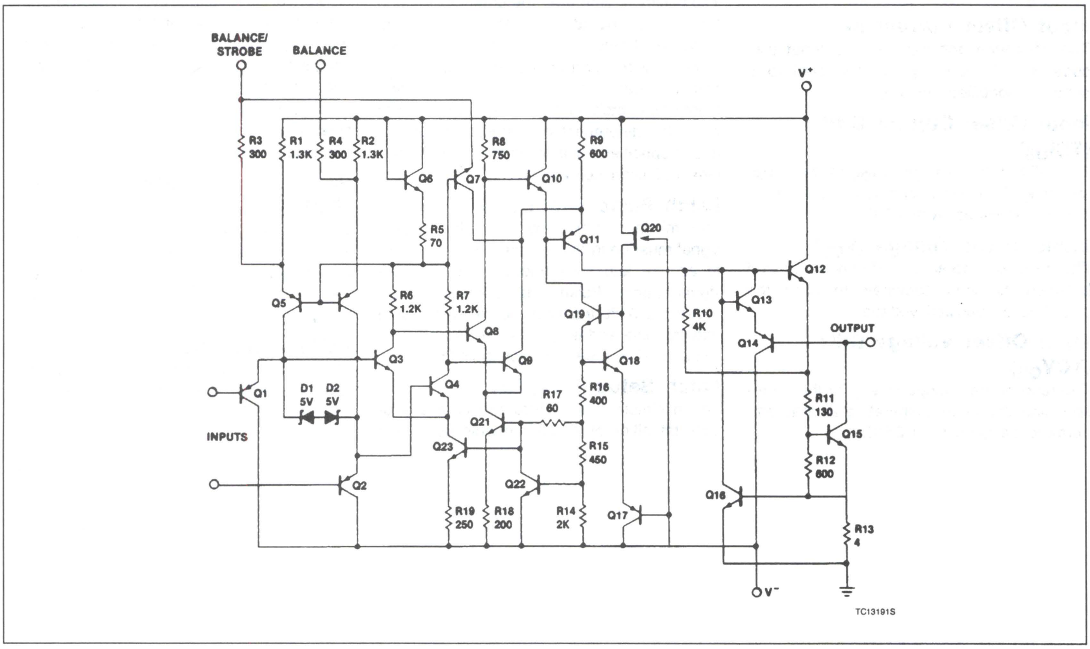
PIN CONFIGURATION


D, FE, N Packages
GND 1
INPUT 2
INPUT 3
V− 4
8 V+
7 OUTPUT
6 BAL/STROBE
5 BALANCE
CD10950S

APPLICATIONS

- **Zero crossing detector**
- **Precision squarer**
- **Positive/negative peak detector**
- **Low voltage adjustable reference supply**
- **Switching power amplifier**

EQUIVALENT SCHEMATIC


BALANCE/ STROBE
BALANCE
V+
R3 300
R1 1.3K
R4 300
R2 1.3K
R8 750
R9 600
Q6
Q7
Q10
R5 70
Q11
Q20
Q12
Q5
R6 1.2K
R7 1.2K
Q19
R10 4K
Q13
Q8
Q14
OUTPUT
Q3
Q9
Q18
Q1
D1 5V
D2 5V
Q4
R17 60
R16 400
R11 130
INPUTS
Q21
Q23
R15 450
Q15
R12 600
Q2
Q22
Q16
R19 250
R18 200
R14 2K
Q17
R13 4
V−
TC13191S

Voltage Comparator LM111/211/311

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	0 to +70°C	LM111FE
8-Pin Cerdip	0 to +70°C	LM211FE
8-Pin Plastic DIP	0 to +70°C	LM211N
8-Pin Plastic SO	0 to +70°C	LM311D
8-Pin Cerdip	0 to +70°C	LM311FE
8-Pin Plastic DIP	0 to +70°C	LM311N
8-Pin Plastic SO	0 to +70°C	LM211D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage: LM111/LM211 LM311	 50 40	 V V
	Ground to negative supply voltage	30	V
	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 780 1160 780	 mW mW mW
I	Output short-circuit duration	10	sec
T_A	Operating ambient temperature range LM111 LM211 LM311	 −55 to +125 −25 to +85 0 to +70	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2m/W°C

Voltage Comparator LM111/211/311

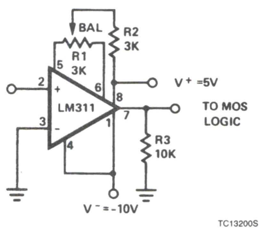
DC ELECTRICAL CHARACTERISTICS [1, 2, 3]

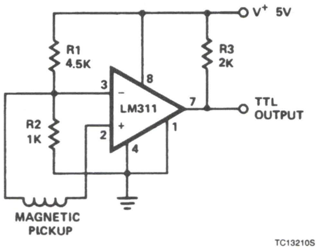
SYMBOL	PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[3]	$T_A = 25°C$, $R_S \leqslant 50k\Omega$		0.7	3.0		2.0	7.5	mV
I_{OS}	Input offset current[3]	$T_A = 25°C$		4.0	10		6.0	50	nA
I_{BIAS}	Input bias current	$T_A = 25°C$		60	100		100	250	nA
A_V	Voltage gain	$T_A = 25°C$		200			200		V/mV
	Response time[4]	$T_A = 25°C$		200			200		ns
	Saturation voltage	$V_{IN} \leqslant -5mV$, $I_{OUT} = 50mA$ $T_A = 25°C$		0.75	1.5		0.75	1.5	V
	Strobe on current	$T_A = 25°C$		3.0			3.0		mA
	Output leakage current	$V_{IN} \geqslant 5mV$, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3mA$		0.2	10		0.2	50	nA
V_{OS}	Input offset voltage[3]	$R_S \leqslant 50k\Omega$			4.0			10	mV
I_{OS}	Input offset current[3]				20			70	nA
I_{BIAS}	Input bias current				150			300	nA
V_{IN}	Input voltage range	V = ±15V (Pin 7 may go to 5V)	−14.5	13.8 −14.7	13.0	−14.5	13.8 −14.7	13.0	V
	Saturation voltage	V=p0 ≥ 4.5V, V− = 0							
V_{OL}		$V_{IN} \leqslant -6mV$, $I_{SINK} \leqslant 8mA$		0.23	0.4		0.23	0.4	V
I_{OH}	Output leakage current	$V_{IN} \geqslant 5mV$, $V_{OUT} = 35V$		0.1	0.5				µA
I_{SC}	Positive supply current	$T_A = 25°C$		5.1	6.0		5.1	7.5	mA
	Negative supply voltage	$T_A = 25°C$		4.1	5.0		4.1	5.0	mA

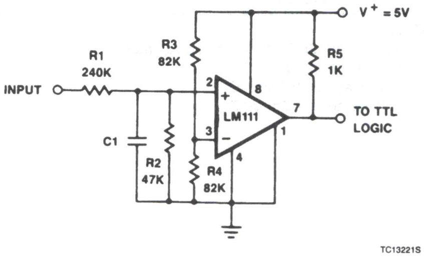
NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < 70°C$ unless otherwsie specified. With the LM211, however, all temperature specifications are limited to $-25°C \leqslant T_A \leqslant 85°C$ and for the LM111 is limited to $-55°C < T_A < 125°C$. The offset voltage, offset current, and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified is for a 100mV input step with 5mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3mA to 5mA.

TYPICAL APPLICATIONS







* Values shown are for a 0 to 30V logic swing and a 15V threshold.
† May be added to control speed and reduce susceptibility to noise spikes.

Zero-Crossing Detector Driving MOS Logic

Detector for Magnetic Transducer

TTL Interface With High Level Logic

LM119/219/319
Dual Voltage Comparator

Product Specification

DESCRIPTION

The LM119 series are precision high-speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μA710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL, and TTL as well as capable of driving lamps and relays at currents up to 25mA.

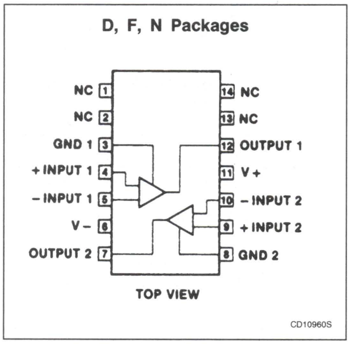
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high-speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μA711.

The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

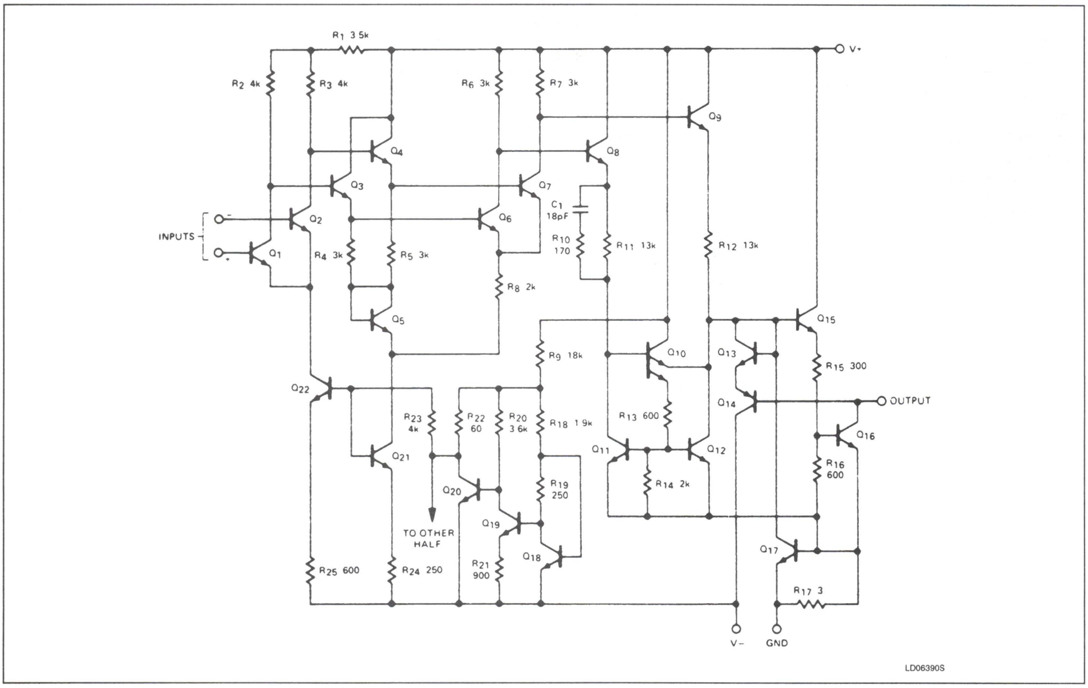
FEATURES

- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Minimum fanout of 3 (each side)**
- **Maximum input current of 1μA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common-mode slew rate**
- **MIL-STD-883A, B, C available**

PIN CONFIGURATION


D, F, N Packages
NC 1
NC 2
GND 1 3
+INPUT 1 4
−INPUT 1 5
V− 6
OUTPUT 2 7
14 NC
13 NC
12 OUTPUT 1
11 V+
10 −INPUT 2
9 +INPUT 2
8 GND 2
TOP VIEW
CD10960S

EQUIVALENT SCHEMATIC


R1 3.5k
V+
R2 4k
R3 4k
R6 3k
R7 3k
Q9
Q4
Q8
Q3
Q7
C1 18pF
Q2
Q6
INPUTS
Q1
R4 3k
R5 3k
R10 170
R11 13k
R12 13k
R8 2k
Q5
Q15
R9 18k
Q10
Q13
R15 300
Q22
Q14
OUTPUT
R23 4k
R22 60
R20 3.6k
R18 1.9k
R13 600
Q16
Q21
Q11
Q12
R16 600
R14 2k
Q20
R19 250
Q19
TO OTHER HALF
Q18
Q17
R21 900
R25 600
R24 250
R17 3
V−
GND
LD06390S

Dual Voltage Comparator LM119/219/319

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	−55°C to +125°C	LM119F
14-Pin Cerdip	−25°C to +85°C	LM219F
14-Pin Plastic SO	0 to +70°C	LM319D
14-Pin Cerdip	0 to +70°C	LM319F
14-Pin Plastic DIP	0 to +70°C	LM319N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage	36	V
	Ground to negative supply voltage	25	V
	Ground to positive supply voltage	18	V
	Differential input voltage	±5	V
V_{IN}	Input voltage[1]	±15	V
	Maximum power dissipation, $T_A = 25°C$ (still-air)[2]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
	Output short-circuit duration	10	s
T_A	Operating temperature range		
	LM119	−55 to +125	°C
	LM219	−25 to +85	°C
	LM319	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

Dual Voltage Comparator LM119/219/319

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, for LM119, $-55°C \leq T_A \leq 125°C$
LM219, $-25°C \leq T_A \leq 85°C$
LM319, $0°C \leq T_A \leq 70°C$
unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM119/219			LM319			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[1, 2]	$R_S \leq 5k\Omega$, $T_A = 25°C$		0.7	4.0		2.0	8.0	mV
		Over temp.			7			10	mV
I_{OS}	Input offset current[1, 2]	$T_A = 25°C$		30	75		80	200	nA
		Over temp.			100			300	nA
I_B	Input bias current[1]	$T_A = 25°C$		150	500		250	1000	nA
		Over temp.			1000			1200	nA
A_V	Voltage gain	$T_A = 25°C$	10	40		8	40		V/mV
V_{OL}	Saturation voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 25mA$, $T_A = 25°C$		0.75	1.5				V
		$V_{IN} \leq -10mV$, $I_{OUT} = 25mA$, $T_A = 25°C$					0.75	1.5	V
		$V+ \geq 4.5V$, $V- = 0$							
		$V_{IN} \leq -6mV$, $I_{OUT} = 3.2mA$							
		$T_A \geq 0°C$		0.23	0.4				V
		$T_A \leq 0°C$			0.6				
		$V_{IN} \leq -10mV$, $I_{OUT} = 3.2mA$					0.3	0.4	V
I_{OH}	Output leakage current	$V- = 0V$, $V_{IN} \geq 5mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$		0.2	2				μA
		Over temp.		1	10				μA
		$V- = 0V$, $V_{IN} \geq 10mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$					0.2	10	μA
V_{IN}	Input voltage range	$V_S = \pm 15V$		±13			±13		V
		$V+ = 5V$, $V- = 0V$	1		3	1		3	V
V_{ID}	Differential input voltage				±5			±5	V
I+	Positive supply current	$V+ = 5V$, $V- = 0V$, $T_A = 25°C$		4.3			4.3		mA
I+	Positive supply current	$V_S = \pm 15V$, $T_A = 25°C$		8.0	11.5		8.0	12.5	mA
I–	Negative supply current	$V_S = \pm 15V$, $T_A = 25°C$		3.0	4.5		3.0	5.0	mA

NOTES:

1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of $V_S = \pm 15V$ down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1V of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

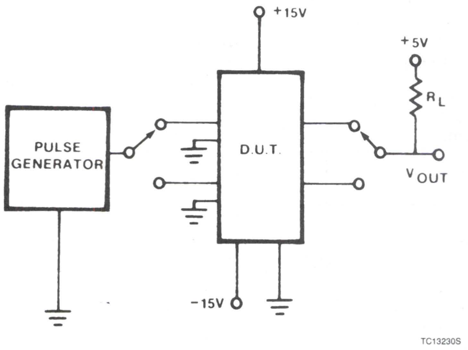
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Response time[1]	$V_S = \pm 15V$, $T_A = 25°C$ $R_L = 500\Omega$ (see test figure)		80		ns

NOTE:

1. The response time specified is for a 100mV step with 5mV overdrive.

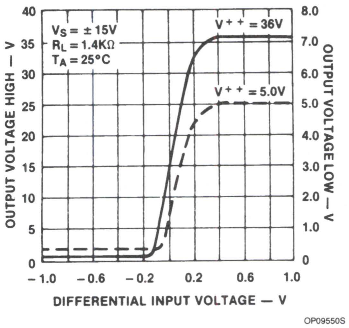
TEST CIRCUIT


+15V
+5V
RL
PULSE GENERATOR
D.U.T.
VOUT
−15V
TC13230S

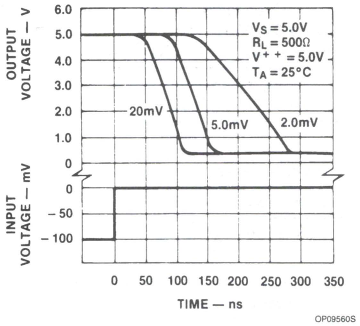
Response Time Measurement

TYPICAL PERFORMANCE CHARACTERISTICS

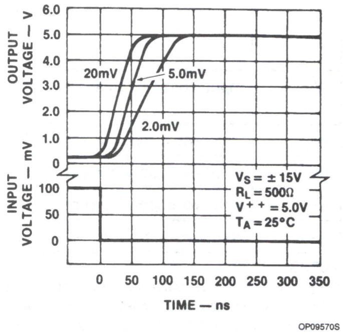
Transfer Function



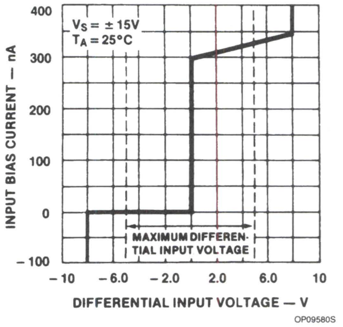
Response Time for Various Input Overdrives



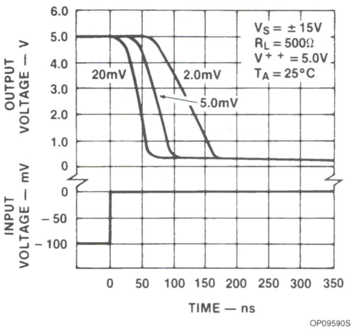
Response Time for Various Input Overdrives



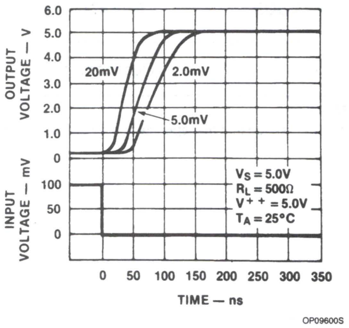
Input Characteristics



Response Time for Various Input Overdrives

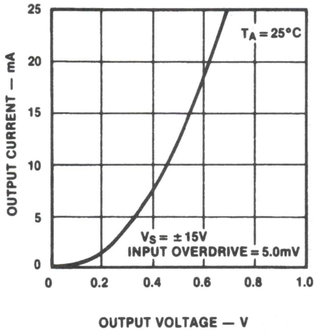


Response Time for Various Input Overdrives



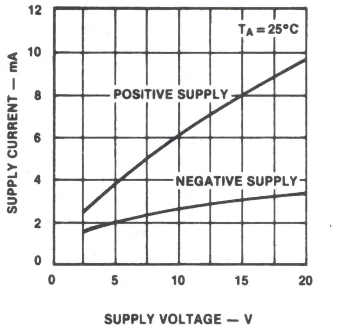
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Output Saturation Voltage



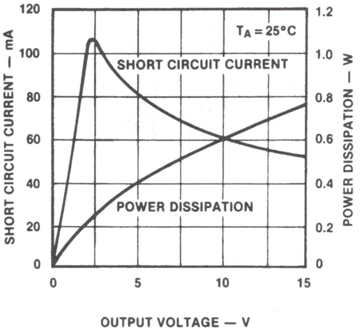
OP09610S

Supply Current



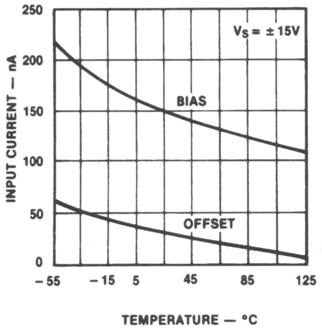
OP09620S

Output Limiting Characteristics



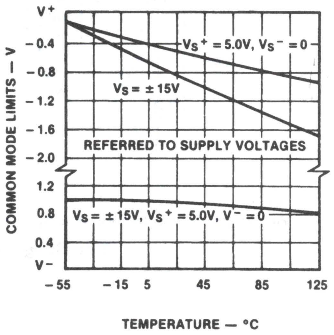
OP09630S

Input Currents (LM119/219)



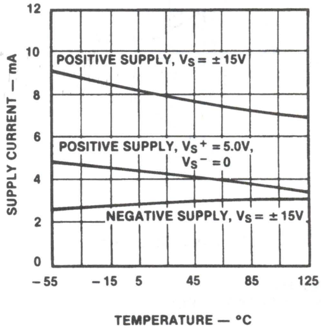
OP09640S

Common-Mode Limits (LM119/219)



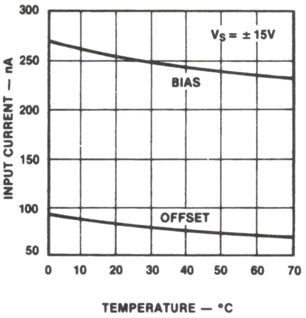
OP09650S

Supply Current (LM119/219)



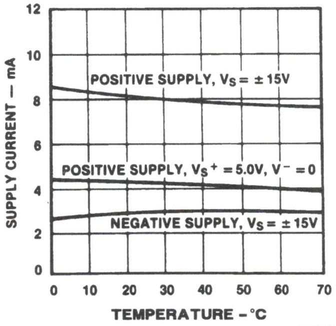
OP09660S

Input Currents (LM319)



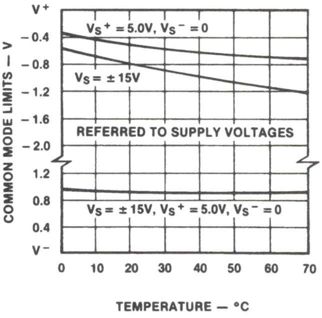
OP09670S

Supply Currents (LM319)



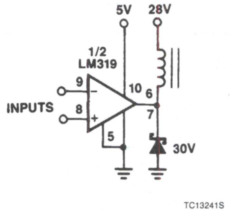
OP09681S

Common-Mode Limits (LM319)

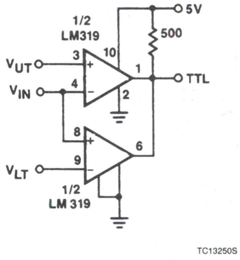


OP09690S

TYPICAL APPLICATIONS

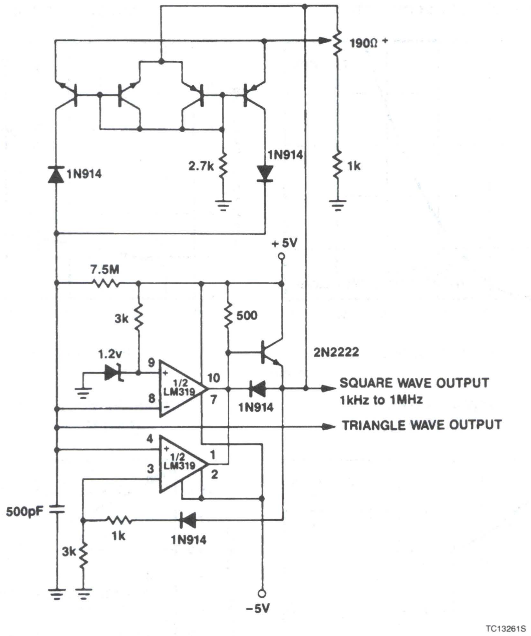

5V
28V
1/2
LM319
9
8
INPUTS
10
6
7
5
30V
TC13241S

Relay Driver


1/2
LM319
5V
500
V_{UT}
V_{IN}
3
4
10
1
2
TTL
8
9
6
V_{LT}
1/2
LM 319
TC13250S

Window Detector

NOTES:
$V_{OUT} = 5V$ for $V_{LT} < V_{IN} < V_{UT}$
$V_{OUT} = 0V$ for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$


190Ω
1N914
2.7k
1N914
1k
+5V
7.5M
3k
500
2N2222
1.2v
9
8
1/2
LM319
10
7
1N914
SQUARE WAVE OUTPUT
1kHz to 1MHz
TRIANGLE WAVE OUTPUT
4
3
1/2
LM319
1
2
500pF
1k
1N914
3k
−5V
TC13261S

NOTE:
Frequency adjust must be buffered for $R_L \leqslant 10\Omega$

Wide Range Variable Oscillator

Signetics

LM139A/239A/339A/LM139/239/339/LM2901/MC3302

Quad Voltage Comparator

Linear Products

Product Specification

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though they are operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

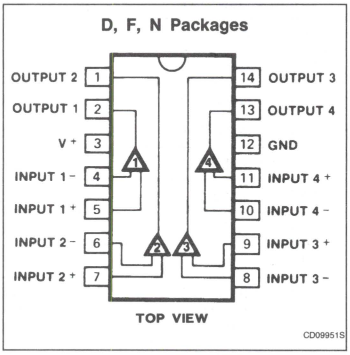
FEATURES

- **Wide single supply voltage range $2.0V_{DC}$ to $36V_{DC}$ or dual supplies $\pm 1.0V_{DC}$ to $\pm 18V_{DC}$**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at $5.0V_{DC}$)**
- **Low input biasing current 25nA**
- **Low input offset current ±5nA and offset voltage**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

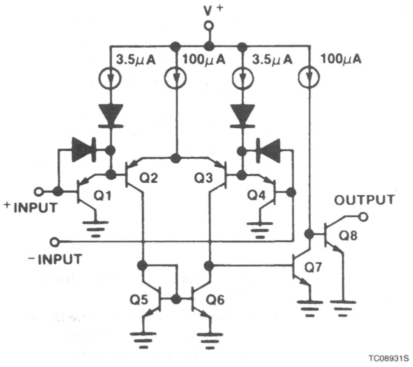
APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION


D, F, N Packages
OUTPUT 2 1
OUTPUT 1 2
V+ 3
INPUT 1− 4
INPUT 1+ 5
INPUT 2− 6
INPUT 2+ 7
14 OUTPUT 3
13 OUTPUT 4
12 GND
11 INPUT 4+
10 INPUT 4−
9 INPUT 3+
8 INPUT 3−
1
2
3
4
TOP VIEW
CD09951S

EQUIVALENT CIRCUIT


V+
3.5µA
100µA
3.5µA
100µA
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
+INPUT
−INPUT
OUTPUT
TC08931S

(1 Comparator Only)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to +125°C	LM139AF
14-Pin Cerdip	0 to +125°C	LM139F
14-Pin Plastic DIP	-25°C to +85°C	LM239AN
14-Pin Plastic DIP	-25°C to +85°C	LM239N
14-Pin Cerdip	-25°C to +85°C	LM239F
14-Pin Cerdip	-40°C to +85°C	LM2901F
14-Pin Plastic DIP	-40°C to +85°C	LM2901N
14-Pin Plastic DIP	0 to +70°C	LM339AN
14-Pin Plastic SO	0 to +70°C	LM339D
14-Pin Plastic DIP	0 to +70°C	LM339N
14-Pin Cerdip	0 to +70°C	LM339AF
14-Pin Cerdip	0 to +70°C	LM339F
14-Pin Plastic SO	-40°C to +85°C	MC3302D
14-Pin Cerdip	-40°C to +85°C	MC3302F
14-Pin Plastic DIP	-40°C to +85°C	MC3302N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to +36	V_{DC}
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 1190 1420 1040	 mW mW mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3V_{DC}$)[3]	50	mA
T_A	Operating temperature range LM139A LM239A LM339A LM2901/MC3302	 -55 to +125 -25 to +85 0 to +70 -40 to +85	 °C °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F Package at 9.5mW/°C
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is aproximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, LM139A/LM139: $-55°C \leqslant T_A \leqslant 125°C$, unless otherwise specified.
LM239: $-25°C \leqslant T_A \leqslant 85°C$, unless otherwise specified.
LM339: $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified.

$V+ = 5V_{DC}$, LM339A: $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified.
LM239A: $-25°C \leqslant T_A \leqslant 85°C$, unless otherwise specified.
LM2901/LM3302: $-40°C \leqslant T_A \leqslant 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM139A			LM239A/339A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$T_A = 25°C$ Over temp.		±1.0	±2.0 4.0		±1.0	±2.0	mV
V_{CM}	Input common-mode voltage range[6]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN}s \geqslant 0V_{DC}$ (or V− if need)			V+			V+	V
I_{BIAS}	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leqslant 1.5V_{DC}$, $T_A = 25°C$ $V_O = 800mV$, over temp.	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geqslant 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, over temp.		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	$V+ = 28V$, $R_L = \infty$ on comparators, $T_A = 25°C$ $V+ = 30V$		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	$R_L \geqslant 15k\Omega$, $V+ = 15V_{DC}$	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leqslant 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
t_R	Response time[8]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

See notes on page 6.

DC AND AC ELECTRICAL CHARACTERISTICS

V+ = $5V_{DC}$, LM139A/LM139: −55°C ≤ T_A ≤ 125°C, unless otherwise specified.
LM239: −25°C ≤ T_A ≤ 85°C, unless otherwise specified.
LM339: 0°C ≤ T_A ≤ 70°C unless otherwise specified.

V+ = $5V_{DC}$, LM339A: 0°C ≤ T_A ≤ 70°C, unless otherwise specified
LM239A: −25°C ≤ T_A ≤ 85°C, unless otherwise specified.
LM2901/LM3302: −40°C ≤ T_A ≤ 85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	T_A = 25°C Over temp.		±2.0	±5.0 9.0		±2.0	±5.0 9.0	mV
V_{CM}	Input common-mode voltage range[6]	T_A = 25°C Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN}s \geq 0V_{DC}$ (or V− if need)			V+			V+	V
I_{BIAS}	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5V_{DC}$, T_A = 25°C V_O = 800mV, over temp.	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, T_A = 25°C $V_O = 30V_{DC}$, over temp.		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	V+ = 28V, $R_L = \infty$ on comparators, T_A = 25°C V+ = 30V		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, V+ = $15V_{DC}$	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ T_A = 25°C Over temp.		250	400 700		250	400 700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, T_A = 25°C		300			300		ns
t_R	Response time[8]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, T_A = 25°C		1.3			1.3		μs

See notes on page 6.

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, LM139A/LM139: $-55°C \leqslant T_A \leqslant 125°C$, unless otherwise specified.
LM239: $-25°C \leqslant T_A \leqslant 85°C$, unless otherwise specified.
LM339: $0°C \leqslant T_A \leqslant 70°C$ unless otherwise specified.

$V+ = 5V_{DC}$, LM339A: $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified
LM239A: $-25°C \leqslant T_A \leqslant 85°C$, unless otherwise specified.
LM2901/LM3302: $-40°C \leqslant T_A \leqslant 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$T_A = 25°C$		±2.0	±7.0		±3.0	±2.0	mV
		Over temp.		±9	±15			±40	
V_{CM}	Input common-mode voltage range[6]	$T_A = 25°C$	0		V+−1.5	0		V+−1.5	V
		Over temp.	0		V+−2.0	0		V+−2.0	
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN}s \geqslant 0V_{DC}$ (or V− if need)			V+			V+	V
I_{BIAS}	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$		25	250		25	500	
		Over temp.		200	500			1000	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$		±5	±50		±5	±100	nA
		Over temp.		±50	±200			±300	nA
I_{OL}	Output sink current	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leqslant 1.5V_{DC}$, $T_A = 25°C$	6.0	16			6		mA
		$V_O = 800mV$, over temp.				2.0			
I_{OH}	Output leakage current	$V_{IN(+)} \geqslant 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$		0.1			0.1		nA
		$V_O = 30V_{DC}$, over temp.			1.0			1.0	µA
I_{CC}	Supply current	$V+ = 28V$, $R_L = \infty$ on comparators,					.8	1.8	
		$T_A = 25°C$		0.8	2.0				mA
		$V+ = 30V$		1.0	2.5				
A_V	Voltage gain	$R_L \geqslant 15k\Omega$, $V+ = 15V_{DC}$	25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leqslant 4mA$ $T_A = 25°C$			400		150	400	mV
		Over temp.		400	700			700	
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
t_R	Response time[8]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		µs

See notes on following page.

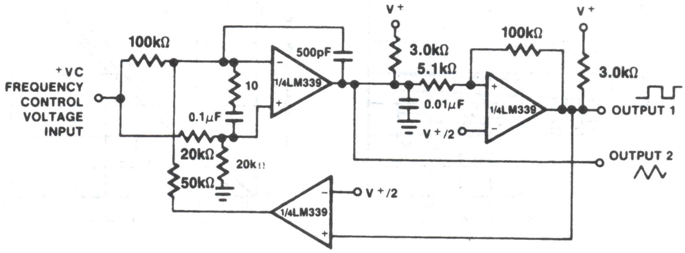
Quad Voltage Comparator

LM139A/239A/339A/LM139/239/339/ LM2901/MC3302

NOTES:

1. For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a 150°C maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leqslant 100mW$), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.
4. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$ below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$; and over the full input common-mode range ($0V_{DC}$ to $V+ - 1.5V_{DC}$).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ – 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see typical performance characteristics section).

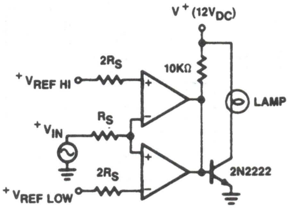
TYPICAL APPLICATIONS


+VC FREQUENCY CONTROL VOLTAGE INPUT
100kΩ
10
0.1µF
20kΩ
20kΩ
50kΩ
500pF
1/4LM339
V+
3.0kΩ
5.1kΩ
0.01µF
V+/2
100kΩ
1/4LM339
V+
3.0kΩ
OUTPUT 1
OUTPUT 2
1/4LM339
V+/2

TC08940S

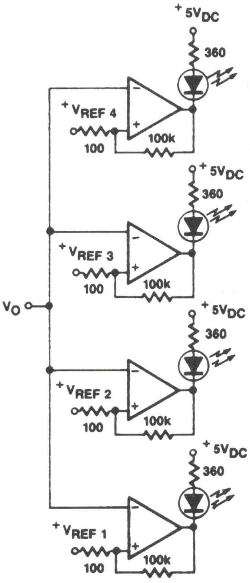
NOTES:
$V+ = +30V_{DC}$
$+250m\ V_{DC} \leqslant V_C + 50V_{DC}$
$700Hz \leqslant f_O \leqslant 100kHz$

Two-Decade High-Frequency VCO


V+ (12VDC)
2RS
10KΩ
+VREF HI
LAMP
RS
+VIN
2RS
2N2222
+VREF LOW

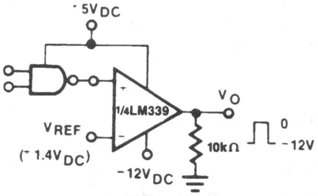
TC13290S

Limit Comparator


+5VDC
360
+VREF 4
100
100k
+5VDC
360
+VREF 3
100
100k
VO
+5VDC
360
+VREF 2
100
100k
+5VDC
360
+VREF 1
100
100k

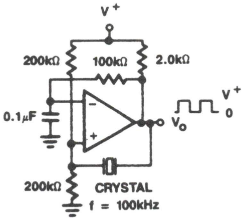
LD06401S

Visible Voltage Indicator


+5VDC
1/4LM339
VO
VREF
(+1.4VDC)
-12VDC
10kΩ
0
-12V

TC08960S

TTL-to-MOS Logic Converter

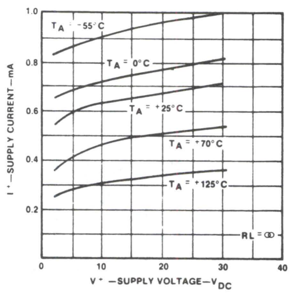

V+
200kΩ
100kΩ
2.0kΩ
0.1µF
V+
0
VO
200kΩ
CRYSTAL
f = 100kHz

TC13310S

Crystal-Controlled Oscillator

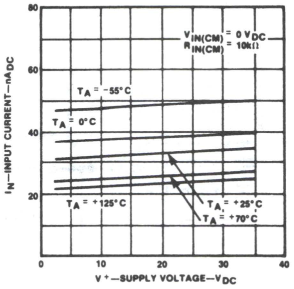
NOTE:
Inputs of unused comparators should be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS



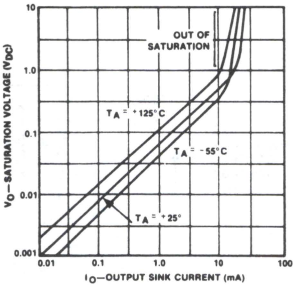
Supply Current

OP05570S



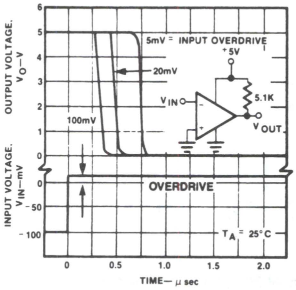
Input Current

OP05580S



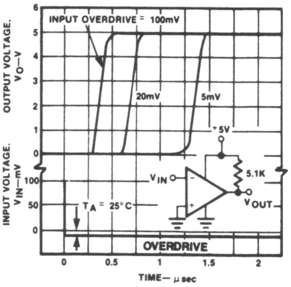
Output Saturation Voltage

OP05590S



Response Time for Various Input Overdrives — Negative Transition

OP05600S



Response Time for Various Input Overdrives — Positive Transition

OP05610S

Signetics

LM193/A/293/A/393/A/2903

Low Power Dual Voltage Comparator

Linear Products

Product Specification

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

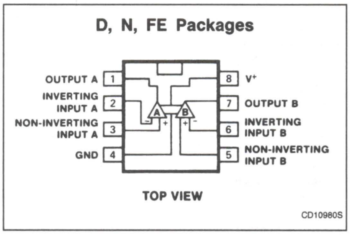
FEATURES

- **Wide single supply voltage range $2.0V_{DC}$ to $36V_{DC}$ or dual supplies $\pm 1.0V_{DC}$, to $\pm 18V_{DC}$**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at $5.0V_{DC}$)**
- **Low input biasing current 25nA**
- **Low input offset current ±5nA and offset voltage ±2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

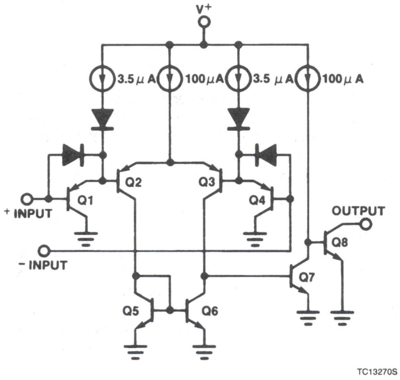
APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION


D, N, FE Packages
OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
GND 4
8 V+
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B
TOP VIEW
CD10980S

EQUIVALENT CIRCUIT


V+
3.5μA
100μA
3.5 μA
100μA
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
+ INPUT
− INPUT
OUTPUT
TC13270S

(One Comparator Only)

Low Power Dual Voltage Comparator LM193/A/293/A/393/A/2903

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	−55°C to +125°C	LM193AF
8-Pin Cerdip	−55°C to +125°C	LM193FE
8-Pin Cerdip	−25°C to +85°C	LM293AFE
8-Pin Cerdip	−25°C to +85°C	LM293FE
8-Pin Plastic DIP	−25°C to +85°C	LM293N
8-Pin Plastic DIP	−25°C to +85°C	LM293AN
8-Pin Cerdip	0 to +70°C	LM393AFE
8-Pin Cerdip	0 to +70°C	LM393FE
8-Pin Plastic SO	0 to +70°C	LM393D
8-Pin Plastic DIP	0 to +70°C	LM393N
8-Pin Plastic DIP	0 to +70°C	LM393AN
8-Pin Plastic DIP	−40°C to +85°C	LM2903N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	−0.3 to +36	V_{DC}
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[4]		
	F package	780	mW
	N package	1160	mW
	D package	780	mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3V_{DC}$)[3]	50	mA
T_A	Operating temperature range		
	LM193/193A	−55 to +125	°C
	LM293/293A	−25 to +85	°C
	LM393/393A	0 to +70	°C
	LM2903	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)[1,2,3]	300	°C

NOTES:

1. For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small ($P_D \leqslant 100mW$), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.
4. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, LM193/193A: $-55°C \leqslant T_A \leqslant +125°C$, unless otherwise specified.
LM293/293A: $-25°C \leqslant T_A \leqslant +85°C$, unless otherwise specified.
LM393/393A: $0°C \leqslant T_A \leqslant +70°C$, unless otherwise specified.
LM2903: $-40°C \leqslant T_A \leqslant +85°C$, unless otherwise specified.[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common-mode voltage range[3, 7]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geqslant 0V_{DC}$ (or V− if need)			V+			V+			V+	V
I_{BIAS}	Input bias current[5]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400		25 200	250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN(+)} = 0$, $V_0 \leqslant 1.5V_{DC}$ $T_A = 25°C$	6.0	16		6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geqslant 1V_{DC}$, $V_{IN(-)} = 0$ $V_0 = 30V_{DC}$ Over temp. $V_0 = 5V_{DC}$, $T_A = 25°C$		0.1	1.0		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_A = 25°C$ $V+ = 30V$, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA
A_V	Voltage gain	$R_L \geqslant 15k\Omega$, $V+ = 15V_{DC}$, $T_A = 25°C$	50	200		50	200		25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leqslant 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700		400	400 700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$ $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300			300		ns
t_R	Response time[6]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$ $T_A = 25°C$		1.3			1.3			1.3		μs

DC ELECTRICAL CHARACTERISTICS (Continued)

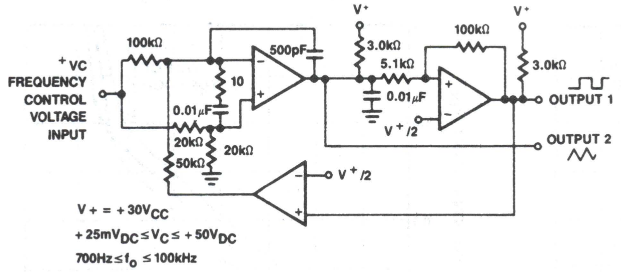
$V+ = 5V_{DC}$, LM193/193A: $-55°C \leqslant T_A \leqslant +125°C$, unless otherwise specified.
LM293/293A: $-25°C \leqslant T_A \leqslant +85°C$, unless otherwise specified.
LM393/393A: $0°C \leqslant T_A \leqslant +70°C$, unless otherwise specified.
LM2903: $-40°C \leqslant T_A \leqslant +85°C$, unless otherwise specified.[7]

SYMBOL	PARAMETER	TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV
V_{CM}	Input common-mode voltage range[3, 7]	$T_A = 25°C$ Over temp.	0 0		V±−1.5 V±−2.0	0 0		V±−1.5 V±−2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geqslant 0V_{DC}$ (or V− if need)			V+			V+	V
I_{BIAS}	Input bias current[5]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	
I_{OL}	Output sink current	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN(+)} = 0$, $V_0 \leqslant 1.5V_{DC}$ $T_A = 25°C$	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geqslant 1V_{DC}$, $V_{IN(-)} = 0$, $V_0 = 5V_{DC}$ $T_A = 25°C$ $V_0 = 30VDC$ over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators $T_A = 25°C$ V+ = 30V, over temp.		0.8	1 2.5		0.8	1 2.5	mA
A_V	Voltage gain	$R_L \geqslant 15k\Omega$, $V+ = 15V_{DC}$	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geqslant 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leqslant 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV
t_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$ $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
t_R	Response time[6]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$ $T_A = 25°C$		1.3			1.3		μs

NOTES:

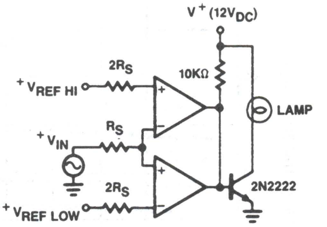
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$ and over the full input common-mode range ($0V_{DC}$ to $V+ - 1.5V_{DC}$).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. With LM293/293A, all temperature specifications are limited to $-25°C \leqslant T_A \leqslant +85°C$ and the LM393/393A, all temperature specifications are limited to $0°C \leqslant T_A \leqslant +70°C$. The LM2903 is limited to $-40°C \leqslant T_A \leqslant 85°C$.
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The response time specified is for a 100mV input step with a 5mV overdrive.
7. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

TYPICAL APPLICATIONS


V+
V+
100kΩ
+VC
FREQUENCY
CONTROL
VOLTAGE
INPUT
100kΩ
500pF
3.0kΩ
5.1kΩ
10
0.01μF
0.01μF
V+/2
3.0kΩ
OUTPUT 1
OUTPUT 2
20kΩ
20kΩ
50kΩ
V+/2
V+ = +30VCC
+25mVDC ≤ VC ≤ +50VDC
700Hz ≤ fo ≤ 100kHz

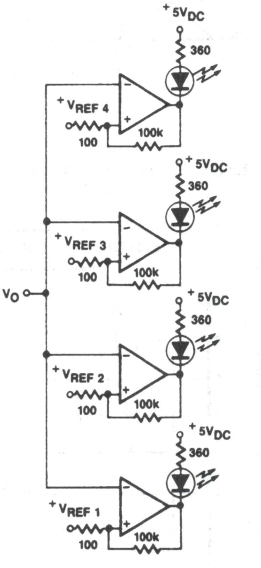
TC13280S

Two-Decade High-Frequency VCO


V+ (12VDC)
2RS
10KΩ
+VREF HI
LAMP
RS
+VIN
2RS
2N2222
+VREF LOW

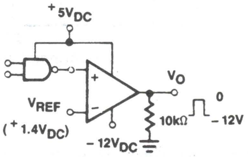
TC13290S

Limit Comparator


+5VDC
360
+VREF 4
100
100k
+5VDC
360
+VREF 3
100
100k
VO
+5VDC
360
+VREF 2
100
100k
+5VDC
360
+VREF 1
100
100k

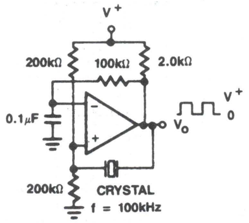
LD06400S

Visible Voltage Indicator


+5VDC
VO
0
VREF
(+1.4VDC)
10kΩ
-12V
-12VDC

TC13300S

TTL-to-MOS Logic Converter


V+
200kΩ
100kΩ
2.0kΩ
0.1μF
V+
0
VO
200kΩ
CRYSTAL
f = 100kHz

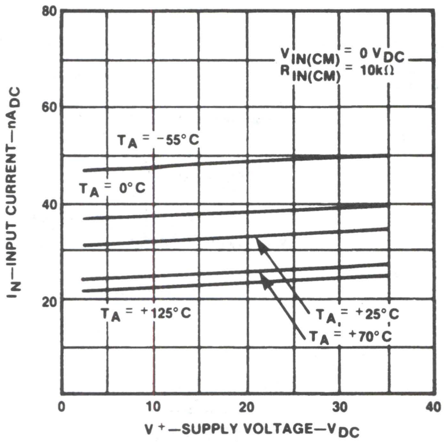
TC13310S

Crystal-Controlled Oscillator

NOTE:
All pins of any unused comparators should be grounded.

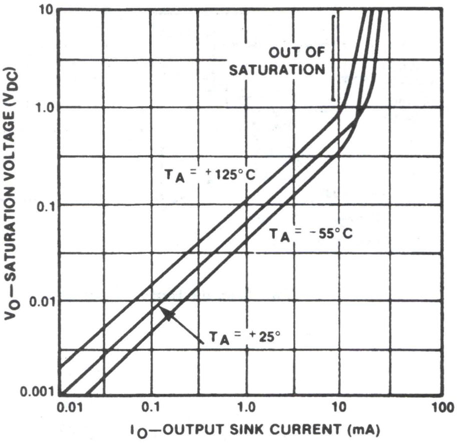
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current



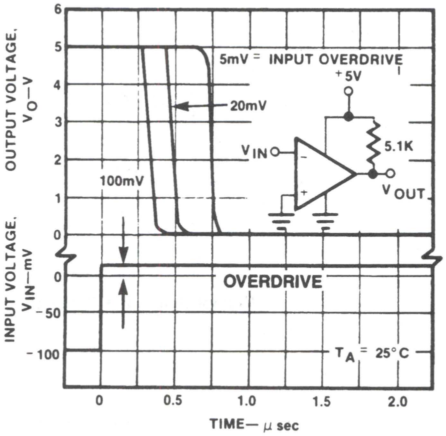
OP05580S

Output Saturation Voltage



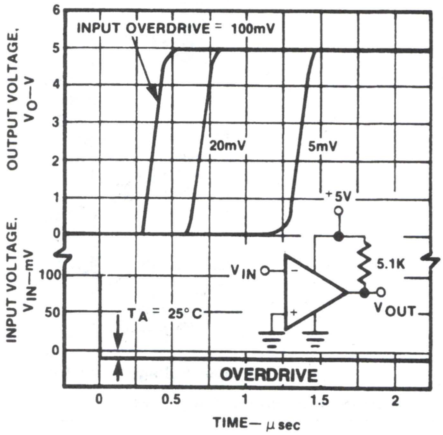
OP05590S

Response Time for Various Input Overdrives — Negative Transition



OP05600S

Response Time for Various Input Overdrives — Positive Transition



OP05610S

Signetics

Linear Products

NE/SA/SE5105/A
Precision High-Speed Comparator With Latch

Objective Specification

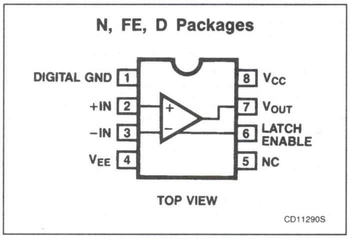
DESCRIPTION

The NE/SA/SE5105/A is a precision high-speed comparator ideally suited for applications requiring ultra-precision and speed. A typical application may be in a 12-bit successive approximation A/D converter. Input offset voltage is factory trimmed to typically 100μV (0.04 LSB for a 12-bit, 10V system); the 36ns response time (measured at 1.2mV overdrive), low input offset current, and high gain remain essentially constant over the entire operating temperature range. Thus, the same degree of precision and speed can be maintained over the specified temperature range. A latch function incorporated with the comparator allows added flexibility to the system designer. A TTL high input at the latch enable pin forces the output of the comparator to stay at its existing logical state irrespective of subsequent signal transitions at the input.

FEATURES

- **Precision input stage:**
  Input offset voltage 100μV
  Input offset current 3nA
- **Fast response time:**
  5mV overdrive 32ns
  1.2mV overdrive 36ns
  (constant over temperature)
- **High voltage gain 26,000V/V (constant over temperature)**
- **Low power dissipation 100mW**
- **TTL output capable of driving 10 TTL gates**
- **Latch function with TTL compatible input**

PIN CONFIGURATION

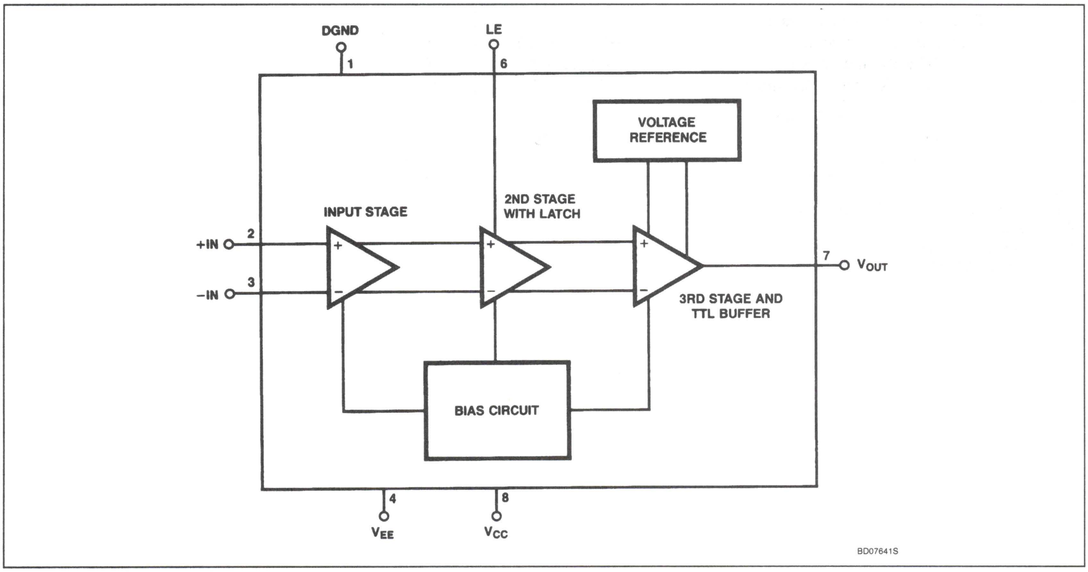


N, FE, D Packages
DIGITAL GND 1
+IN 2
−IN 3
V_EE 4
8 V_CC
7 V_OUT
6 LATCH ENABLE
5 NC
+
−
TOP VIEW
CD11290S

APPLICATIONS

- **High-speed, high-resolution successive approximation A/D converters**
- **Precision zero-crossing detectors**
- **Precision latching window comparators**
- **Fast latching ECL-to-TTL line translators**
- **Precision signal regenerators**

BLOCK DIAGRAM



DGND
1
LE
6
VOLTAGE REFERENCE
INPUT STAGE
2ND STAGE WITH LATCH
+IN
2
−IN
3
+
−
7
V_OUT
3RD STAGE AND TTL BUFFER
BIAS CIRCUIT
4
V_EE
8
V_CC
BD07641S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5105AN
8-Pin Plastic DIP	0 to +70°C	NE5105N
8-Pin Plastic DIP	−40°C to +85°C	SA5105AN
8-Pin Plastic DIP	−40°C to +85°C	SA5105N
8-Pin Plastic SO	0 to +70°C	NE5105AD
8-Pin Plastic SO	0 to +70°C	NE5105D
8-Pin Plastic SO	−40°C to +85°C	SA5105AD
8-Pin Plastic SO	−40°C to +85°C	SA5105D
8-Pin Cerdip	−55°C to +125°C	SE5105AFE
8-Pin Cerdip	−55°C to +125°C	SE5105FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC} V_{EE}	Power supply Power supply	+6 −18	V V
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1] FE package N package D package	 885 1160 780	 mW mW mW
	Differential input voltage	±5	V
	LATCH ENABLE input voltage	V_{CC} to V_{EE}	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range SE5105 (FE package) SA5105 (N and D package) NE5105 (N and D package)	 −55 to +125 −40 to +85 0 to +70	 °C °C °C
I_{SC}	Output short-circuit duration To ground To V_{CC}	 Indefinite 1	 Minute

NOTE:

1. Derate above 25°C, at the following rates:
   FE package at 6.75mW/°C.
   N package at 9.3mW/°C.
   D package at 6.2mW/°C.

Precision High-Speed Comparator With Latch NE/SA/SE5105/A

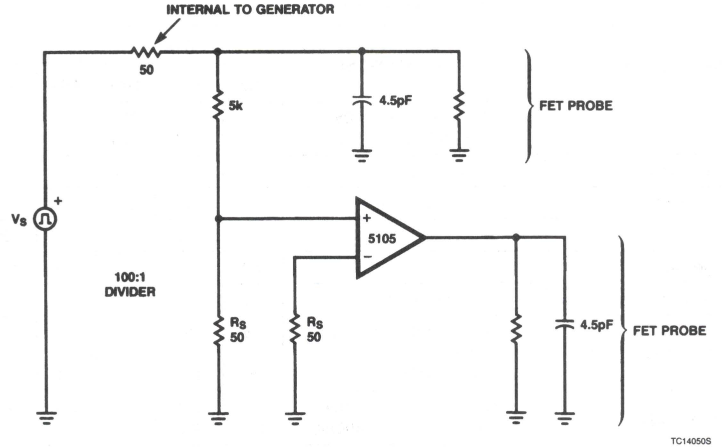
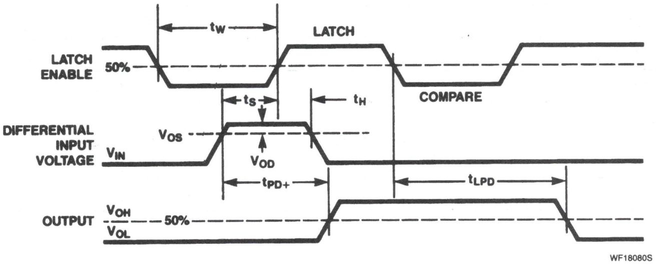

INTERNAL TO GENERATOR
50
5k
4.5pF
FET PROBE
VS
+
5105
100:1
DIVIDER
RS
50
RS
50
4.5pF
FET PROBE
TC14050S

Figure 1. Test Setup for Delay Measurement

TIMING DIAGRAMS


tW
LATCH
LATCH ENABLE
50%
tS
tH
COMPARE
DIFFERENTIAL INPUT VOLTAGE
VOS
VIN
VOD
tPD+
tLPD
OUTPUT
VOH
50%
VOL
WF18080S

SYMBOL	PARAMETER	CONDITIONS	MINIMUM LIMIT	UNIT
t_S	Setup time	V_{IN} = 100mV	28	
t_H	Hold time	V_{OD} = 5mV	10	ns
t_W	Latch pulse width		20	

DC ELECTRICAL CHARACTERISTICS V_{CC} = +5V, V_{EE} = −5V, T_A=25°C; V_{IN+} = V_{IN-} = 0V and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A			5105			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 25\Omega$, V_{CM} = 0V $R_S = 25\Omega$, V_{CM} = ±3V		100 140	250 400			600 750	µV
I_{OS}	Input offset current	$V_{LATCH} = V_{CC}$		3	20			40	nA
I_B	Input bias current	$V_{LATCH} = V_{CC}$		400	1200			1400	nA
A_{VO}	Voltage gain[1]		18	26		18	26		V/mV
CMVR	Input voltage range		±3	±3.3		±3	±3.3		V
CMRR	Common mode rejection ratio	V_{CM} = ±3V	86	99		84			dB
PSRR	Power supply rejection ratio	V_{CC}/V_{EE} = ±4.5V to ±5.5V V_{CC} = +5V and V_{EE} = −4.5V to −15V	78 86	94 104		78 84			dB dB
V_{OH}	Output high voltage	$V_{IN} \geqslant 10mV$, $I_{OH} = 0\mu A$ $V_{IN} \geqslant 10mV$, $I_{OH} = 400\mu A$	2.4 2.4	2.8 2.6		2.4 2.4	2.8 2.6		V V
V_{OL}	Output low voltage	$V_{IN} \leqslant 10mV$, $I_{OL} = 0\mu A$ $V_{IN} \leqslant 10mV$, I_{OL} = 16mA		0.2 0.3	0.4 0.4		0.2 0.3	0.4 0.4	V V
I_{CC}	Positive supply current	$V_O \leqslant 0.4V$, $I_O = 0\mu A$		11	14			16	mA
I_{EE}	Negative supply current	$V_O \leqslant 0.4V$, $I_O = 0\mu A$		9	12			14	mA
P_D	Power dissipation			100	130			150	mW
V_{LH}	Logic 1 at latch input		2			2			V
V_{LL}	Logic 0 at latch input				0.8			0.8	V
	Latch input current								
I_{LH}	Logic 1	V_{LATCH} = 3V		4	20		4	20	µA
I_{LL}	Logic 0	V_{LATCH} = 0.8V		1	5		1	5	µA
R_{IN}	Differential input resistance			1000			1000		MΩ

NOTE:

1. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, V_{EE} = −5V; −55°C ≤ T_A ≤ +125°C for SE5105A/5105; −40°C ≤ T_A ≤ +85°C for SA5105A/5105; and, 0°C ≤ T_A ≤ +70°C for NE5105A/5105. V_{IN+} = V_{IN-} = 0V and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A			5105			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S = 25Ω, V_{CM} = 0V R_S = 25Ω, V_{CM} = ±3V		0.25 0.3	0.6 0.75			1 1.2	mV
TC V_{OS}	Input offset voltage drift	V_{CM} = 0V		1.5	7.5			10	μV/°C
I_{OS}	Input offset current	V_{LATCH} = V_{CC}		4	25			60	nA
I_B	Input bias current	V_{LATCH} = V_{CC}		0.5	1.5			1.8	μA
A_{VO}	Voltage gain[1]		16	23		16	23		V/mV
CMVR	Input voltage range		±3	±3.2		±3	±3.2		V
CMRR	Common mode rejection ratio	V_{CM} = ±3V	83	93		80			dB
PSRR	Power supply rejection ratio	V_{CC}/V_{EE} = ±4.5V to ±5.5V V_{CC} = +5V and V_{EE} = −4.5V to −15V	75 75	94 94		72 72			dB dB
V_{OH}	Output high voltage	V_{IN} ≥ 10mV, I_{OH} = 0μA V_{IN} ≥ 10mV, I_{OH} = 320μA	2.4 2.4			2.4 2.4			V V
V_{OL}	Output low voltage[2]	V_{IN} ≤ 10mV, I_{OL} = 9.6mA V_{IN} ≤ 10mV, I_{OL} = 12.8mA		0.28 0.35	0.4 0.45		0.28 0.35	0.4 0.45	V V
I_{CC}	Positive supply current	V_O < 0.4V, I_O = 0μA		15	19			22	mA
I_{EE}	Negative supply current	V_O ≤ 0.4V, I_O = 0μA		12	17			20	mA
P_D	Power dissipation			135	180			210	mW
V_{LH}	Logic 1 at latch input		2			2			V
V_{LL}	Logic 0 at latch input				0.8			0.8	V
	Latch input current								
I_{LH}	Logic 1	V_{LATCH} = 3V		6	20		6	20	μA
I_{LL}	Logic 0	V_{LATCH} = 0.8V		1	10		1	10	μA
R_{IN}	Differential input resistance			1000			1000		MΩ

NOTES:

1. Guaranteed by design.
2. V_{OL} = 0.45V max at T_A ≤ −40°C and I_{OL} = 12.8mA.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V; V_{EE} = −5V; T_A = 25°C and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A/5105			UNIT
			Min	Typ	Max	
t_{PD+}	Input to output high propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		36 32	 50	ns ns
t_{PD-}	Input to output low propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		34 32	 50	ns ns
t_{LPD}	Latch disable time[1, 2]			25	38	ns

NOTES:

1. Guaranteed by design.
2. Times are for 100mV step inputs. See Timing Diagrams, Figures 3 and 4.

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5V$; $V_{EE} = -5V$; $-55°C \leqslant T_A \leqslant +125°C$ for SE5105A/5105; $-40°C \leqslant T_A \leqslant +85°C$ for SA5105/5105A, and, $0°C \leqslant T_A \leqslant +70°C$ for NE5105A/5105 Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	5105A/5105			UNIT
			Min	Typ	Max	
t_{PD+}	Input to output high propagation delay[1, 2]	$V_{OD} = 1.2mV$ $V_{OD} = 5mV$		50 45		ns ns
t_{PD-}	Input to output low propagation delay[1, 2]	$V_{OD} = 1.2mV$ $V_{OD} = 5mV$		43 40		ns ns
t_{LPD}	Latch disable time[1, 2]			34		ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See Timing Diagrams, Figures 3 and 4.

SYMBOLS AND DEFINITIONS

Common-Mode Rejection Ratio (CMRR)
The ratio of the change in common-mode voltage to the corresponding change in V_{OS}. CMRR is expressed in dB, CMRR = 20 log ($\Delta CMV/\Delta V_{OS}$).

Differential Input Resistance (R_{IN})
Resistance looking into either input terminal with the other referred to a specified voltage.

Input Bias Current (I_{BIAS})
The current into either input terminal with both inputs referred to a specified voltage.

Input Offset Current (I_{OS})
The difference between the two input bias currents with both inputs referred to a specified voltage

Input Offset Voltage (V_{OS})
The minimum potential difference required between the input terminals to force the output to a specified voltage.

Input Offset Voltage Drift (TCV_{OS})
The ratio of the change in V_{OS} to the change in temperature as that temperature deviates from a +25°C ambient.

Input to Output Propagation Delay (t_{PD+} and t_{PD-})
The propagation delay measured from the time the input signal crosses V_{OS} to the 50% transition point of the output signal. Delay is measured with a specified input step size (V_{IN}) and overdrive (V_{OD}).

Input Voltage Range (CMVR)
The range of common-mode voltage at the input for which operation within specifications is guaranteed.

Latch Disable Propagation Delay (t_{LPD})
The propagation delay measured between the 50% transition points of the LATCH ENABLE signal falling edge and the output signal transition point.

Latch Hold Time (t_H)
The minimum time after the positive transition of the LATCH ENABLE signal that the input signal must remain unchanged in order to be acquired and held at the output. Hold time is measured from the 50% transition point of the LATCH ENABLE signal to the point where comparator input signal crosses V_{OS}.

Latch Pulse Width (t_W)
The minimum time that the LATCH ENABLE signal must be low in order to acquire and subsequently hold the input signal change. Pulse width is measured between the 50% transition points of the falling and rising edges of the latch pulse.

Latch Setup Time (t_S)
The minimum time before the positive transition of the LATCH ENABLE signal that an input signal change must be present in order to be acquired and held at the output. Setup time is measured from the point the input signal crosses V_{OS} to the 50% transition point of the LATCH ENABLE signal.

Output High Current (I_{OH})
The current that the comparator output can source at a specified output voltage and input overdrive.

Output High Voltage (V_{OH})
The high output voltage with a specified source current and input overdrive.

Output Low Voltage (V_{OL})
The low output voltage with a specified sink current and input overdrive.

Output Sink Current (I_{OL})
The current that the comparator output can sink at a specified output voltage and input overdrive.

Overdrive (V_{OD})
The applied input differential voltage in excess of input offset voltage (V_{OS}).

Power Supply Rejection Ratio (PSRR)
The ratio of the change in input offset voltage to the specified change in power supply voltage.

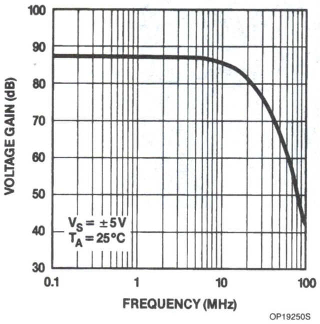
Voltage Gain (A_V)
The ratio of the change in output voltage (over a specified range) to the change in differential input voltage.

APPLYING THE NE/SA/SE5105/A

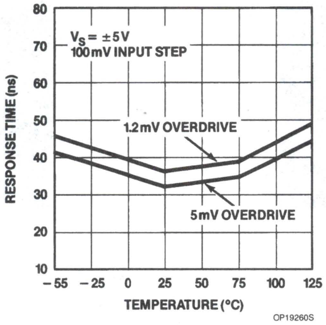
PC Board Layout

As with any high-speed circuit, layout of the PC board becomes critical for optimum performance. The supplies should be bypassed with good high frequency capacitors mounted as close to the IC as possible. A combination of high frequency ceramic and tantalum capacitors provide adequate suppression of transients on the supply lines. Since the comparator is an uncompensated amplifier with high gain, even a small amount of feedback from the output to the input can cause oscillation. A poor layout of the PC board not only increases the uncertainty region (due to oscillation) of the comparator, but also introduces hysteresis. Use of ground planes is essential since ground planes not only minimize inductance, but also reduce stray feedback capacitances by referring them to ground. Separate analog and digital ground planes should be used; the inputs are referred to the analog ground while the supplies and output are referred to the digital ground (Pin 1). Furthermore, the analog and digital ground planes should only meet at one point. Comparator output and input pins should be isolated from each other along with the traces from the respective pins. Stray capacitance from the IC pins to ground can be minimized by keeping the lead lengths and traces as short as possible.

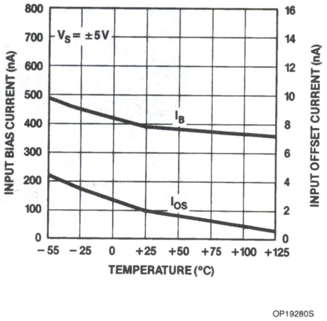
TYPICAL PERFORMANCE CHARACTERISTICS



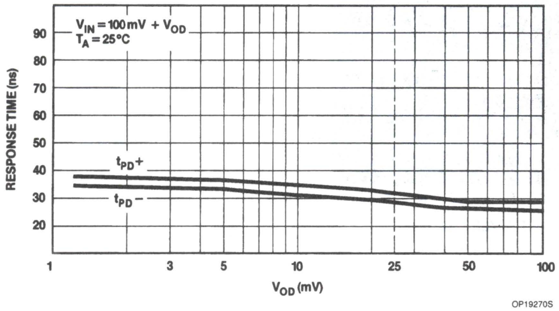
Voltage Gain vs Frequency



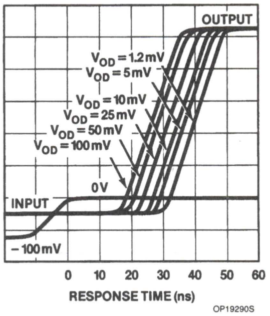
Response Time vs Temperature



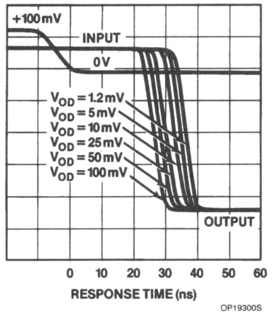
Input Current vs Temperature



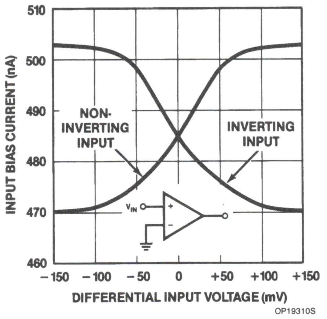
Response Time vs Overdrive Voltage



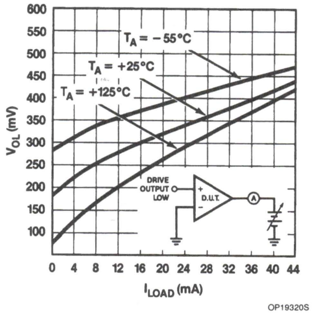
t_{PD}+ Response Time



t_{PD}− Response Time



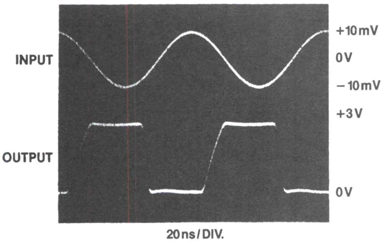
Input Bias Current vs Differential Input Voltage



V_{SAT} vs Load Current

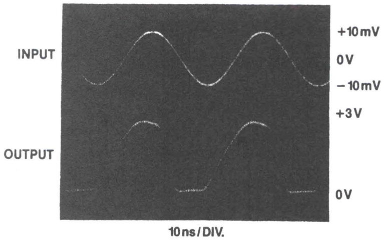
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Response to 10MHz Sine Wave



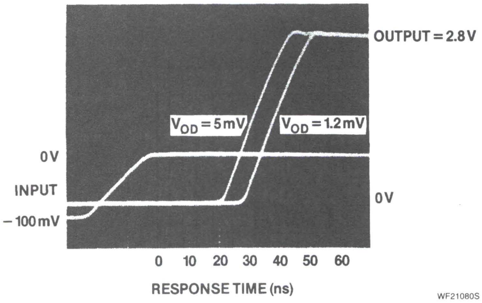
WF21060S

Response to 25MHz Sine Wave



WF21070S

Response Time to 5m V and 1.2mV Overdrive



WF21080S

Signetics

NE/SE521
High-Speed Dual-Differential Comparator/Sense Amp

Product Specification

Linear Products

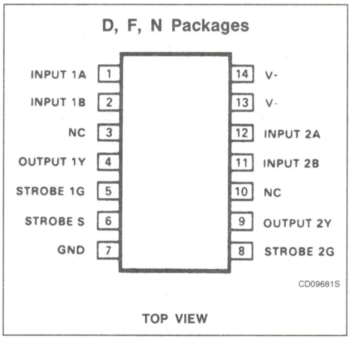
FEATURES

- 12ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

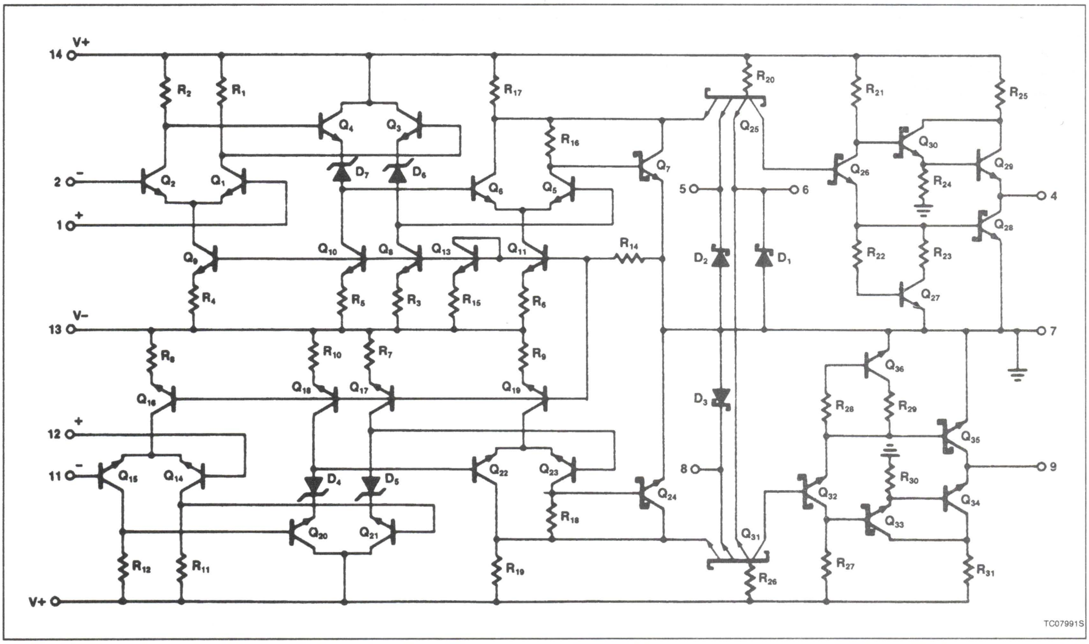
PIN CONFIGURATION


D, F, N Packages
INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GND 7
14 V+
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G
CD09681S
TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE521N
14-Pin SO Package	0 to +70°C	NE521D
14-Pin Cerdip	0 to +70°C	NE521F
14-Pin Cerdip	-55°C to +125°C	SE521F

EQUIVALENT SCHEMATIC


V+
14
V-
13
2 -
1 +
12 +
11 -
V+
5
6
8
4
7
9
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
D1
D2
D3
D4
D5
D6
D7
TC07991S

High-Speed Dual-Differential Comparator/Sense Amp NE/SE521

LOGIC FUNCTIONS

V_{ID} A^+, B^-	STROBE S	STROBE G	OUTPUT (Y)
$V_{ID} \leqslant -V_{OS}$	H	H	L
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$V_{ID} \geqslant V_{OS}$	H	H	H
X	L	X	H
X	X	L	H

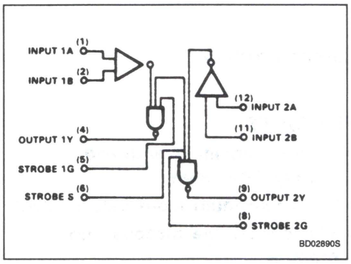
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
V+	Positive	+7	V
V–	Negative	–7	V
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		
	Common mode	±5	V
	Strobe/gate	+5.25	V
P_D	Maximum power dissipation[1]		
	T_A = 25°C (still-air)		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range		
	NE521	0 to 70	°C
	SE521	–55 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	+300	°C

NOTE:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

BLOCK DIAGRAM


(1) INPUT 1A
(2) INPUT 1B
(4) OUTPUT 1Y
(5) STROBE 1G
(6) STROBE S
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G
BD02890S

High-Speed Dual-Differential Comparator/Sense Amp NE/SE521

DC ELECTRICAL CHARACTERISTICS (SE521) V+ = +5V, V− = −5V, T_A = −55°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.5V, V− = −4.5V				
	At 25°C			6	7.5	mV
	Over temperature range				15	
I_{BIAS}	Input bias current	V+ = +5.5V, V− = −5.5V				
	At 25°C			7.5	20	μA
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.5V, V− = −5.5V				
	At 25°C			1.0	5	μA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+ = +4.5V, V− = −4.5V	±3			V
V_{IL}	Low level input voltage					
	At 25°C				0.8	V
	Over temperature				0.7	
V_{IH}	High level input voltage		2.0			V
	Input current	V+ = +5.5V, V− = −5.5V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
	Input Current					
I_{IL}	Low	V_{IL} = 0.5V				
		1G or 2G strobe			−2.0	mA
		Common strobe S			−4.0	mA
	Output voltage	$V_{I(S)}$ = 2.0V				
V_{OH}	High	V+ = +4.5V, V− = −4.5V, I_{LOAD} = −1mA	2.5	3.4		V
V_{OL}	Low	V+ = +4.5V, V− = −4.5V, I_{LOAD} = 10mA			0.5	
		T_A = 25°C, I_{LOAD} = 20mA			0.5	
	Supply voltage					
V+	Positive		4.5	5.0	5.5	V
V−	Negative		−4.5	−5.0	−5.5	
	Supply current	V+ = 5.5V, V− = −5.5V, T_A = 25°C				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			−15	−28	
I_{SC}	Short-circuit output current		−35		−115	mA

High-Speed Dual-Differential Comparator/Sense Amp NE/SE521

DC ELECTRICAL CHARACTERISTICS (NE521) V+ = +5V, V- = -5V, T_A = 0 to 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				
	At 25°C			6	7.5	mV
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				
	At 25°C			7.5	20	μA
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				
	At 25°C			1.0	5	μA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
	Input Current					
I_{IL}	Low	V_{IL} = 0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$ = 2.0V				
V_{OH}	High	V+ = +4.75V, V- = -4.75V, I_{LOAD} = -1mA	2.7	3.4		V
V_{OL}	Low	V+ = +5.25V, V- = -5.25V, I_{LOAD} = 20mA			0.5	
	Supply voltage					
V+	Positive		4.75	5.0	5.25	V
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			-15	-28	
I_{SC}	Short-circuit output current		-40		-100	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω C_L = 15pF V+ = 5V V- = 5V.

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large-signal switching speed							
	Propagation delay						
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	ns
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	6	
f_{MAX}	Max. operating frequency			40	55		MHz

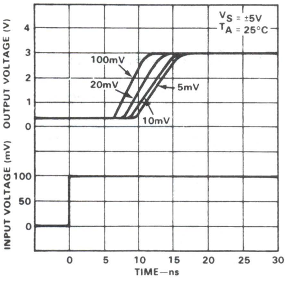
NOTES:

1. Response time measured from 0V point of ±100mV$_{P-P}$ 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.

High-Speed Dual-Differential Comparator/Sense Amp NE/SE521

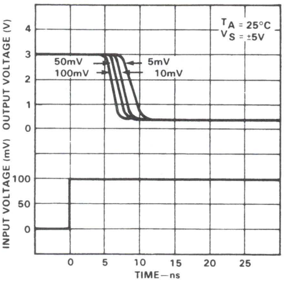
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time for Various Input Overdrives



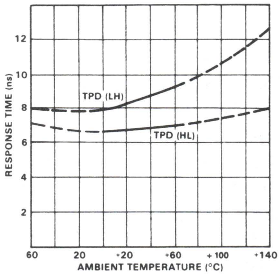
OP03890S

Response Time for Various Input Overdrives



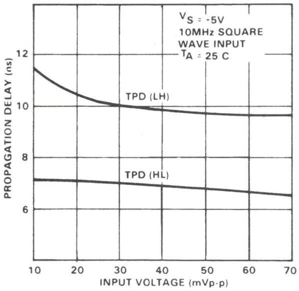
OP03900S

Response Time vs Temperature



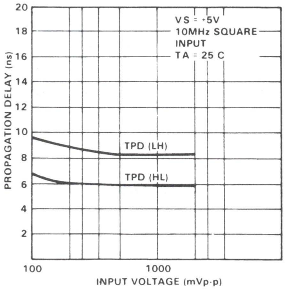
OP03910S

Propagation Delay for Various Input Voltage



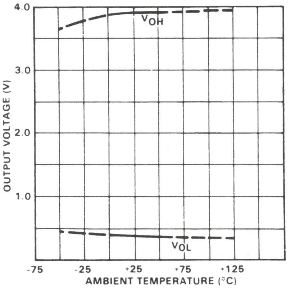
OP03920S

Propagation Delay for Various Input Voltages



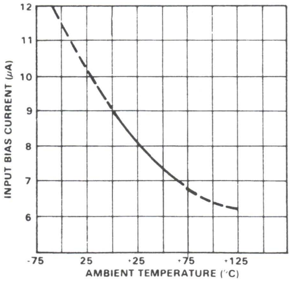
OP03930S

Output Voltage vs Ambient Temperature



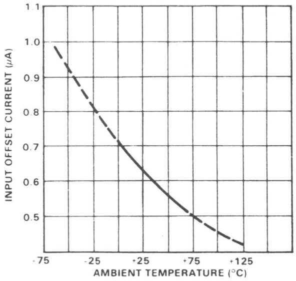
OP03940S

Input Bias Current vs Ambient Temperature



OP03950S

Input Offset Current vs Ambient Temperature



OP03960S

Signetics

Linear Products

NE/SE522
High-Speed Dual-Differential Comparator/Sense Amp

Product Specification

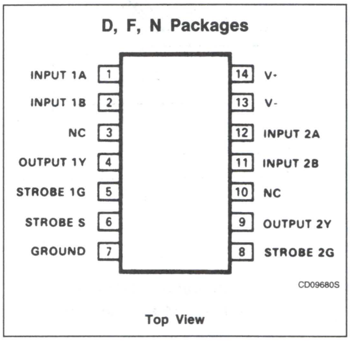
FEATURES

- 15ns maximum guaranteed propagation delay
- 20µA maximum input bias current
- TTL-compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages

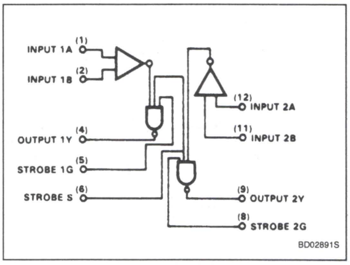
APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

PIN CONFIGURATION


D, F, N Packages
INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V-
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G
CD09680S
Top View

BLOCK DIAGRAM


INPUT 1A (1)
INPUT 1B (2)
OUTPUT 1Y (4)
STROBE 1G (5)
STROBE S (6)
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G
BD02891S

ORDERING INFORMATION

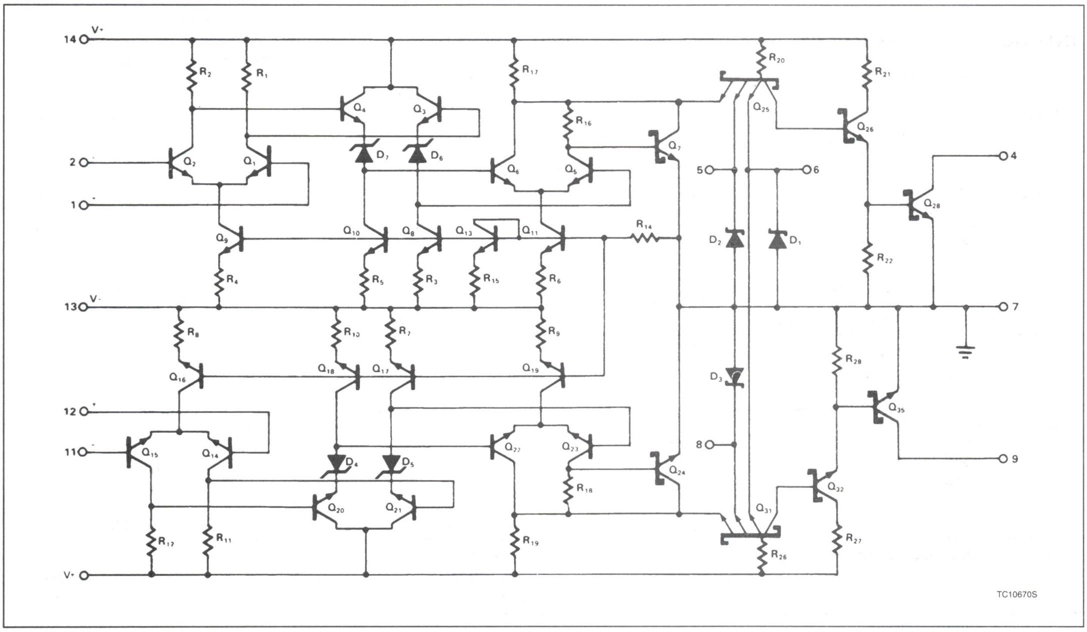
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to 70°C	NE522F
14-Pin Cerdip	−55°C to 125°C	SE522F
14-Pin Plastic DIP	0 to +70°C	NE522N
14-Pin Plastic SO	0 to 70°C	NE522D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
 V+ V−	Supply voltage Positive Negative	 +7 −7	V
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage Common-mode Strobe/gate	 ±5 +5.25	V
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE522 SE522	0 to 70 -55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

High-Speed Dual-Differential Comparator/Sense Amp NE/SE522

EQUIVALENT SCHEMATIC


14
V+
R2
R1
Q4
Q3
D7
D6
2
Q2
Q1
1
Q9
Q10
Q8
Q13
Q11
R14
R4
R5
R3
R15
R6
13
V-
R8
R10
R7
R9
Q16
Q18
Q17
Q19
12
11
Q15
Q14
D4
D5
Q22
Q23
R18
Q20
Q21
R17
R11
R19
V+
R17
R16
Q6
Q5
Q7
R20
Q25
R21
Q26
4
5
6
D2
D1
Q28
R22
7
R28
D3
Q35
8
Q24
9
Q32
Q31
R26
R27
TC10670S

DC ELECTRICAL CHARACTERISTICS (SE522)± 5V ± 10%, $T_A = -55$ to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.5V, V− = −4.5V				
	At 25°C			6	7.5	mV
	Over temperature range				15	
I_{BIAS}	Input bias current	V+ = +5.5V, V− = −5.5V				
	At 25°C			7.5	20	µA
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.5V, V− = −5.5V				
	At 25°C			1.0	5	µA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+ = +4.5V, V− = −4.5V	±3			V
V_{IL}	Low level input					
	Voltage at 25°C				0.8	V
	Over temperature				0.7	
V_{IH}	High level temperature		2.0			V
I_{IH}	Input current	V+ = +5.5V, V− = −5.5V				
	High	$V_{IH} = 2.7V$				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
I_{IL}	Low input current	$V_{IL} = 0.5V$				
		1G 2G strobe			−2	mA
		Common strobe S			−4	mA
V_{OL}	Output voltage					
	Low	V+ = +4.5V, V− = −4.5V				V
		$I_{OL} = 20mA$, $T_A = 25°C$			0.5	
		$I_{OL} = 10mA$			0.5	
I_{OH}	Output current					
	High	$V_{CC+} = +4.5$, $V_{CC-} = -4.5V$, $V_{OH} = 5.5V$			250	µA
	Supply voltage					
V+	Positive		4.5	5.0	5.5	V
V−	Negative		−4.5	−5.0	−5.5	
	Supply current	V+ = 5.5V, V− = −5.5V				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			−15	−28	

High-Speed Dual-Differential Comparator/Sense Amp NE/SE522

DC ELECTRICAL CHARACTERISTICS (NE522)± 5V ±5%, $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.75V, V− = −4.75V		6	7.5 10	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.25V, V− = −5.25V		7.5	20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.25V, V− = −5.25V		1.0	5 12	μA
V_{CM}	Common-mode voltage range	V+ = +4.75V, V− = −4.75V	±3			V
I_{IH}	Input current High	V+ = +5.25V, V− = −5.25V $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S			50 100	μA μA
I_{IL}	Low	$V_{IL} = 0.5V$ 1G 2G strobe Common strobe S			−2.0 −4.0	mA mA
V_{OL}	Output voltage low	V+ = +5.25V, V− = −5.25V, $V_{I(S)} = 2.0V$ $I_{LOAD} = 20mA$			0.5	V
I_{OH}	Output current high High	$V_{CC+} = +4.75$ $V_{CC-} = -4.75V$, $V_{OH} = 5.25V$			250	μA
V+ V−	Supply Voltage Positive Negative		4.75 −4.75	5.0 −5.0	5.25 −5.25	V
I_{CC+} I_{CC-}	Supply current Positive Negative	V+ = 5.25V, V− = −5.25V, $T_A = 25°C$		27 −15	50 −28	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $R_L = 280\Omega$, $C_L = 15pF$

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
I_R	Input resistance				4		kΩ
I_C	Input capacitance				3		pF
Large-signal switching speed							
	Propagation delay						
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	ns
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	13	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	9	
f_{MAX}	Maximum operating frequency			25	35		MHz

NOTES:

1. Response time measured from 0V point of $\pm 100mV_{P-P}$ 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of the input to 1.5V point of the output.

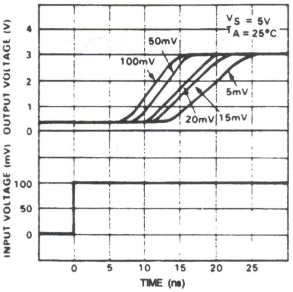
LOGIC FUNCTION TABLE

V_{ID} (A^+, B^-)	STRS	STRG	Output Transistor
$< -V_{OS}$	H	H	ON
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$> V_{OS}$	H	H	OFF
X	L	X	OFF
X	X	L	OFF

High-Speed Dual-Differential Comparator/Sense Amp NE/SE522

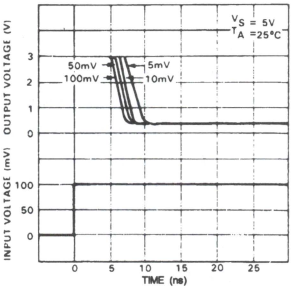
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time for Various Input Overdrives



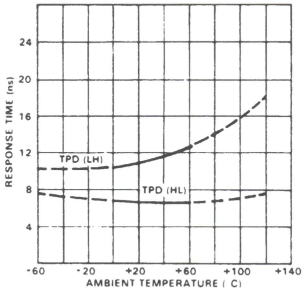
OP06701S

Response Time for Various Input Overdrives



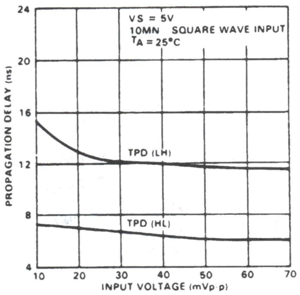
OP06711S

Response Time vs Temperature



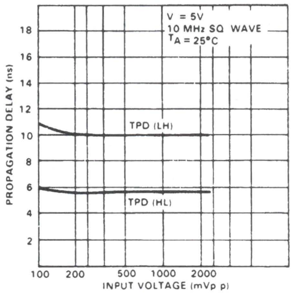
OP06721S

Propagation Delay for Various Input Voltages



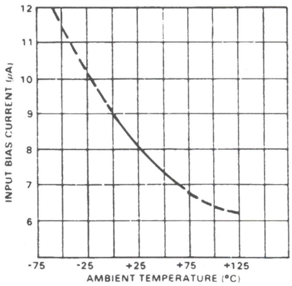
OP06731S

Propagation Delay for Various Input Voltages



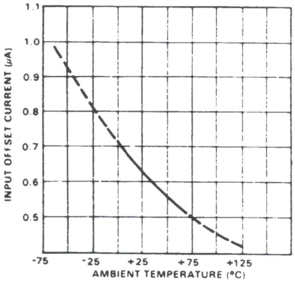
OP06741S

Input Bias Current vs Ambient Temperature



OP06751S

Input Offset Current vs Ambient Temperature



OP06761S

Signetics

NE/SE527
Voltage Comparator

Product Specification

Linear Products

DESCRIPTION

The NE/SE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE/SE527 is similar in design to the Signetics NE/SE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

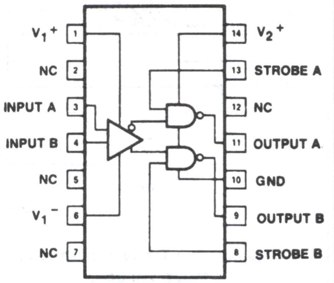
- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- MIL-STD-883A, B, C available
- Typical gain of 5000

APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

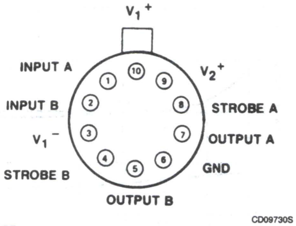
PIN CONFIGURATIONS

D, F, N Packages



V1+ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
V1− 6
NC 7
14 V2+
13 STROBE A
12 NC
11 OUTPUT A
10 GND
9 OUTPUT B
8 STROBE B
CD09722S

H Package[1]



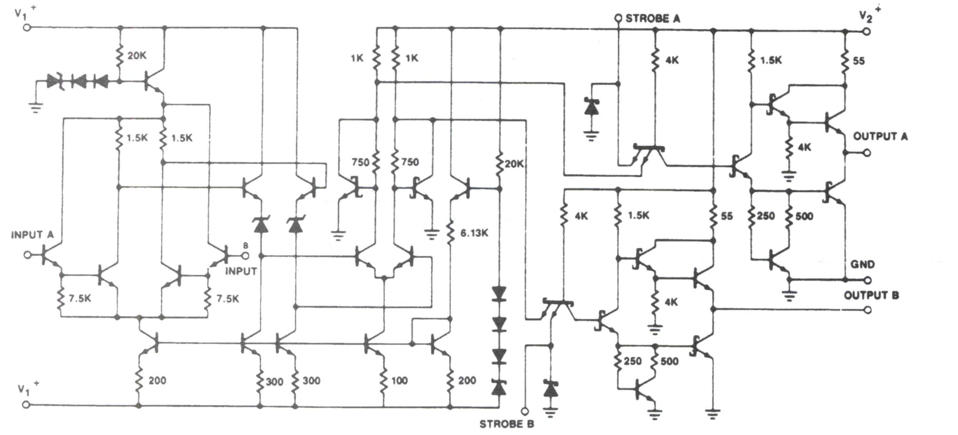
V1+
INPUT A
INPUT B
V1−
STROBE B
OUTPUT B
V2+
STROBE A
OUTPUT A
GND
1
2
3
4
5
6
7
8
9
10
CD09730S

NOTE:
1. Metal cans (H) not recommended for new designs.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE527N
14-Pin Cerdip	0 to +70°C	NE527F
14-Pin SO	0 to +70°C	NE527D
14-Pin Cerdip	−55°C to +125°C	SE527F
10-Lead metal can	0 to +70°C	NE527H
10-Lead metal can	−55°C to +125°C	SE527H

EQUIVALENT SCHEMATIC



V1+
20K
1.5K
1.5K
INPUT A
B INPUT
7.5K
7.5K
200
300
300
100
200
V1+
1K
1K
750
750
20K
6.13K
STROBE B
STROBE A
4K
4K
1.5K
55
V2+
1.5K
55
4K
250
500
OUTPUT A
4K
250
500
GND
OUTPUT B
TC08004S

Voltage Comparator NE/SE527

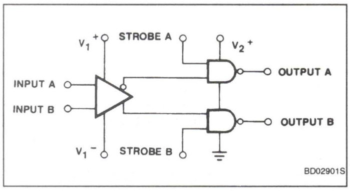
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	−15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Max power dissipation[1] 25°C ambient (still air) F package N package D package	 1190 1420 1040	 mW mW mW
T_A	Operating temperature range NE527 SE527	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package 9.5mW/°C
   N package 11.4mW/°C
   D package 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $V_1+ = 10V$, $V_1- = -10V$, $V_2+ = +5.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
			Min	Typ	Max	Min	Typ	Max	
Input characteristics									
V_{OS}	Input offset voltage @ 25°C				4			6	mV
	over temperature range				6			10	mV
I_{BIAS}	Input bias current @ 25°C				2			2	μA
	over temperature range				4			4	μA
I_{OS}	Input offset current @ 25°C				0.5			0.75	μA
	over temperature range	$V_{IN} = 0V$			1			1	μA
	common-mode voltage range				±5			±5	V
Gate characteristics									
V_{OUT}	Output Voltage								
	"1" State	$V_2+ = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
	"0" State	$V_2+ = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
	Strobe inputs								
	"0" Input current[1]	$V_2+ = 5.25V$, $V_{STROBE} = 0.5V$			−2			−2	mA
	"1" Input current @ 25°C[1]	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			50			100	μA
	Over temperature range	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			200			200	μA
	"0" Input voltage	$V_2+ = 4.75V$			0.8			0.8	V
	"1" Input voltage	$V_2+ = 4.75V$	2.0			2.0			V
I_{SC}	Short-circuit output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	−18		−70	−18		−70	mA
Power supply requirements									
	Supply voltage								
V_1+			5		10	5		10	V
V_1-			−6		−10	−6		−10	V
V_2+			4.5	5	5.5	4.75	5	5.25	V
	Supply current	$V_1+ = 10V$, $V_1- = -10V$							
		$V_2+ = 5.25V$							
I_1+		Over temp.			5			5	mA
I_1-		Over temp.			10			10	mA
I_2+		Over temp.			20			20	mA

NOTE:

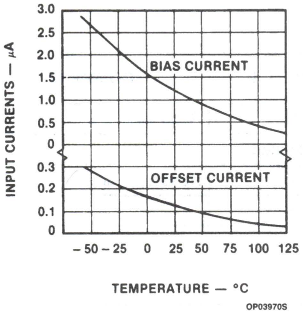
1. See Logic Function Table.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified. (See AC test circuit)

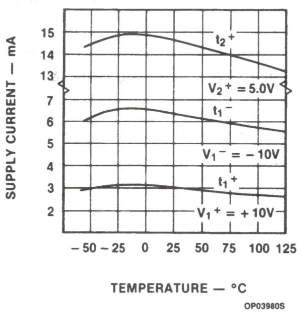
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Transient response propagation delay time					
t_{PLH}	Low-to-High	$V_{IN} = \pm 100mV$ step		16	26	ns
t_{PHL}	High-to-Low			14	24	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	Turn-on time			6		ns
t_{OFF}	Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

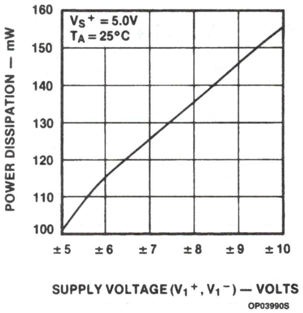
Input Currents vs Temperature



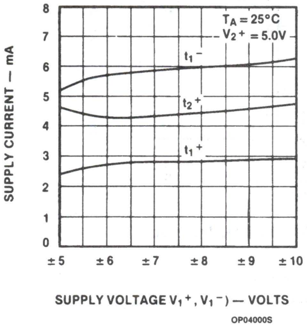
Supply Current vs Temperature



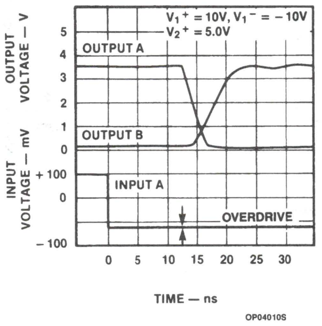
Power Dissipation vs Supply Voltage



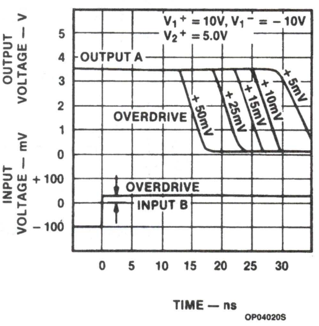
Supply Current vs Supply Voltage



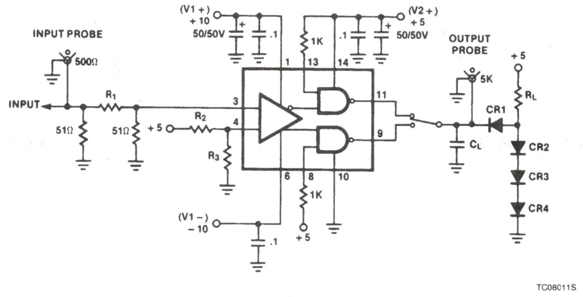
Output Propagation Delays



Response Time for Various Input Overdrives



RESPONSE TIME TEST CIRCUIT


(V1+)
+10
50/50V
.1
(V2+)
+5
50/50V
.1
1K
1
13
14
INPUT PROBE
500Ω
INPUT
R1
51Ω
51Ω
+5
R2
R3
3
4
11
9
6
8
10
1K
+5
(V1−)
−10
.1
OUTPUT PROBE
5K
+5
RL
CR1
CL
CR2
CR3
CR4
TC08011S

NOTES:
CR1 – CR4 = IN914
R1 selected for 15:1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
T_r = T_f = 2ns
Amplitude = 3.00V

Output
R_L = 390Ω
C_L = 25pF (including stray capacitance)

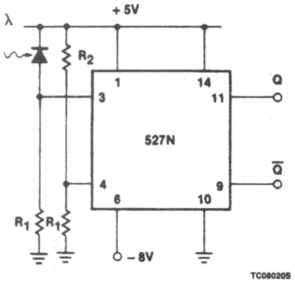
APPLICATIONS

One of the main features of the device is that supply voltages (V_1+, V_1-) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V_1-) should always be at least 6V more than the ground terminal (Pin 6). Input common-mode range should be limited to values of 2V less than the supply voltages (V_1+ and V_1-) up to a maximum of ±6V as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

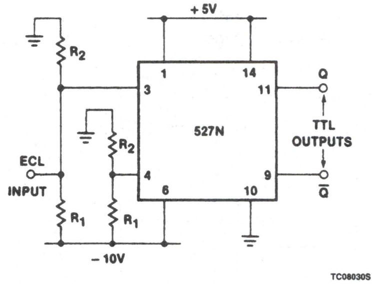
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \leqslant -V_{OS}$	H	X	L	H	Read I_{IHA}, I_{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined	
$V_{ID} \geqslant V_{OS}$	X	H	H	L	Read I_{ILA}, I_{IHB}
X	L	L	H	H	

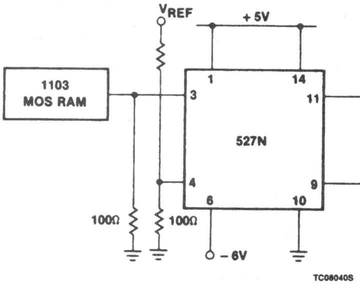
TYPICAL APPLICATIONS


λ
+5V
R2
1
14
3
11
Q
527N
Q̄
4
9
6
10
R1
R1
-8V
TC08020S

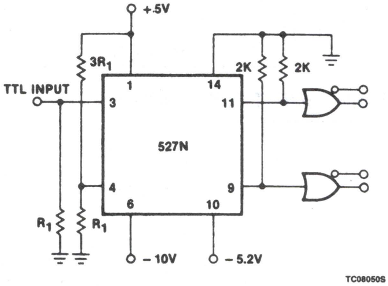
Photodiode Detector


+5V
R2
1
14
3
11
Q
527N
TTL OUTPUTS
R2
ECL INPUT
4
9
6
10
Q̄
R1
R1
-10V
TC08030S

ECL-to-TTL Interface


VREF
+5V
1103 MOS RAM
1
14
3
11
Q
527N
Q̄
4
9
6
10
100Ω
100Ω
-6V
TC08040S

MOS Memory Sense AMP


+5V
3R1
2K
2K
TTL INPUT
1
14
3
11
527N
4
9
6
10
R1
R1
-10V
-5.2V
TC08050S

TTL-to-ECL Interface

Signetics

NE/SE529
Voltage Comparator

Product Specification

Linear Products

DESCRIPTION

The NE/SE529 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high-speed TTL gates with a precision linear amplifier on a single monolithic chip.

FEATURES

- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common-mode and differential voltage range**
- **Typical gain 5000**

APPLICATIONS

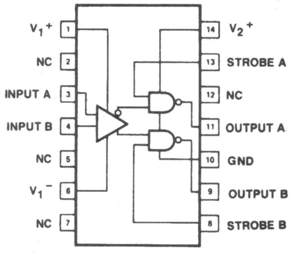
- **A/D conversion**
- **ECL-to-TTL interface**
- **TTL-to-ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **MIL-STD-883A, B, C available**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE529N
14-Pin Cerdip	0 to +70°C	NE529F
14-Pin Cerdip	−55°C to +125°C	SE529F
14-Pin SO	0 to +70°C	NE529D
10-Lead Metal Can	0 to +70°C	NE529H
10-Lead Metal Can	−55°C to +125°C	SE529H

PIN CONFIGURATIONS

D, F, N Packages

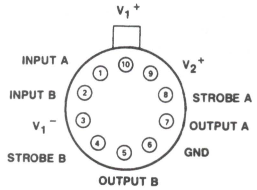


$V_1{}^+$ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
$V_1{}^-$ 6
NC 7
14 $V_2{}^+$
13 STROBE A
12 NC
11 OUTPUT A
10 GND
9 OUTPUT B
8 STROBE B

TOP VIEW

CD09722S

H Package*

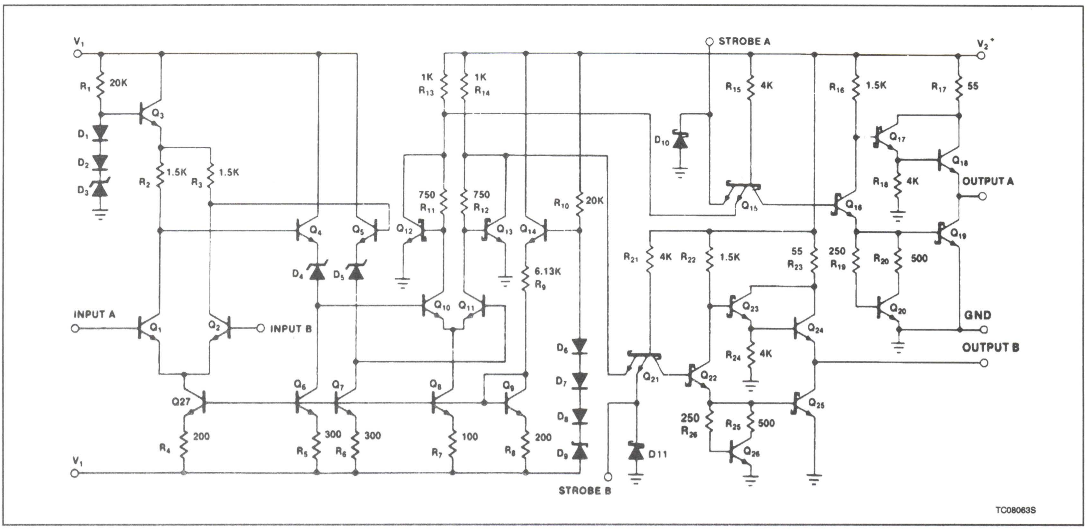


$V_1{}^+$
INPUT A
$V_2{}^+$
INPUT B
STROBE A
$V_1{}^-$
OUTPUT A
STROBE B
GND
OUTPUT B
1
2
3
4
5
6
7
8
9
10

CD09730S

NOTE:
*Metal cans (H) not recommended for new designs.

EQUIVALENT SCHEMATIC



V_1
R_1 20K
Q_3
D_1
D_2
D_3
R_2 1.5K
R_3 1.5K
INPUT A
Q_1
Q_2
INPUT B
Q27
R_4 200
V_1
Q_4
Q_5
D_4
D_5
Q_6
Q_7
R_5 300
R_6 300
1K R_{13}
1K R_{14}
750 R_{11}
750 R_{12}
Q_{12}
Q_{13}
Q_{14}
Q_{10}
Q_{11}
Q_8
Q_9
R_7 100
R_8 200
R_{10} 20K
6.13K R_9
D_6
D_7
D_8
D_9
STROBE B
STROBE A
D_{10}
R_{15} 4K
Q_{15}
R_{21} 4K
R_{22} 1.5K
Q_{21}
Q_{22}
Q_{23}
Q_{24}
Q_{25}
Q_{26}
R_{24} 4K
250 R_{26}
R_{25} 500
D11
55 R_{23}
250 R_{19}
$V_2{}^+$
R_{16} 1.5K
R_{17} 55
Q_{17}
Q_{18}
R_{18} 4K
Q_{16}
OUTPUT A
Q_{19}
R_{20} 500
Q_{20}
GND
OUTPUT B
TC08063S

Voltage Comparator

NE/SE529

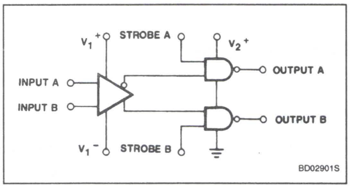
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	-15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Maximum power dissipation[1] T_A = 25°C (still-air) F package N package D package	 1190 1420 1040	 mW mW mW
T_A	Operating temperature range NE529 SE529	 0 to +70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	 +300	 °C

NOTE:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C.
   N package at 11.5mW/°C.
   D package at 8.3mW/°C.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $V_1+ = +10V$, $V_2+ = +5.0V$, $V_1- = -10V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT
			Min	Typ	Max	Min	Typ	Max	
Input characteristics									
V_{OS}	Input offset voltage @ 25°C				4			6	mV
	Over temperature range				6			10	mV
I_{BIAS}	Input bias current @ 25°C			5	12		5	20	µA
	Over temperature range	$V_{IN} = 0V$			36			50	µA
I_{OS}	Input offset current @ 25°C			2	3		2	5	µA
	Over temperature range	$V_{IN} = 0V$			9			15	µA
	Common-mode voltage range			0	±5		0	±5	V
Gate characteristics									
V_{OUT}	Output voltage								
	"1" state	$V_2+ = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
	"0" state	$V_2+ = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
	Strobe inputs								
	"0" Input current[1]	$V_2+ = 5.25V$, $V_{STROBE} = 0.5V$			−2			−2	mA
	"1" Input current @ 25°C[1]	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			50			100	µA
	Over temperature range	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			200			200	µA
	"0" input voltage	$V_2+ = 4.75V$			0.8			0.8	V
	"1" input voltage	$V_2+ = 4.75V$	2.0			2.0			V
I_{SC}	Short-circuit output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	−18		−70	−18		−70	mA
Power supply requirements									
	Supply voltage								
V_1+			5		10	5		10	V
V_1-			−6		−10	−6		−10	V
V_2+			4.5	5	5.5	4.75	5	5.25	V
	Supply current	$V_1+ = 10V$, $V_1- = -10V$ $V_2+ = 5.25V$							
I_1+		Over temp.			5			5	mA
I_1-		Over temp.			10			10	mA
I_2+		Over temp.			20			20	mA

NOTES:

1. See logic function table.

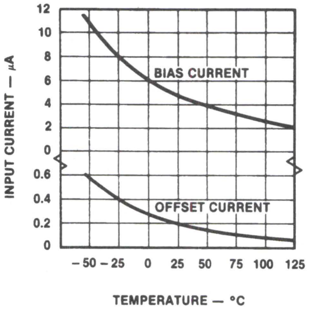
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ (See AC test circuit).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Transient response	$V_{IN} = \pm 100mV$ step				
	Propagation delay time					
t_{PLH}	Low-to-high			12	22	ns
t_{PHL}	High-to-low			10	20	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	turn-on time			6		ns
t_{OFF}	turn-off time			6		ns

Voltage Comparator NE/SE529

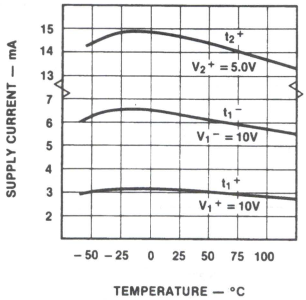
TYPICAL PERFORMANCE CHARACTERISTICS

Input Currents vs Temperature



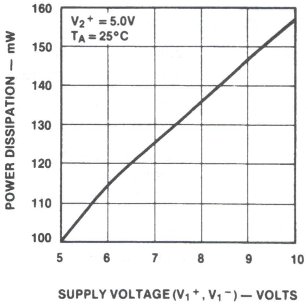
OP04030S

Supply Current vs Temperature



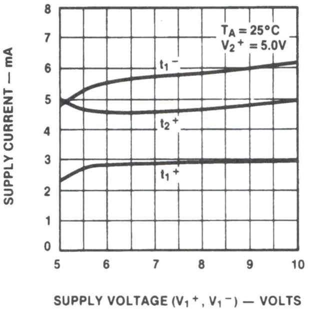
OP04040S

Power Dissipation vs Supply Voltage



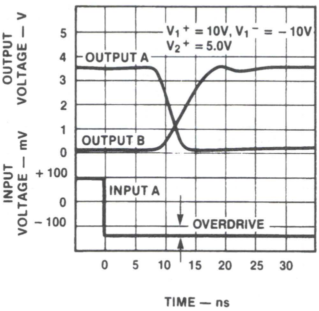
OP04050S

Supply Current vs Supply Voltage



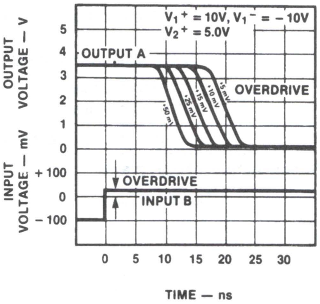
OP04060S

Output Propagation Delays



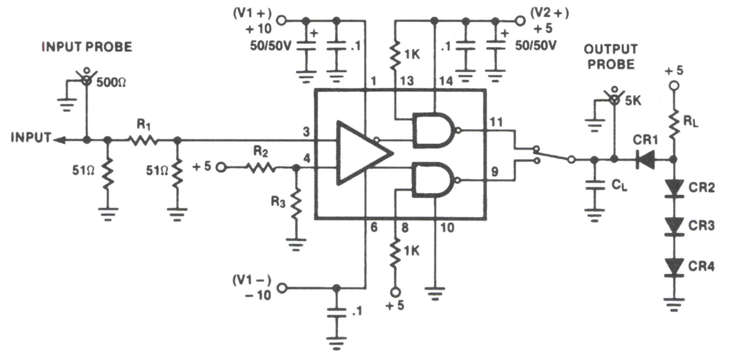
OP04070S

Response Time For Various Input Overdrives



OP04080S

RESPONSE TIME TEST CIRCUIT


(V1+)
+10
50/50V
.1
1K
.1
(V2+)
+5
50/50V
INPUT PROBE
500Ω
INPUT
R1
51Ω
51Ω
+5
R2
R3
1
13
14
3
4
11
9
6
8
10
1K
(V1−)
−10
.1
+5
OUTPUT PROBE
5K
CL
+5
RL
CR1
CR2
CR3
CR4

TC08071S

NOTES:

CR1 – CR4 = IN914
R1 selected for 15:1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
$R_L = 390\Omega$
C_L = 25pF (including stray capacitance)

Voltage Comparator NE/SE529

APPLICATIONS

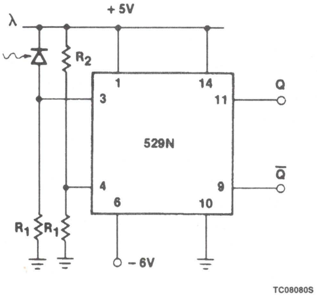
One of the main features of the device is that supply voltages (V+, V−) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V−) should always be at least 6V more than the ground terminal (pin 6). Input Common-Mode range should be limited to values of 2V less than the supply voltages (V+ and V−) up to a maximum of ± 6V as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

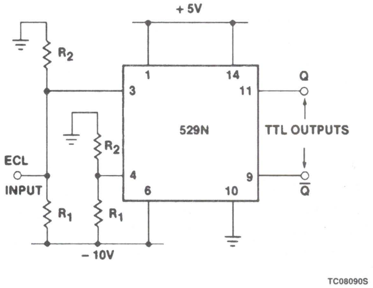
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B
$V_{ID} \leqslant -V_{OS}$	H	X	L	H
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined
$V_{ID} \geqslant V_{OS}$	X	H	H	L
X	L	L	H	H

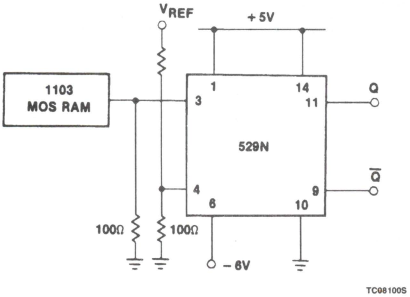
TYPICAL APPLICATIONS


λ
+5V
R2
1
14
3
11
Q
529N
Q̄
4
9
6
10
R1
R1
−6V
TC08080S

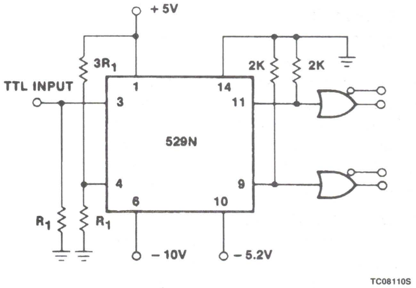
Photodiode Detector


+5V
R2
1
14
3
11
Q
529N
TTL OUTPUTS
R2
ECL
INPUT
4
9
6
10
Q̄
R1
R1
−10V
TC08090S

ECL-to-TTL Interface


VREF
+5V
1103
MOS RAM
1
14
3
11
Q
529N
Q̄
4
9
6
10
100Ω
100Ω
−6V
TC08100S

MOS Memory Sense AMP


+5V
3R1
2K
2K
TTL INPUT
1
14
3
11
529N
4
9
6
10
R1
R1
−10V
−5.2V
TC08110S

TTL-to-ECL Interface

Signetics

Linear Products

AN116

Applications for the NE521/522/527/529

Application Note

COMPARATORS

Voltage comparators are high gain differential input-logic output devices. They are specifically designed for open-loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function. Device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input.

Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example, the circuit of Figure 1 produces a logic 1 level when the non-inverting input is more positive than the reference voltage.

DEFINITIONS

Many similarities exist between operational amplifiers and the amplifier section of voltage comparators. In fact, op amps can be used to implement the comparator function at low frequencies.

Thus, the characteristic definitions presented here are similar to those reviewed for op amps.

Input Offset Voltage

As with operational amplifiers, the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the DC voltage required at the input to force the output to the logic threshold of ensuing devices (1.2V for TTL).

Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Input bias current is the average of the two input currents.

Common-Mode Range

When specifying voltage comparators, one of the key parameters is common-mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions or device degradation. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common-mode signals at threshold. All ranges of input signals thus must be within the common-mode range of the input amplifier.

Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general, higher gains would be advantageous for resolving smaller input signals. Of course, the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000V/V. This gain provides 5V of output swing with 1mV input signal change for reasonable accuracy, but does not contribute severely to the overload recovery delay.

Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the analog signal in the meantime has changed value. At low frequencies the delay is of small consequence, but at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes, as a prime goal, the minimizing of transit times.

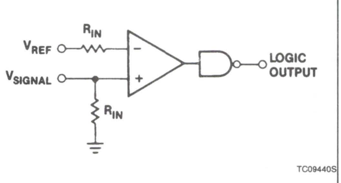


Figure 1. Basic Comparator Circuit

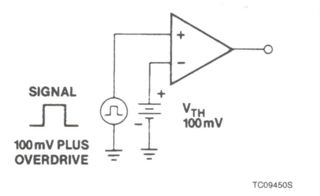


Figure 2. Propagation Delay Test Setup

Propagation delay testing is done under worst-case conditions. The recovery from saturation varies, depending upon the initial state of the amplifier and the overdrive. Worst-case conditions begin by applying a 100mV signal on the reference terminal. With no signal applied, the amplifier is in saturation in one direction. A step input pulse on the signal line of 100mV $\pm V_{OS}$ will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching, a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 2. The input is a step function of 100mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst-case propagation delay. Note that larger overdrive reduces delay time as can be seen in Figure 3. An overdrive of 5mV causes 12ns delay, whereas a 100mV overdrive improves transit time to only 6ns.

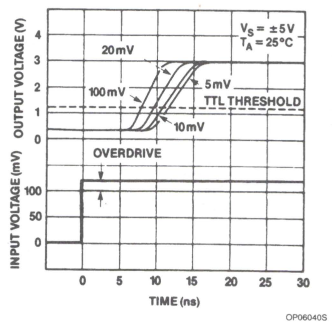


Figure 3. Response Time for NE/SE521 Comparator for Various Input Overdrives

If the measurement were made without initial saturation (less than 100mV/V threshold) the delay time would be less, due to the decreased storage times of unsaturated transistors.

Applications for the NE521/522/527/529 AN116

STATE-OF-THE-ART

Comparator design has always been optimized for four basic parameters. They are:

1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately, these four parameters are not compatible. For instance, gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that older comparators such as the 710 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately, the transistor beta is adversely affected by gold, causing slightly higher bias and offset currents.

It was not until the advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky barrier diode's (SBD) location is illustrated in Figure 4.

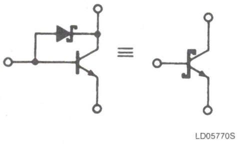


Figure 4. Schottky Clamped Transistor

The Schottky clamped transistor is formed by paralleling the Schottky diode with the base-collector junction of the NPN transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4V — less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction.

The Schottky diode becomes forward-biased when the collector voltage falls 0.4V below the base voltage. Excess base drive is then shunted into the collector circuit, prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

A cross sectional area of the Schottky diode is shown in Figure 5.

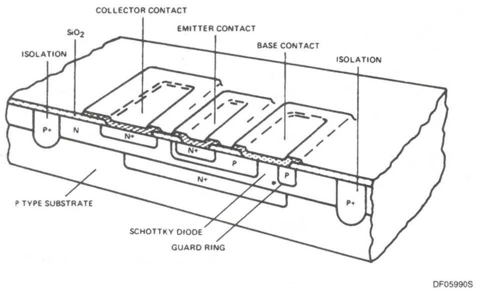


Figure 5. Schottky Clamped Transistor Geometry

DEVICE	PROP DELAY (ns)	V_{OS} (mV)	I_{OS} (μA)	I_{BIAS} (μA)	GAIN	CMR (V)	BENEFITS
NE521	12	7.5	5	20	5000	±3	Dual, very fast, standard supplies TTL compatible, individual & common strobe.
NE522	15	7.5	5	20	5000	±3	Same as NE521 plus open-collector outputs for additional decoding.
NE527	26	6	0.75	2	5000	±6	Fast, very low input current, differential outputs, flexible surplus wide common-mode range.
NE529	22	6	5	20	5000	±6	Same as NE527 but with faster response.
LM311	200	7.5	0.05	0.25	200k	±30	High common-mode input range, ±5V to ±15V supply, strobe input, open-collector output.
LM319	80	8	0.2	1.2	40k	±5	Low input bias, dual, +5V to ±15V supply, open-collector output.
LM339	1300	2	0.05	0.25	200k	V+ −1.5V	High common-mode input range, low input bias, quad, +5V to ±15V supply, open-collector output.
LM393	1300	2	0.05	0.25	200k	V+ −1.5V	Same as LM339 but dual.

NOTE:
Parameters are based on min/max limits at 25°C as defined in the individual data sheet.

Figure 6. Comparator Selection Guide

Applications for the NE521/522/527/529

AN116

COMPARING THE COMPARATORS

Presently available comparator ICs range from the ultra fast SE/NE521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Speed of conversion is often of primary importance to minimize pulse position errors of high frequency signals. At other times the requirements are much less stringent, allowing the use of a general purpose comparator.

A handy reference guide to the major parameters is summarized in Figure 6. The necessary parameters can be chosen to select the proper device.

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.

NE/SE521/522 Comparators

Processed with state-of-the-art Schottky barrier diodes, the NE521/522 series devices provide good input characteristics while providing the fastest analog-to-TTL conversion to date. Total delay from input to output is typically 6ns with a guaranteed speed of 12ns. Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The NE522, although sacrificing some speed, features open-collector outputs for party line or wired-OR configurations for additional system flexibility.

NE/SE527 Comparator

Featuring Darlington inputs for very low bias current, the NE527 is generically related to the NE529 comparator. Emitter-follower inputs to the differential amplifier are used to trade better input parameters for slightly less speed. As Figure 6 shows, a factor of 10 improvement in I_{BIAS} is gained with a propagation delay increase of only 4ns maximum.

NE529 Comparator

The NE529 is manufactured using Schottky technology. Although a few nanoseconds slower than the NE521, the NE529 features variable supplies from ±5 to ±10V with a high common-mode range of ±6V. Both the NE527 and NE529 Schottky comparators boast complementary logic outputs with output A being in phase with input A. In addition, the supplies of both the NE527 and NE529 may be non-symmetrical to produce a desired shift in the common-mode range.

This technique is illustrated by the ECL-to-TTL and TTL-to-ECL transistor of Figures 16 and 17, respectively. The only major requirement of the supplies is that the negative supply be at least 5V more negative than the ground terminal of the gate. This is necessary to insure that the internal bias arrangement has sufficient voltage to operate normally.

APPLICATIONS

Today's state-of-the-art ultra high-speed comparators are capable of making logic decisions in less than 10ns. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs, however, some preliminary steps should be taken in their use.

GENERAL PRECAUTIONS

Layout

The comparator is capable of resolving sub-millivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high-speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies, hidden signal paths become dominant. Distributed capacitance is a particular nuisance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.

Another source of spurious signals is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, ringing, or excessive V_{OS}. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

Power Supplies

Another general precaution that should always be exercised is power supply bypassing. As mentioned, the name of the game is speed. Very high-speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason, good power supply bypassing very close to the device itself is always mandatory. A tantalum capacitor of 1 to 10μF in parallel with 500 to 1000pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

Unused Inputs

Some currently available comparators such as the NE521 and NE522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain-bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100mV to insure the comparator assumes a known state.

If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

If the strobe inputs are not used, they should be connected to the output of a logic gate that is always high, or to the +5V supply through a 5 to 10kΩ resistor. They should never be tied directly to the +5V supply as the relatively minor spiking on the supply may damage these inputs.

Common-Mode Signals

Manufacturers specify the maximum voltage range over which the inputs may be taken. In addition, the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the NE529 comparator, the differential voltage is restricted to less than ±5V, with a common-mode of ±6V. That these two quantities interact cannot be overlooked. For instance, with both inputs at ±4V the common-mode restriction is satisfied. If V_{REF} is now left at +4V the signal input may not be taken more than 1V below ground because the differential signal becomes 5V.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

It is also important to note that response time is specified for a common-mode voltage of zero and may degrade when the common-mode voltage approaches the common-mode specification limits.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

Applications for the NE521/522/527/529

BASIC APPLICATIONS

The basic comparator circuit and its transfer function were presented by Figure 1.

When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A-to-D converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic circuit. Both are only a small deviation from the basic level detector.

Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.

They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore, if the compared voltages remain at or near the threshold for long periods of time, the comparator may oscillate or respond to noise pulses. For instance, this is a common problem with successive approximation D/A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 7 defines the arrangement. Both positive and negative feedback is provided by R_{IN} and R_F.

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 8, prevents output chatter with signals having slow and erratic zero crossings.

As shown in Figure 7, the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_F}$$

where E_{OUT} is the gate high output voltage.

The hysteresis voltage is bounded by the common-mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired, an additional inverting gate is required if the comparator does not have differential outputs. The NE527 and NE529 devices provide inverted signals from differential outputs while the NE521 and NE522 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum, especially for very high-speed comparators such as the NE521.

Line Receiver

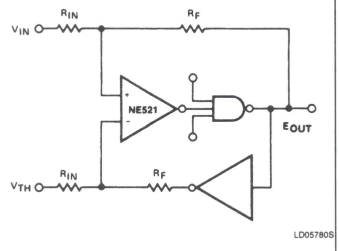
Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted-pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common-mode signal, the very high common-mode rejection of the NE521/522 makes the unit ideal for differential line receivers. Figure 9 depicts the simple schematic arrangement. The NE521 is used as a differential amplifier having a logic level output. Because common-mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 10 illustrates the NE521 response to the 200mV$_{P-P}$ 10MHz differential signal. In Figure 11 the same signal has been buried in 5V$_{P-P}$ of 1HMz common-mode "noise."

The circuit suffers no degradation of signal. If desired, several NE522 comparators may be "wire-ORed," or a latched output can be built as shown in Figure 9.

The NE521 and NE529 comparators have the advantage of wider bandwidth to permit higher data rates.



NOTE: $V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_F}$

Figure 7. Level Detector With Hysteresis

Double-Ended Limit (Window) Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single NE522 package. The schematic and transfer curve of the circuit is shown in Figure 12.

Each half of the NE522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open-collectors of the NE522 minimizes external components and connections.

Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The NE521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 13 shows a typical oscillator circuit.

The crystal is operated in its series-resonant mode, providing the necessary feedback through the capacitor to the input of the NE521. The resistor R_{ADJ} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The NE521 will oscillate up to 70MHz. However, crystals with frequencies higher than about 20MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out, the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using input and output mode suppression or tuning. The NE522 is especially desirable since the open-collector topology allows the output to be collector-tuned readily.

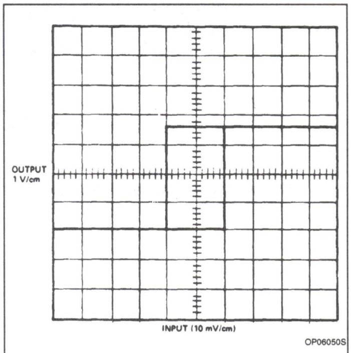
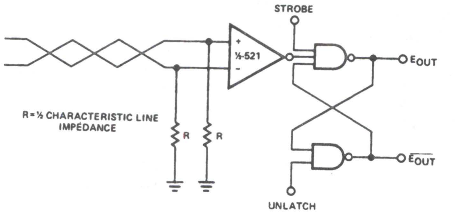
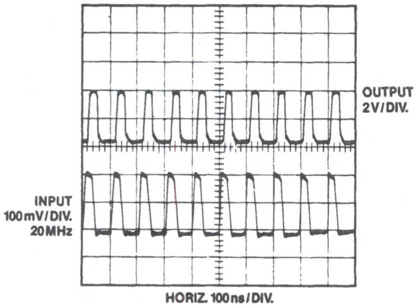


Figure 8. 0V Level Detector With ± 10mV Hysteresis


STROBE
½-521
+
-
EOUT
$\overline{E_{OUT}}$
R = ½ CHARACTERISTIC LINE IMPEDANCE
R
R
UNLATCH

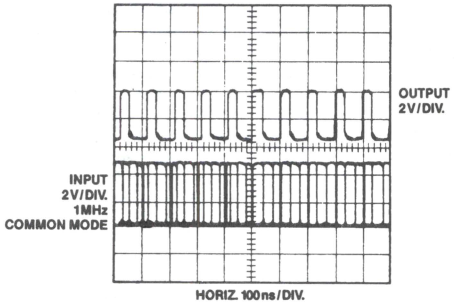
TC09460S

Figure 9. Line Receiver



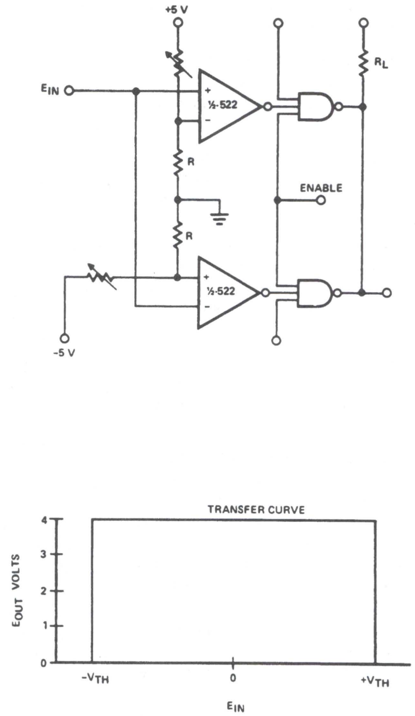
OP06060S

Figure 10. Line Receiver Response



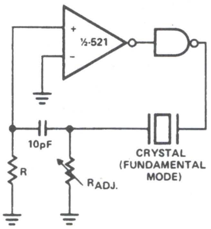
OP06070S

Figure 11. Response During Common-Mode Noise


+5 V
EIN
+
-
½-522
R
R
RL
ENABLE
½-522
-5 V
TRANSFER CURVE
EOUT VOLTS
4
3
2
1
0
-VTH
0
+VTH
EIN

LD05790S

Figure 12. Double-Ended Limit Detector


+
-
½-521
10pF
R
RADJ.
CRYSTAL (FUNDAMENTAL MODE)

TC09470S

Figure 13. Crystal Oscillator

Applications for the NE521/522/527/529 AN116

Analog-to-Digital Converter

There are many types of A-to-D converter designs, each having its own merits. However, where speed of conversion is of prime interest, the multi-threshold conversion type is used exclusively. It is apparent from Figure 14 that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N-bit converter is 2n-1. Although the NE521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3-bit parallel A/D converter is shown in Figure 15 with a 3-bit digital equivalent of an analog input shown in Figure 14.

Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of ± ½ bit.

It is apparent from the schematic that the individual strobe line and duality features of the NE521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 14. All 3-bit outputs have settled and are true a mere 15ns after the input step of 3V has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

Logic Interface

During the design of the NE527 and NE529 devices, particular attention was paid to the biasing network so that balanced supplies need not be provided. For example, if the "ground" terminal is set at −5.2V and the other supplies are adjusted accordingly, the output logic 1 state will be at −1.5V and logic 0 will be at −5.0V. With this freedom of power supply voltage, the user may adjust the output swings to match the desired logic levels even if that logic is other than TTL levels.

ECL-to-TTL Interface

Emitter-coupled logic is very popular due to its speed. Systems are often built around standard TTL logic with those portions requiring higher speed being implemented with emitter-coupled logic. As soon as such a decision is made the problem of interfacing TTL-to-ECL logic levels is encountered.

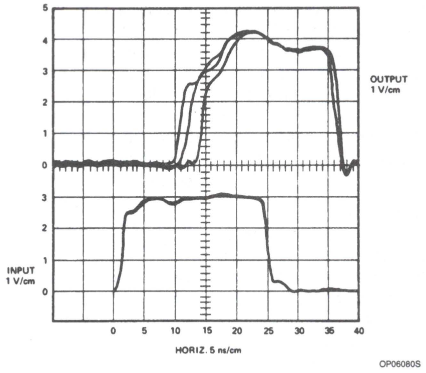


Figure 14. Parallel A/D Response

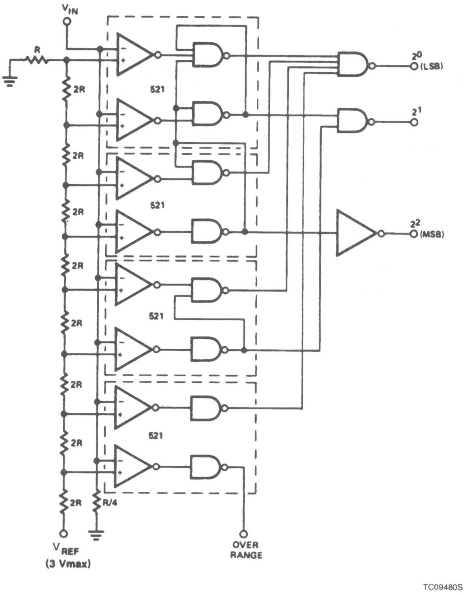


Figure 15. 3-Bit Parallel A/D Converter

The standard logic output swings of ECL are −0.8V to −1.8V at room temperature. Converting these signals to TTL levels is accomplished simply by using the basic voltage comparator circuit with slight modifications. Figure 16 reveals that the power supplies have been shifted in order to shift the common-mode range more negative. This insures that the common-mode range is not exceeded by the logic inputs. Since ECL is extremely fast, the NE529 is usually selected because of its superior speed so that a minimum of time is lost in translation.

TTL-to-ECL INTERFACE

Operating in the reverse, TTL levels can also be converted to ECL levels by the NE529. Again the NE529 is selected as the fastest converter with the necessary power supply flexibility to accomplish the level shifting with a minimum of effort and cost.

A check of output voltage for the NE529 reveals that the voltage is slightly less than required by the ECL logic for fast switching. R2 and the diode of Figure 17 raises the gate supply voltage and therefore the NE529 output voltage by 0.7, sufficient to guarantee fast switching of the translator. Resistive pull-up from the NE529 output to V_{CC} can also be used with the gate supply grounded. This method is dependent upon RC time constants of distributed capacitance and is therefore much slower.

Photo Diode Detector

Responding to the presence or absence of light, the photo diode increases or decreases the current through it. Detecting the changes becomes a matter of converting light and dark currents to voltage across a resistor as shown in Figure 18. R1 is selected to be large enough to generate detectable differences between light and dark conditions. Once the signal levels are defined by R1 and the diode characteristics, the average between light and dark signals is used for V reference and is produced by the resistive divider consisting of R1 and R2. The comparator then produces an output dependent upon the presence or absence of light upon the diode.

SENSE AMPLIFIERS

Closely related to the comparator is the sense amplifier. Signals derived from the many sources, such as transducers, are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

Some transducers produce an output current. It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice, resistors larger than 1kΩ are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. Signetics comparators NE521 and NE522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.

Design of the sense amplifier network depends upon the transducer used and the input characteristics of the sense amplifier. The significant specifications are given in Table 1.

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

$$V_{REF} \leqslant (I_T - I_B)R1 - V_{DIFF}$$

Where I_T is the transducer output current, I_B is sense amplifier bias current and V_{DIFF} is minimum differential voltage to switch the sense amplifier.

In large systems, noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines as short as possible will help, but will not always be sufficient. One method of eliminating noise is to use a balance sense line as shown in Figure 19.

A dummy line should be run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the V_{REF} point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common-mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp, causing the output to switch.

Table 1. Important Sense Amplifier Parameters

DEVICE	V_{OS} (mV)	I_B (μA)	$V_{IN\ (MIN)}$ (mV)	SPEED (ns) (V_{IN} = 100mV)	GAIN
521	10	40	15	12	5000
522	10	40	15	15	5000

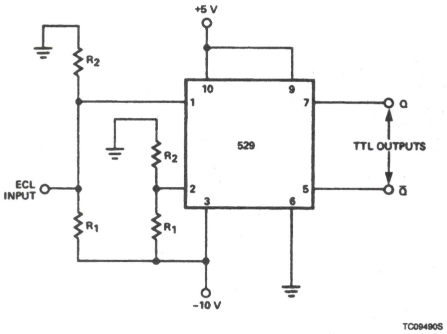

+5 V
R2
10
9
1
7
Q
529
TTL OUTPUTS
R2
ECL INPUT
2
5
3
6
Q̄
R1
R1
−10 V
TC09490S

Figure 16. ECL-to-TTL Translator

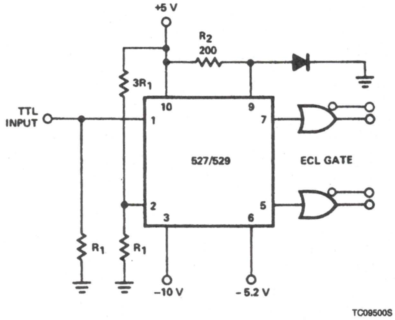

+5 V
R2
200
3R1
TTL INPUT
10
9
1
7
527/529
ECL GATE
2
5
3
6
R1
R1
−10 V
− 5.2 V
TC09500S

Figure 17. TTL-to-ECL Translator

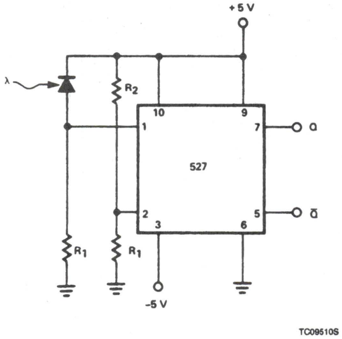

+5 V
λ
R2
10
9
1
7
Q
527
2
5
Q̄
3
6
R1
R1
−5 V
TC09510S

Figure 18. Photo Diode Detector

Applications for the NE521/522/527/529

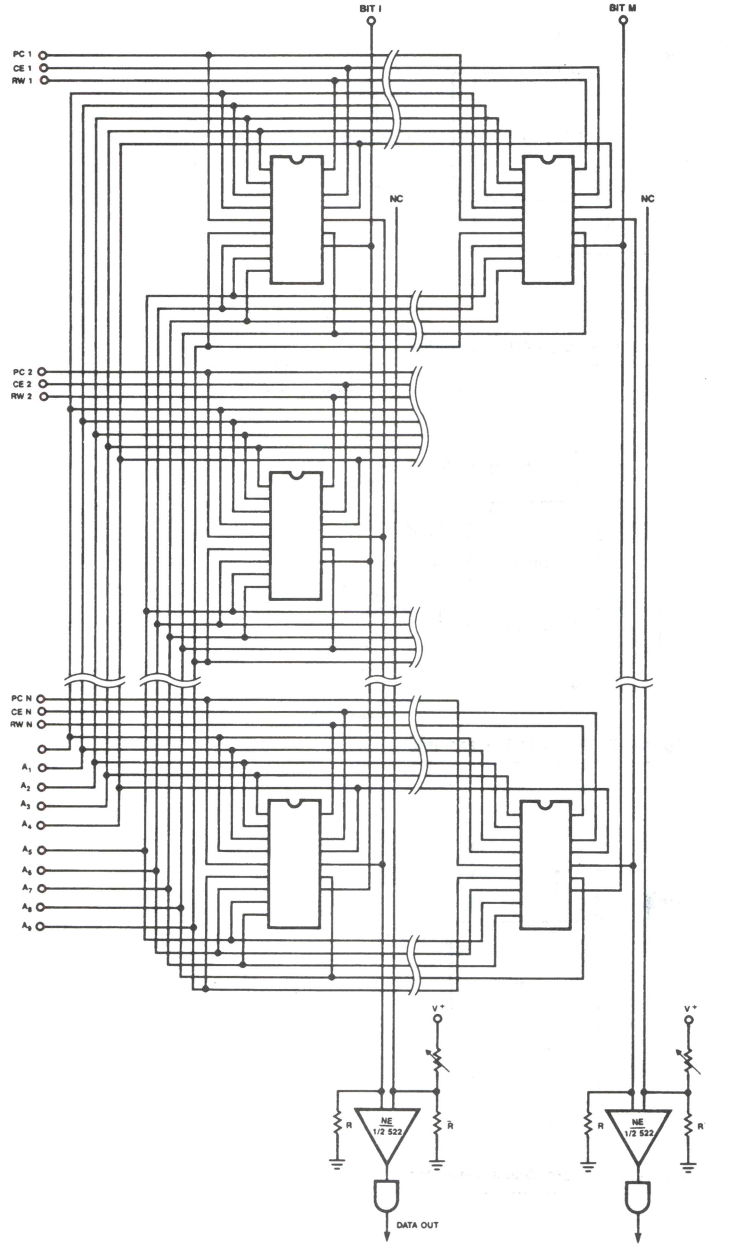

BIT I
BIT M
PC 1
CE 1
RW 1
NC
NC
PC 2
CE 2
RW 2
PC N
CE N
RW N
A₁
A₂
A₃
A₄
A₅
A₆
A₇
A₈
A₉
V⁺
V⁺
R
NE
1/2 522
R̄
R
NE
1/2 522
R
DATA OUT
TC09520S

Figure 19. Balanced Sense Line to Reduce Noise

Signetics

Symbols and Definitions for Sample-and-Hold Circuits

Linear Products

Acquisition Time (t_{AQ})

The time delay between the 50% (or threshold) point of the hold-to-sample transition of the sample/hold signal and the point at which the output voltage begins to track the input voltage to within a specified error band. By convention the acquisition time is defined for sampling a positive (or negative) full-scale input voltage after previously holding a negative (or positive) full-scale output voltage.

Aperture Delay (t_{APD})

The time delay between the 50% (or threshold) point of the sample-to-hold transition of the sample/hold signal and the instant at which the switch is just opening. This latter instant can be defined as the time at which the internal control voltage across the switch element has moved by 10% of its full voltage swing, i.e., the instant at which the switch is 10% open.

Aperture Time (t_{AP})

The time required for the sample-and-hold switch to open. The switch opening time can be defined as the interval between the conditions of 10% open and 90% open and does not include any delays of the sample/hold signal through the switch buffer circuitry.

Aperture Uncertainty (t_{APU})

The range of variation of total aperture delay time (see definition below) due to internal circuit noise of all forms.

Charge Transfer (Q_T)

The amount of charge transferred to the holding capacitor (when switching from the sample-to-hold mode) originating from stray or parasitic capacitance associated with the sample-and-hold switch. Charge transfer is directly related to hold step (see definition below) by the following relationship:

$$V_{HS}(V) = \text{Charge transfer}(pC)/C_H(pF)$$

where V_{HS} is the hold step and C_H is the holding capacitor. It can be seen that increasing C_H will reduce V_{HS}, since the charge transfer is constant for a given circuit.

Input Resistance (R_{IN})

The large-signal input resistance over the specified input voltage range.

Droop Rate (dV_H/dt)

The rate of change of output voltage while the circuit is in the hold mode. It is due to leakage currents to, or from, the holding capacitor and can be positive or negative. It is related to the droop current, I_D (defined below), by the following relationship;

$$dV_H/dt = I_D(pA)/C_H(pF)$$

Droop Current (I_D)

The current flowing *into* the C_H terminal when the circuit is in the hold mode.

Effective Aperture Delay Time (t_{EAPD})

The difference between the propagation time of the analog input voltage to the sample-and-hold switch and the aperture delay (t_{APD}). The value of t_{EAPD} may be positive, negative or zero. For precise timing of the point on the input voltage to be held, the sample-to-hold transition of the sample/hold signal must be advanced by t_{EAPD}.

Full Power Bandwidth (f_P)

The maximum frequency at which the full-scale output voltage can be achieved without significant distortion. The full power bandwidth is related to the slew rate, SR (defined below) by the following relationship;

$$F_P = SR/2\pi V_{CC}$$

where V_{CC} is the peak value of the input signal; i.e., $V_{IN} = V_{CC}\sin(2\pi F_P t)$.

Gain Error

In a unity gain configuration this is the ratio of the difference between the input and output voltages to the input voltage expressed as a percentage.

Hold Mode Feedthrough

A measure of the amount of an input sinusoidal voltage that appears at the output of a sample-and-hold circuit when it is in the hold mode. It is usually expressed as a percentage or as an output RMS voltage for a specified input RMS voltage.

Hold Mode Settling Time (t_{HM})

The time delay between the 50% (or threshold) point of the sample-to-hold transition of the sample/hold signal and the point at which the output settles to within a specified error band of its final value before hold mode droop becomes significant.

Hold Step (V_{HS})

The step in the output voltage caused by charge transfer (defined above).

Input Bias Current (I_{BIAS})

The bias current *into* the input terminal.

Linearity Error (E_L)

The maximum deviation of the output voltage from an ideal straight line drawn between the two output voltages corresponding to the extremes of the input voltage range. It is usually expressed as a percentage of the full-scale input voltage range.

Output Resistance (R_O)

The ratio of the change in output voltage to a change in output load current in either the hold mode or for a fixed input voltage in the sample mode.

Overshoot

The maximum overshoot of the output voltage, in the sample mode, when slewing at its maximum rate over the full-scale output voltage range. It is usually expressed as a percentage of the full-scale output voltage range.

Power Supply Rejection Ratio (PSRR)

The ratio of the change in power supply voltage (over a specified power supply voltage range ΔPSV) to the corresponding change in zero-scale error, V_{ZS} (defined below); it is expressed in dB where $PSRR(dB) = 20\log(\Delta PSV/\Delta V_{ZS})$.

Slew Rate (SR)

The maximum possible rate of change of the output voltage, in the sample mode, when changing over the full-scale output voltage range.

Total Aperture Delay Time (t_{TAPD})

The sum of the aperture delay and the aperture time.

$$t_{TAPD} = t_{APD} + t_{AP}$$

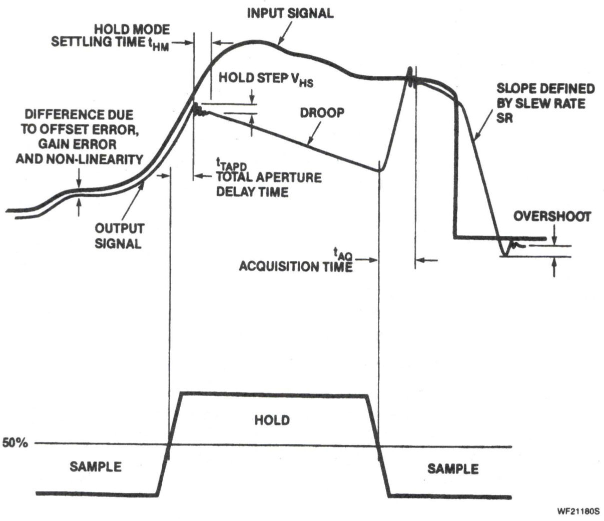
Voltage Gain (A_V)

The ratio of the output voltage to the input voltage when operating in the sample mode and over a specified input voltage range.

Zero-Scale Error (V_{ZS}) or Input Offset Voltage (V_{OS})

The difference between the output and input voltages when operating in the sample mode and in a unity gain configuration.

Symbols and Definitions for Sample-and-Hold Circuits


INPUT SIGNAL
HOLD MODE SETTLING TIME t_{HM}
HOLD STEP V_{HS}
DROOP
SLOPE DEFINED BY SLEW RATE SR
DIFFERENCE DUE TO OFFSET ERROR, GAIN ERROR AND NON-LINEARITY
t_{TAPD} TOTAL APERTURE DELAY TIME
OUTPUT SIGNAL
OVERSHOOT
t_{AQ} ACQUISITION TIME
HOLD
50%
SAMPLE
SAMPLE
WF21180S

Signetics

LF198/LF298/LF398

Sample-and-Hold Amplifiers

Product Specification

Linear Products

DESCRIPTION

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize high-voltage ion-implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS; differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in an 8-lead TO-5 package, or an 8-pin plastic DIP.

FEATURES

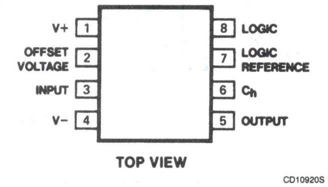
- **Operates from ±5V to ±18V supplies**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_H = 0.01\mu F$**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

APPLICATION

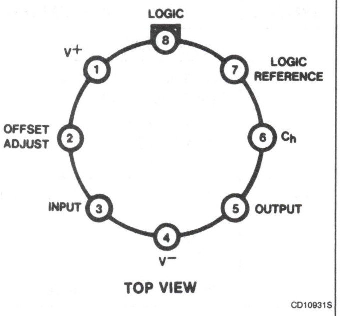
- **The LF198/LF298/LF398 are ideally suited for a wide variety of sample-and-hold applications, including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup**

PIN CONFIGURATIONS

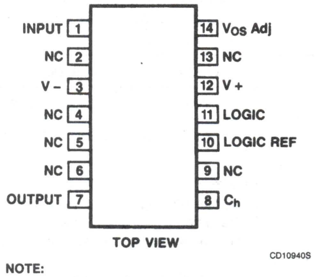
FE, N Packages



H Package



D Package[1]



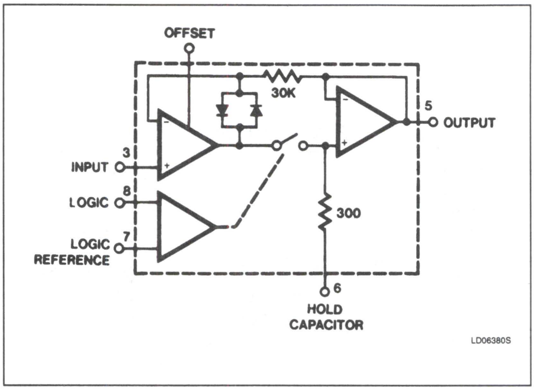
NOTE:
1. SO and non-standard pinouts.

ORDERING INFORMATION

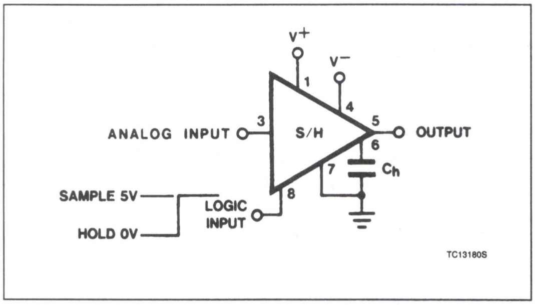
DESCRIPTION	TEMPERATURE	ORDER CODE
8-Pin Cerdip	−55°C to +125°C	LF198FE
8-Pin Metal Can	−55°C to +125°C	LF198H
14-Pin Plastic SO Package	0 to +70°C	LF398D
8-Pin Cerdip	0 to +70°C	LF398FE
8-Pin Metal Can	0 to +70°C	LF398H
8-Pin Plastic DIP	0 to +70°C	LF398N
8-Pin Cerdip	−25°C to +85°C	LF298FE
8-Pin Metal Can	−25°C to +85°C	LF298H

Sample-and-Hold Amplifiers LF198/LF298/LF398

FUNCTIONAL DIAGRAM


OFFSET
30K
5
OUTPUT
3
INPUT
8
LOGIC
7
LOGIC
REFERENCE
300
6
HOLD
CAPACITOR
LD06380S

TYPICAL APPLICATIONS


V+
V−
1
4
3
ANALOG INPUT
S/H
5
OUTPUT
6
7
Ch
SAMPLE 5V
HOLD 0V
LOGIC
INPUT
8
TC13180S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
	Maximum power dissipation $T_A = 25°C$ (still-air)[3]		
	F package	780	mW
	N package	1160	mW
	D package	1040	mW
T_A	Operating ambient temperature range		
	LF198	−55 to +125	°C
	LF298	−25 to +85	°C
	LF398	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic-to-logic reference differential voltage[2]	+7, −30	V
	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	10	sec
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the packages must be derated based on the thermal resistance specified.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply: unit is in "sample" mode; $V_S = \pm 15V$; $T_J = 25°C$; $-11.5V \leqslant V_{IN} \leqslant +11.5V$; $C_H = 0.01\mu F$; and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

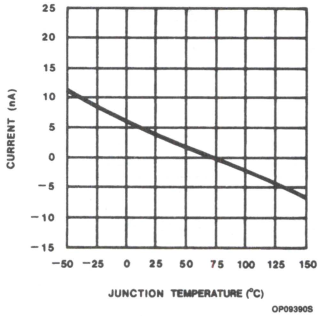
SYMBOL	PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	$T_J = 25°C$		1	3 5		2	7 10	mV mV
I_{BIAS}	Input bias current[4]	$T_J = 25°C$ Full temperature range		5	25 75		10	50 100	nA nA
	Input impedance	$T_J = 25°C$		10^{10}			10^{10}		Ω
	Gain error	$T_J = 25°C$, $R_L = 10k$ Full temperature range		0.002	0.005 0.02		0.004	0.01 0.02	% %
	Feedthrough attenuation ratio at 1kHz	$T_J = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
	Output impedance	$T_J = 25°C$, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω Ω
	"HOLD" step[2]	$T_J = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_J \leqslant 25°C$		4.5	5.5		4.5	6.5	mA
	Logic and logic reference input current	$T_J = 25°C$		2	10		2	10	μA
	Leakage current into hold capacitor[4]	$T_J = 25°C$[3], "HOLD" mode		30	100		30	200	pA
t_{AC}	Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4 20			4 20		μs μs
	Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
	Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
	Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

1. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_J = 25°C$, $-11.5V \leqslant V_{IN} \leqslant +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. The parameters are guaranteed over a supply voltage of ±5 to ±18V.

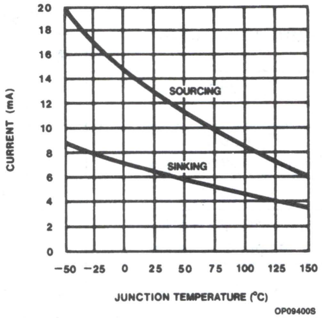
TYPICAL DC PERFORMANCE CHARACTERISTICS

Input Bias Current



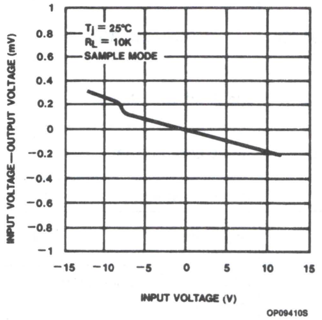
OP09390S

Output Short Circuit Current



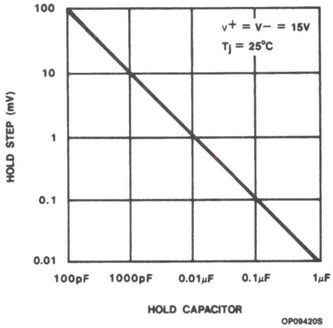
OP09400S

Gain Error



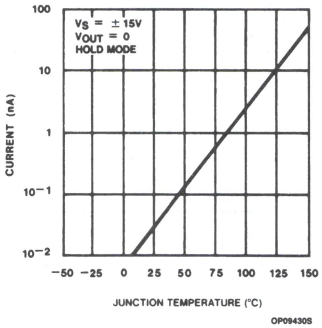
OP09410S

Hold Step



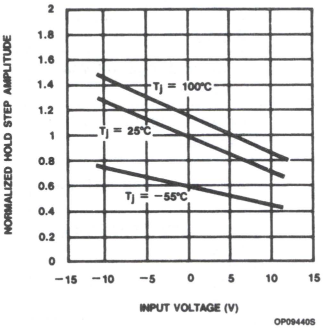
OP09420S

Leakage Current Into Hold Capacitor



OP09430S

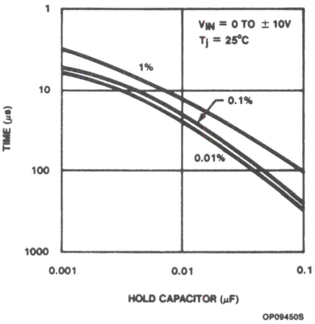
Hold Step Input Voltage



OP09440S

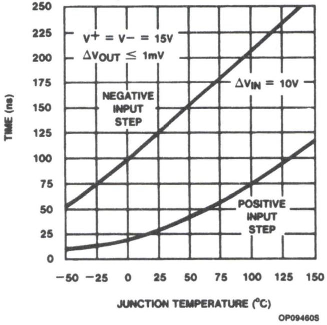
TYPICAL AC PERFORMANCE CHARACTERISTICS

Acquisition Time



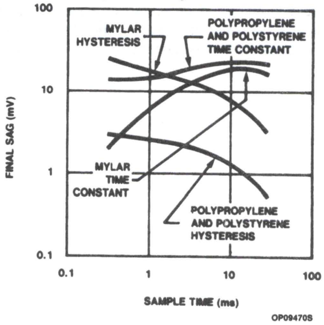
OP09450S

Aperture Time



OP09460S

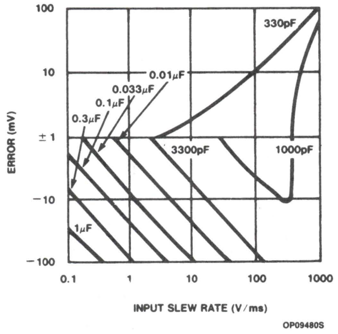
Capacitor Hysteresis



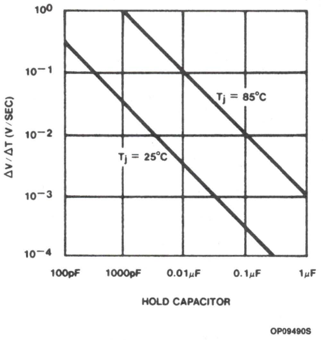
OP09470S

TYPICAL AC PERFORMANCE CHARACTERISTICS (Continued)

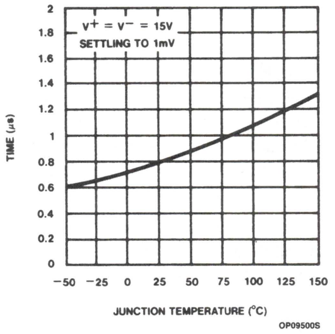
Dynamic Sampling Error



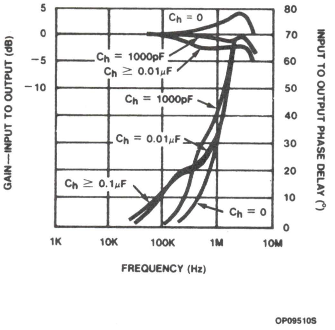
Output Droop Rate



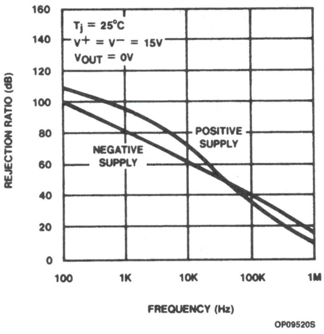
'Hold' Settling Time



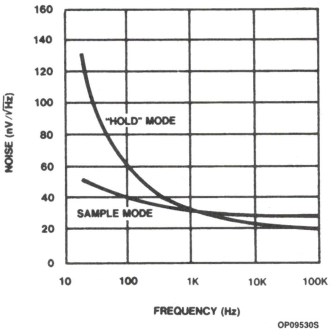
Phase And Gain (Input to Output, Small-Signal)



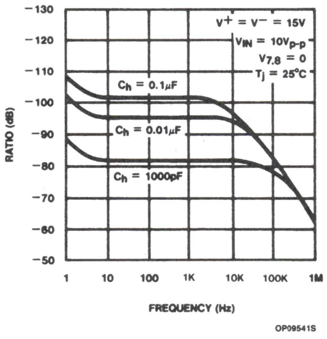
Power Supply Rejection



Output Noise



Feedthrough Rejection Ratio (Hold Mode)



Signetics

Linear Products

NE/SE5060

Precision High-Speed Sample-and-Hold Amplifier

Objective Specification

DESCRIPTION

The NE/SE5060 is a high-performance, monolithic sample-and-hold amplifier that features high accuracy, low droop rate, and fast acquisition times required in high-speed data acquisition systems.

The circuit consists of two high impedance buffer amplifiers connected by an analog switch. In the sample mode, the device is in a non-inverting unity-gain configuration. The switch (S2) (see Block Diagram) is implemented as a unique switchable output stage of the input buffer which has been optimized for fast charging of the hold capacitor and a low sample-to-hold step size. In the hold mode, the input signal is effectively disconnected from the circuit by switch S1 to give a low feedthrough, and GM2 maintains 0V across the switch S2, ensuring a low droop rate. The device includes a 100pF hold capacitor. If lower droop rates and smaller sample-to-hold step error is desired at the expense of acquisition time, additional hold capacitance may be added externally. The voltage at the hold capacitor is buffered by the output buffer amplifier to drive the external load.

The device utilizes high voltage ion-implanted JFETs to obtain the low droop rates. The circuit has been designed to minimize the initial zero offset error, which is trimmed at the wafer level to be less than 0.5mV. The NE5060 operates from ±9V to ±17V power supplies.

FEATURES

- **Voltage gain 0.99970**
- **Low signal non-linearity 0.0035%**
- **Low offset error 0.5mV**
- **Fast acquisition time 850ns**
- **Low sample-to-hold step 1mV**
- **Low droop rate 0.08μV/μs**
  - **+25°C (SE/NE5060) 0.08μV/μs**
  - **+70°C (NE5060) 2.0μV/μs**
  - **+125°C (SE5060) 150.0μV/μs**
- **Internal 100pF hold capacitor**
- **TTL CMOS Logic compatible**
- **Functional equivalent replacement for HA2420, HA2425, HA5320, AD583 and SMP11**

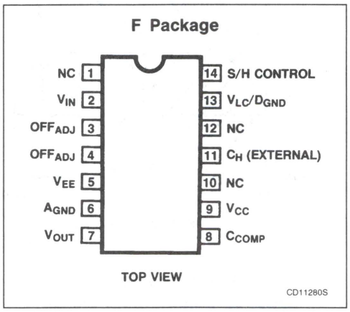
APPLICATIONS

- **Precision data acquisition systems**
- **D/A converter deglitching**
- **Auto-zero circuits**
- **Peak detectors**

ORDERING INFORMATION

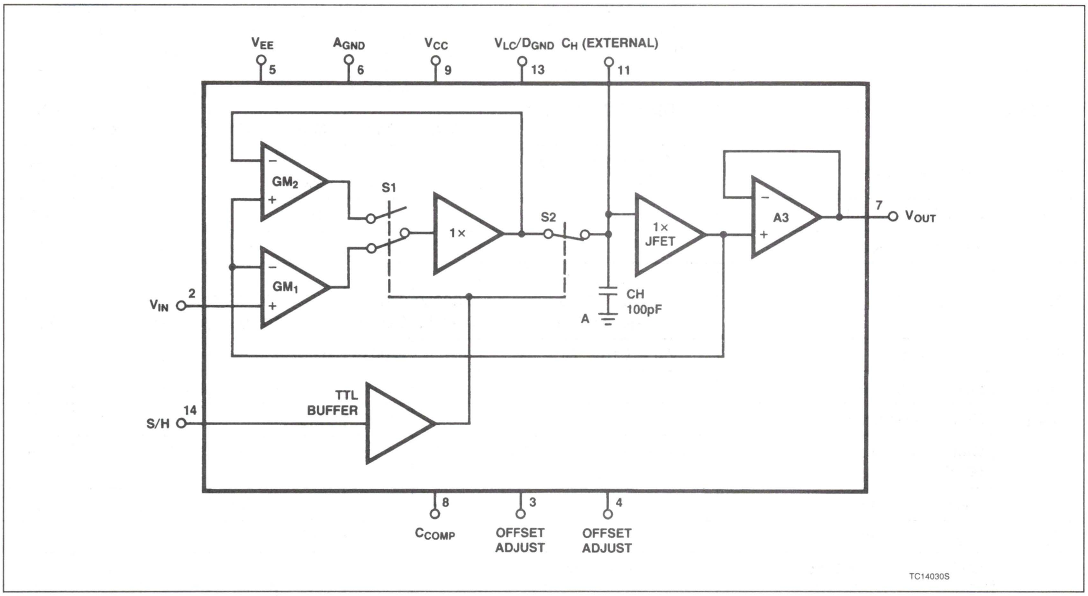
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Hermetic Cerdip	0 to +70°C	NE5060F
14-Pin Hermetic Cerdip	-55°C to +125°C	SE5060F

PIN CONFIGURATION



Precision High-Speed NE/SE5060

BLOCK DIAGRAM


VEE
5
AGND
6
VCC
9
VLC/DGND
13
CH (EXTERNAL)
11
GM2
GM1
S1
S2
1×
1×
JFET
A3
7
VOUT
VIN
2
CH
100pF
A
TTL
BUFFER
S/H
14
8
CCOMP
3
OFFSET
ADJUST
4
OFFSET
ADJUST
TC14030S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Voltage between V_{CC} and V_{EE}	±36	V
V_{IN}	Analog input voltage	±15	V
$V_{S/H}$	Logic input voltage	±15	V
V_{LC}	Logic reference voltage	±15	V
I_{SC}	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	60	Sec
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1] F package	1190	mW
T_A	Operating temperature range NE5060 SE5060	0 to +70 −55 to +125	°C °C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

Test conditions, unless otherwise noted: V_{CC} = 15V; V_{EE} = −15V; −10V ⩽ V_{IN} ⩽ 10V; V_{LC} = 0V; $V_{S/H}$ < 0.8V (for sample mode); $V_{S/H}$ > 2.0V (for hold mode); C_H = Internal; device in sample mode; 0°C ⩽ T_A ⩽ +70°C for NE5060; −55°C ⩽ T_A ⩽ +125°C for SE5060.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5060			SE5060			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{ZS}	Zero-scale error	V_{IN} = 0V; T_A = 25°C		0.5			0.5	5.0	mV
		T_{MIN} to T_{MAX}		1.0	2.0		3.0	5.0	mV
I_{BIAS}	Input bias current	V_{IN} = 0V		70	150		70	150	nA
R_{IN}	Input resistance		150	250		150	250		MΩ
A_V	Voltage gain	V_{IN} = ±10V							
		T_A = 25°C	0.99960	0.99975		0.99960	0.99975		V/V
		T_{MIN} to T_{MAX}	0.99950	0.99965		0.99940	0.99955		V/V
E_L	Linearity error	V_{IN} = ±10V, R_L = 5k		0.0035	0.007		0.0035	0.007	%
V_{INR}	Input voltage range		±10.5	±11		±10.5	±11		V
R_{OUT}	Output resistance			0.15	0.5		0.15	0.5	Ω
I_{LOAD}	Output load current (@ R_O < 0.5Ω)	V_{IN} = ±10V; T_A = 25°C	±10	±15		±10	±15		mA
		T_{MIN} to T_{MAX}	±8	±11		±7	±11		mA
V_{IH}	Logic "1" voltage		2.0			2.0			V
V_{IL}	Logic "0" voltage				0.8			0.8	V
I_{IH}	Logic input current high	$V_{S/H}$ = 5V			0.1			0.1	μA
I_{IL}	Logic input current low	$V_{S/H}$ = 0V			−15			−15	μA
$E_{N\ RMS}$	Output noise	DC to 260kHz		250			250		μV
V_{CC}	Positive supply voltage		13.5	15	16.5	13.5	15	16.5	V
V_{EE}	Negative supply		−13.5	−15	−16.5	−13.5	−15	−16.5	V
I_{CC}	Positive supply current			11.5	14		11.5	14	mA
I_{EE}	Negative supply current			−11.5	−14		−11.5	−14	mA
PSRR+	Positive supply rejection ratio	V_{CC} = 15V ±5%							dB
		V_{IN} = 0V	85	100		85	100		dB
		V_{IN} = ±10V	80	90		80	90		dB
PSRR−	Negative supply rejection ratio	V_{EE} = −15V ±5%							
		V_{IN} = 0V	65	72		65	72		dB
		V_{IN} = ±10V	57	63		57	63		dB

AC ELECTRICAL CHARACTERISTICS Test conditions, unless otherwise specified:
$V_{CC} = 15V$; $V_{EE} = -15V$; $V_{IN} = 0V$; $V_{LC} = 0V$; $R_L = 2k\Omega$; $C_L = 50pF$; C_H = Internal;
$V_{S/H} = 0.4V$ (for sample mode); $V_{S/H} = 3.5V$ (for hold mode); $T_A = +25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
SR	Slew rate[1]		16	20		V/µs
	Overshoot[1]			6		%
BW	Full power bandwidth	$V_{IN} = 20V_{P\text{-}P}$		260		kHz
t_{AQ}	Acquisition time,[1, 2]			850	1250	ns
t_{APD}	Aperture delay			30		ns
t_{AP}	Aperture time			25		ns
t_{APU}	Aperture uncertainty			1		ns
V_{HT}	Sample – Hold transient (peak to peak)[3]			5	15	mV
t_{HM}	Hold mode settling[2, 3]			75	125	ns
Q_t	Charge transfer[3]			0.1	0.25	pC
	Hold step[3, 4]			1.0	2.5	mV
	$T_A = +25°C$		0.08	0.2	µV/µs	
dV_H/dt	Droop rate	0°C to +70°C		1.0	2.0	µV/µs
		-55°C to +125°C		100	160	µV/µs
I_D	Droop current	$T_A = +25°C$		8	20	pA
		0°C to +70°C		100	200	pA
		-55°C to +125°C		10	20	nA
	Hold mode feedthrough	$V_{IN} = 10V_{P\text{-}P}$; 100kHz		2		mV

NOTES:
1. $V_{IN} = \pm 10V$ step.
2. To within 1.0mV of its final value (0.01%).
3. $V_{S/H\ (HIGH)} = 3.5V$; $t_R = 50ns$ (V_{IL} to V_{IH}).
4. Can be adjusted to zero.

APPLYING THE NE/SE5060

The NE/SE5060 is a high-performance sample-and-hold amplifier. In the track mode the device behaves as a non-inverting unity gain amplifier. In the hold mode the device holds the value of the output voltage that was present at the instant the sample-to-hold signal goes high.

Hold Capacitor

The NE/SE5060 includes an on-chip hold capacitor and achieves fast acquisition, low hold step, and droop rate which are adequate for most high-speed applications. However, if a smaller hold step and lower droop rate are desired, then an external hold capacitor (C_H) may be added from Pin 11 to ground (Pin 6). The external hold capacitor should have high insulation resistance and low dielectric absorption to minimize droop errors.

If an external hold capacitor is used, then additional compensation capacitance of value $0.03C_H$ should be connected between Pin 8 and ground. Exact value and type are not critical. The additional hold capacitor will reduce the slew rate and increase acquisition time.

Offset Adjustment

The NE/SE5060 hold step error can be adjusted to zero using the offset adjustment pins as shown in the 'Typical Connections'. The error should be adjusted with the device in the hold mode, so that both the initial offset error and the hold-step error are nulled to zero. If desired, the center-tap of the offset adjustment potentiometer may be connected to V_{CC} through a 1MΩ resistor in series with the center-tap of the potentiometer.

Layout and Other Considerations

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01μF to 0.1μF ceramic) should be provided for each power supply terminal to Pin 6 as close to the device as possible.

The ideal ground connections are as follows:

- a wide trace between Pin 6 and Pin 13
- Pin 6 to each power supply ground
- a separate trace from Pin 6 to the signal ground
- Pin 13 to digital ground.

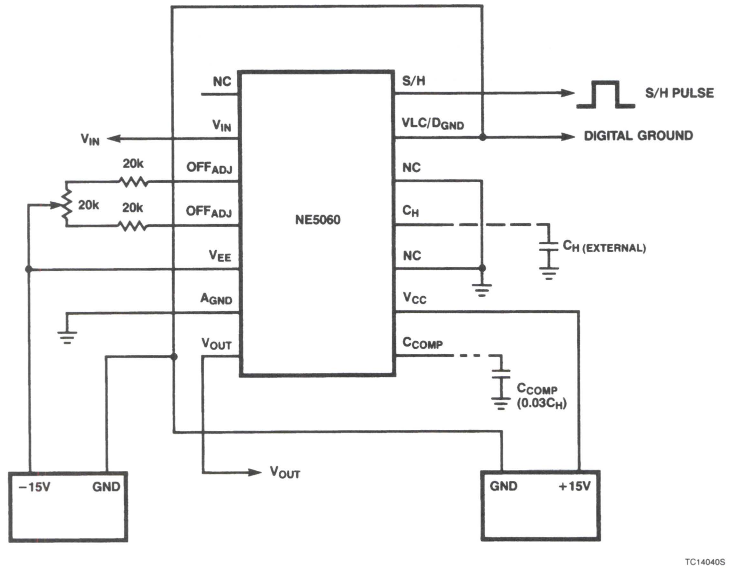
The hold capacitor (Pin 11) is sensitive to stray coupling. Any connection made to this pin should be kept short and guarded by a ground plane since nearby signal lines or power supply voltages will introduce errors in the hold mode.

In unity gain applications requiring no external hold capacitor, the NE/SE5060 can directly replace the HA2420, HA2425, and HA5320. In applications requiring an additional hold capacitor, it should be remembered that the capacitor should be connected from Pin 11 to ground.

Sample/Hold Input

Optimum performance is achieved with a clean (no ringing) sample-to-hold pulse with a rise time between 20ns and 50ns.

NE/SE5060 is compatible with all logic families. For TTL and DTL interface, simply ground Pin 13. The internal threshold voltage is set to 1.4V above the voltage at Pin 13. For CMOs and HTL interface, the appropriate voltage may be applied to Pin 13. For proper operation the voltage applied at Pin 13 must be at least 4V below the positive supply and 3V above the negative supply.



NOTE:
C_H and C_{COMP} required only if external hold capacitance is desired.

Figure 1. NE5060 Typical Connections

Signetics

NE/SE5537
Sample-and-Hold Amplifier

Product Specification

Linear Products

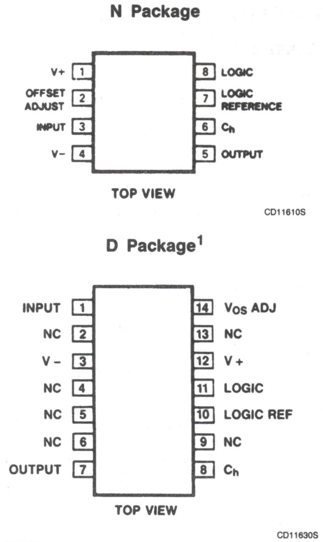
DESCRIPTION

The NE5537 monolithic sample-and-hold amplifier combines the best features of ion-implanted JFETs with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin-compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which give the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2kΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the sample mode occurring when the logic input is high. It is available in 8-lead TO-5, 8-pin plastic DIP packages, and 14-pin SO packages.

FEATURES

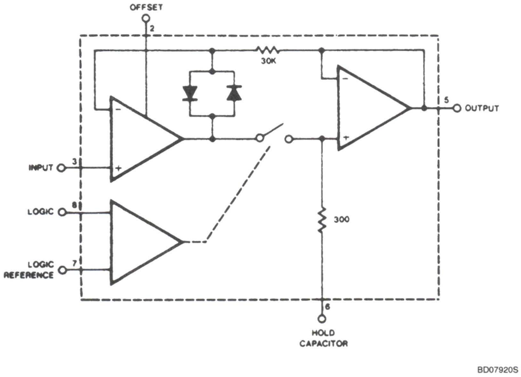
- **Operates from ±5V to ±18V supplies**
- **Hold leakage current 6pA @ $T_J = 25°C$**
- **Less than 4µs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_H = 0.01\mu F$**
- **Low input offset: 1MV (typical)**
- **0.002% gain accuracy with $R_L = 2k\Omega$**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

PIN CONFIGURATIONS


N Package
V+ 1
OFFSET ADJUST 2
INPUT 3
V− 4
8 LOGIC
7 LOGIC REFERENCE
6 Ch
5 OUTPUT
TOP VIEW
CD11610S
D Package¹
INPUT 1
NC 2
V− 3
NC 4
NC 5
NC 6
OUTPUT 7
14 VOS ADJ
13 NC
12 V+
11 LOGIC
10 LOGIC REF
9 NC
8 Ch
TOP VIEW
CD11630S

NOTE:
1. SO and non-standard pinouts.

BLOCK DIAGRAM


OFFSET
2
30K
5
OUTPUT
INPUT
3
LOGIC
8
LOGIC REFERENCE
7
300
6
HOLD CAPACITOR
BD07920S

Sample-and-Hold Amplifier NE/SE5537

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5537N
14-Pin Plastic SO	0 to +70°C	NE5537D
8-Pin Plastic DIP	-55°C to +125°C	SE5537N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Voltage supply	±18	V
P_D	Maximum power dissipation T_A = 25°C (still-air)[1] N package D package	 1160 1090	 mW mW
T_A	Operating ambient temperature range SE5537 NE5537	 -55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic to logic reference differential voltage[2]	+7, -30	V
	Output short circuit duration	Indefinite	
	Hold capacitor short circuit duration	10	s
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 8.3mW/°C
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Sample-and-Hold Amplifier NE/SE5537

DC ELECTRICAL CHARACTERISTICS[1]

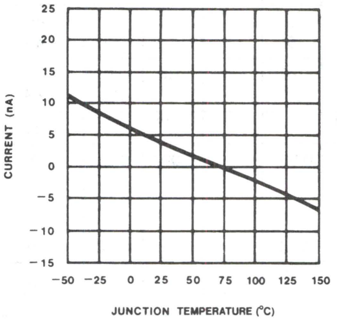
SYMBOL	PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	$T_J = 25°C$		1	3		2	7	mV
		Full temperature range			5			10	mV
I_{BIAS}	Input bias current[4]	$T_J = 25°C$		5	25		10	50	nA
		Full temperature range			75			100	nA
	Input impedance	$T_J = 25°C$		10^{10}			10^{10}		Ω
	Gain error	$T_J = 25°C$, $-10V \leqslant V_{IN} \leqslant 10V$, $R_L = 2k\Omega$ $-11.5V \leqslant V_{IN} \leqslant 11.5V$, $R_L = 10k\Omega$		0.002	0.007		0.004	0.01	%
		Full temperature range			0.02			0.02	%
	Feedthrough attenuation ratio at 1kHz	$T_J = 25°C$, $C_H = 0.01\mu F$	86	96		80	90		dB
	Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
		Full temperature range			4			6	
	"HOLD" Step[2]	$T_J = 25°C$, $C_H = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_J = 25°C$		4.5	6.5		4.5	7.5	mA
	Logic and logic reference input current	$T_J = 25°C$		2	10		2	10	μA
	Leakage current into hold capacitor[4]	$T_J = 25°C$ "hold" mode[3]		6	50		6	100	pA
	Acquisition time to 0.1%	$V_{OUT} = 10V$, $C_H = 1000pF$		4			4		μs
		$C_H = 0.01\mu F$		20			20		μs
	Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
SVRR	Supply voltage rejection ratio	$V_{OUT} = 0V$	80	110		80	110		dB
	Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

1. Unless otherwise specified, the following conditions apply: Unit is in "sample" mode. $V_S = \pm 15V$, $T_J = 25°C$, $-11.5V \leqslant V_{IN} \leqslant 11.5V$, $C_H = 0.01\mu F$, and $R_L = 2k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. These parameters guaranteed over a supply voltage range of ±5 to ±18V.

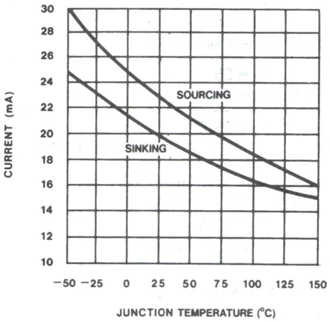
Sample-and-Hold Amplifier NE/SE5537

TYPICAL PERFORMANCE CHARACTERISTICS



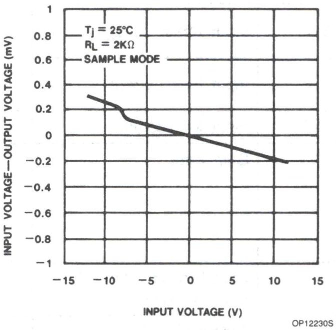
Input Bias Current

OP12200S



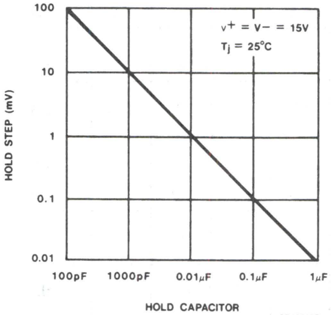
Output Short-Circuit Current

OP12210S



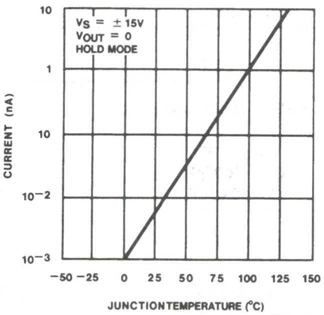
Gain Error

OP12230S



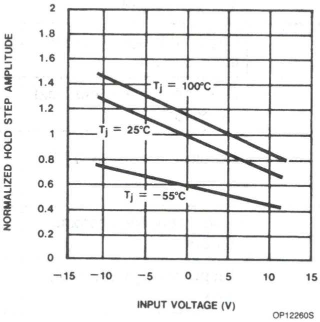
Hold Step

OP12240S



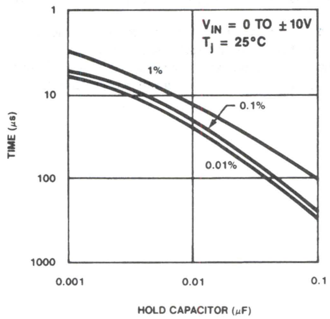
Leakage Current Into Hold Capacitor

OP12250S



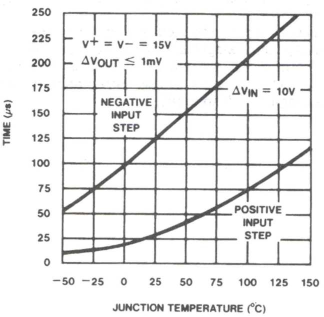
Hold Step vs Input Voltage

OP12260S



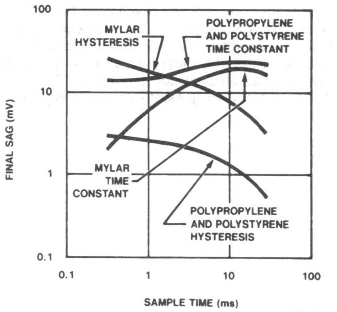
Acquisition Time

OP12270S



Aperture Time

OP12281S

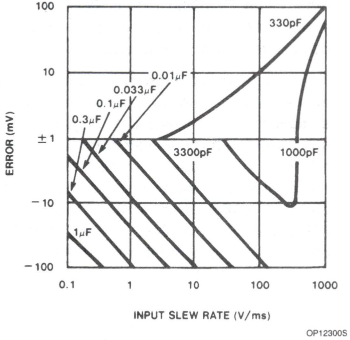


Capacitor Hysteresis

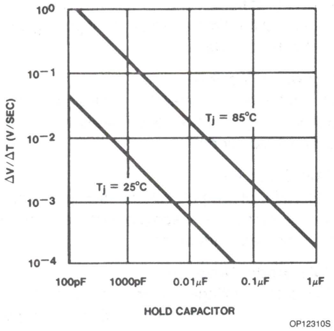
OP12290S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

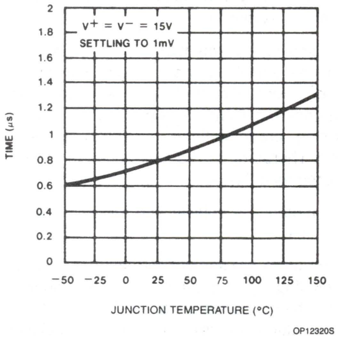
Dynamic Sampling Error



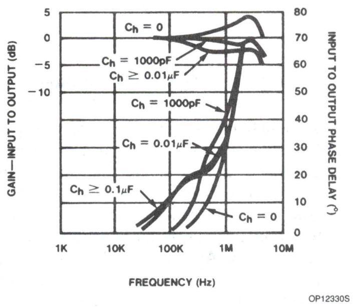
Output Droop Rate



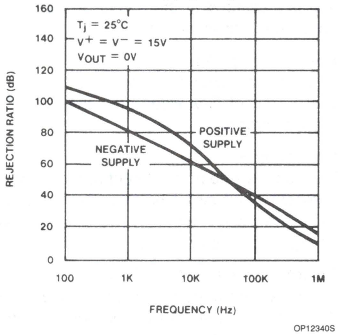
Hold Settling Time



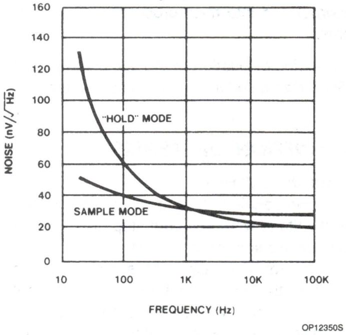
Phase and Gain (Input-to-Output, Small-Signal)



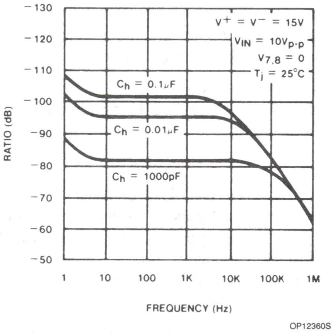
Power Supply Rejection



Output Noise



Feedthrough Rejection Ratio (Hold Mode)



Sample-and-Hold Amplifier NE/SE5537

SAMPLE-AND-HOLD

For many years designers have used the sample-and-hold (or track-and-hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout, the designer maintains certain freedom in performing predetermined manipulative functions. Therefore, the sample-and-hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample-and-hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog-to-digital converter products available today, the "DC memory" of the sample-and-hold can be easily converted to digital format and further incorporated into microprocessor-based systems.

Parametric evaluation of the sample-and-hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

Acquisition Time —
The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time —
The time elapsed from the hold command to the opening of the switch.

Aperture Jitter —
Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time —
The delay required between "HOLD" command and an input analog transition, so that the transition does not affect the held output.

Bandwidth —
The frequency at which the gain is down 3dB from its DC value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Dynamic Sampling Error —
The error introduced into the hold output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Effective Aperture Delay —
The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure of Merit —
The ratio of the available charging current during sample mode to the leakage current during hold mode.

Gain Error —
The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Mode Droop —
The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold Mode Feedthrough —
The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time —
The time required for the output to settle within 1mV of final value after the "HOLD" logic command.

Hold Step —
The voltage step at the output of the sample-and-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

Sample-to-Hold Offset Error —
The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate —
The fastest rate at which the sample-and-hold output can change (specified in V/μs).

Threshold Level —
That level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample-and-hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions).

The block diagram of the NE5537 is a closed loop, non-inverting unity gain sample-and-hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop so that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to all sample-and-hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode), the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample-and-hold device (See Figure 1). The switch control has a floating reference (Pin 7), referred to as the logic reference which makes the sample-and-hold device compatible to several types of external logic signals (TTL, PMOS, and CMOS). The switching device operates at a threshold level of 1.4V.

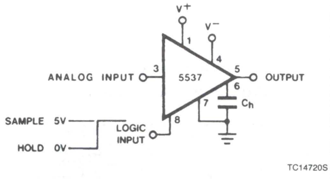


Figure 1. Typical Connection

The switch mechanism is on (sampling an information stream) when the logic level is high (Pin 8 is 1.4V higher than Pin 7) and presents a load of 5μA to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period, the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (Pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This input impedance of this amplifier is effectively:

$$R = R_{IN}(A_{OL})/(1 + 1/A)$$

where R = Effective input impedance
R_{IN} = Open-loop input impedance
A_{OL} = Open-loop gain
A = AC loop gain

Therefore, the higher the open-loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality, the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation. (Remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature.)

Sampling time for the NE5537 is less than 10μs (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

BASIC APPLICATIONS

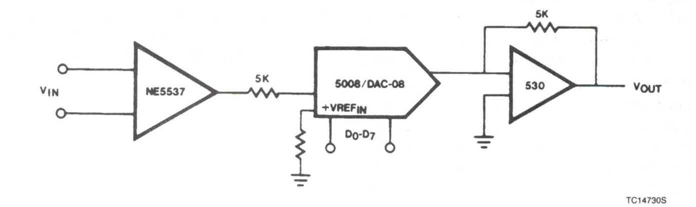
Multiplying DAC

As depicted in the block diagram of Figure 2, the sample-and-hold circuit is used to supply a "variable" reference to the digital-to-analog converter. As the input reference varies, the output will change in accordance with Equation 1, shown in Figure 2.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DACs used are the Signetics NE/SE5008; however, if the rate of change of the reference variation is kept slow enough, a microprocessor-compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however, he is limited by the fact that only one analog-to-digital converter channel is available to him. Figure 3 shows the means by which a multiplexing system may be accomplished.



NOTE:
$V_{OUT} = V_{IN} \times \frac{1}{256} \left\{ 20\ D_0 + 2^1 D_1 + 2^7 D_7 \right\}$ Equation 1

Figure 2. Multiplying DAC Application

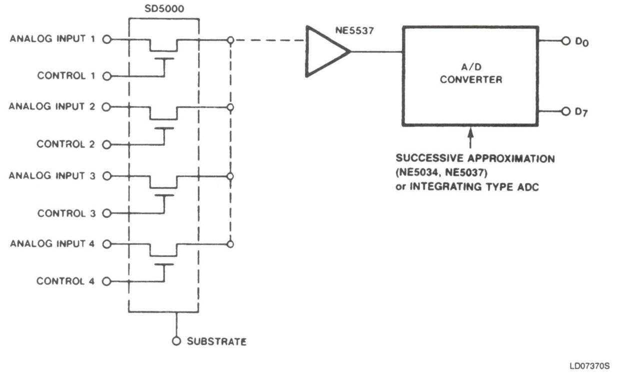


Figure 3. Analog Data Multiplexing

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample-and-hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back in the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10 – 50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give ≃0.6mA through the 1kΩ potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample-and-hold circuits. There exist finite phase delays through the sample-and-hold circuit causing an input-output phase of differential for moving signals. In addition, the series protection resistor (300Ω to Pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "HOLD" command arrives, the hold capacitor voltage may be somewhat different from the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 V_{P-P} at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) = 60mV error if the "HOLD" signal arrived near maximum dV/dt of the input. A positive-going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs) = −96mV (analog) for a total of −36mV. To add to the confusion, analog delay is proportional to hold capacitor value, while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled "Aperture Time" has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "HOLD" command. This curve is based on a 1mV error fed into the output.

A second curve, "Hold Settling Time," indicates the time required for the output to settle to 1mV after the "HOLD" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a PC card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample-and-hold systems.
2. Reference should be made to *Design Engineering*, Volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc., for a further discussion of sample-and-hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

Signetics

Linear Products

TDA1535

High-Speed Sample-and-Hold Amplifier

Preliminary Specification

DESCRIPTION

The TDA1535 is a high-speed sample-and-hold amplifier with a total harmonic distortion of 0.001% and high signal-to-noise ratio. The circuit uses high-speed operational amplifiers with new frequency compensation techniques, and a switch design that permits a low pedestal error.

The high performance of the circuit makes it suita ble for data acquisition systems with resolution up to 16 bits, such as hi-fi digital audio.

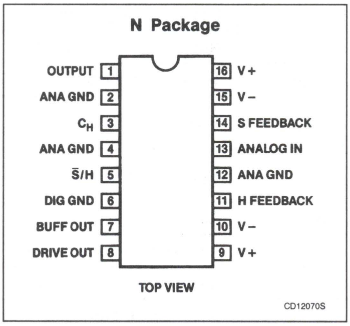
FEATURES

- **Fast acquisition time (2μs typ)**
- **Wide bandwidth (2MHz typ)**
- **JFET input**
- **Low aperture uncertainty time (0.5ns)**
- **TTL compatible logic input/outputs**
- **High S/N ratio (110dB typ)**
- **High output current (100mA)**

APPLICATIONS

- **Instrumentation**
- **Medical electronics**
- **Digital audio**
- **Modems**

PIN CONFIGURATION


N Package
OUTPUT 1
ANA GND 2
C$_H$ 3
ANA GND 4
S̄/H 5
DIG GND 6
BUFF OUT 7
DRIVE OUT 8
16 V+
15 V−
14 S FEEDBACK
13 ANALOG IN
12 ANA GND
11 H FEEDBACK
10 V−
9 V+
TOP VIEW
CD12070S

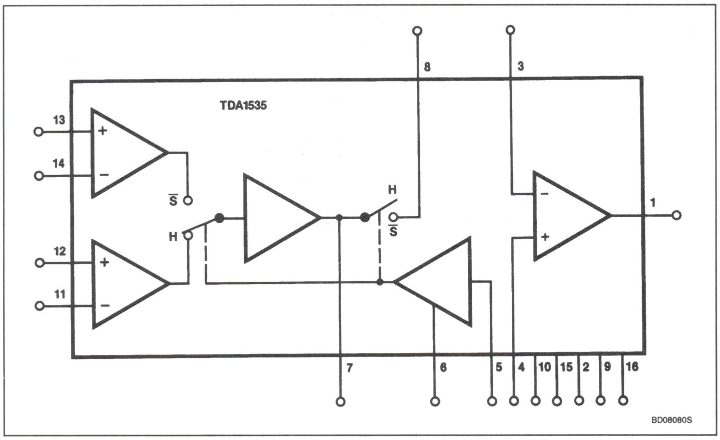
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−20°C to +70°C	TDA1535N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Positive supply (Pin 9, 16)	10	V
V−	Negative supply (Pin 10, 15)	−10	V
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C
T_J	Junction temperature	150	°C

BLOCK DIAGRAM

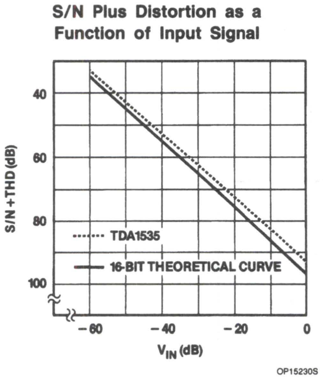

TDA1535
13
14
12
11
+
−
S̄
H
8
3
H
S̄
1
7
6
5
4
10
15
2
9
16
BD08080S

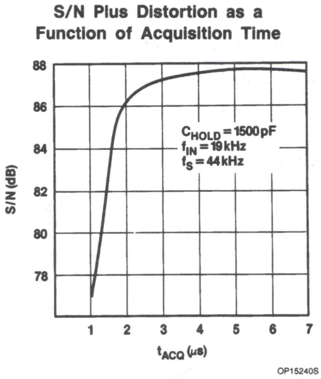
High-Speed Sample-and-Hold Amplifier TDA1535

DC ELECTRICAL CHARACTERISTICS $V_+ = 5V$, $V_- = -5V$, $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V +	Positive supply voltage		4	5	8	V
V −	Negative supply voltage		−4	−5	−8	V
I +	Positive supply current			27		mA
I −	Negative supply current			−27		mA
P_{TOT}	Total power dissipation			270		mW
THD	Total harmonic distortion	20Hz to 20kHz in tracking mode with 8-V_{P-P} signal		−100		dB
S/N	Signal to noise ratio	20Hz to 20kHz in tracking mode with 8-V_{P-P} signal		110		dB
G	Gain	Tracking mode		−1		V/V
T_{AC}	Acquisition time to 0.001%	8V step		2		μs
I_{AU}	Aperture uncertainty time				0.5	μA
B	Small signal bandwidth			2		MHz
dV/dT	Droop rate			50	TBD	mV/s
V_H	Hold step (pedestal error)			2	TBD	mV
V_I	Input voltage				±4	V_{P-P}
V_{IH} V_{IL}	Digital input voltage	Hold mode Track mode	2.0 0		V + 0.8	V V
I_{IH} I_{IL}	Digital input current	Hold mode Track mode			20 −400	μA μA

TYPICAL PERFORMANCE CHARACTERISTICS





CIRCUIT DESCRIPTION

The sample-and-hold amplifier is a crucial part in high resolution A/D converter systems. To achieve the performance required of a sample-and-hold amplifier in such systems, this circuit uses high-speed operational amplifiers with new frequency compensation techniques, and a specially designed wide-band class B output amplifier with high current drive capability. The switches are optimized for a low pedestal error. The capacitance between the two metal layers is used for the compensation capacitors. This configuration yields a very small voltage coefficient of capacitance, or voltage dependance, minimizing system distortion.

The usual solution for frequency compensation in a two-stage amplifier is pole splitting, or having the amplifier split into a transconductance stage followed by a voltage amplifier stage. At low frequencies the open-loop gain equals the total gain of the two cascaded stages, while at higher frequencies the output current of the transconductance stage goes through the Miller capacitance, resulting in a first-order response.

The problem with this technique is the relatively low bandwidth of the lateral PNP transistors that are usually used in the input stage. This limitation is solved in the TDA1535 by interchanging the transconductance and voltage amplifier stages. Frequency compensation is performed with a feed-forward capacitor from the output of the voltage amplifier to the output of the transconductance stage. At low frequencies the open-loop gain is that of the two cascaded amplifiers combined. At higher frequencies the compensation capacitor short-circuits the transconductance stage, producing a single-stage response. Careful choice of transconductance capacitor value has yielded a nearly ideal first-order response.

This system produces an order of magnitude improvement in bandwidth. Note that the input and output signals of the second stage are in phase. The low output impedance of the voltage amplifier removes the danger of instability.

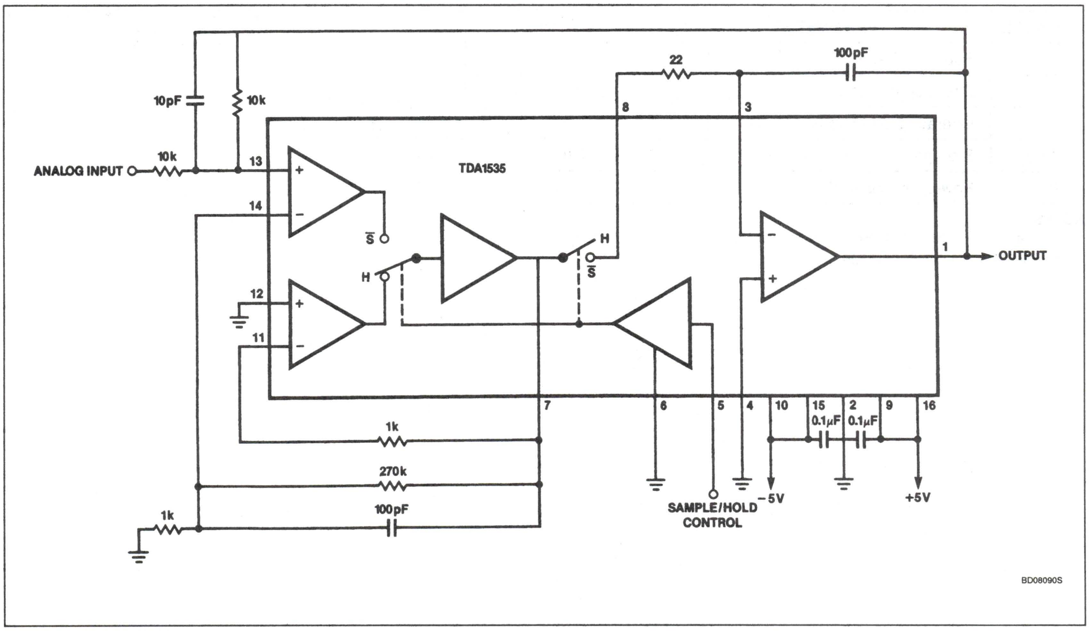
High distortion is the penalty paid for the other advantages of this circuit. However, this problem is overcome by the addition of another voltage amplifier at the output, again connected as a Miller integrator. The amplifier now consists of a voltage amplifier stage, followed by a transconductance stage, followed by a voltage gain stage. The result is three cascaded amplifier stages at low frequencies.

Frequency compensation is obtained with two capacitors. At higher frequencies the output current of the transconductance stage flows through the Miller capacitor. At even higher frequencies the feed-forward capacitor comes into play. Together with the Miller integrator, a capacitive inverter is formed, resulting in the output voltage of the first amplifier stage appears at the output of the capacitive inverter. Careful choice of the two capacitor values and the value of transconductance yields a very nice first-order response with large bandwidth.

Feed-forward systems, however, have a problem with inexact frequency compensation due to the inaccurate cancellation of the pole-zero pair, resulting in slow-setting of the amplifier. This design uses a high feed-forward takeover frequency to achieve a negligible influence on overall system performance.

Wide-band op amps need wide-band output stages if they are to be useful. Standard complementary circuits cannot be used because of frequency limitations in lateral PNP transistors. Therefore, an all-NPN output stage with feed-forward frequency compensation has been designed for this circuit.

TDA1535 APPLICATION EXAMPLE



Signetics

NE5520

LVDT Signal Conditioner

Product Specification

Linear Products

DESCRIPTION

The NE5520 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT). The chip includes a low distortion amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT; a synchronous demodulator to convert the LVDT output amplitude and phase to position information; and an output amp to provide gain and filtering.

FEATURES

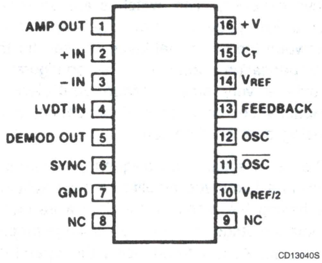
- **Oscillator frequency: 1kHz to 20kHz**
- **Low distortion**
- **Capable of ratiometric operation**
- **Single supply operation 5V to 20V or dual supply ±2.5V to ±10V**
- **Low power consumption**

APPLICATIONS

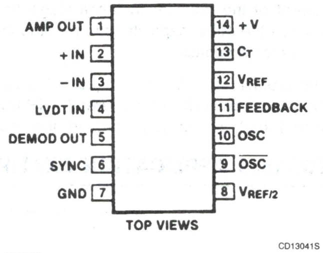
- **LVDT signal conditioning**
- **RVDT signal conditioning**

PIN CONFIGURATIONS

D[1], F Packages


AMP OUT 1
+IN 2
−IN 3
LVDT IN 4
DEMOD OUT 5
SYNC 6
GND 7
NC 8
16 +V
15 C_T
14 V_{REF}
13 FEEDBACK
12 OSC
11 $\overline{OSC}$
10 $V_{REF/2}$
9 NC
CD13040S

N Package


AMP OUT 1
+IN 2
−IN 3
LVDT IN 4
DEMOD OUT 5
SYNC 6
GND 7
14 +V
13 C_T
12 V_{REF}
11 FEEDBACK
10 OSC
9 $\overline{OSC}$
8 $V_{REF/2}$
TOP VIEWS
CD13041S

NOTE:
1. SOL — Released in large SO package only.

ORDERING INFORMATION

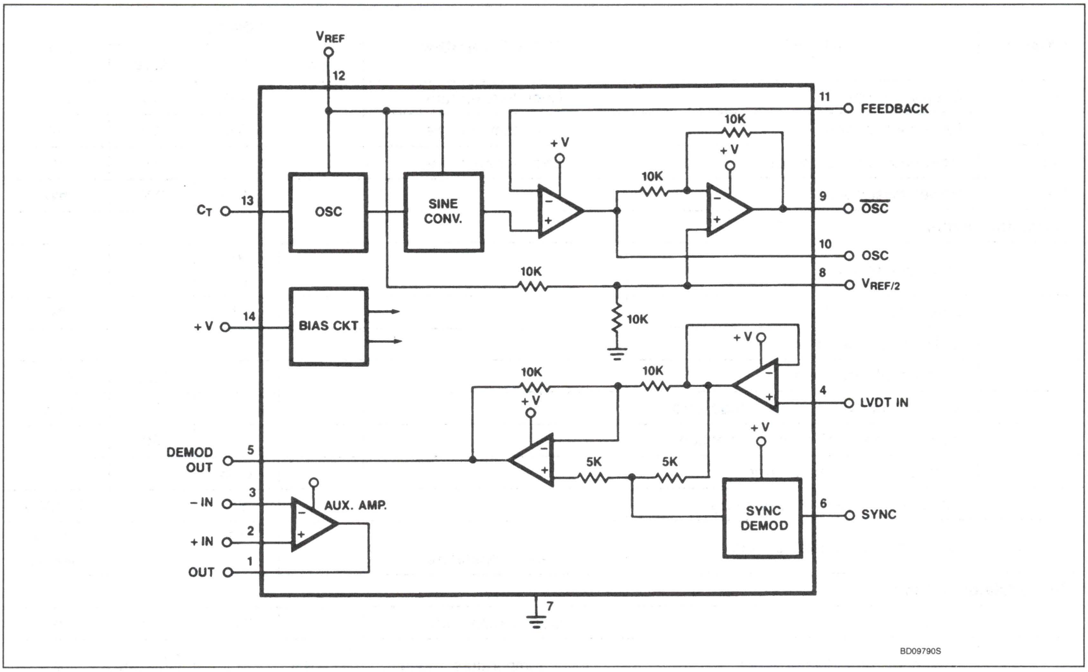
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5520N
16-Pin SO Package	0 to +70°C	NE5520D
16-Pin Ceramic DIP	0 to +70°C	NE5520F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	+20	V
	Split supply voltage	±10	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +165	°C
P_D	Power Dissipation[1]	840	mW

NOTES:
1. Supplied only in large SO (Small Outline) package. See package diagram.
2. Pin numbers are for N package.

BLOCK DIAGRAM


VREF
12
11
FEEDBACK
10K
+V
+V
10K
CT
13
OSC
SINE CONV.
9
OSC
10
OSC
10K
8
VREF/2
+V
14
BIAS CKT
10K
+V
10K
10K
+V
4
LVDT IN
+V
DEMOD OUT
5
5K
5K
−IN
3
AUX. AMP.
+IN
2
SYNC DEMOD
6
SYNC
OUT
1
7
BD09790S

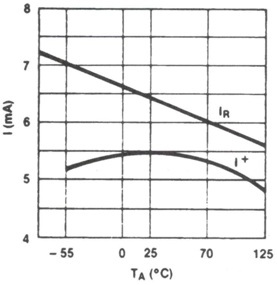
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_R = V+ = 10V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{CC}	Supply current	Over temperature		7.0	10	mA
I_{REF}	Reference current	Over temperature		5.5	10	mA
V_{REF}	Reference voltage range	Over temperature	5		V+	V
P_D	Power dissipation			120	220	mW
Oscillator section						
	Oscillator output			$\frac{V_R}{8.7}$		V_{RMS}
	Sine wave distortion			4		%
	Initial amplitude error				±3	%
	Tempco of amplitude				0.05	%/°C
	Voltage coefficient of amplitude error				2.5	%/V
	Initial accuracy of oscillator frequency				20	%
	Tempco of frequency error			0.05		%/°C
	Voltage coefficient of frequency			2.5		%/V(V_R)
	Oscillator output load current	 Over temperature	 8	15 		mA_{RMS} mA_{RMS}
Demodulator section						
E_r	Linearity error	Over temperature		0.05	0.1	%
	Maximum demodulator input	Over temperature range	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	V
	Demodulator offset voltage	Over temperature range			65	mV
	Demodulator input current	Over temperature	−1000	−300		nA
	$V_{R/2}$ accuracy	Over temperature	−3	±0.5	+3	%
Auxiliary output amplifier						
V_{OS}	Input offset voltage	Over temperature	−10		10	mV
I_{BIAS}	Input bias current	Over temperature range	−500	−300		nA
I_{OS}	Input offset current		−100		100	nA
A_V	Gain	$R_L = 10k\Omega$ over temperature		100		V/mV
SR	Slew rate			1.5		V/μs
GBW	Gain bandwidth	$A_V = 1$		1		MHz
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$ over temperature	1.5		V+ − 1.5	V
I_{SC}	Output short-circuit current			50		mA

NOTE:
Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 7.6mW/°C for the plastic package and 7.3mW/°C for the cerdip package.

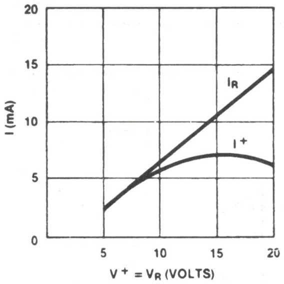
TYPICAL PERFORMANCE CHARACTERISTICS

I_R and I^+ vs Temperature



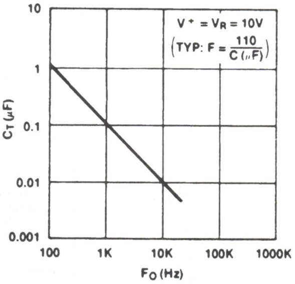
OP18460S

I_R and I^+ vs Voltage



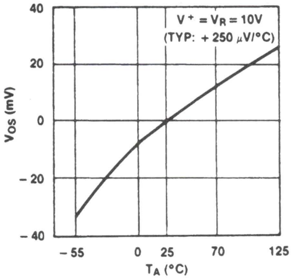
OP18470S

F_O vs C_T



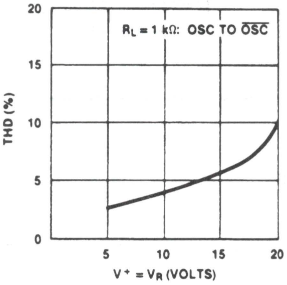
OP18480S

Demodulator Offset vs Temperature (Normalized to 25°C)



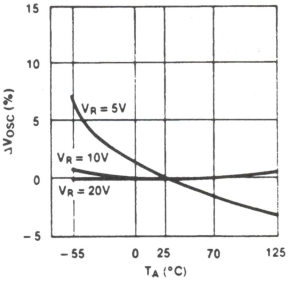
OP18490S

Distortion of Sine Wave vs Reference Voltage



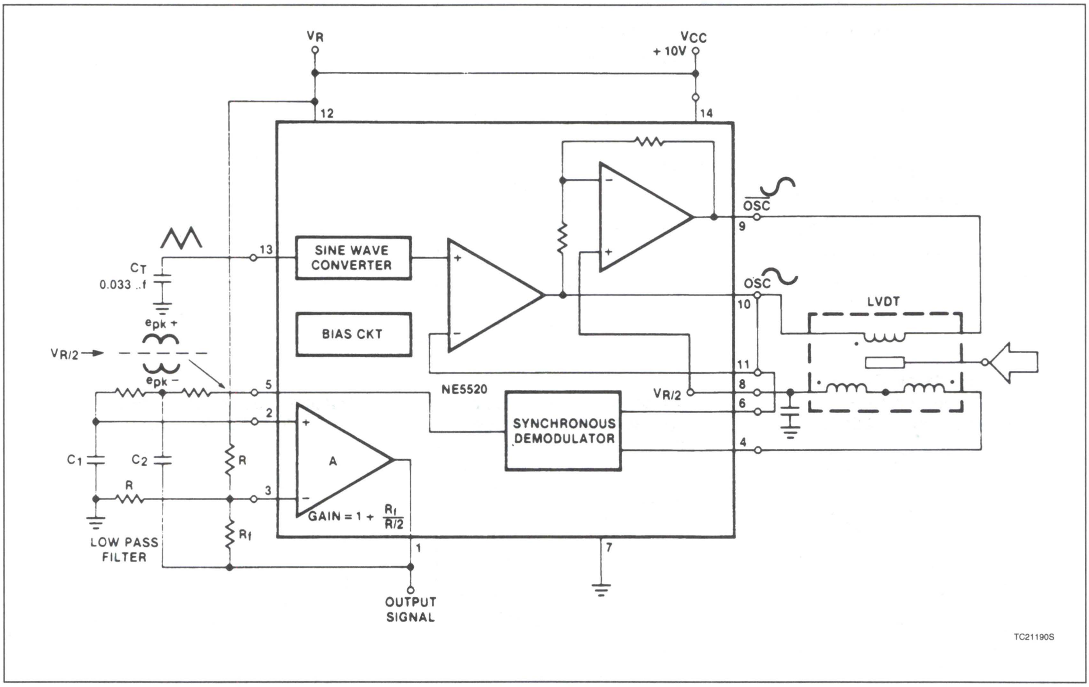
OP18500S

Oscillator Amplitude Variation With Temperature



OP18510S

TYPICAL SINGLE SUPPLY LVDT CIRCUIT


VR
VCC
+10V
12
14
OSC
9
OSC
10
LVDT
13
SINE WAVE CONVERTER
BIAS CKT
CT
0.033 μf
epk +
VR/2
epk −
5
NE5520
VR/2
11
8
6
4
2
3
SYNCHRONOUS DEMODULATOR
A
C1
C2
R
R
Rf
GAIN = 1 + Rf/(R/2)
LOW PASS FILTER
1
7
OUTPUT SIGNAL
TC21190S

Signetics

Linear Products

AN118
Using the LVDT Signal Conditioner

Application Note

INTRODUCTION

An LVDT is an electromechanical transducer which makes possible the measurement of very small motion in a structure or mechanical device. Mechanical motion is translated to an electrical signal which contains position information much as a radio frequency carrier contains sound information. The position information from the LVDT is contained in the phase and amplitude of the output AC waveform. In order to remove the position information (demodulation), a system such as is shown in block form in Figure 1 must be used. Once signal demodulation is achieved, the position data may be read out on a meter or digital display in addition to being processed by microprocessor or computer. The Signetics NE5520 is a Monolithic LVDT Driver-Demodulator designed to interface with most LVDTs presently being used in the industry.

Uses will range over a large number of potential applications including the accurate measurement of position, pressure, load weight, angular position and even acceleration. Historically, LVDTs have been used in the following applications:

- Load cell
- Linear motion
- Torque cell
- Vibration
- Fluid pressure
- Accelerometer
- Inclinometer
- Seismic load cell

Motion may be

- Linear
- Rotary

The NE5520 provides sinusoidal drive to the Linear Variable Differential Transformer (LVDT), the output of which is buffered, rectified and phase-demodulated to obtain both direction and displacement information in the form of a DC output signal (Figure 2).

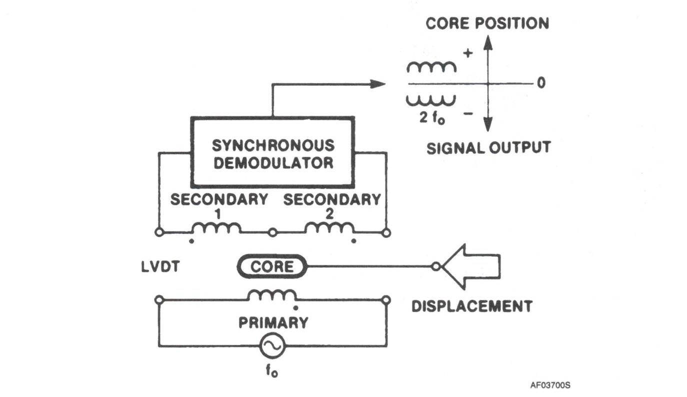


Figure 1. The LVDT With Sine Wave Excitation and Synchronous Demodulation

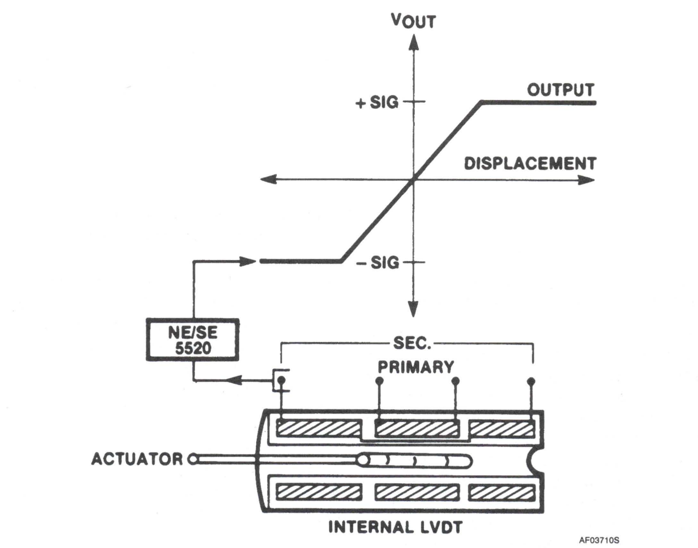


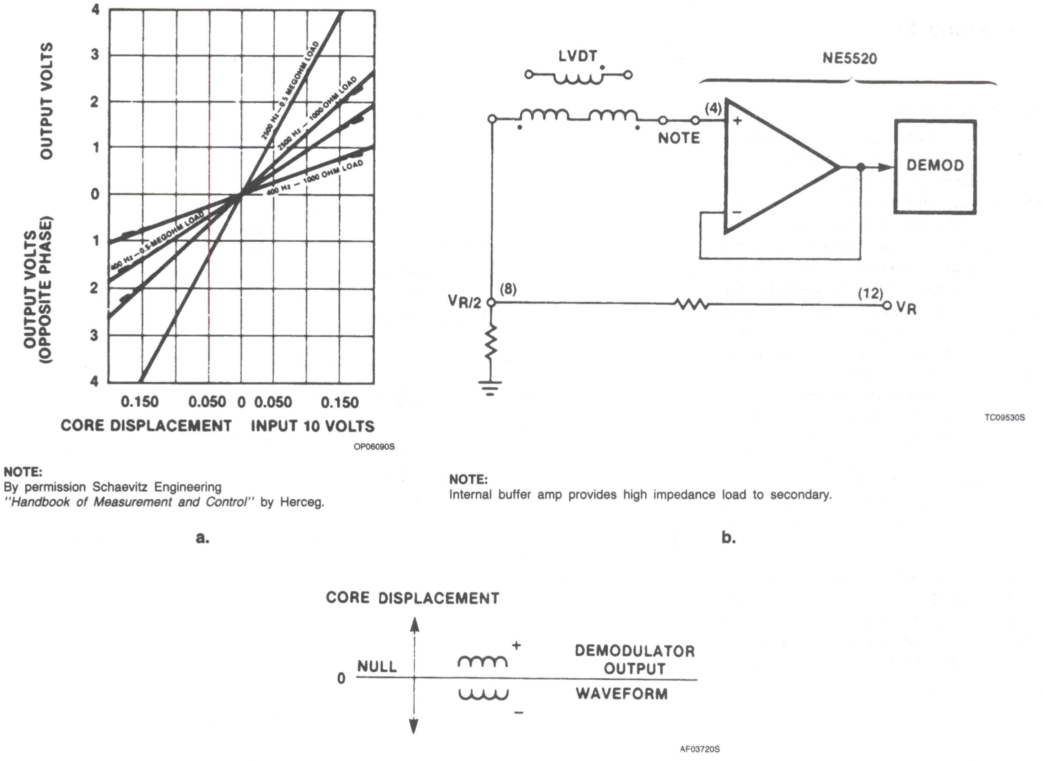
Figure 2. LVDT System Transfer Function

LVDT LOADING

Due to the loosely coupled characteristics of the typical LVDT, loading effects versus frequency may be critical to a successful design. The graph (Figure 3a) shows this relationship in the form of a family of curves relative to LVDT core displacement for 400Hz and 2500Hz. From the curves it is obvious that the linearity and output level versus displacement is superior for an LVDT operated at 2500Hz with a very high impedance load (0.5MΩ). The NE5520 demodulator presents a very high input impedance to the LVDT secondary for maximum linearity (Figure 3b).

LVDT INTERFACING: SIGNAL CONDITIONING IS REQUIRED

In order to obtain usable information from the LVDT a series of signal-conditioning circuit operations are required. First, a stable source



NOTE:
By permission Schaevitz Engineering
"Handbook of Measurement and Control" by Herceg.

a.

NOTE:
Internal buffer amp provides high impedance load to secondary.

b.

c.

Figure 3. Output Characteristics of a Typical LVDT for Various Loads and Excitation Frequencies

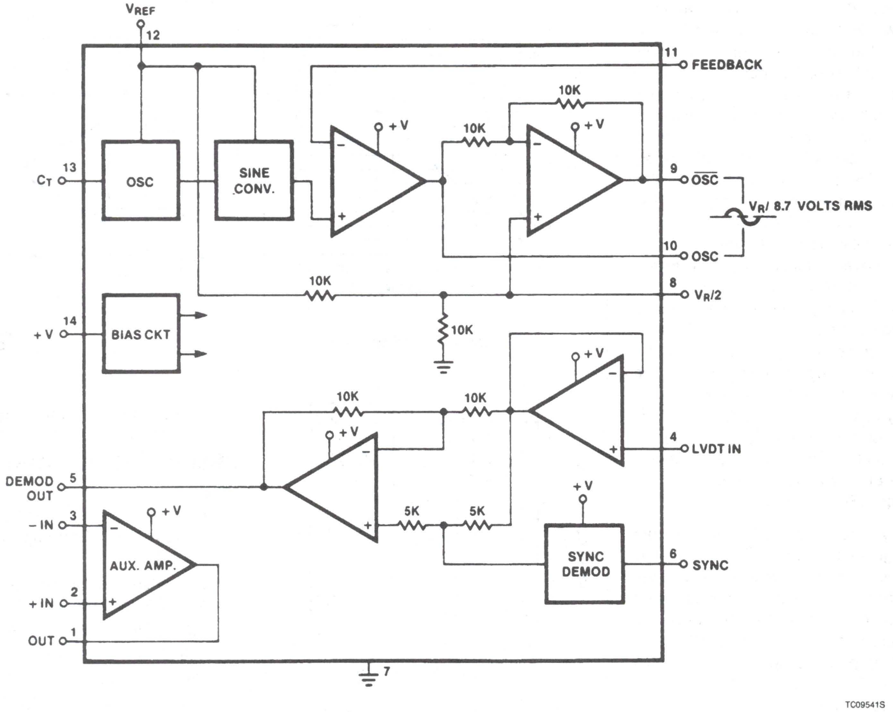
of constant frequency excitation voltage must be applied to the primary of the LVDT.

Next, some form of demodulator is needed to extract position information from the LVDT secondary output signal. A full-wave rectifier will provide usable amplitude information when adequately filtered; however, relative phase information is lacking. In order to obtain both phase and amplitude information, synchronous demodulation is needed. This type of demodulator exists in the Signetics NE5520. Once phase and amplitude information is obtained in the form of a polar full-wave rectified signal (see Figure 3c) from the synchronous demodulator, the carrier component (actually 2nd harmonic of the carrier plus higher-order spectral components) must be filtered out, leaving only the true position information. This is accomplished by passing the demodulated signal through a low-pass active filter. An auxiliary operational amplifier is provided for this purpose within the NE5520, in addition to adjustable signal gain for proper full-scale output (span adjustment). In addition, DC offsets are nulled by a simple offset adjustment at the auxiliary amplifier. The resulting system is a complete LVDT signal conditioner. Figure 4 shows a block diagram of the NE5520. The device will operate in a single supply range from 5 to $20V_{DC}$ or with split supplies of ± 5 to ± $10V_{DC}$. A device current, I_{CC}, of 10mA at an operating voltage of 10V is typical.

DESCRIPTION OF THE NE5520 (Figure 4)

The NE5520 oscillator consists of a triangle wave generator, a current source-sink circuit which switches when the capacitor voltage reaches discrete levels at ¼ and ¾ V_{REF}. The total swing being $V_{REF/2}$ V_{P-P}. The triangle wave is fed into a non-linear load which generates a sinusoidal waveform with low distortion. The sine wave output is then buffered by two op amps, the output of which appear on Pins 9 and 10 in phase opposition. This then is the excitation signal for the LVDT primary.

The second major functional portion of the NE5520 is the synchronous demodulator and this section performs full-wave rectification in phase synchronism (Pin 6) with the above oscillator output. In order to extract true position information, the phase relationship of the LVDT secondary must be obtained. This means that as the LVDT core passes through null an abrupt 180° phase change occurs. Once full-wave rectification is accomplished, the resulting signal carrier frequency must be removed by filtering. Demodulator output appears on Pin 5. This is accomplished by an active filter incorporating the auxiliary op amp (Pins 1, 2, 3). The original position information



NOTE:
Pin numbers for N package.

Figure 4. Block Diagram

then appears ripple-free on Pin 1 of the auxiliary amplifier.

Other functions include buffer amplifier feedback in the oscillator circuit. The loop is closed with negative feedback around both amplifiers (Pin 10 to 11) operating at unity gain.

The oscillator timing capacitor controls the frequency as shown in the graph, Figure 5. The frequency is related by the equation $f_{OSC} = 110C_T(\mu F)$. Absolute output frequency will vary slightly with supply voltage.

BIASING THE REFERENCE V_{REF} (Pin 12)

The manner in which the V_R pin is biased will effect the output voltage function of the NE5520 and consideration must be given to this in order to arrive at an optimum system design. There are two basic modes of operation involved as listed below:

1) Ratiometric

2) Fixed Reference

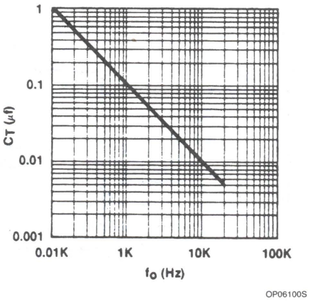


Figure 5. Oscillator Frequency vs Capacitance

With the ratiometric mode, Pin 12 (V_{REF}) is connected to Pin 14 (+V). Since V_R controls the DC common-mode voltage of the demodulator and the oscillator RMS output, these magnitudes will now change with supply voltage. The DC output from Pin 1, using a single ground-referenced supply, will be ratiometric with the supply voltage and centered within the common-mode range of the output amplifier when the LVDT transducer is at null. Single or dual supply operation will be ratiometric when +V is connected to V_R.

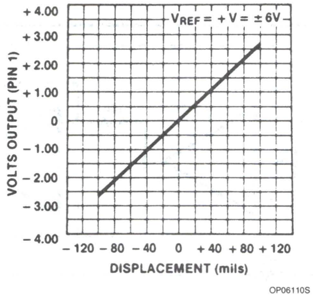
The alternate method of biasing is the fixed reference mode with Pin 12 (V_R) connected to a fixed reference voltage such as +10V and Pin 14 (+V) allowed to vary with an incoming poorly regulated supply. This might occur in automotive applications where battery voltage may vary from 10 to 14V. However, with a fixed reference driving V_R, DC voltage at the output will not vary with supply but will vary within the common-mode limits of the amplifier as the LVDT core traverses its path. Output voltage of Pin 1 at LVDT null will be $V_R/2$. Thus, for the case mentioned with $V_R = 10V$, the null voltage will be +5V. The maximum linear swing would be 1.5 − 8.5V around this value. The fixed reference mode may be used with single or dual supply operation.

Using the LVDT Signal Conditioner AN118

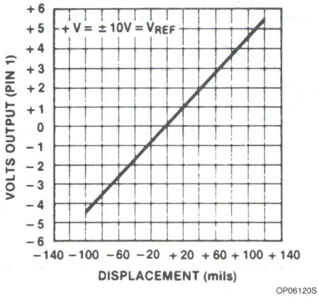
DUAL SUPPLY OPERATION

When connected to a typical LVDT transducer as shown in Figure 6, the NE5520 will exhibit an extremely linear transfer function. Very important to precision position measurement is the inherent repeatability of the system. The graphs in Figure 7a and b illustrate the highly linear transfer function and its repeatable accuracy with different supply voltages, in this case ±6V and ±10V. The transducer motion was over a range of ±150 milliinches each side of the LVDT null. Typical DC output signal is Note that linearity remains constant, however, full-scale Note that linearity remains constant, however, full-scale output varies with supply voltage. This is due to the increased excitor drive to the LVDT with increased reference voltage. LVDT output is a linear function of excitor amplitude on the primary winding. The addition of a single gain control may easily be added between Pins 1 and 3 to reduce gain in order to retain constant output for different supply voltages (see Figure 8) or V_R may be connected to a fixed voltage. (See 'Biasing.')

It is strongly recommended that dual output tracking regulated supplies be used in this type of application in order to minimize system DC offset and impaired measurement accuracy due to power supply unbalance. An optional circuit capable of automatically tracking and nulling power supply offset is shown in Figure 9. The bipolar output signal is referenced to ground.



a. Transfer Function ±6V



b. Transfer Function ±10V

Figure 7

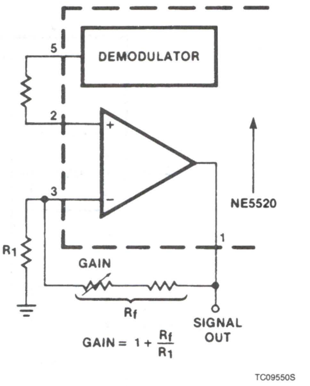


Figure 8. Typical Gain Adjust Circuit

NULLING PROCEDURE

(Figure 9)

1. Null transducer position by observing Pin 4 waveform. Set supply voltage for ±6.00V.
2. Set offset adjust pot (feeds Pin 3 of NE5520) for $0.00V_{DC}$ at Pin 1 of NE5520.
3. Adjust offset null pot (NE5512) for zero output on Terminal A.
4. Check for equal voltage ± deflection when transducer is displaced equal distances from physical null position.
5. Adjust tracking control for minimum DC output change when either supply is varied over operating range at 'A'.

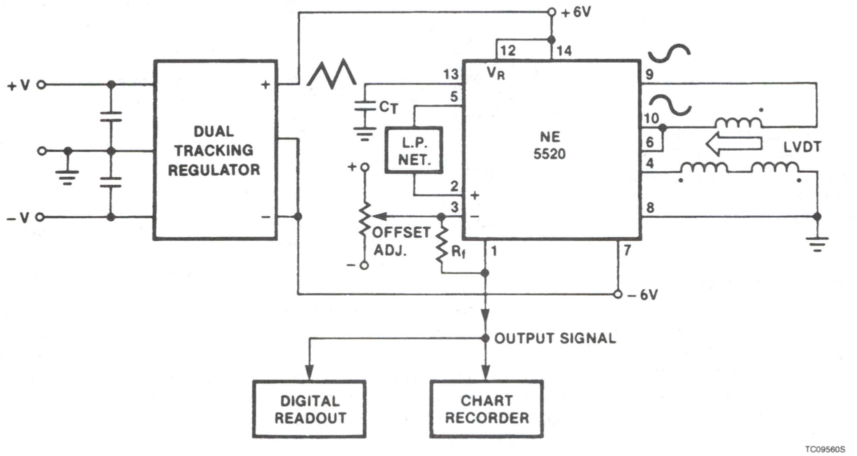


Figure 6. Typical Measuring System (Ratiometric Mode)

Using the LVDT Signal Conditioner AN118

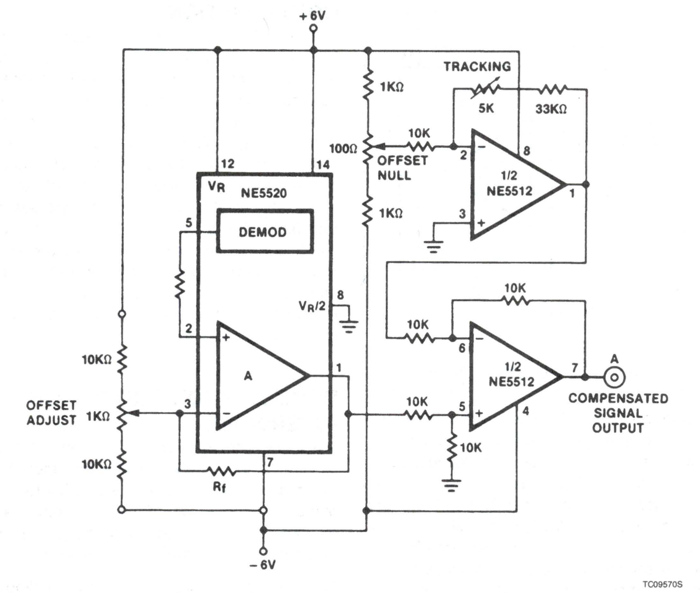

+6V
TRACKING
1KΩ
5K
33KΩ
10K
100Ω
OFFSET NULL
12
14
2
8
1/2 NE5512
1
VR
NE5520
1KΩ
3
5
DEMOD
VR/2
8
10K
2
10K
6
1/2 NE5512
7
A
10KΩ
A
1
COMPENSATED SIGNAL OUTPUT
OFFSET ADJUST
1KΩ
3
10K
5
4
10K
10KΩ
Rf
7
−6V
TC09570S

Figure 9. Auto PSRR for Use With Non-Tracking Supplies

SINGLE SUPPLY OPERATION

Single-ended supply operation requires a different circuit approach to obtain measurement system interface. Figure 10 shows a typical circuit using a single 10V supply. Note that the output (Pin 1) of the NE5520 is now floating above ground at approximately $V_R/2$. Simple measuring circuits may be realized (Figures 11a, b, c) by placing a DC microammeter between Pin 1 and a resistive divider creating a bridge readout which is ratiometric with supply voltage variations. In case more precision is necessary, a buffer amplifier may be added between the voltage divider or $V_R/2$ and the readout circuit in order to minimize offset due to measuring circuit loading. DC offset due to internal tracking error in the NE5520 may be reduced by using the nulling circuit shown in Figure 12. Offset sensitivity and its effect on system accuracy will be inversely proportional to full-scale signal output of the NE5520 which is a function of the DC gain of the auxiliary amplifier and LVDT output. A typical full-scale output with 10V supply operation is $V_R/2 \pm 3.5V$ with gain equal to 10.

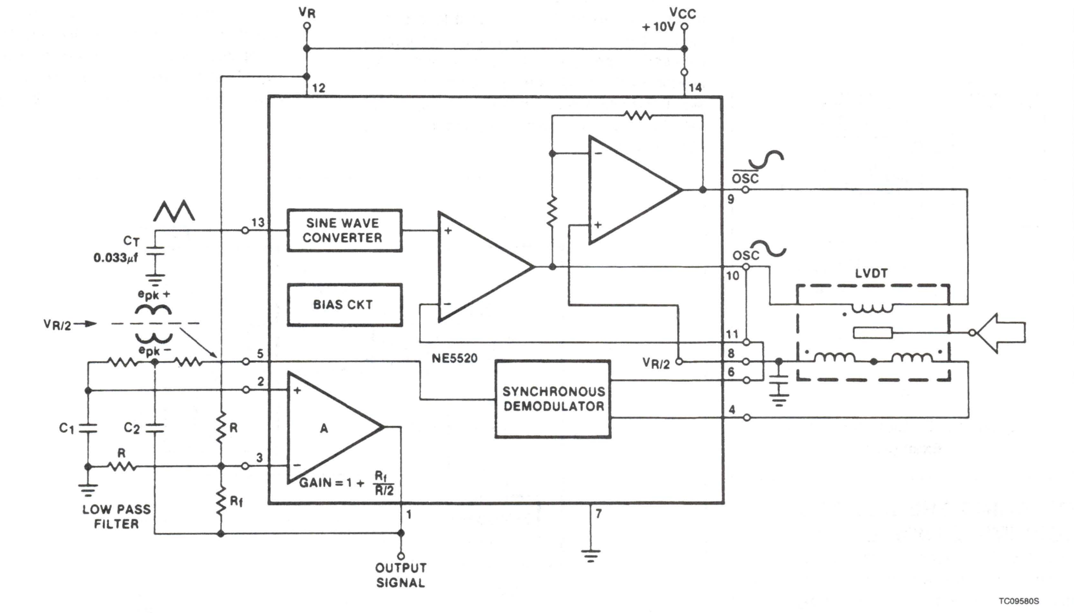

VR
VCC
+10V
12
14
OSC
9
13
SINE WAVE CONVERTER
CT
0.033µf
epk +
OSC
10
LVDT
BIAS CKT
VR/2
epk −
11
5
NE5520
VR/2
8
6
2
SYNCHRONOUS DEMODULATOR
4
C1
C2
R
R
A
3
GAIN = 1 + Rf/R/2
Rf
LOW PASS FILTER
1
7
OUTPUT SIGNAL
TC09580S

Figure 10. Typical Single Supply LVDT Circuit

Using the LVDT Signal Conditioner AN118

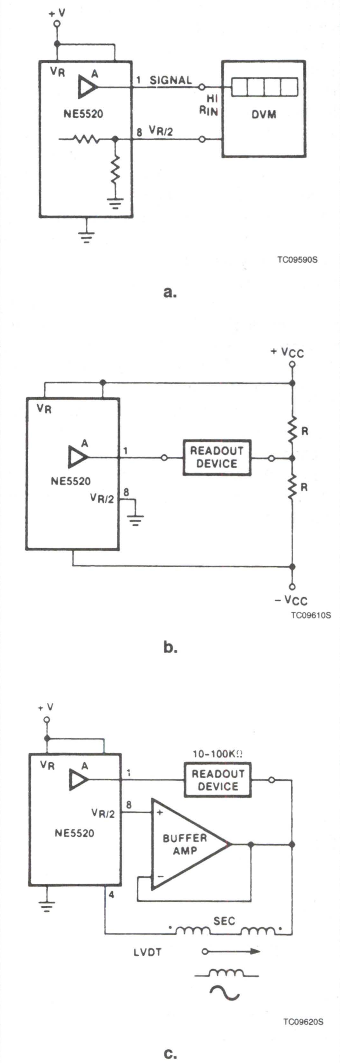

+V
VR
A
NE5520
1 SIGNAL
HI
RIN
DVM
8 VR/2
TC09590S
a.
+VCC
VR
A
1
READOUT DEVICE
R
R
NE5520
VR/2
8
−VCC
TC09610S
b.
+V
VR
A
1
10-100KΩ
READOUT DEVICE
VR/2
8
NE5520
BUFFER AMP
4
SEC
LVDT
TC09620S
c.

Figure 11. Output Interfacing Examples

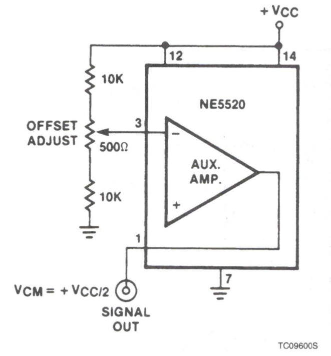

+VCC
12
14
10K
NE5520
OFFSET ADJUST
3
500Ω
AUX. AMP.
10K
1
7
VCM = +VCC/2
SIGNAL OUT
TC09600S

Figure 12. DC Offset Adjust

MATCHING THE NE5520 TO LOW IMPEDANCE LVDTS

The NE5520 exciter output is capable of driving LVDT primary windings with a minimum impedance of 1kΩ. When a significantly lower impedance primary is driven by the device some form of step-down impedance matching or a power buffer is recommended. Figure 13 shows a step-down matching transformer approach. A transformer with primary impedance of approximately 1kΩ (audio type) with the proper secondary impedance to match the LVDT primary is used to couple oscillator excitation. Depending on the output efficiency of the LVDT, output signal losses may occur with a corresponding loss in measuring sensitivity. The auxiliary amplifier gain may be increased to offset this loss.

A second approach makes use of a power buffer amplifier constructed from discrete transistors (2N2222, 2N3644). This circuit (Figure 14) results in less signal loss and is inexpensive. A DC decoupling capacitor must be used to prevent DC offset currents from flowing in the LVDT primary winding. A 3dB signal reduction is noted when driving a 15Ω load to $6V_{P-P}$ (10V operation); and $12V_{P-P}$ for 20V supply.

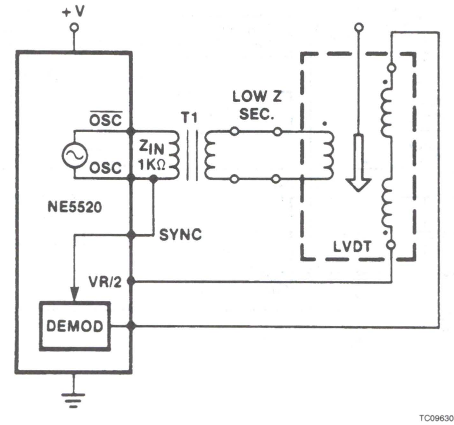

+V
OSC
T1
LOW Z SEC.
ZIN 1KΩ
OSC
NE5520
SYNC
LVDT
VR/2
DEMOD
TC09630S

Figure 13. Driving Low-Z LVDTs With the NE/SE5520

NE5520 TEMPERATURE COMPENSATION

Internal offset voltages originating in the NE5520 synchronous demodulator require external compensation to obtain best measurement accuracy when operating over the full temperature range. The circuits shown (Figures 15a, b) give a simple approach using a thermistor inserted in series with the offset null resistors to reduce voltage drift to a reasonable level. These tolerances are based on ±3.5V full-scale output for LVDT displacements each side of physical null. A thermistor having a positive coefficient of +0.7%/°C is used. Obviously, if the total divider resistance is changed, a different thermistor resistance will be required.

DEMODULATOR DISTORTION (OVERDRIVE)

When the demodulator input exceeds $2V_{P-P}$ clipping distortion will increase and must be avoided by controlling oscillator drive to the primary of the LVDT. Figure 16 shows an example of a circuit for attenuating primary excitation using a 1kΩ potentiometer.

The procedure for adjusting the level is simply to:

1. Set LVDT core position for maximum output from the secondary.
2. Monitor the waveform on (Pin 5 demodulator output) and adjust oscillator level for the amplitude just below clipping. Normally, this should result in a maximum of $2\ V_{P-P}$ at Pin 4 of the NE5520 (25°C).

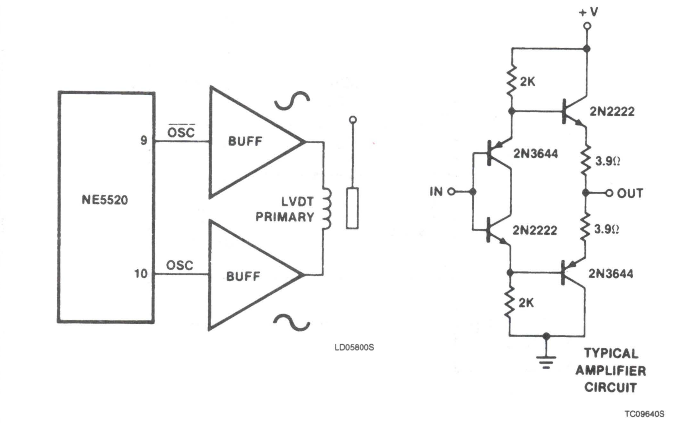
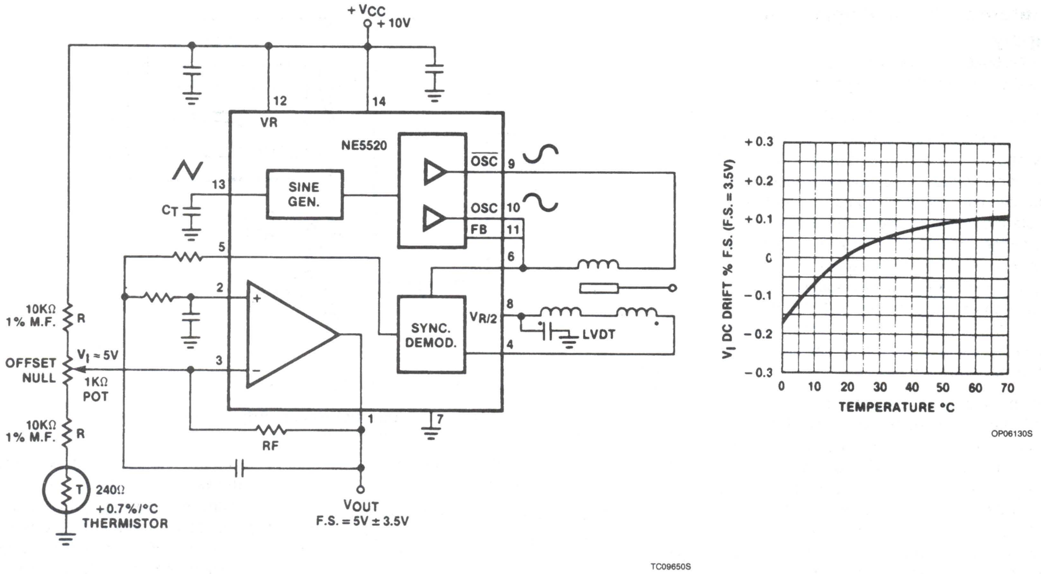

NE5520
9
$\overline{OSC}$
BUFF
10
OSC
BUFF
LVDT
PRIMARY
LD05800S
+V
2K
2N2222
2N3644
3.9Ω
IN
OUT
2N2222
3.9Ω
2N3644
2K
TYPICAL
AMPLIFIER
CIRCUIT
TC09640S

Figure 14. Low-Z LVDT

LVDT SECONDARY PHASE ANGLE COMPENSATION BY EXCITATION FREQUENCY

The LVDT has a frequency-dependent phase shift associated with the particular characteristics of the device and its excitation frequency. This phase shift is in addition to the 180° shift which occurs when passing through null position.

By adjusting the frequency of the sine wave excitation a condition results which causes secondary voltage to be in phase with primary excitation. The adjustment of relative primary and secondary phase angles has several effects. First, if the primary excitation is referenced to the synchronous demodulator, as in the NE5520, optimum rectification occurs at zero phase differential between secondary AC phase and demodulator switching relative to the waveform zero crossings. Second, "Exciting an LVDT at its zero phase angle frequency results in minimum sensitivity to frequency and temperature variations" (Schaevitz *Handbook of Measurement and Control*, 1976).


+VCC
+10V
12
14
VR
NE5520
SINE GEN.
13
CT
$\overline{OSC}$
9
OSC
10
FB
11
6
5
2
3
SYNC. DEMOD.
VR/2
8
4
LVDT
1
7
RF
10KΩ 1% M.F.
R
OFFSET NULL
VI ≈ 5V
1KΩ POT
10KΩ 1% M.F.
R
T
240Ω
+0.7%/°C
THERMISTOR
VOUT
F.S. = 5V ± 3.5V
TC09650S
+0.3
+0.2
+0.1
0
−0.1
−0.2
−0.3
VI DC DRIFT % F.S. (F.S. = 3.5V)
0
10
20
30
40
50
60
70
TEMPERATURE °C
OP06130S

a. LVDT Driver Demodulator with Temperature Compensation 0 – 70°C

b. Thermistor Temperature Compensation

Figure 15

DEMODULATOR SYNC PHASE

A second method of phase compensation of the NE5520 versus the LVDT is to use a variable phase shift network between the oscillator output and the sync input to the NE5520. This is shown in Figure 17. The oscillator frequency remains fixed and the pot is tuned for optimum demodulator phasing.

It is emphasized that an external phasing adjustment as outlined above is not always necessary. Some LVDTs operating in the 1 – 5kHz range will be near zero phase and will need no phase compensation. Experimental evaluation of the prototype design combined with system specifications will be the best means of making this decision.

The waveform photo in Figures 18a and b shows the demodulator output signal when phasing of the synchronous demodulator is correct (a) and improperly adjusted (b).

Proper phasing of the sync signal to the demodulator results in optimum sensitivity and linearity.

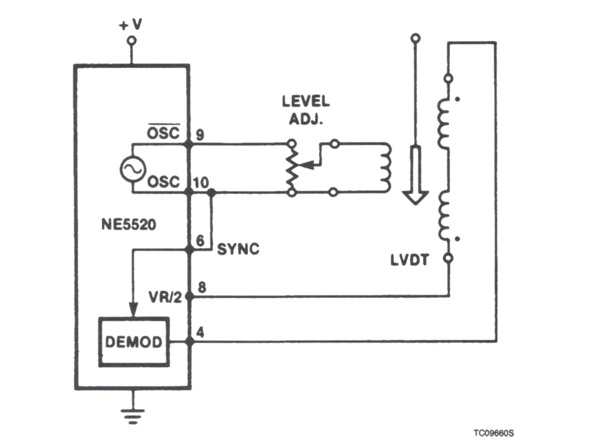
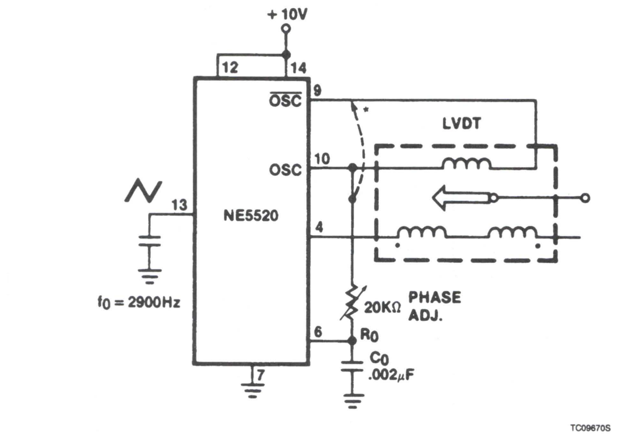


Figure 16. Limiting LVDT Excitation to Prevent Demodulator Distortion



NOTE:
*Alternate connection may be required for some LVDTs.

Figure 17. External Phase Adjustment

NE5520 LVDT DRIVER DEMODULATOR APPLICATIONS

Operated With a Single Power Supply

The NE5520 may be operated with a single-ended power supply ranging from +5 to 20V.

A very simple motion transducer may be constructed using the circuit shown in Figures 19a and b. The output is biased to one-half the supply voltage. This requires special interface circuitry for the signal readout. One simple method is to use a zero center meter in a bridge configuration, as shown. Displacement now may be measured as a positive or negative meter reading. Readout sensitivity is a function of the particular LVDT and of the gain of the error amplifier. DC offsets may be nulled by using a simple offset adjustment circuit as indicated.

The transducer is centered in its displacement and the offset adjust pot set for a zero meter reading. Once this procedure is completed, the circuit is capable of making measurements based on transducer displacement. Displacement sensitivity is a function of the LVDT transducer rated in volts-per-inch in addition to the transfer gain of the NE5520 demodulator. The input excitation is generally a fixed level as is the LVDT transducer transformer ratio. However, the auxiliary gain stage may be used to adjust the overall system sensitivity. This section of the device is also used to obtain a low-pass active filter for the smoothing of demodulator ripple. The design examples use a simple VCVS low-pass filter which allows gain and cut-off frequency to be adjusted independently. Gain equals ten in the example.

Note that using a single supply results in a DC common-mode voltage at the output of one-half the reference voltage on Pin 12. *This voltage, V_R, may be equal to but not greater than the supply voltage on Pin 14.*

LVDT Measuring Circuit Using a Dual Supply

A second mode of operation makes use of dual power supply. A common choice may be ±5, ±6, or ±10V. Special consideration must be made in properly biasing the internal circuitry to operate under these conditions. Figure 20 shows a simple design for working with ±6V supplies. Special provisions for minimizing DC power supply offsets may be made by using the NE5512 dual op amp as a tracking voltage source and difference amplifier-output buffer (see Figure 9). A second method is to use a dual tracking regulator to supply the NE5520.

LVDT in Closed-Loop Servo

The LVDT provides an excellent method of obtaining position information for closed-loop servo drive systems. Pressure rollers, hydraulic drivers, and motor driven linear motion

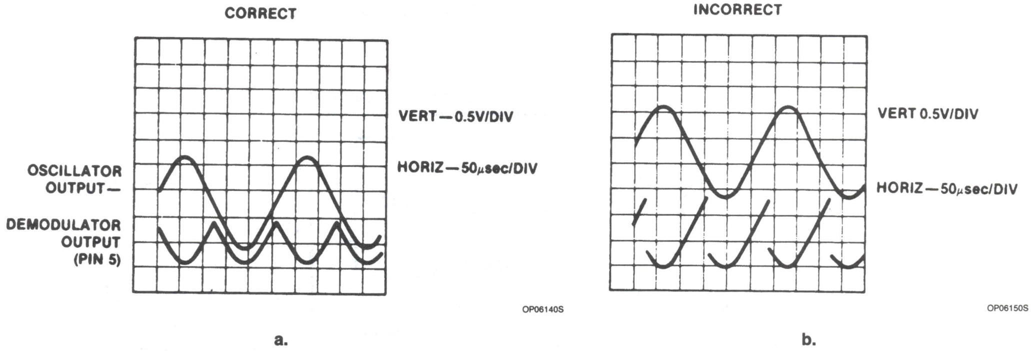


Figure 18. NE5520 Demodulator Phasing

transducers are a few of the general applications which may benefit from the accuracy and speed of response inherent in the LVDT sensor.

A simple block diagram (Figure 21a) shows one possible application in which the NE5520 with LVDT sensor provides accurate position control in a closed-loop servo. Linear motion from millimeters to inches of translational motion are possible using the LVDT technique.

In practice, the position voltage may be the output of a D/A converter which in turn is activated digitally from a controlling microprocessor. Keyboard information or software commands are translated directly into mechanical motion (Figure 21b).

LVDT SIGNAL TRANSMISSION BY CURRENT LOOP

In certain situations the demodulated output signal must be transmitted over long wires or cables before reaching the signal monitoring equipment. The receiver end may consist of chart recorders, digital panel meters and computers or microprocessors. In some systems, many LVDT signals must be monitored from different locations, thus requiring variable wire length between transmitter and receiver producing a different line resistance in each case. If voltage feed were used, signal accuracy would be affected by line resistance. This need for accurate signal transmission necessitates the use of a current loop. A current loop develops a current exactly in proportion to the demodulated LVDT output voltage. It is not affected by line resistance within certain limits governed by the current generator.

One method of current loop transmission uses the $V_{R/2}$ common-mode reference to create a null balance signal circuit which is converted to a bipolar current signal corresponding to the LVDT transducer null (i.e. physical displacement center null position at which zero current occurs). This method is shown in Figure 22 and requires the use of an external dual op amp, half of which is used to provide a buffered reference ($V_{R/2}$) voltage return for the current loop. With $R_2 = 200\Omega$, the current loop sensitivity is 5mA/V of input signal. In all cases, the current output to the loop receiver will remain constant with fixed input voltage (LVDT demodulator), even for varying line resistance up to 600Ω. This resistance must include all wire and load drops in the loop. Various full-scale current limits require different supply voltages and, without external supplies, will be limited by op amp swing characteristics, for to force a given current across $R_L + R_2$ results in an ultimate voltage limit from the op amp output in the current converter as total resistance increases.

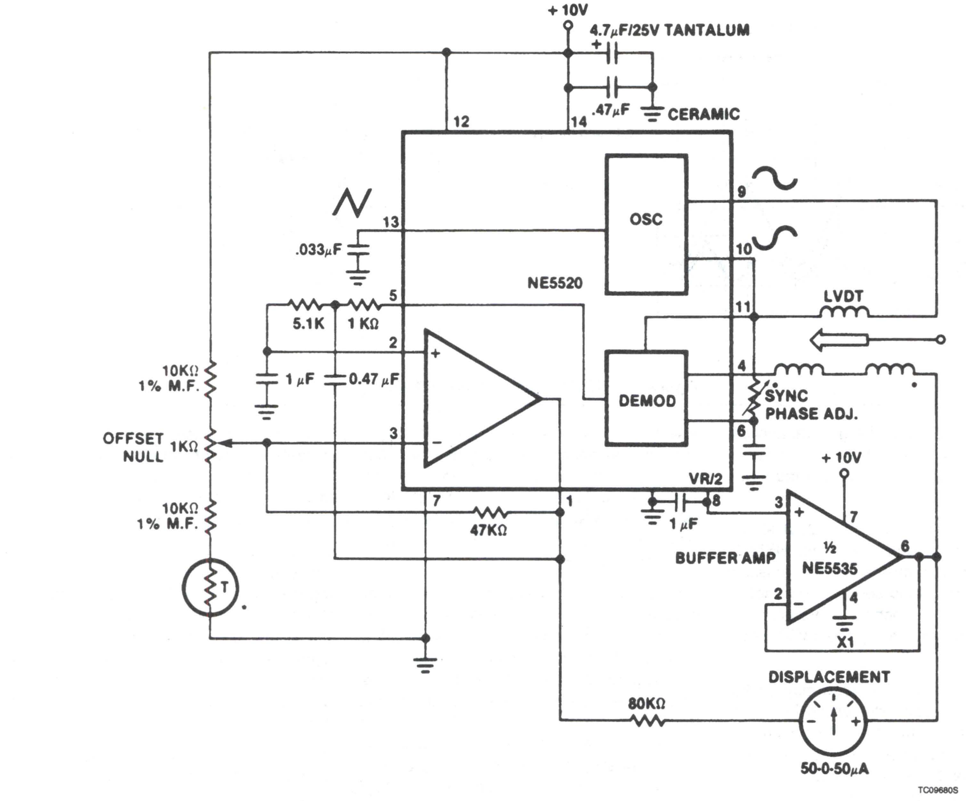
Another method uses an external supply and discrete transistor controlled by the closed-loop op amp referenced to shunt resistor R_{SH} in the emitter return circuit. This, of course, is a unipolar current loop. See Figure 23.

Some systems in common use require two-wire source to include both the device operating current and the signal loop current. Thus the quiescent device current must be nulled out at the receiver end, leaving the residual signal loop current. The NE5520 is not well suited to this particular application since the device standby current is approximately 10mA.

A current loop operated from supply voltage sources at the transducer location is a better choice for the operation of an output signal loop where long lines must carry locally-generated LVDT signals after demodulation back to the monitor site.

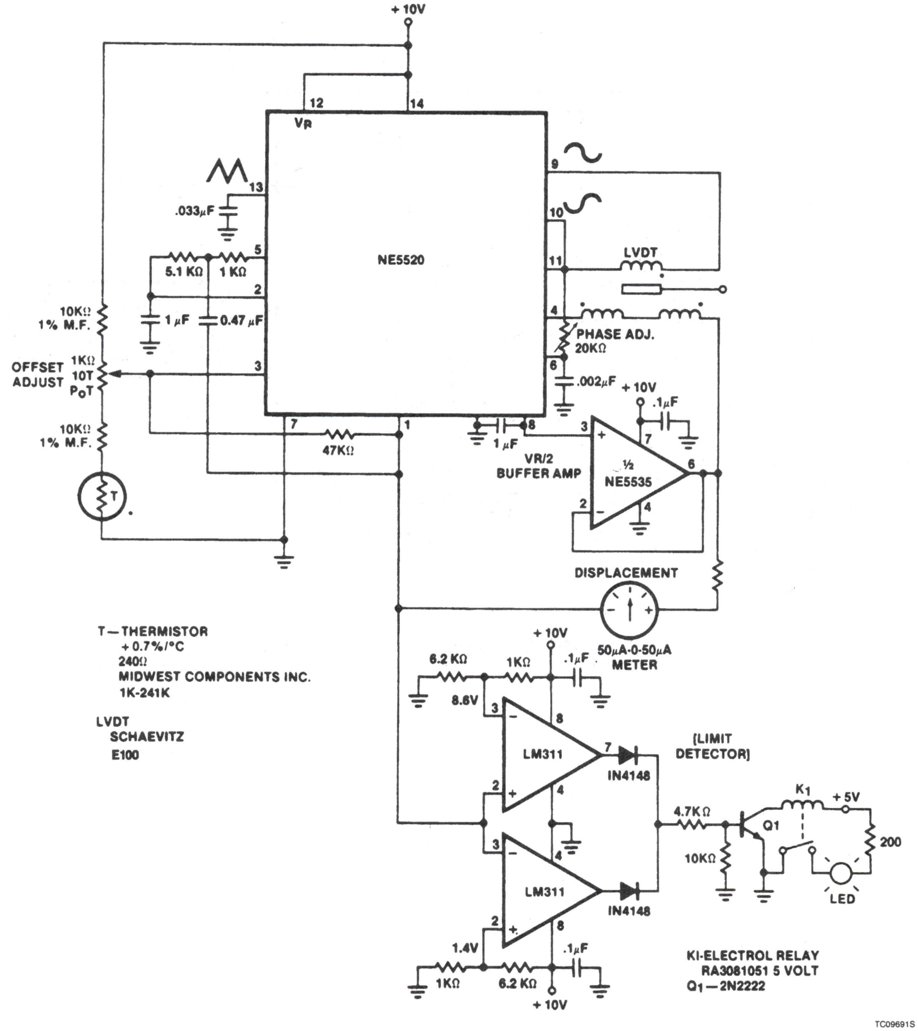
POSITIONING THE NE5520 LVDT 3-WIRE REMOTE DRIVER DEMODULATOR SENSING HEAD

The NE5520 may be placed in close proximity to the LVDT transducer, provided the environment stays within device specifications. This physical arrangement allows only DC supply and low frequency signal lines (3 wires) being run between the transducer-conditioner unit and the signal processing station as shown in Figure 24.


+10V
4.7μF/25V TANTALUM
.47μF
CERAMIC
12
14
9
10
11
13
.033μF
OSC
NE5520
5
5.1K
1 KΩ
2
1 μF
0.47 μF
3
DEMOD
LVDT
4
SYNC PHASE ADJ.
6
VR/2
8
1 μF
7
1
47KΩ
10KΩ 1% M.F.
OFFSET NULL
1KΩ
10KΩ 1% M.F.
T
+10V
BUFFER AMP
½ NE5535
X1
DISPLACEMENT
80KΩ
50-0-50μA
TC09680S

NOTE:
Thermistor 240Ω + 0.7%/°C

Figure 19a. LVDT Measuring Gauge


+10V
12
14
VR
13
.033μF
5
5.1 KΩ
1 KΩ
2
1 μF
0.47 μF
3
NE5520
9
10
11
LVDT
4
PHASE ADJ.
20KΩ
6
.002μF
+10V
.1μF
10KΩ
1% M.F.
OFFSET ADJUST
1KΩ
10T
PoT
10KΩ
1% M.F.
T
7
47KΩ
1
8
1 μF
VR/2
BUFFER AMP
3
7
½
NE5535
6
2
4
DISPLACEMENT
50μA-0-50μA
METER
+10V
6.2 KΩ
1KΩ
.1μF
8.6V
3
8
LM311
7
IN4148
(LIMIT
DETECTOR)
2
4
3
4
LM311
IN4148
2
8
1.4V
.1μF
1KΩ
6.2 KΩ
+10V
4.7KΩ
K1
+5V
Q1
200
10KΩ
LED
TC09691S

T—THERMISTOR
+0.7%/°C
240Ω
MIDWEST COMPONENTS INC.
1K-241K

LVDT
SCHAEVITZ
E100

KI-ELECTROL RELAY
RA3081051 5 VOLT
Q1—2N2222

Figure 19b. NE5520 LVDT Measuring Circuit With Limit Detector

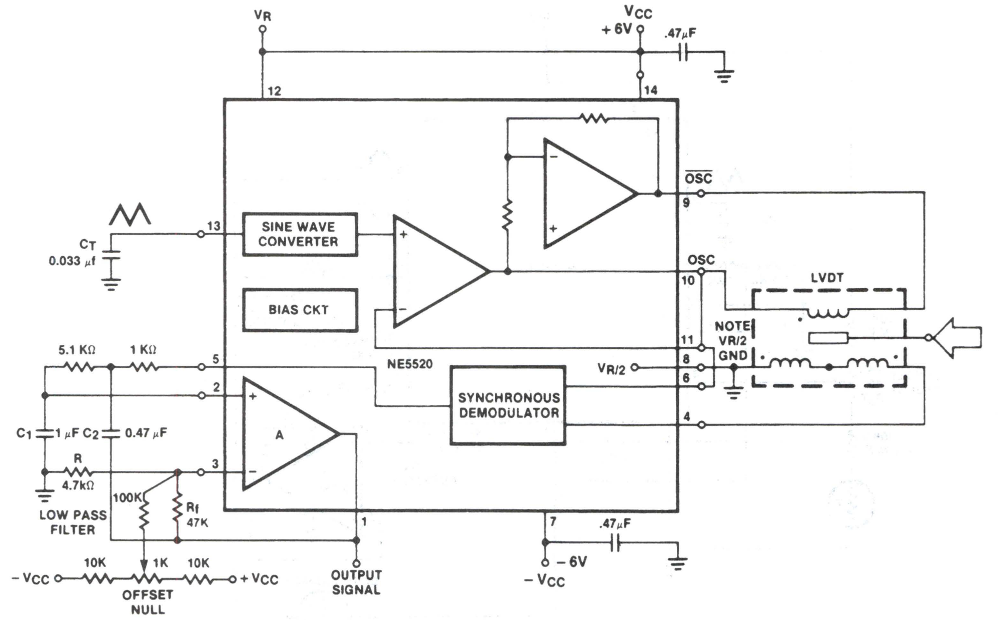
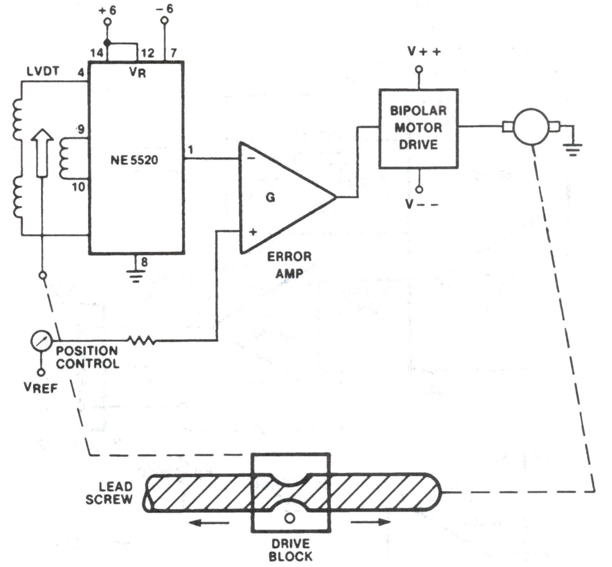
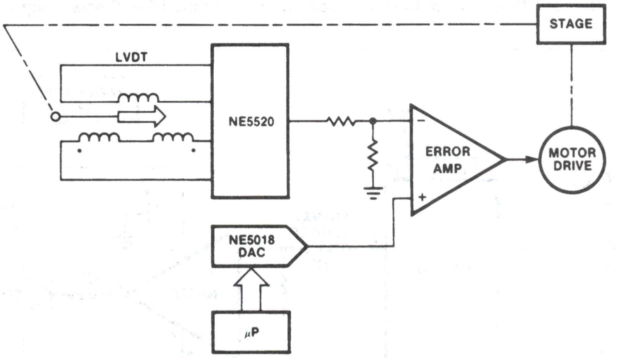

VR
VCC
+6V
.47μF
12
14
OSC
9
13
CT
0.033 μf
SINE WAVE CONVERTER
BIAS CKT
OSC
10
LVDT
NOTE
VR/2
GND
11
8
6
4
5.1 KΩ
1 KΩ
5
2
3
NE5520
VR/2
SYNCHRONOUS DEMODULATOR
C1
1 μF
C2
0.47 μF
R
4.7kΩ
A
LOW PASS FILTER
100K
Rf
47K
1
7
.47μF
−6V
−VCC
10K
1K
10K
−VCC
+VCC
OFFSET NULL
OUTPUT SIGNAL
TC09700S

Figure 20. NE5520 LVDT Driver-Demodulator ($f_O = 2900Hz$)


+6
−6
14
12
7
VR
LVDT
4
9
10
NE 5520
1
8
V++
BIPOLAR MOTOR DRIVE
V−−
−
G
+
ERROR AMP
POSITION CONTROL
VREF
LEAD SCREW
DRIVE BLOCK

TC09710S

a. NE5520 Position Servo With LVDT Sensor


STAGE
LVDT
NE5520
−
ERROR AMP
+
MOTOR DRIVE
NE5018 DAC
μP

TC09720S

b. Microprocessor Control Interface

Figure 21

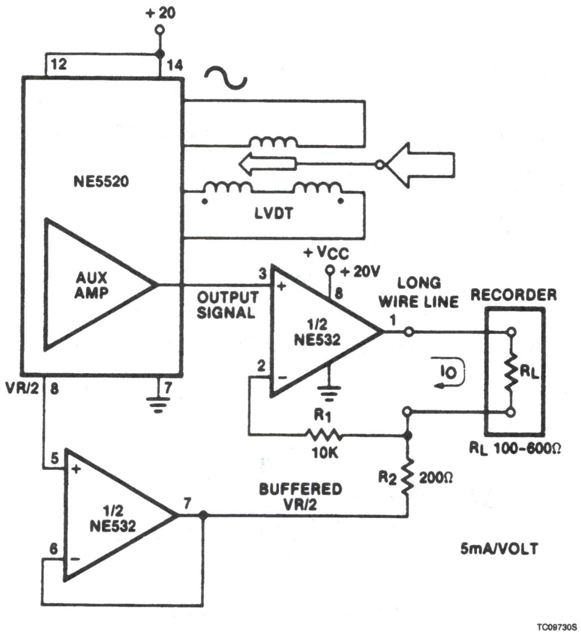
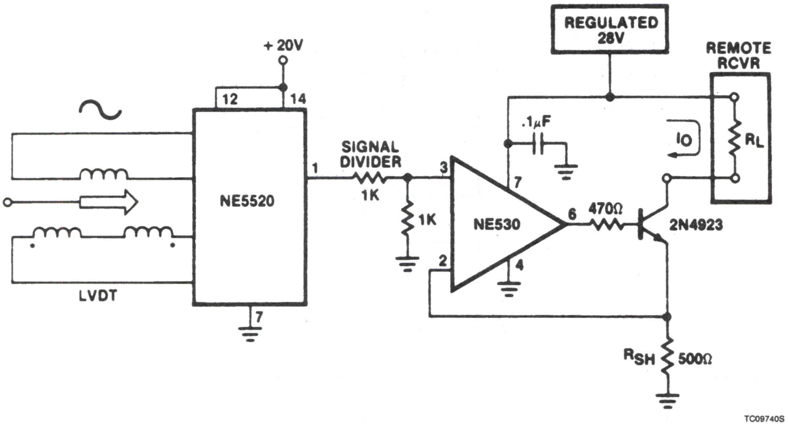

+20
12
14
NE5520
LVDT
AUX AMP
+VCC
+20V
3
8
OUTPUT SIGNAL
1/2 NE532
LONG WIRE LINE
RECORDER
1
2
IO
RL
VR/2
8
7
R1
10K
RL 100-600Ω
5
R2
200Ω
BUFFERED VR/2
1/2 NE532
7
6
5mA/VOLT
TC09730S

Figure 22. NE5520 With Bipolar Current Loop Output ± 10mA FS — Single Supply Operation


REGULATED 28V
+20V
REMOTE RCVR
12
14
.1μF
IO
RL
SIGNAL DIVIDER
1
1K
3
7
NE5520
1K
NE530
6
470Ω
2N4923
2
4
LVDT
7
RSH
500Ω
TC09740S

NOTES:
- Sensitivity 2mA/V.
- LVDT null occurs at 10mA outpt, i.e., half-scale.

Figure 23. NE5520 With Unipolar Current Source

Using the LVDT Signal Conditioner AN118

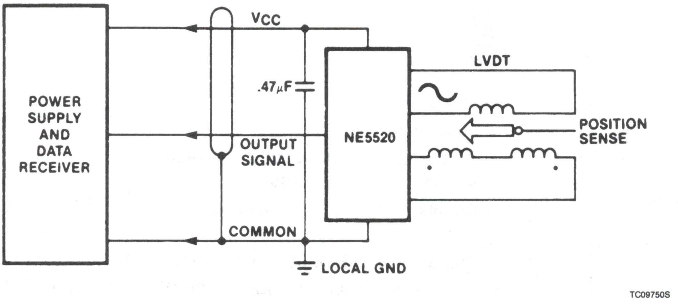

POWER SUPPLY AND DATA RECEIVER
VCC
.47μF
OUTPUT SIGNAL
COMMON
LOCAL GND
NE5520
LVDT
POSITION SENSE
TC09750S

Figure 24. Positioning the NE/SE5520 LVDT 3-Wire Remote Demodulator Sensing Head

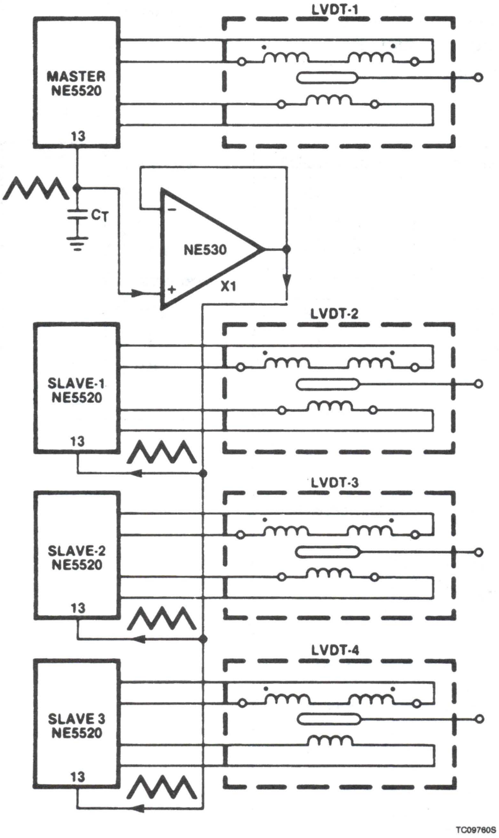

LVDT-1
MASTER NE5520
13
CT
NE530
X1
LVDT-2
SLAVE-1 NE5520
13
LVDT-3
SLAVE-2 NE5520
13
LVDT-4
SLAVE 3 NE5520
13
TC09760S

Figure 25. Multiple Transducer Operation — Synchronous Oscillator Mode

REFERENCES

Handbook of Measurement and Control, Revised Edition 1976, by Edward Herceg, Schaevitz Engineering Publication, Pennsauken, New Jersey.

Handbook of Integrated-Circuit Operational Amplifiers, by George B. Rutkowski, Prentice Hall 1975, Englewood Cliffs, New Jersey.

Signetics

NE/SA/SE5521
LVDT Signal Conditioner

Product Specification

Linear Products

DESCRIPTION

The SA/SE/NE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LDVTs) and Rotary Variable Differential Transformers (RVDTs). The chip includes a low distortion, amplitude-stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

FEATURES

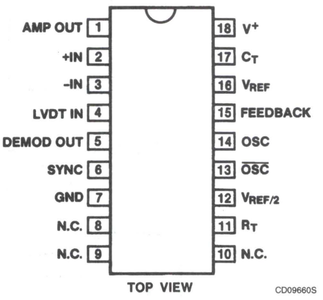
- **Low distortion**
- **Single supply 5V to 20V, or dual supply ±2.5V to ±10V**
- **Oscillator frequency 1kHz to 20kHz**
- **Capable of ratiometric operation**
- **Low power consumption (182mV typ)**

APPLICATIONS

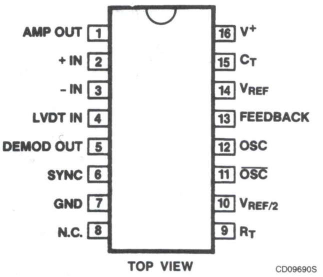
- **LVDT signal conditioning**
- **RVDT signal conditioning**
- **LPDT signal conditioning**
- **Bridge circuits**

PIN CONFIGURATIONS

F, N Packages


AMP OUT 1
+IN 2
-IN 3
LVDT IN 4
DEMOD OUT 5
SYNC 6
GND 7
N.C. 8
N.C. 9
18 V+
17 CT
16 VREF
15 FEEDBACK
14 OSC
13 OSC
12 VREF/2
11 RT
10 N.C.
TOP VIEW
CD09660S

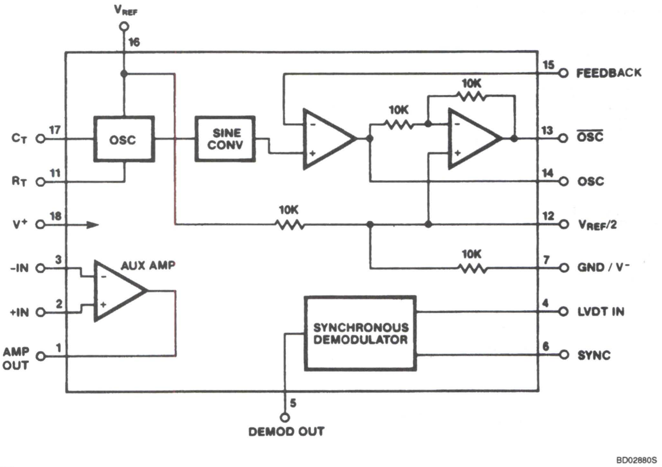
D Package


AMP OUT 1
+IN 2
-IN 3
LVDT IN 4
DEMOD OUT 5
SYNC 6
GND 7
N.C. 8
16 V+
15 CT
14 VREF
13 FEEDBACK
12 OSC
11 OSC
10 VREF/2
9 RT
TOP VIEW
CD09690S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP	0 to +70°C	NE5521N
18-Pin Cerdip	0 to +70°C	NE5521F
16-Pin SO DIP	0 to +70°C	NE5521D
18-Pin Plastic DIP	-40°C to +85°C	SA5521N
18-Pin Cerdip	-55°C to +125°C	SE5521F
16-Pin SO DIP	-40°C to +85°C	SA5521D

BLOCK DIAGRAM


VREF
16
15 FEEDBACK
10K
10K
CT 17
OSC
SINE CONV
13 OSC
RT 11
14 OSC
V+ 18
10K
12 VREF/2
10K
-IN 3
AUX AMP
7 GND / V-
+IN 2
4 LVDT IN
SYNCHRONOUS DEMODULATOR
AMP OUT 1
6 SYNC
5
DEMOD OUT
BD02880S

NOTE:
Pin numbers are for F, N packages.

LVDT Signal Conditioner NE/SA/SE5521

PIN DEFINITIONS FOR D, F AND N PACKAGES

PIN NO.		SYMBOL	DEFINITION
D	F, N		
1	1	Amp Out	Auxiliary Amplifier Output.
2	2	+IN	Auxiliary Amplifier non-inverting input.
3	3	−IN	Auxiliary Amplifier inverting input.
4	4	LVDT IN	Input to Synchronous Demodulator from the LVDT/RVDT secondary.
5	5	DEMOD OUT	Pulsating DC output from the Synchronous Demodulator output. This voltage should be filtered before use.
6	6	SYNC	Synchronizing input for the Synchronizing Demodulator. This input should be connected to the OSC or $\overline{\text{OSC}}$ output. Sync is referenced to $V_{REF}/2$.
7	7	GND	Device return. Should be connected to system ground or to the negative supply.
8	8	NC	No internal connection.
—	9	NC	No internal connection.
—	10	NC	No internal connection.
9	11	R_T	A temperature stable 18kΩ resistor should be connected between this pin and Pin 7.
10	12	$V_{REF}/2$	A high impedance source of one half the potential applied to V_{REF}. The LVDT/RVDT secondary return should be to this point. A bypass capacitor with low impedance at the oscillator frequency should also be connected between this pin and ground.
11	13	$\overline{\text{OSC}}$	Oscillator sine wave output that is 180° out of phase with the OSC signal. The LVDT/RVDT primary is usually connected between OSC and $\overline{\text{OSC}}$ pins.
12	14	OSC	Oscillator sine wave output. The LVDT/RVDT primaries are usually connected between OSC and $\overline{\text{OSC}}$ pins.
13	15	FEEDBACK	Usually connected to the OSC output for unity gain, a resistor between this pin and OSC, and one between this pin and ground can provide for a change in the oscillator output pin amplitudes.
14	16	V_{REF}	Reference voltage input for the oscillator and sine converter. This voltage MUST be stable and must not exceed +V supply voltage.
15	17	C_T	Oscillator frequency-determining capacitor. The capacitor connected between this pin and ground should be a temperature-stable type.
16	18	+V	Positive supply connection.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+20	V
	Split supply voltage	±10	V
T_A	Operating temperature range		
	NE5521	0 to +70	°C
	SA5521	−40 to +85	°C
	SE5521	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation[1]	910	mW

NOTE:

1. For derating, see typical power dissipation versus load curves (Figure 1).

DC ELECTRICAL CHARACTERISTICS

$V+ = V_{REF} = 10V$, $T_A = 0$ to 70°C for NE5521, $T_A = -55$ to $+125°C$ for SE5521, $T_A = -40$ to $+85°C$ for SA5521, Frequency = 1kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NE5521			SA/SE5521			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply current			12.9	20		12.9	18	mA
I_{REF}	Reference current			5.3	8		5.3	8	mA
V_{REF}	Reference voltage range		5		V+	5		V+	V
P_D	Power dissipation			182	280		182	260	mW
Oscillator Section									
	Oscillator output	$R_L = 10k\Omega$		$\frac{V_{REF}}{8.8}$			$\frac{V_{REF}}{8.8}$		V_{RMS}
THD	Sine wave distortion	No load		1.5			1.5		%
	Initial amplitude error	$T_A = 25°C$		0.4	±3		0.4	±3	%
	Tempco of amplitude			0.005	0.01		0.005	0.01	%/°C
	Init. accuracy of oscillator freq.	$T_A = 25°C$		±0.9	±5		±0.9	±5	%
	Temperature coeff. of frequency[1]			0.05			0.05		%/°C
	Voltage coeff. of frequency			2.5			3.3		%/ $V(V_{REF})$
	Min OSC ($\overline{OSC}$) Load[2]		300	170		300	170		=0m
Demodulator Section									
ϵ_r	Linearity error	$5V_{P-P}$ input		±0.05	±0.1		±0.05	±0.1	%FS
	Maximum demodulator input				$\frac{V_{REF}}{2}$		$\frac{V_{REF}}{2}$		V_{P-P}
V_{OS}	Demodulator offset voltage			±1.4	±5		±1.4	±5	mV
TCV_{OS}	Demodulator offset voltage drift			5	25		5	25	μV/°C
I_{BIAS}	Demodulator input current		-600	-234		-500	-234		nA
	$V_{R/2}$ accuracy			±0.1	±1		±0.1	±1	%
Auxiliary Output Amplifier									
V_{OS}	Input offset voltage			±0.5	±5		±0.5	±5	mV
I_{BIAS}	Input bias current		-600	-210		-500	-210		nA
I_{OS}	Input offset current			10	50		10	50	nA
A_V	Gain		100	385		100	385		V/mV
SR	Slew rate			1.3			1.3		V/μs
GBW	Unity gain bandwidth product	$A_V = 1$		1.6			1.6		MHz
	Output voltage swing	$R_L = 10k\Omega$	7	8.2		7	8.2		V
	Output short circuit current to ground or to V_{CC}	$T_A = 25°C$		42	100		42	100	mA

NOTES:

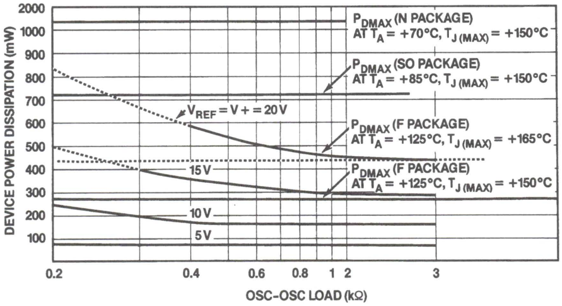
1. This is temperature coefficient of frequency for the device only. It is assumed that C_T and R_T are fixed in value and C_T leakage is fixed over the operating temperature range.
2. Minimum load impedance for which distortion is guaranteed to be less than 5%.

DEFINITION OF TERMS

Oscillator Output	RMS value of the AC voltage available at the oscillator output pin. This output is referenced to $V_{REF/2}$ and is a function of V_{REF}.
Sine Wave Distortion	The Total Harmonic Distortion (THD) of the oscillator output with no load. This is not a critical specification in LVDT/RVDT systems. This figure could be 15% or more without affecting system performance.
Initial Amplitude Error	A measure of the interchangeability of NE/SA/SE5521 parts, *not* a characteristic of any one part. It is the degree to which the oscillator output of a number of NE/SA/SE5521 samples will vary from the median of that sample.
Initial Accuracy of Oscillator Frequency	Another measure of the interchangeability of individual NE/SA/SE5521 parts. This is the degree to which the oscillator frequency of a number of NE/SA/SE5521 samples will vary from the median of that sample with a given timing capacitor.
Tempco of Oscillator Amplitude	A measure of how the oscillator amplitude varies with ambient temperature as that temperature deviates from a 25°C ambient.
Tempco of Oscillator Frequency	A measure of how the oscillator frequency varies with ambient temperature as that temperature deviates from a 25°C ambient.
Voltage Coeffecient of Oscillator Frequency	The degree to which the oscillator frequency will vary as the reference voltage (V_{REF}) deviates from +10V.
Min OSC ($\overline{OSC}$) Load	Minimum load impedance for which distortion is guaranteed to be less than 5%.
Linearity Error	The degree to which the DC output of the demodulator/amplifier combination matches a change in the AC signal at the demodulator input. It is measured as the worst case nonlinearity from a straight line drawn between positive and negative fullscale end points.
Maximum Demodulator Input	The maximum signal that can be applied to the demodulator input without exceeding the specified linearity error.

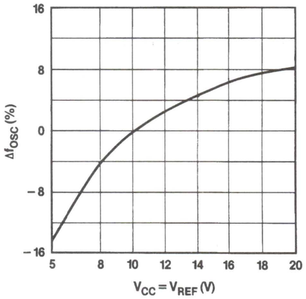
APPLICATION INFORMATION

$$\text{OSC frequency} = \frac{V_{REF} - 1.3V}{V_{REF}(R_T + 1.5k)C_T}$$



OP18050S

Figure 1. Device Power Dissipation vs OSC - $\overline{OSC}$ Load at +25°C



OP18060S

Figure 2. Oscillator Frequency Variation With Voltage (Normalized to $V_{REF} = V_{CC}$=10V) T_A = +25°C

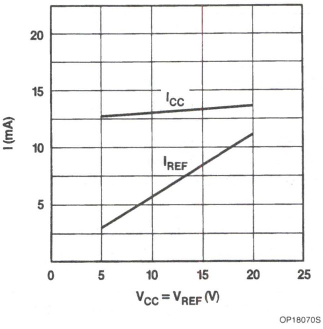


Figure 3. I_{REF} and I_{CC} vs Voltage ($T_A = +25°C$)

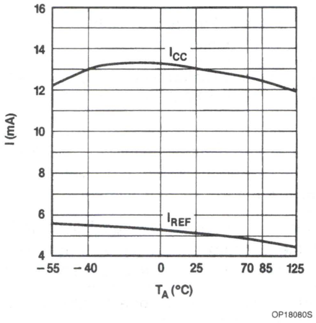


Figure 4. I_{REF} and I_{CC} vs Temperature ($V_{REF} = V_{CC} = 10V$)

Signetics

AN1181

NE/SE5521 Simplifies Modulated Light Source Design

Linear Products

Application Note

Author: Zahid Rahim

Photoelectric light sources and detectors are widely used for detecting motion and the absence or presence of objects. The major advantage with photoelectric sensors is that one can sense the target without making any physical contact with it. Although the NE5521 chip is designed to interface with position transducers, it is possible to take advantage of the chip's functional blocks to configure a transmitter and a receiver for a modulated light source device (see Figure 1).

By using an incandescent light source (or an LED because of its long life) and a photosensor which produces current in response to the infrared (IR) light striking it, a transimpedance amplifier will convert the photosensor current to voltage. However, there are several disadvantages with the above approach. Incandescent light source devices cannot be used outdoors in the sunlight or near high intensity sources such as welding arcs, strobe lamps, and mercury lamps, because the IR light radiated from such sources can provide a false output at the receiver. Also, they are generally not recommended for applications where vibration can cause misalignment between the emitter and the receiver.

By frequency modulating the transmitter and tuning the receiver to respond only to the modulating frequency, undesirable modulation frequencies can be electronically filtered out. Due to the high degree of ambient light rejection and noise immunity, the modulated light source devices are thus not significantly affected by direct or diffused exposure to sunlight or by indirect or diffused exposure to mercury lamps or welding arcs. Ambient light rejection can be increased further by tuning the receiver to look for the proper phase of the modulating signal. Modulated light source devices also offer the advantage of greater scanning distance, greater penetration through contaminated environments, and effective use for applications where the emitter and/or receiver may be subject to high vibration.

For the circuit in Figure 1, the oscillator output of the NE5521 chip produces a sine wave referenced to $V_{R/2}$ (in this case 5V) which causes the LM311 comparator to pulse the LED (Light Emitting Diode) at a high current level. In response to such an excitation, the LED produces high energy infrared pulses that can travel long distances and penetrate severely contaminated environments.

The photodiode in the photoreceiver produces pulsating currents in response to the IR light striking it. A pulsed signal thus appears at the anode of the photodiode. The uncommitted amplifier of the NE5521 chip is configured as an AC-coupled amplifier with gain. Keep in mind that ambient light produces a DC voltage at the photoreceiver; however, capacitor C_1 blocks the DC voltage and allows only AC signals to pass through. The cutoff frequency is given by the following equation:

$$f_{CO} = \frac{1}{(2\pi R_1 C_1)}$$

At the frequency of interest, you can consider the capacitor to be a short circuit. Thus the uncommitted amplifier operates as an inverter with gain, the gain being determined by the ratio of R_2 and R_1. Since the non-inverting input of the amplifier is connected to the $V_{R/2}$ pin, the AC signal arising from the photoreceiver is referenced to $V_{R/2}$.

The receiver part of the NE5521 chip is comprised of the synchronous demodulator which provides precise rectification of the amplified photoreceiver signal in sync with the modulating signal of the LED. The modulating signal of the LED also drives the demodulator's comparator, which compares the modulating signal with the $V_{R/2}$ reference voltage (Figure 2). When the demodulator's sync input signal is below $V_{R/2}$, the demodulator inverts the AC input signal. When the sync signal is above the $V_{R/2}$ voltage, however, the AC signal passes through the follower to the output. As a result, the demodulator's full wave rectification occurs in sync with the demodulator's input signal. Synchronously rectifying (demodulating) the square wave AC signal from the photoreceiver produces a DC signal at the demodulator output (Figure 3). A simple RC filter at the demodulator output filters out any spurious noise and transients generated at the switching points. When the IR light source is blocked, no AC signal arises from the photoreceiver. Thus, the demodulator output is biased at $V_{R/2}$ (5V in this case). For the circuit in Figure 1, the voltage at the output of the filter is 2.9V when the light source is uninterrupted. However, the output voltage changes to 5V when the light source is interrupted. One can thus apply the output signal to a level detector that energizes an external device, such as a switch or an alarm, whenever an object interrupts the light source.

A timing resistor of fixed value ($R_T = 18k\Omega$) and a variable timing capacitor (C_T) determine the frequency of the NE5521 chip's internal oscillator. The oscillator output signal's frequency (which is also the modulating signal of the LED) can be calculated from the equation below.

$$f_{OSC} = \frac{(V_R - 1.3V)}{[V_R(R_T + 1.5k\Omega)C_T]}$$

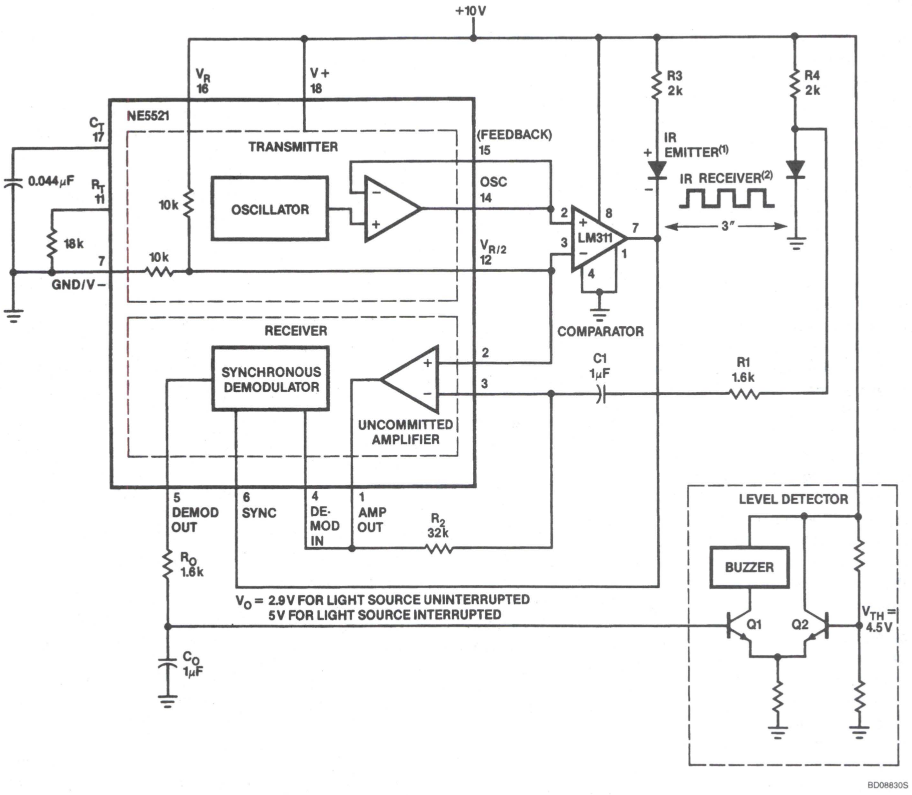
When the scanning distance between the emitter and the receiver is increased, the sensitivity of the receiver decreases. There are, however, two ways of increasing the receiver sensitivity — reducing R_3, which has the effect of increasing the intensity of the pulsed beam, or increasing the gain of the uncommitted amplifier, or using a combination of the two. When the gain of the amplifier is increased, keep in mind that the output swing of the amplifier should not be large enough to saturate the amplifier.

IMPROVE AMBIENT LIGHT REJECTION BY PHASE DETECTION

Nearly perfect rejection of ambient light can be achieved by tuning the receiver section of the NE5521 chip to look for the proper phase of the modulating signal (Figure 4). Here, the synchronous demodulator is operated as a phase detector. The sine wave signal from the oscillator (which is also the modulating signal of the LED) is the demodulator input signal. The amplified photoreceiver signal (referenced to 5.45V) is the sync input of the demodulator. When the light source is interrupted, the 5.45V at the sync input causes the demodulator's comparator to allow the AC signal at the demodulator's input to pass through to the output. The output filter puts out a 5V DC signal (zero-scale voltage).

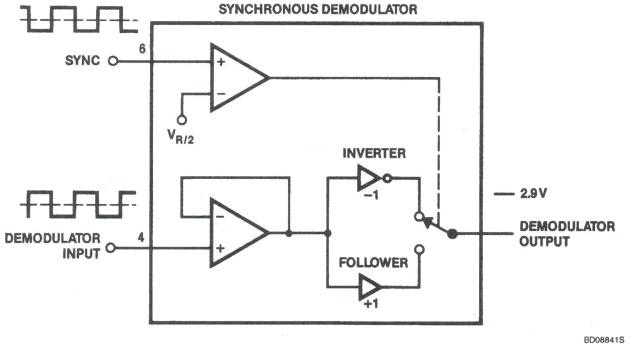
When the light source is uninterrupted, however, the demodulator puts out a full-wave rectified signal of negative polarity (Figure 5). The DC signal at the output filter is the negative full-scale voltage ($-V_{FS}$) and is less than 5V. For any other modulation frequency (available from nearby IR sources such as welding arcs, strobe lamps, and mercury lamps), the output filter's voltage is close to

– V_{FS}. False triggering of the receiver in the presence of undesirable modulation frequencies is thus eliminated since the demodulator puts out a 5V DC signal only when the light source is completely blocked. The level detector can be set up so that a relay or an alarm is energized only when the filter's output is at 5V. Keep in mind that the gain of the uncommitted amplifier should be large enough so that the pulsed signal at the sync input swings above and below the $V_{R/2}$ voltage so as to enable the demodulator's comparator to switch the demodulator input signal between the follower and the inverter.


+10V
V_R 16
V+ 18
NE5521
C_T 17
0.044µF
R_T 11
18k
7
GND/V–
TRANSMITTER
10k
OSCILLATOR
10k
(FEEDBACK) 15
OSC 14
$V_{R/2}$ 12
2
3
8
7
1
4
LM311
COMPARATOR
R3 2k
R4 2k
IR EMITTER(1)
IR RECEIVER(2)
3″
RECEIVER
SYNCHRONOUS DEMODULATOR
UNCOMMITTED AMPLIFIER
2
3
C1 1µF
R1 1.6k
5 DEMOD OUT
6 SYNC
4 DE-MOD IN
1 AMP OUT
R_2 32k
R_O 1.6k
C_O 1µF
V_O = 2.9V FOR LIGHT SOURCE UNINTERRUPTED 5V FOR LIGHT SOURCE INTERRUPTED
LEVEL DETECTOR
BUZZER
Q1
Q2
V_{TH} = 4.5V
BD08830S

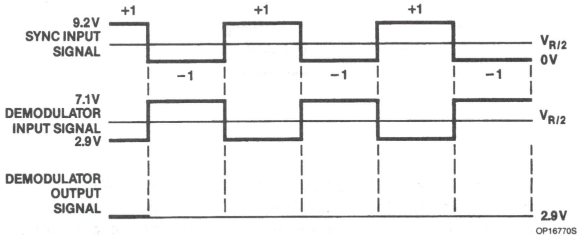
NOTES:
1. IR Emitter = FE-MTEI, microswitch.
2. IR Receiver = FE-MTRI, microswitch.

Figure 1. In a Typical Modulated Light Source Device, a High Degree of Ambient Light Rejection can be Achieved When the NE5521's Oscillator is Used to Frequency-Modulate an LED and the Demodulator is Used to Synchronously Rectify the Photoreceiver's AC Signal. DC Signal Produced by Ambient Light is Rejected by AC-Coupling NE5521's Uncommitted Amplifier


SYNCHRONOUS DEMODULATOR
SYNC
6
+
−
$V_{R/2}$
INVERTER
−1
2.9V
DEMODULATOR OUTPUT
DEMODULATOR INPUT
4
FOLLOWER
+1
BD08841S

NOTE:
When the comparator's input is synchronized with the demodulator input signal, the circuit precisely rectifies the demodulator's input signal.

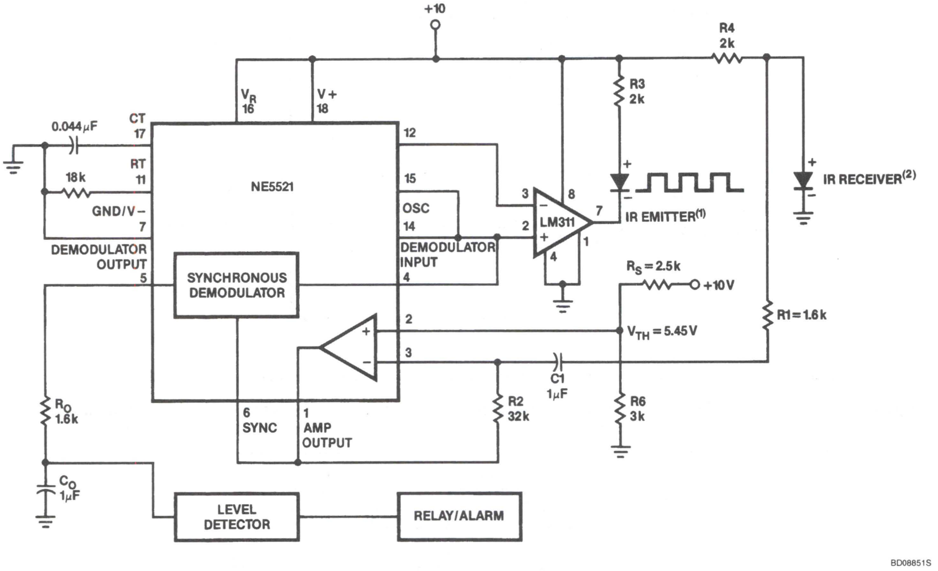
Figure 2. The NE5521's Demodulator Circuit Switches the Output Line Between an Inverter and a Follower


+1
+1
+1
9.2V
SYNC INPUT SIGNAL
$V_{R/2}$
0V
−1
−1
−1
7.1V
DEMODULATOR INPUT SIGNAL
2.9V
$V_{R/2}$
DEMODULATOR OUTPUT SIGNAL
2.9V
OP16770S

NOTE:
However, when the sync input signal is below $V_{R/2}$, the demodulator's input signal appears inverted at the output. By synchronously rectifying a square wave AC signal at the demodulator input, the circuit produces a DC signal at the demodulator output.

Figure 3. When the Demodulator's Sync Input Signal is Above $V_{R/2}$, the Demodulator's Output Follows the Demodulator's Input Signal

NE/SE5521 Simplifies Modulated Light Source Design AN1181


+10
R4
2k
R3
2k
V_R
16
V+
18
0.044µF
CT
17
RT
11
18k
NE5521
GND/V−
7
12
15
OSC
14
DEMODULATOR OUTPUT
5
DEMODULATOR INPUT
4
SYNCHRONOUS DEMODULATOR
3
2
8
7
1
4
LM311
IR EMITTER(1)
IR RECEIVER(2)
R_S = 2.5k
+10V
R1 = 1.6k
V_{TH} = 5.45V
C1
1µF
R_O
1.6k
R2
32k
R6
3k
6
SYNC
1
AMP OUTPUT
C_O
1µF
LEVEL DETECTOR
RELAY/ALARM
BD08851S

NOTES:
1. IR Emitter = FE-MTEI, microswitch.
2. IR Receiver = FE-MTRI, microswitch.

Figure 4. When the NE5521's Receiver is Tuned to Look for the Proper Phase of the Modulating Signal, Optimum Rejection of Undesirable Modulation Frequencies (Produced by High Intensity IR Light Sources Such as Welding Arcs, Strobe Lamps, and Mercury Lamps) Can be Achieved

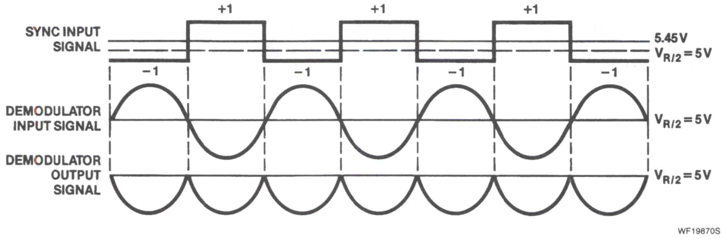

SYNC INPUT SIGNAL
+1
+1
+1
−1
−1
−1
−1
5.45V
V_{R/2} = 5V
DEMODULATOR INPUT SIGNAL
V_{R/2} = 5V
DEMODULATOR OUTPUT SIGNAL
V_{R/2} = 5V
WF19870S

Figure 5. When a Sinusoidal Signal at the Demodulator Input That is 180° Out of Phase With the Sync Input Signal is Synchronously Rectified (as is the Case With the Circuit in Figure 4), the Circuit Puts Out a Full-Wave Rectified Signal of Negative Polarity. If the Phase Difference Between the Sync Input Signal and the Demodulator Input Signal Changes, the Demodulator Output Signal Also Changes Relative to the Phasing of the two Input Signals

AN1182
Using the NE5521 Signal Conditioner in Multi-Faceted Applications

Application Note

Author: Zahid Rahim

Position transducers call for a great deal of complex interface circuitry for input and output signal conditioning. The Signetics NE/SA/SE5521 packs all the interface circuitry on one chip and provides a complete monolithic solution to all the signal conditioning required for position transducers.

Position transducers are widely used in industrial and commercial applications for measuring very small displacement or rotation. In fact, such transducers can be used for any application where a given parameter can be converted to linear or angular motion. Weight, force, pressure, torque, and acceleration are often converted to linear displacement or linear rotation using position transducers. The displacement or rotation information is next conditioned to provide an accurate measurement of the parameter.

SE5521 can interface with all of the popular position transducers such as the LVDT, RVDT, and LPDT. In addition, by varying the arrangement of external components, you can also configure a phase detector, an AC bridge circuit, and an AC voltmeter. For a brief description of the IC, see the section entitled "A Look at the Signal Conditioning IC."

IC PROVIDES SINGLE-CHIP SOLUTION TO LVDT MEASUREMENTS

Figure 1a shows a typical single supply LVDT displacement measurement circuit. The uncommitted amplifier is configured as a second-order, low-pass Butterworth filter with gain. The gain of the amplifier is $1 + R_F/(R/2)$. The 1k offset adjust potentiometer is used to trim out the LVDT/signal conditioner system offset at null.

Exciting an LVDT at zero phase angle frequency results in minimum null voltage and optimum linearity (for a discussion, see "How an LVDT Works"). There are two ways of reducing null voltage — the first method is to adjust the oscillator frequency so that the secondary voltage is in phase with the primary excitation. The demodulator and oscillator voltage can be monitored on an oscilloscope for correct phasing as depicted in Figures 1b and 1c. A second method of phase compensation is to use a variable phase shift network between the oscillator output and the sync input to the device. An optional phase shift network in Figure 1a consists of a 20k phase adjust potentiometer in series with capacitor C_3. The potentiometer is adjusted for correct demodulator phasing as illustrated in Figures 1b and 1c. With $R_O = 10k$, $C_O = 2nF$, and at oscillator frequency, $f_{OSC} = 2900Hz$, the phase shift is $\varphi = -\tan^{-1}(\omega R_O C_O) = -20°$.

The LVDT output is referenced to $V_{R/2}$ by tying one end of the secondary to Pin 12 of the device. A capacitor between Pin 12 and ground provides an AC ground for $V_{R/2}$. Since the output of Pin 12 is a source of high impedance, Pin 12 may need to be buffered in some applications so as to prevent loading effects on the voltage divider. The common mode voltage and the RMS value of the oscillator signals are determined by V_R; consequently, V_R should be a fixed reference voltage. By making V+ greater than V_R, the output swing of the auxiliary amplifier is increased and the filter can accommodate higher closed-loop gain.

The demodulator output has positive polarity when the LVDT output signal is 180° out of phase with the primary excitation (see Figure 1d), and has negative polarity when the LVDT output is in phase with the primary excitation (see Figure 1e). The polarity of the demodulator signal indicates on which side of null the core is while the amplitude indicates the relative displacement of the core from the null position.

Filtered DC output appears at Pin 1 of the device. Measurements with 10-bit accuracy at −55°C to +125°C temperature range are easily achieved by the circuit in Figure 1.

PHASE DETECTOR MEASURES PHASE DIFFERENCE WITH 10-BIT ACCURACY

The synchronous demodulator easily lends itself to phase detection as illustrated in Figure 2a. If signals of identical frequency are applied to sync input (Pin 6) and to the demodulator input (Pin 4), respectively, the demodulator functions as a phase detector with output DC component being proportional to phase difference between the two inputs. The signals must be referenced to 0V for dual supply operation or to $V_{R/2}$ for single supply operation. At ±5V supplies, the demodulator can easily handle 7V peak-to-peak signals. The low-pass network configured with the uncommitted amplifier provides DC output at Pin 1 of the device. The DC output is maximum (+full-scale) when V_1 and V_2 are 180° out of phase (see Figure 1d) and minimum (−full-scale) when the signals are in phase (see Figure 1e). At quadrature ($\varphi = 90°$), the DC output is 0V as shown in Figure 2b. By calibrating the −FS, 0, and +FS points, any unknown phase difference may be determined by just measuring the DC output at Pin 1. A linear relationship between the DC output and phase difference is shown by the transfer curve in Figure 2c.

Even though the oscillator signals are not utilized in this particular application, the use of C_T and R_T is still recommended in order to prevent saturation of active devices in the IC.

SIGNAL CONDITIONER EASES LPDT MEASUREMENTS

Figure 3 shows a simple dual supply setup for LPDT measurements. Op amp IC_1 is configured as a low-pass filter with cut-off frequency equal to the oscillator frequency of 2900Hz. The filter attenuates the higher order spectral components of the oscillator signal and produces a low-distortion sine wave at the output. This sine wave excites one primary, while the other primary is excited by a cosine wave produced by amp IC_2. Amp IC_2 is configured as a constant amplitude lag circuit that preserves the amplitude of the sine wave input from IC_1, but phase shifts the signal by 90° at the output. The phase shift, φ, is given by $\varphi = -2\tan^{-1}(2\pi f_{OSC} R_5 C_3)$. Thus, at 90° phase shift, $f_{OSC} = 1/(2\pi R_5 C_3)$. R_5 is a 10k potentiometer with its center wiper tied to one end. The potentiometer is tweaked and the wave forms from IC_1 and IC_2 are observed on an oscilloscope for 90° phase difference and 0V at the output of the device (Pin 1). The system is now ready to make phase measurements as discussed earlier.

For dual supply operation, both the positive and negative supplies should be closely regulated since the oscillator common mode voltage varies with the supplies.

AC BRIDGE CALIBRATES RESISTORS AND CAPACITORS WITH 10-BIT ACCURACY

An AC bridge, shown in Figure 4, provides a simple and cost-effective solution to matching resistors and capacitors on production

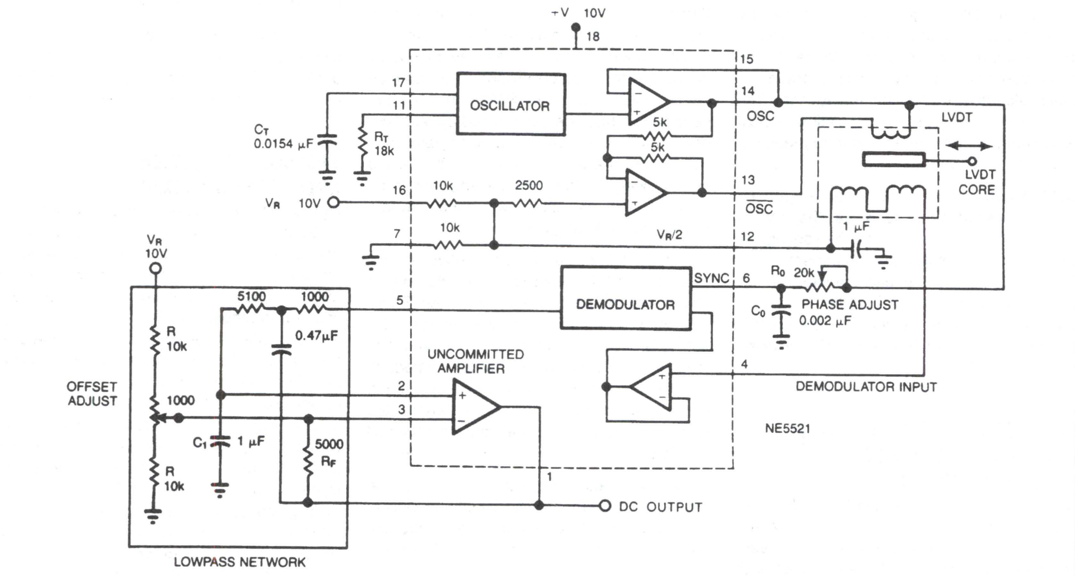
Using the NE5521 Signal Conditioner in Multi-Faceted Applications

lines. Impedances Z_R and Z_X form a half-bridge, while OSC and $\overline{OSC}$ excite the bridge differentially. The external op amp is a JFET input amplifier (LF356) with very low input bias current on the order of 30pA (typical). C_1 allows AC coupling by blocking the DC common mode voltage from the bridge, while R_1 biases the output of LF356 to 0V at DC. Use of FET input op amp insures that DC offset due to bias current through R_1 is negligible. AC output of the demodulator is filtered via the uncommitted amp to provide DC voltage for the meter. The 10k potentiometer, R_5, limits the current into the meter to a safe level. Calibration begins by placing equal impedances at Z_R and Z_X, and the system offset is nulled by the offset adjust circuit so that Pin 1 is at 0V. Next, known values are placed at Z_X and the meter deviations are calibrated. The bridge is now ready to measure an unknown impedance at Z_X with ±0.05% accuracy or better.

RMS-TO-DC CONVERTER YIELDS 10-BIT ACCURACY

An AC voltmeter may be easily constructed as in Figure 5; the simplicity of the circuit and low component count make it particularly attractive. The demodulator output is a full-wave rectified signal from the AC input at Pin 4. DC component of the rectified signal at Pin 5 varies linearly with the RMS input at Pin 4 and thus provides an accurate RMS-to-DC conversion at the output of the filter (Pin 1). C_T is a variable capacitor that is tweaked until the oscillator signal to the sync input of the demodulator is in phase with the AC signal at Pin 4.

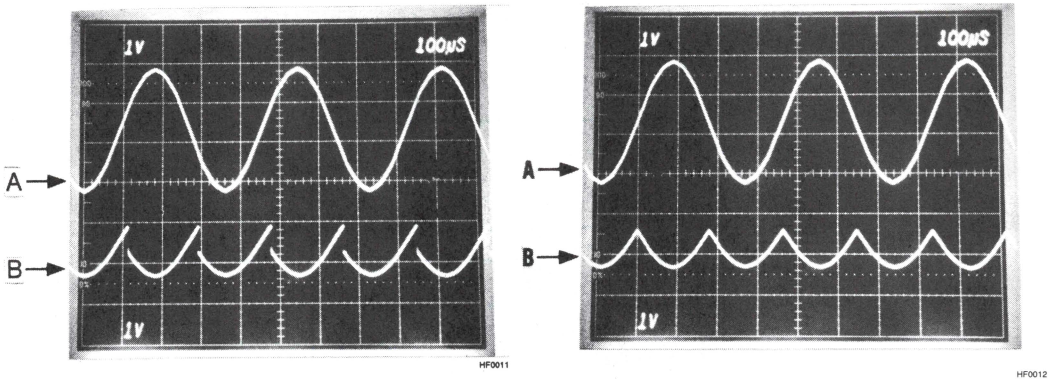
In many applications it may not be desirable to adjust C_T each time the AC signal frequency changes. An alternate approach is to use a zero-crossing detector to excite the sync input of the device. The LM311 comparator in Figure 6 produces a square wave (trace A in Figure 6b) in phase with the AC signal (trace B). Optimum rectification thus occurs at the demodulator output (trace C). For precision measurements at high frequencies, a fast, low offset comparator is recommended.


+V 10V
18
15
17
11
OSCILLATOR
14
OSC
5k
5k
LVDT
LVDT CORE
C_T 0.0154 µF
R_T 18k
16
10k
2500
V_R 10V
13
$\overline{OSC}$
7
10k
$V_R/2$
12
1 µF
V_R 10V
SYNC
6
R_0 20k
PHASE ADJUST
C_0
0.002 µF
DEMODULATOR
5100
1000
5
0.47µF
R 10k
UNCOMMITTED AMPLIFIER
4
DEMODULATOR INPUT
OFFSET ADJUST
1000
2
3
C_1 1 µF
5000 R_F
R 10k
NE5521
1
DC OUTPUT
LOWPASS NETWORK
BD08871S

NOTE:
V_R is a fixed reference voltage. OSC frequency, $f_{OSC} = 2.9kHz$. Phase shift, $\phi = -\tan^{-1}(\omega R_O C_O)$.

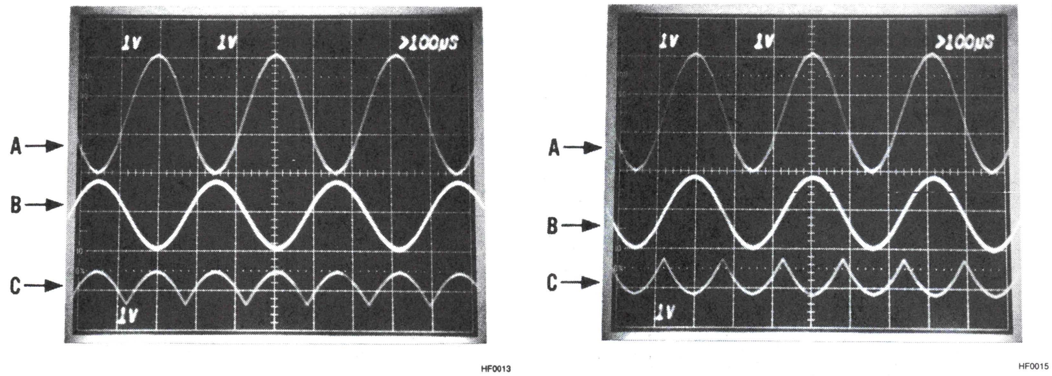
a. Typical Single Supply LVDT Measuring Circuit

Figure 1



b. Trace A is the Oscillator Signal and Trace B is the Demodulator Output Resulting from LVDT Phase Shift

c. Trace B is the Demodulator Output After Proper Phase Adjustment



d. With LVDT Output (Trace B) at 180° Out of Phase With Excitation Signal (Trace A), the Demodulator Output has Positive Polarity (Trace C)

e. Demodulator Output has Negative Polarity (Trace C) When LVDT Output (Trace B) is in Phase With Primary Signal (Trace A)

Figure 1 (Continued)

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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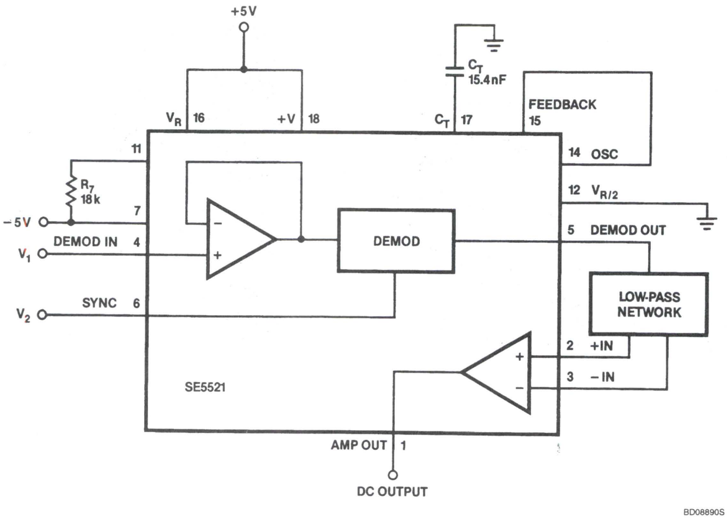
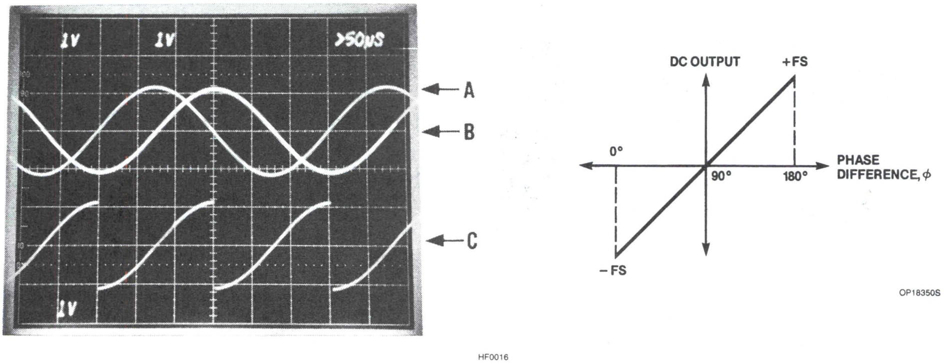

+5V
V_R
16
+V
18
C_T
15.4nF
C_T
17
FEEDBACK
15
11
14 OSC
R_7
18k
12 $V_{R/2}$
7
−5V
DEMOD IN 4
V_1
DEMOD
5 DEMOD OUT
LOW-PASS NETWORK
SYNC 6
V_2
2 +IN
3 −IN
SE5521
AMP OUT 1
DC OUTPUT
BD08890S

a. Phase Detector Measures Phase Difference Between Signals V_1 and V_2 and Provides DC Output at Pin 1



b. When V_1 and V_2 in (a) are at Quadrature (Traces A and B), the DC Component of Demodulator Output (Trace C) is at 0V

c. The DC Output and Phase Vary Linearly

Figure 2

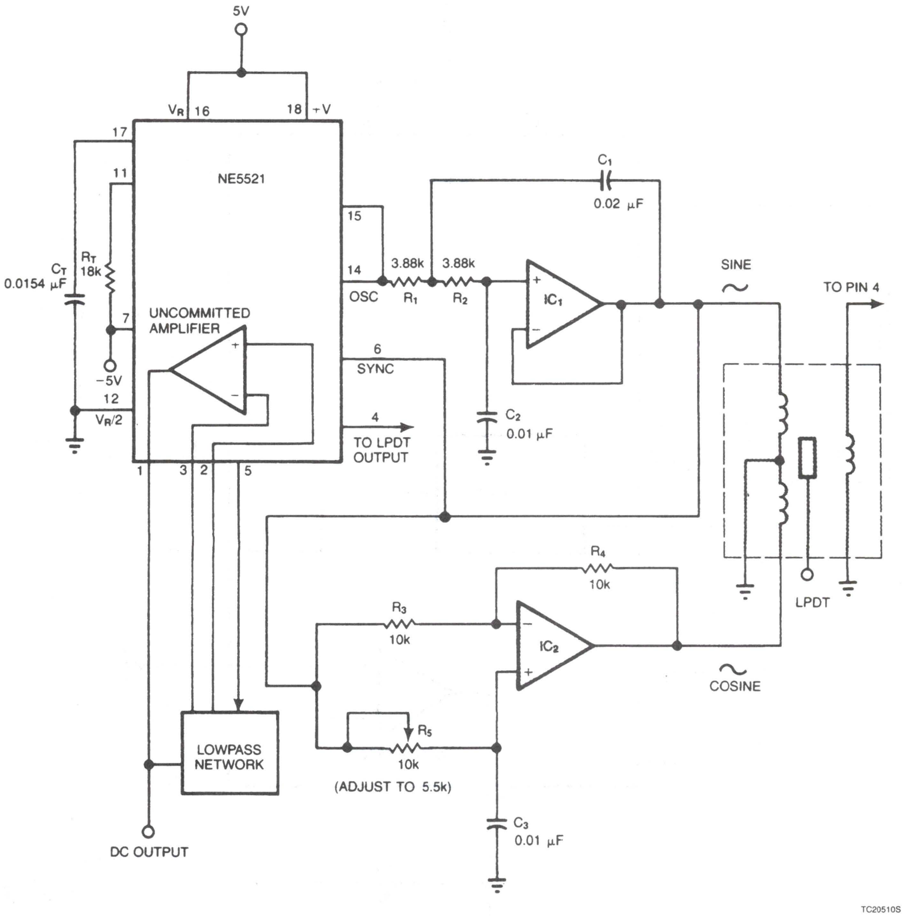

5V
VR 16
18 +V
17
11
NE5521
15
14
OSC
3.88k
R1
3.88k
R2
C1
0.02 µF
IC1
SINE
TO PIN 4
RT
18k
CT
0.0154 µF
7
UNCOMMITTED
AMPLIFIER
-5V
12
VR/2
6
SYNC
4
TO LPDT
OUTPUT
C2
0.01 µF
1
3
2
5
R4
10k
R3
10k
IC2
LPDT
COSINE
R5
10k
(ADJUST TO 5.5k)
LOWPASS
NETWORK
C3
0.01 µF
DC OUTPUT
TC20510S

Figure 3. LPDT Interface

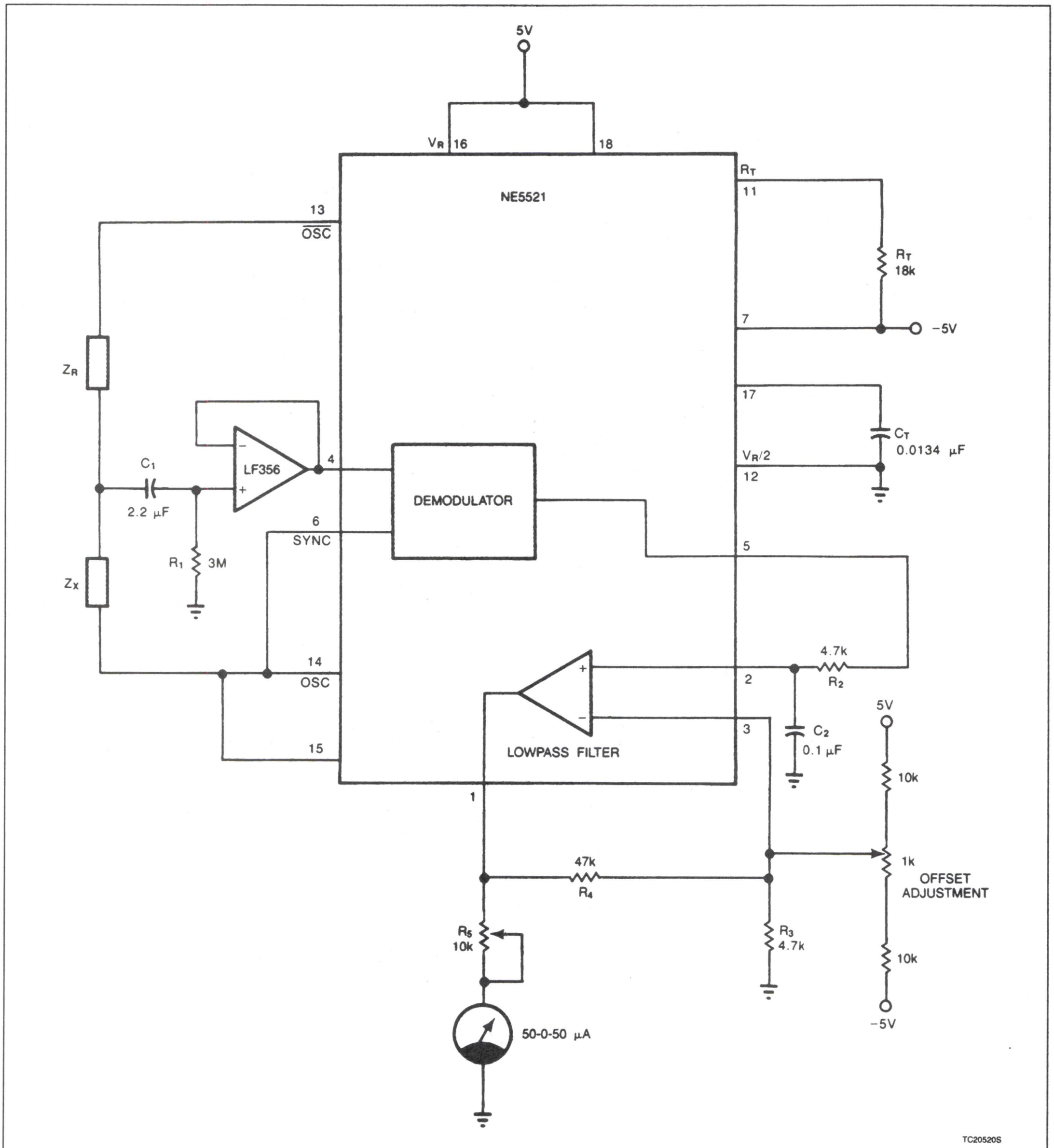
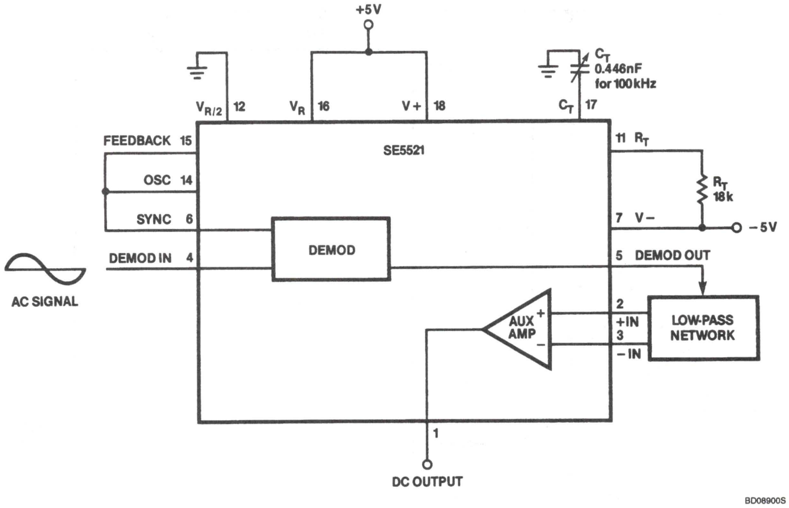

5V
VR 16
18
NE5521
RT 11
RT 18k
7
−5V
13
OSC
17
CT 0.0134 μF
VR/2 12
ZR
C1
2.2 μF
LF356
4
DEMODULATOR
6
SYNC
5
R1 3M
ZX
14
OSC
15
4.7k
R2
2
3
C2 0.1 μF
LOWPASS FILTER
5V
10k
1
47k
R4
1k
OFFSET ADJUSTMENT
R5 10k
R3 4.7k
10k
−5V
50-0-50 μA
TC20520S

Figure 4. Signal Conditioner Used as an AC Bridge to Calibrate Resistors/Capacitors

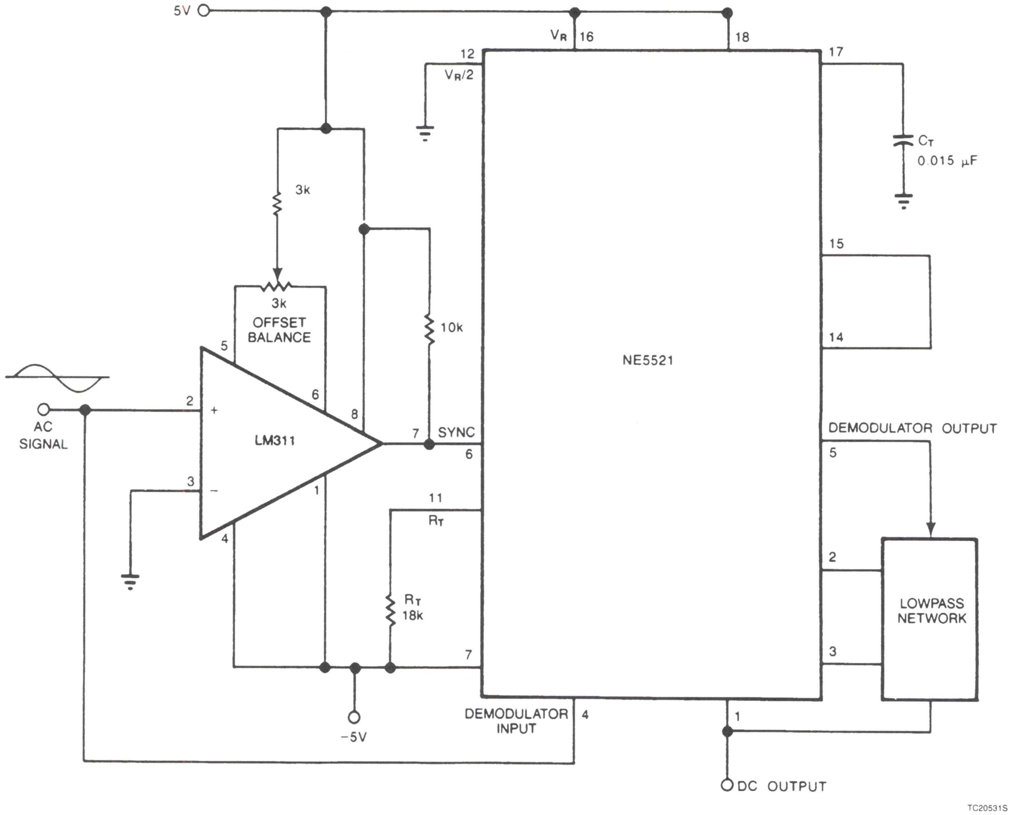
Using the NE5521 Signal Conditioner in Multi-Faceted Applications

AN1182


+5V
$V_{R/2}$ 12
V_R 16
V+ 18
C_T 0.446nF for 100kHz
C_T 17
SE5521
FEEDBACK 15
OSC 14
SYNC 6
DEMOD IN 4
AC SIGNAL
DEMOD
11 R_T
R_T 18k
7 V−
−5V
5 DEMOD OUT
AUX AMP
2 +IN
3 −IN
LOW-PASS NETWORK
1
DC OUTPUT
BD08900S

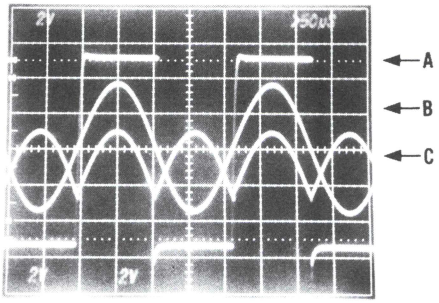
NOTE:
1. The DC output at Pin 1 varies linearly with the RMS input at Pin 4.
2. C_T is tweaked until the sync signal is in phase with the AC signal.

Figure 5. AC Voltmeter


5V
VR
16
18
12
VR/2
17
CT
0.015 µF
3k
3k
OFFSET
BALANCE
10k
15
14
NE5521
5
6
8
2
+
AC
SIGNAL
LM311
7
SYNC
6
3
−
1
11
RT
4
RT
18k
7
DEMODULATOR OUTPUT
5
2
3
LOWPASS
NETWORK
−5V
DEMODULATOR
INPUT
4
1
DC OUTPUT

TC20531S

a. AC Voltmeter. Comparator CI (LM311), Used as a Zero-Crossing Detector, Produces a Constant Amplitude Square Wave to Excite the Sync Input of the Demodulator. DC Output Appears at Pin 1



HF0014

b. Trace B is the AC Signal at the Comparator and Demodulator Input. The Output of the Zero-Crossing Detector (Trace A) at Sync Input Causes Synchronous Rectification at the Demodulator Output (Trace C). Auxiliary Amplifier Filter Produces DC Output at Pin 1

Figure 6

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

AN1182

APPENDIX I

A LOOK AT THE SIGNAL CONDITIONING IC

The signal conditioner essentially consists of three major blocks: an oscillator with programmable frequency, a synchronous demodulator, and an auxiliary amplifier (see Figure I).

The oscillator generates a stable amplitude sine wave with an RMS value determined by a fixed reference voltage, V_R, at Pin 16 of the device, and referenced to $V_{R/2}$. Next, the oscillator signal is buffered by two high-gain, low-offset op amps to produce the buffered oscillator signal, OSC, and the inverted signal, $\overline{OSC}$. The OSC and $\overline{OSC}$ signals exhibit less than 50ppm/°C amplitude drift (at −55°C to +125°C temperature range) with total harmonic distortion under 2%. OSC and $\overline{OSC}$ signals are used to differentially excite the primary of the LVDT/RVDT. A fixed 18k resistor, R_T (external to chip), and an external timing capacitor, C_T, determine the frequency of the oscillator. The oscillator frequency is given by the following: $f_{OSC} = (V_R - 1.3V)/[V_R(R_T + 1.5k\Omega)\ C_T]$.

The signal conditioner employs a synchronous demodulatorulation technique to extract position and phase information of the transducer core. The synchronous demodulator block not only conditions the transducer output to provide usable information, but also provides a very high impedance load to the transducer output (on the order of several MΩ for maximum linearity and for relative insensitivity to frequency drift (see "How an LVDT Works", Figure iii). Figure II shows how the demodulator functions. The oscillator signal, which is also the primary drive for the transducer, is tied to the sync input of the demodulator. Note that the OSC signal and the transducer output (demodulator input) are both referenced to $V_{R/2}$. The sync signal is compared to an internally-generated reference voltage, $V_{R/2}$. During the first half-cycle, as the sync signal goes above $V_{R/2}$, the demodulator functions as an inverter and, thus, the demodulator input appears inverted at the output. However, during the second half-cycle, as the sync signal goes below $V_{R/2}$, the demodulator functions as a follower and, thus, the demodulator input appears at the output with unity gain. Full-wave rectification thus occurs in synchronism with the primary drive signal. The amplitude of the rectified signal tells the position of the core, while the polarity of the output indicates on which side of null the core is. The demodulator offset is measured at less than 2mV with 5μV/°C offset drift, and linearity error is measured at ±0.05% full-scale (at −55°C to +125°C temperature range). A low offset is essential for transducer systems in precision applications since a high offset will not only mask the transducer null, but will also make position measurements inaccurate as the ambient temperature varies.

Since all readout devices (meters, recorders, etc.) are DC input devices, the AC output of the demodulator has to be converted to filtered DC before being applied to the readouts. Consequently, an on-chip amplifier may be used as an active filter with programmable gain for the demodulator output. The filter removes the carrier frequency and other higher-order harmonics from the demodulator output and produces a ripple-free DC output. The amplifier exhibits an open-loop gain of 380V/mV (typical) and 0.5mV input offset (typical). DC offsets from the transducer/signal conditioner system can be nulled by offset adjustment at the auxiliary amplifier. The device operates from 4.5V to 22V with single supply, or ±2.25V to ±11V with dual supplies.

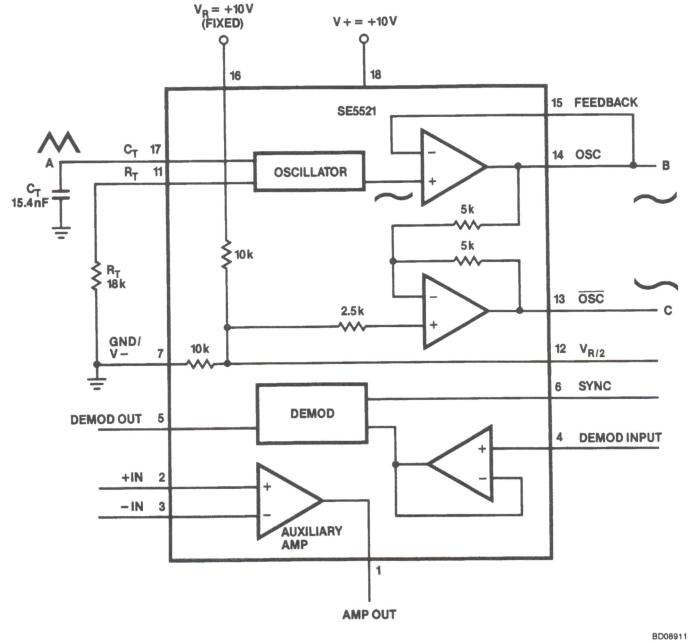


Figure I. SE5521 Block Diagram

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

AN1182

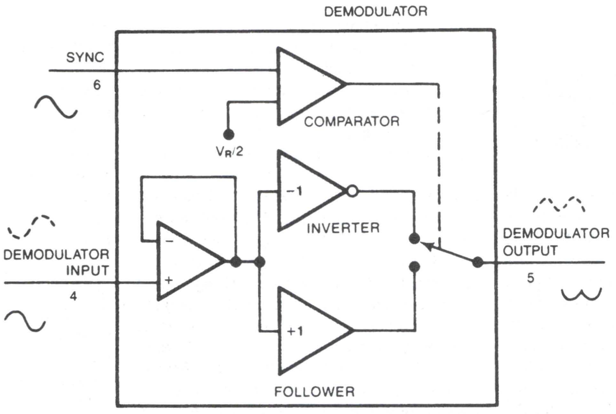

DEMODULATOR
SYNC
6
COMPARATOR
$V_R/2$
−1
INVERTER
−
+
DEMODULATOR INPUT
4
+1
FOLLOWER
DEMODULATOR OUTPUT
5
BD08880S

Figure II. Synchronous Demodulator Full-Wave Rectifies the Demodulator Input Signal in Synchronization With the Sync Signal at Pin 6

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

AN1182

APPENDIX II

HOW AN LVDT WORKS

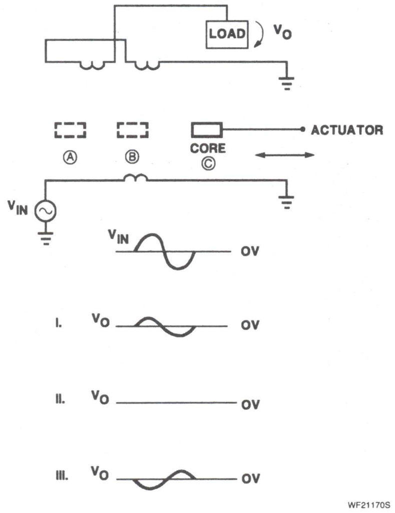
Linear Variable Differential Transformers (LVDTs) are position transducers that have long been used to measure very small displacement and any parameter that can be converted to linear motion. LVDTs are mutual inductance devices consisting of a primary winding and a pair of secondary windings that are wound on an insulated bobbin, and a non-contacting magnetic core capable of free motion inside the transformer. The secondaries are tied together externally in a series-opposing configuration.

With AC excitation at the primary, the core controls the coupling between the primary and the secondaries and produces a differential voltage across the secondaries. The magnitude of the voltage across the secondaries varies linearly with core displacement and contains both the position and phase information (direction of motion) of the core with respect to the center of the secondaries (null position).

With the core at null, the voltage induced at each secondary is equal and of opposite phase; thus cancellation occurs, resulting in a zero AC output. As the core traverses away from the null position, a sinusoidal voltage is developed across the secondaries, the amplitude of which contains the position information. Once the core moves through null, a 180° phase reversal occurs in the output signal with respect to the primary signal. Direction of the core (phase information) with respect to the null position is thus indicated as illustrated in Figure i.

In order to obtain any useful information, some form of signal conditioning is required. Figure ii shows the DC output of the LVDT as a linear function of the core position after proper signal conditioning. The output voltage of the LVDT is directly proportional to the excitation voltage; therefore, it is essential that the excitation signals have a constant amplitude over the operating temperature range. Output voltage also varies with the excitation frequency. However, the change is not directly proportional to frequency, as shown in Figure iii. Most LVDTs show a small amount of phase shift between the excitation signal at the primary and the output signal at the secondaries. The phase shift introduces a DC offset at null and thus tends to mask the LVDT null. The LVDT null voltage may be reduced by exciting the primary at a frequency where both the primary signal and the output signal are in phase — this is the zero phase angle frequency. Exciting the LVDT at its zero-phase angle frequency optimizes linearity and repeatability of the measurements, while a high impedance load at the LVDT output eliminates the need for frequency regulation, as can be observed from Figures iiia and iiib.

Another popular position transducer is the Rotary Variable Differential Transformer (RVDT). The RVDT operation is analogous to the LVDT, except that the core motion is rotary.



NOTES:
1. With core at a, output is in phase with input. Output amplitude decreases as core moves from A to B.
2. AC output is zero when core is at B (null).
3. Output amplitude increases as core moves from B to C. With core at C, output is 180° out of phase with respect to input.

Figure i. The LVDT Output Signal Changes Relative to Core Position

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

AN1182

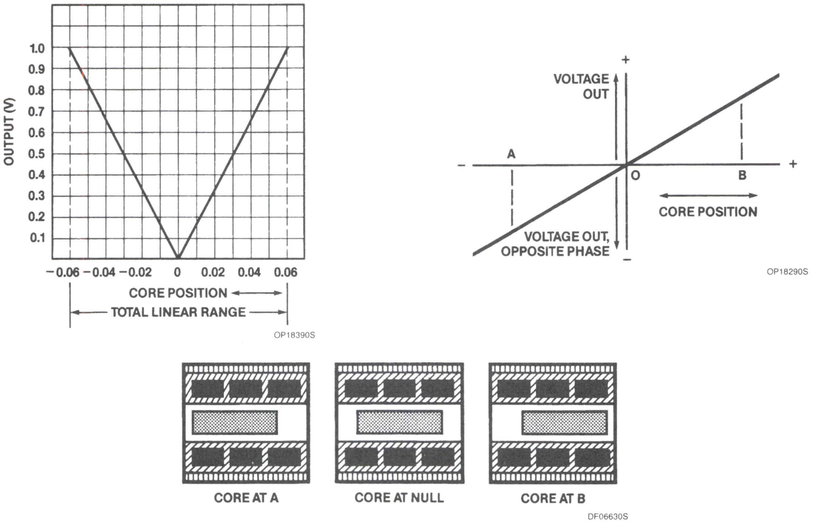
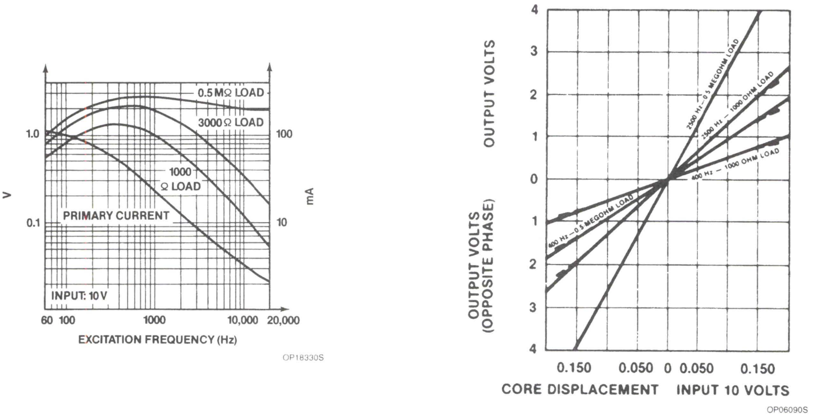


Figure ii. Absolute Magnitude of Output Voltage (Left) and Phase-Referenced Output Voltage (Right) as a Function of LVDT Core Position (Courtesy Schaevitz Engineering)



a. Nominal Full-Scale Output at Various Loads and Primary Current vs Excitation Frequency for a Typical LVDT

b. Output Characteristics of a Typical LVDT for Various Loads and Excitation Frequencies (Courtesy Schaevitz Engineering)

Figure iii

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

APPENDIX III

LPDT CHANGES PHASE INSTEAD OF AMPLITUDE

A recently developed linear position transducer, the LPDT (Linear Phase Differential Transformer), produces a phase output linear with the core motion. The transducer construction is similar to the LVDT, the main exception being that there are six primary coils which are wound on a bobbin at a slant. The excitation to the transducer primaries consists of a sine wave and a cosine wave of equal magnitude. The output at the secondary is an AC signal of constant amplitude, which is the vector sum of the sine and cosine excitation signals, with a phase angle that varies linearly with core position. Figure A shows how the transducer is energized.

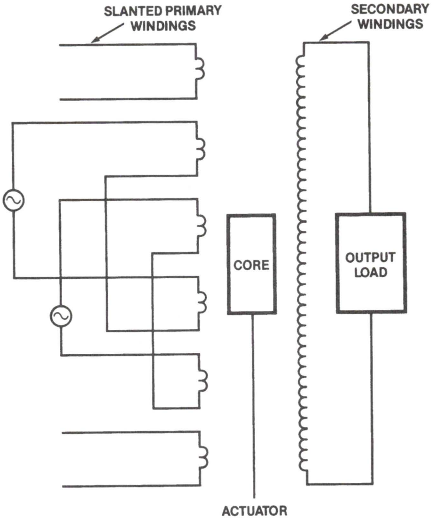


Figure A. LPDT with AC Excitation Signals at the Input

REFERENCES

1. *Handbook of Measurement and Control*, Revised Edition 1976, by Edward Herceg, Schaevitz Engineering Publication, Pennsauken, New Jersey.
2. *Signetics Linear LSI Data and Applications Manual*, 1985 Edition, pg 4-212, 9-41. Signetics Corporation, Sunnyvale, CA, 94086.
3. Frank Yeaple, "Linear Position Transducer Changes Phase Instead Of Amplitude", *Design News*, November 5, 1984, pg 180.

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Signetics

Section 6
Interface

Linear Products

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Symbols and Definitions for Line Drivers

Differential Output Voltage (V_O or $\overline{V}_O$, V_T or $\overline{V}_T$)
For a differential line driver (i.e., an RS-422 driver) this is the differential output voltage for an input voltage which is a logic HIGH (V_O) or LOW ($\overline{V}_O$). V_O is usually measured with no applied output load while V_T is the differential output voltage with a specified output load.

Enable
For line drivers and receivers having an $\overline{\text{ENABLE}}$ (or ENABLE) input, the application of a specified logic voltage to this input will force the outputs into a high resistance (High-Z) state. In this state, the circuit has a minimal loading effect on the transmission or bus line being driven by the output.

Failsafe (FS)
For line receivers having a FAILSAFE (FS) input, the application of specified voltages to this input will force the outputs to correspondingly specified logic states, V_{OFS} (defined below), when fault conditions occur on the transmission line.

Failsafe Output Voltage (V_{OFS})
For line receivers: the voltage to which the outputs are forced when specified fault conditions occur on the transmission line and when a specified voltage is applied to the FAILSAFE (FS) input.

Hysteresis (V_H)
For line receivers: the difference between the high and low threshold voltages, V_{TH} and V_{TL} (defined below).

Input Current (I_{IN})
For a line receiver: the current flowing into the transmission line input at a specified input voltage.

Input Clamp Voltage (V_{CL})
For a line driver: the input voltage applied to an input below which the driver clamps this voltage. V_{CL} is specified for a particular current flowing from the driver into the voltage source.

Input High Current (I_{IH})
The current flowing into or out of a logic input when a specified logic HIGH voltage is applied to that input.

Input High Threshold Voltage (V_{TH})
For a line receiver: the differential input voltage at the transmission line input above which the output is in a defined logic state.

Input High Voltage (V_{IH})
The range of input voltages recognized by a logic input as a logic HIGH.

Input Low Current (I_{IL})
The current flowing into or out of a logic input when a specified logic LOW voltage is applied to that input.

Input Low Threshold Voltage (V_{TL})
For a line receiver: the differential input voltage below which the output is in a defined logic state.

Input Low Voltage (V_{IL})
The range of input voltages recognized by a logic input as a logic LOW.

Input Resistance (R_{IN})
For a line receiver: the DC resistance of the transmission line input over a specified input voltage range.

Mode
For line drivers having a MODE input the application of specified voltages to this input will force the driver outputs to comply with correspondingly specified EIA transmission standards, e.g., RS-232 or RS-423.

Open-Circuit Input Voltage (V_{IOC})
For a line receiver: the voltage to which the transmission line input of the circuit reverts when no external connection is made at this input.

Output Current High-Z (I_O)
The current flowing into or out of an output when that output is in a High-Z state (see ENABLE definition). I_O is specified at a particular applied output voltage.

Output High Voltage (V_{OH})
The HIGH voltage at an output (for a driver or receiver) for specified load conditions, i.e., R_L or I_{OUT}, and input voltages.

Output Low Voltage (V_{OL})
The LOW voltage at an output (for a driver or receiver) for specified load conditions, i.e., R_L or I_{OUT}, and input voltages.

Output Leakage Current (I_{CEX})
The current flowing into or out of an output when no power is applied to the circuit. I_{CEX} is specified at a particular applied output voltage and input conditions.

Output Resistance (R_{OUT})
For a line driver: the output resistance over a specified output voltage range.

Output Short-Circuit Current (I_{OS})
The current flowing into or out of an output when the output is connected to the generator circuit ground for a line receiver or digital ground for a line driver.

Output Unbalance Voltage ($|V_{OH}| - |V_{OL}|$, $|V_T| - |\overline{V}_T|$)
For a line driver: the difference between the absolute values of V_{OH} and V_{OL} or V_T and $\overline{V}_T$.

Output Offset Voltage (V_{OS} or $\overline{V}_{OS}$)
For a differential line driver, i.e. RS-422, the difference between the actual voltage at the center of the output load and the generator circuit ground. V_{OS} is measured with V_T at the output and $\overline{V}_{OS}$ with $\overline{V}_T$ at the output.

Propagation Delay (t_{PXX})
The time delay between specified reference points on the input and output waveforms of a line driver or receiver. The symbol X can be H, L or Z specifying HIGH, LOW or High-Z, respectively; i.e., t_{PLZ} is the propagation delay for the output of a line driver to change from an output LOW to a High-Z state after the application of a signal to the $\overline{\text{ENABLE}}$ input.

Rise and Fall Times (t_R and t_F)
For a line driver: the time delays between the 10% and 90% points on the rising and falling output waveforms following a change in the logic voltage at the input.

Signetics

MC1488
Quad Line Driver

Product Specification

Linear Products

DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

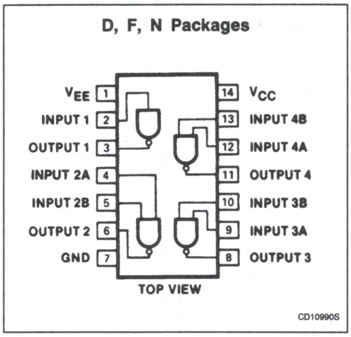
FEATURES

- **Current limited output: ± 10mA Typ**
- **Power-off source impedance: 300Ω min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

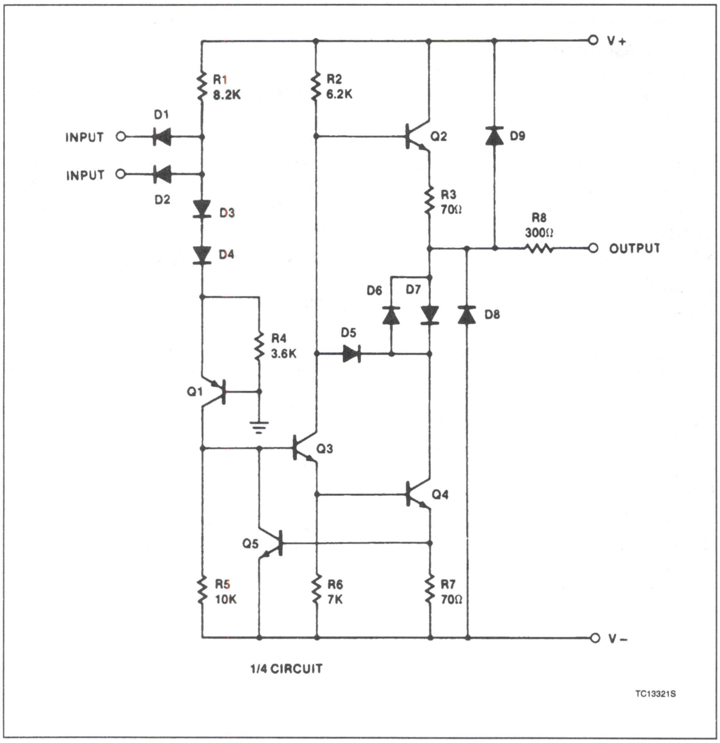
APPLICATIONS

- **Computer port driver**
- **Digital transmission over long lines**
- **Slew rate control**
- **TTL/DTL to MOS translation**

PIN CONFIGURATION


D, F, N Packages
V_{EE} 1
INPUT 1 2
OUTPUT 1 3
INPUT 2A 4
INPUT 2B 5
OUTPUT 2 6
GND 7
14 V_{CC}
13 INPUT 4B
12 INPUT 4A
11 OUTPUT 4
10 INPUT 3B
9 INPUT 3A
8 OUTPUT 3
TOP VIEW
CD10990S

CIRCUIT SCHEMATIC


V+
R1
8.2K
R2
6.2K
D1
INPUT
INPUT
D2
Q2
D9
D3
R3
70Ω
R8
300Ω
OUTPUT
D4
D6
D7
D8
R4
3.6K
D5
Q1
Q3
Q4
Q5
R5
10K
R6
7K
R7
70Ω
V−
1/4 CIRCUIT
TC13321S

Quad Line Driver MC1488

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +75°C	MC1488D
14-Pin Plastic DIP	0 to +75°C	MC1488N
14-Pin Ceramic DIP	0 to +75°C	MC1488F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V+	+15	V
	V−	−15	V
V_{IN}	Input voltage	$-15 \leqslant V_{IN} \leqslant 7.0$	V
V_{OUT}	Output voltage	±15	V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating ambient temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

Quad Line Driver MC1488

DC AND AC ELECTRICAL CHARACTERISTICS

$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$, unless otherwise specifed. All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$[1].

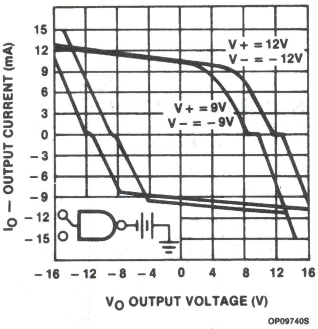
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ	Max	
V_{IH}	Logic "0" input current	$V_{IN} = 0V$			−1.0	−1.6	mA
V_{IL}	Logic "1" input current	$V_{IN} = +5.0V$			0.005	10.0	μA
V_{OH}	High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	$V+ = 9.0V$ $V- = -9.0V$	6.0	7.0		V
			$V+ = 13.2V$ $V- = -13.2V$	9.0	10.5		V
V_{OL}	Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	$V+ = 9.0V$ $V- = -9.0V$	−6.0	−6.8		V
			$V+ = 13.2V$ $V- = -13.2V$	−9.0	−10.5		V
I_{SC+}	High level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{SC-}	Low level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		5.0	10.0	12.0	mA
R_{OUT}	Output resistance	$V+ = V- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
$I+$	Positive supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		15.0	20.0	mA
			$V+ = 12V$, $V- = -12V$		19.0	25.0	mA
			$V+ = 15V$, $V- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		4.5	6.0	mA
			$V+ = 12V$, $V- = -12V$		5.5	7.0	mA
			$V+ = 15V$, $V- = -15V$		8.0	12.0	mA
$I-$	Negative supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		−13.0	−17.0	mA
			$V+ = 12V$, $V- = -12V$		−18.0	−23.0	mA
			$V+ = 15V$, $V- = -15V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		−1	−15	μA
			$V+ = 12V$, $V- = -12V$		−1	−15	μA
			$V+ = 15V$, $V- = -15V$		−0.01	−2.5	mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[2]						
	F package					1190	mW
	N package					1420	mW
	D package					1040	mW
t_{PD1}	Propagation delay to "1"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
t_{PDD}	Propagation delay to "0"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
t_R	Rise time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
t_F	Fall time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

NOTES:

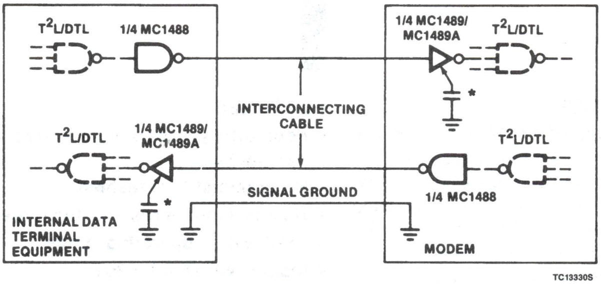
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

Quad Line Driver MC1488

TYPICAL PERFORMANCE CHARACTERISTICS



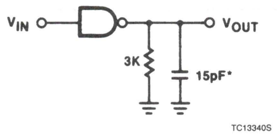
Output Voltage and Current-Limiting Characteristics


T²L/DTL
1/4 MC1488
1/4 MC1489/ MC1489A
T²L/DTL
*
INTERCONNECTING CABLE
T²L/DTL
1/4 MC1489/ MC1489A
*
SIGNAL GROUND
INTERNAL DATA TERMINAL EQUIPMENT
T²L/DTL
1/4 MC1488
MODEM
TC13330S

NOTE:
*Optional for noise filtering

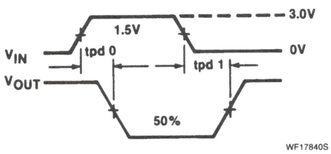
RS-232C Data Transmission

AC LOAD CIRCUIT


V_{IN}
V_{OUT}
3K
15pF*
TC13340S

NOTE:
$^*C_L$ includes probe and jig capacitance.

SWITCHING WAVEFORMS


3.0V
1.5V
0V
V_{IN}
tpd 0
tpd 1
V_{OUT}
50%
WF17840S

NOTE:
t_R and t_F are measured between 10% and 90% of the output waveform.

APPLICATIONS

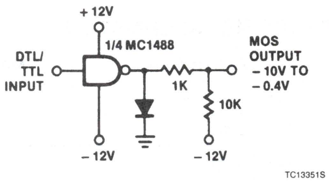
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current-limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}(\Delta T/\Delta V)$$

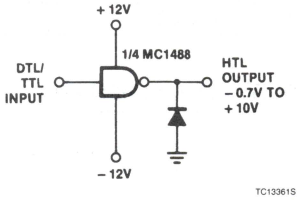
where C is the required capacitor, I_{SC} is the short-circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS-232C specifies that the output slew rate must not exceed 30V/μs. Using the worst-case output short-circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

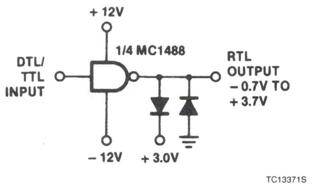
TYPICAL APPLICATIONS


+12V
1/4 MC1488
DTL/ TTL INPUT
MOS OUTPUT −10V TO −0.4V
1K
10K
−12V
−12V
TC13351S

DTL/TTL-to-MOS Translator


+12V
1/4 MC1488
DTL/ TTL INPUT
HTL OUTPUT −0.7V TO +10V
−12V
TC13361S

DTL/TTL-to-HTL Translator


+12V
1/4 MC1488
DTL/ TTL INPUT
RTL OUTPUT −0.7V TO +3.7V
−12V
+3.0V
TC13371S

DTL/TTL-to-RTL Translator

Signetics

MC1489/MC1489A
Quad Line Receivers

Product Specification

Linear Products

DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS-232C.

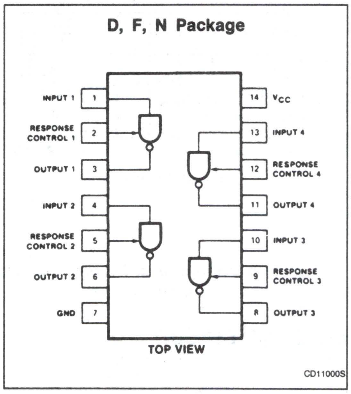
FEATURES

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

APPLICATIONS

- Computer port inputs
- Modems
- Eliminating noise in digital circuitry
- MOS-to-TTL/DTL translation

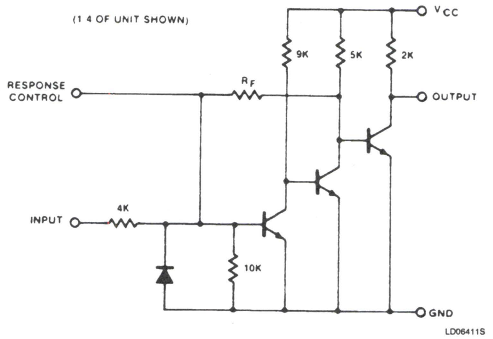
PIN CONFIGURATION


D, F, N Package
INPUT 1
RESPONSE CONTROL 1
OUTPUT 1
INPUT 2
RESPONSE CONTROL 2
OUTPUT 2
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
VCC
INPUT 4
RESPONSE CONTROL 4
OUTPUT 4
INPUT 3
RESPONSE CONTROL 3
OUTPUT 3
TOP VIEW
CD11000S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	MC1489N
14-Pin Plastic DIP	0 to +70°C	MC1489AN
14-Pin Cerdip	0 to +70°C	MC1489F
14-Pin Cerdip	0 to +70°C	MC1489AF
14-Pin Plastic SO	0 to +70°C	MC1489D
14-Pin Plastic SO	0 to +70°C	MC1489AD

EQUIVALENT SCHEMATIC


(1 4 OF UNIT SHOWN)
VCC
9K
5K
2K
RESPONSE CONTROL
RF
OUTPUT
INPUT
4K
10K
GND
LD06411S

NOTES:
1. MC1489: $R_F = 10k\Omega$
2. MC1489A: $R_F = 2k\Omega$

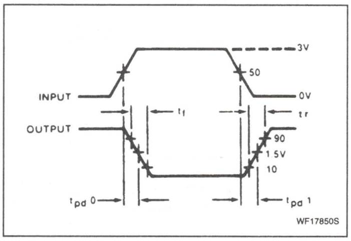
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	10	V
V_{IN}	Input voltage range	±30	V
I_{OUT}	Output load current	20	mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

VOLTAGE WAVEFORMS



DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $0°C \leq T_A \leq +75°C$, unless otherwise specified.[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high threshold voltage	$T_A = 25°C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10mA$	1.0		1.5	1.75		2.25	V
V_{IL}	Input low threshold voltage	$T_A = 25°C$, $V_{OUT} \geq 2.5V$, $I_{OUT} = -0.5mA$	0.75		1.25	0.75		1.25	V
I_{IN}	Input current	$V_{IN} = +25V$	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
		$V_{IN} = -25V$	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	
		$V_{IN} = +3V$	+0.43	+0.53		+0.43	+0.53		
		$V_{IN} = -3V$	-0.43	-0.53		-0.43	-0.53		
V_{OH}	Output high voltage	$V_{IN} = 0.75V$, $I_{OUT} = -0.5mA$	2.6	3.8	5.0	2.6	3.8	5.0	V
		Input = Open, $I_{OUT} = -0.5mA$	2.6	3.8	5.0	2.6	3.8	5.0	V
V_{OL}	Output low voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10mA$		0.33	0.45		0.33	0.45	V
I_{CC}	Output short-circuit current	$V_{IN} = 0.75V$		3.0			3.0		mA
	Supply current	$V_{IN} = 5.0V$		20	26		20	26	mA
P_D	Power dissipation	$V_{IN} = 5.0V$		100	130		100	130	mW

NOTES:

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $T_A = 25°C$, unless otherwise specified.[1, 2]

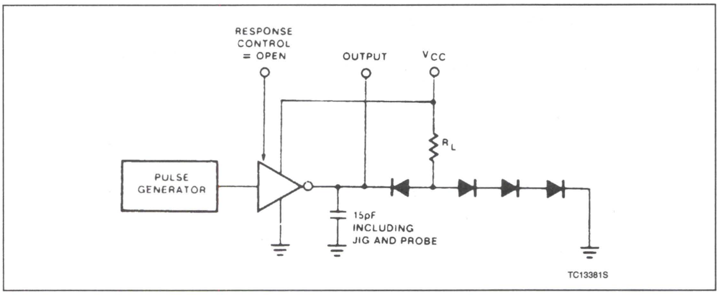
SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PD1}	Input to output "high" Propagation delay	$R_L = 3.9k\Omega$ (AC test circuit)		25	85		25	85	ns
t_{PD0}	Input to output "low" Propagation delay	$R_L = 390\Omega$ (AC test circuit)		20	50		20	50	ns
t_R	Output rise time	$R_L = 3.9k\Omega$ (AC test circuit)		110	175		110	175	ns
t_F	Output fall time	$R_L = 390\Omega$ (AC test circuit)		9	20		9	20	ns

NOTES:

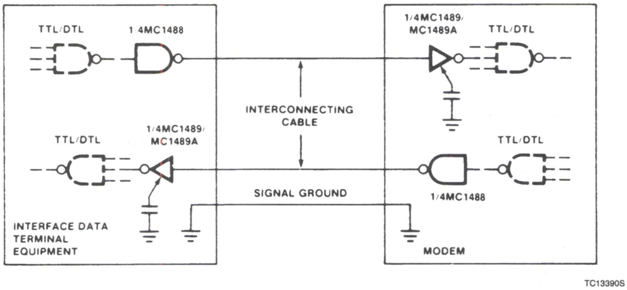
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

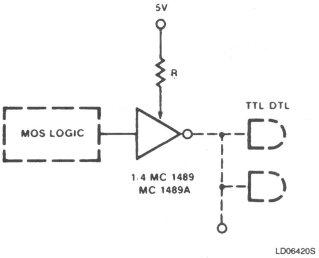
Quad Line Receivers MC1489/MC1489A

AC TEST CIRCUIT


RESPONSE CONTROL = OPEN
OUTPUT
V_{CC}
R_L
PULSE GENERATOR
15pF INCLUDING JIG AND PROBE
TC13381S

TYPICAL APPLICATIONS


TTL/DTL
1/4MC1488
1/4MC1489/ MC1489A
TTL/DTL
INTERCONNECTING CABLE
TTL/DTL
1/4MC1489/ MC1489A
TTL/DTL
SIGNAL GROUND
1/4MC1488
INTERFACE DATA TERMINAL EQUIPMENT
MODEM
TC13390S


5V
R
TTL DTL
MOS LOGIC
1/4 MC 1489 MC 1489A
LD06420S

NOTE:
*Optional for noise filtering

RS-232C Data Transmission

MOS-to-TTL/DTL Translator

Signetics

Linear Products

AN113

Using the MC1488/1489 Line Drivers and Receivers

Application Note

LINE DRIVERS AND RECEIVERS

Many types of line drivers and receivers are available today. Each device has been designed to meet specific criteria. For instance, the device may be extremely wide-band or be intended for use in party line systems. Some include built-in hysteresis in the receiver while others do not.

The EIA Standard

The Electronic Industries Association (EIA) has produced a number of specifications dealing with the transmission of data between data terminal and communications equipment. One of these is EIA Standard RS-232C, which delineates much information about signal levels and hardware configurations in data systems.

MC1488/1489

As line driver and receiver, the MC1488 and MC1489 meet or exceed the RS-232C specification.

Standard RS-232C defines, the voltage level as being from 5 to 15V with positive voltage representing a logic 0. The MC1488 meets these requirements when loaded with resistors from 3k to 7kΩ.

Output slew rates are limited by RS-232C to 30V/μs. To accomplish this specification, the MC1488 is loaded at its output by capacitance as shown by the typical hook-up diagram of Figure 1. A graph of slew rate vs output capacitance is given in Figure 2. For the standard 30V/μs, a capacitance of 400pF is selected.

The short-circuit current charges the capacitance with the relationship

$$C = \frac{I_{SC}\Delta T}{\Delta V}$$

Where C is the required capacitor, I_{SC} is the short-circuit current value, and $\Delta V/\Delta T$ is the slew rate.

Using the worst-case output short-circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output to limit the output slew rate to 30V/μs in accordance with the EIA standard.

The EIA standard also states that output shorts to any other conductor of the cable must not damage the driver. Thus, the MC1488 is designed such that the output will withstand shorts to other conductors indefinitely even if these conductors are at worst-case voltage levels. In addition to output protection, the MC1488 includes a 300Ω, resistor to ensure that the output impedance of the driver will be at least 300Ω, even if the power supply is turned off. In cases where power supply malfunction produces a low impedance to ground, the 300Ω resistors are shorted to ground also. Output shorts then can cause excessive power dissipation. To prevent this, series diodes should be included in both supply lines as pictured in Figure 3.

The companion receiver, MC1489, is also designed to meet RS-232C specifications for receivers. It must detect a voltage from ±3 to ±25V as logic signals but cannot generate an input differential voltage of greater than 2V should its inputs become open circuited. Noise and spurious signals are rejected by incorporating positive feedback internally to produce hysteresis. Featured also in the receiver is an external response node so that the threshold may be externally varied to fit the application. Figure 4 shows the shift in high and low trip points as a function of the programming resistance.

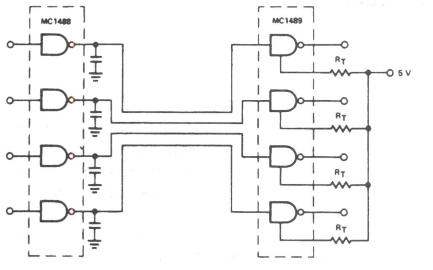
APPLICATIONS

The design of the MC1488 and MC1489 makes them very versatile with many possible applications. The MC1488 output current limiting enables the user to define the output voltage levels independent of supply voltages. Figure 5 shows the MC1488 as a TTL-to-MOS Translator, while Figures 6 and 7 illustrate TTL-to-HTL and TTL-to-MOS Translators.

The MC1489 response control node allows the user to modify the input threshold voltage levels. This is accomplished by adding a resistor between the response control pin and an external power supply. Figure 4 shows the shift thus provided. This feature and the fact that the inputs are designed to withstand ±30V permit the use of the MC1489 for level translation as shown in the MOS-to-TTL Translator of Figure 8. This feature is also useful for level shifting, as illustrated in Figure 9.

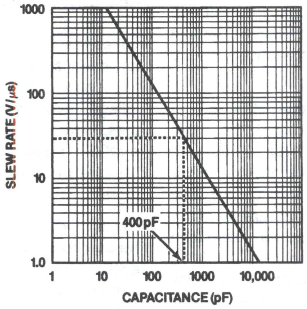
The response control node can also be used to filter out high frequency, high energy noise pulses. Figures 10 and 11 give typical noise pulse rejection curves for various sized external capacitors.

Using the MC1488/1489 Line Drivers and Receivers AN113



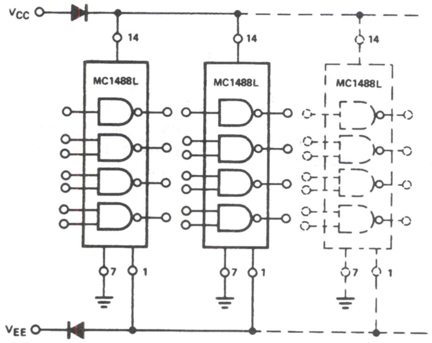
TC09390S

Figure 1. Typical Line Driver-Receiver Application



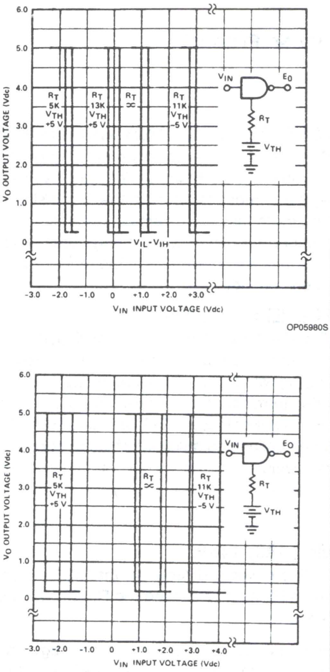
OP11500S

Figure 2. Output Slew Rate vs Load Capacitance



TC09400S

Figure 3. Protection From Power Supply Malfunction



OP05980S

OP05990S

Figure 4. Hysteresis as a Function of Programming Resistance

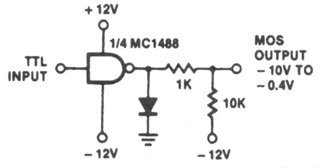

+12V
1/4 MC1488
TTL INPUT
MOS OUTPUT −10V TO −0.4V
1K
10K
−12V
−12V
TC09410S

Figure 5. TTL-to-MOS Translator

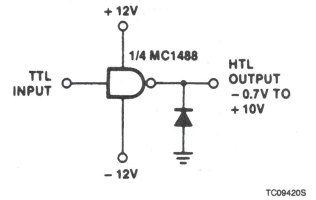

+12V
1/4 MC1488
TTL INPUT
HTL OUTPUT −0.7V TO +10V
−12V
TC09420S

Figure 6. TTL-to-HTL Translator

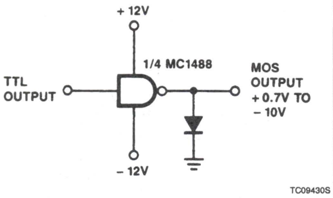

+12V
1/4 MC1488
TTL OUTPUT
MOS OUTPUT +0.7V TO −10V
−12V
TC09430S

Figure 7. TTL-to-MOS Translator

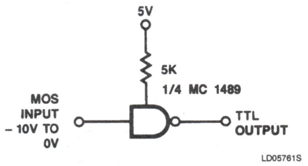
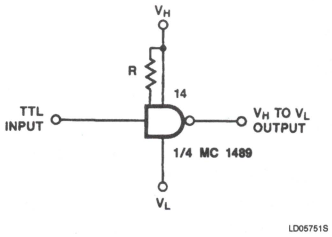

5V
5K
1/4 MC 1489
MOS INPUT −10V TO 0V
TTL OUTPUT
LD05761S

Figure 8. MOS-to-TTL Translator


V_H
R
14
TTL INPUT
V_H TO V_L OUTPUT
1/4 MC 1489
V_L
LD05751S

NOTE:
1. $V_2 \leq 5V$; $3V \leq V_H - V_L \leq 10V$.

Figure 9. Level Shifter[1]

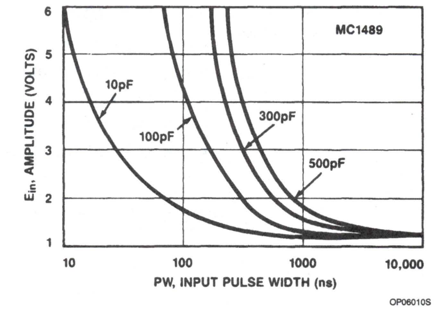


Figure 10. Turn-on Threshold vs Capacitance From Response Control Pin to GND

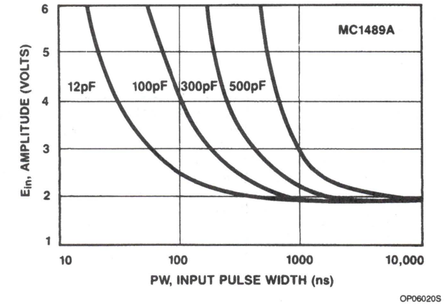


Figure 11. Turn-on Threshold vs Capacitance From Response Control Pin to GND

NE5170
Octal Line Driver

Preliminary Specification

Linear Products

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features, (1) output slew rate (2) output voltage level, and (3) three-state control (high impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

FEATURES

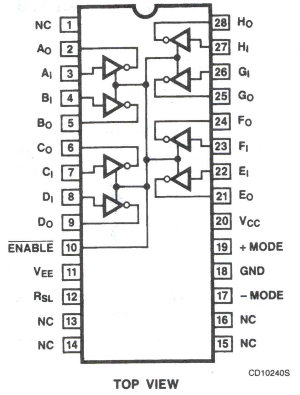
- **Meets EIA RS-232C/423A and CCITT V.10/X.26**
- **Simple slew rate programming with a single external resistor**
- **0.1 to 10V/μs slew rate range**
- **High/low programmable voltage output modes**
- **TTL compatible inputs**

APPLICATIONS

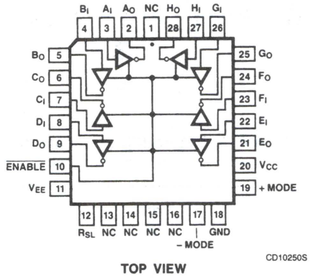
- **High-speed modems**
- **High-speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

PIN CONFIGURATIONS

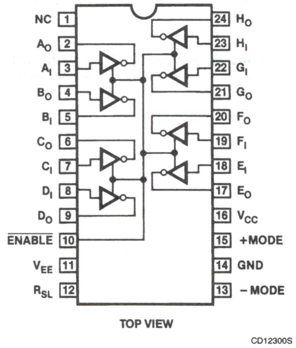
N Package


NC 1
A_O 2
A_I 3
B_I 4
B_O 5
C_O 6
C_I 7
D_I 8
D_O 9
ENABLE 10
V_EE 11
R_SL 12
NC 13
NC 14
28 H_O
27 H_I
26 G_I
25 G_O
24 F_O
23 F_I
22 E_I
21 E_O
20 V_CC
19 +MODE
18 GND
17 −MODE
16 NC
15 NC
TOP VIEW
CD10240S

A Package


B_I A_I A_O NC H_O H_I G_I
4 3 2 1 28 27 26
B_O 5
C_O 6
C_I 7
D_I 8
D_O 9
ENABLE 10
V_EE 11
25 G_O
24 F_O
23 F_I
22 E_I
21 E_O
20 V_CC
19 +MODE
12 13 14 15 16 17 18
R_SL NC NC NC NC −MODE GND
TOP VIEW
CD10250S

D Package


NC 1
A_O 2
A_I 3
B_O 4
B_I 5
C_O 6
C_I 7
D_I 8
D_O 9
ENABLE 10
V_EE 11
R_SL 12
24 H_O
23 H_I
22 G_I
21 G_O
20 F_O
19 F_I
18 E_I
17 E_O
16 V_CC
15 +MODE
14 GND
13 −MODE
TOP VIEW
CD12300S

FUNCTION TABLE

ENABLE	LOGIC INPUT	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	⩾9V
L	H	−5 to −6V	−5 to −6V	⩽−9V
H	X	High-Z	High-Z	High-Z

NOTES:

1. $V_{CC} = +10V$ and $V_{EE} = -10V$; $R_L = 3k\Omega$
2. $V_{CC} = +12V$ and $V_{EE} = -12V$; $R_L = 3k\Omega$

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5170N
28-Pin PLCC	0 to +70°C	NE5170A
28-Pin SO package	0 to +70°C	NE5170D

Octal Line Driver

NE5170

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and – MODE	–15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{\text{Enable}}$, Data)	–1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 10V \pm 10\%$; $V_{EE} = -10V \pm 10\%$; ±MODES = 0V; $R_{SL} = 2k\Omega$, $0°C \leqslant T_A \leqslant 70°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output high voltage	$V_{IN} = 0.8V$ $R_L = 3k\Omega^4$	5	6	V
		$R_L = 450\Omega^4$	4.5	6	
		$R_L = 3k\Omega^5$, $C_L = 2500pF$	$V_{CC} - 3$		
V_{OL}	Output low voltage	$V_{IN} = 2.0V$ $R_L = 3k\Omega^4$	–6	–5	V
		$R_L = 450\Omega^4$	–6	–4.5	
		$R_L = 3k\Omega^5$, $C_L = 2500pF$		$V_{EE}+3$	
V_{OU}	Output unbalance voltage	$V_{CC} = \lvert V_{EE} \rvert$, $R_L = 450\Omega^4$		0.4	V
I_{CEX}	Output leakage current	$\lvert V_O \rvert = 6V$, ENABLE = 2V or $V_{CC} = V_{EE} = 0V$	–100	100	μA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	$V_{IN} = 0.4V$	–400	0	μA
I_{IH}	Logic "1" input current	$V_{IN} = 2.4V$	0	40	μA
I_{OS}	Output short circuit current[1]	$V_O = 0V$	–150	150	mA
V_{CL}	Input clamp voltage	$I_{IN} = -15mA$	–1.5		V
I_{CC}	Supply current	NO LOAD		35	mA
I_{EE}		NO LOAD	–45		mA

NOTES:

1 Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.

2. High impedance mode.

3. Minimum value of the resistor used to set the slew rate.

4. V_{OH}, V_{OL} at $R_L = 450\Omega$ will be $\geqslant \geq 90\%$ of V_{OH}, V_{OL} at $R_L = \infty$.

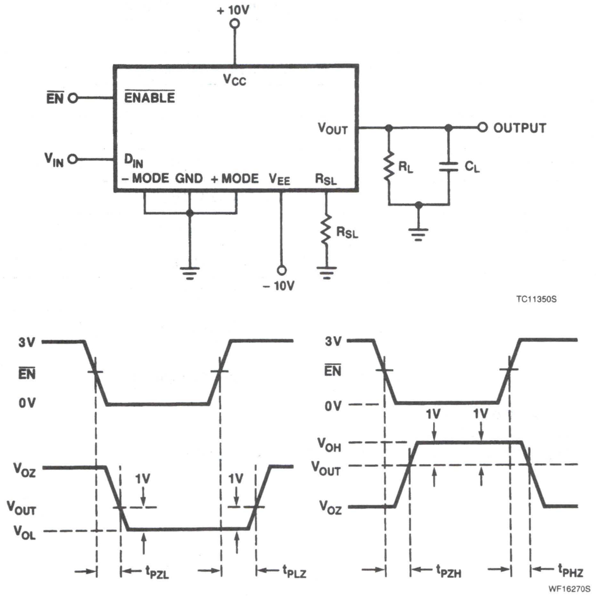
5. High Output Mode; +MODE pin = V_{CC}; –MODE pin = V_{EE}; $9V \leqslant V_{CC} \leqslant 13V$; $-9V \geqslant V_{EE} \geqslant -13V$.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +10V$; $V_{EE} = -10V$; Mode = GND, $0°C \leqslant T_A \leqslant 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHZ}	Propagation delay output high to high impedance	$R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		5	μs
t_{PLZ}	Propagation delay output low to high impedance	$R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		5	μs
t_{PZH}	Propagation delay high impedance to high output	$R_{SL} = 200k$ $R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		150	μs
t_{PZL}	Propagation delay high impedance to low output	$R_{SL} = 200k$ $R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		150	μs
SR	Output slew rate[1]	$R_{SL} = 2k$	8	12	V/μs
		$R_{SL} = 20k$	0.8	1.2	
		$R_{SL} = 200k$	0.06	0.14	

NOTE:
SR: Load condition. (A) For $R_{SL} < 4k\Omega$ use $R_L = 450\Omega$; $C_L = 50pF$; (B) for $R_{SL} > 4k\Omega$ use either $R_L = 450\Omega$, $C_L = 50pF$ or $R_L = 3k\Omega$, $C_L = 2500pF$.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS


+10V
V_CC
EN
ENABLE
V_IN
D_IN
– MODE GND + MODE V_EE R_SL
V_OUT
OUTPUT
R_L
C_L
R_SL
– 10V
TC11350S
3V
EN
0V
V_OZ
V_OUT
V_OL
1V
1V
t_PZL
t_PLZ
3V
EN
0V
1V
1V
V_OH
V_OUT
V_OZ
t_PZH
t_PHZ
WF16270S

NOTES:
1. See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2. V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, $Z_{OUT} = 50\Omega$, $t_r = t_f \leqslant 10ns$.

Octal Line Driver NE5170

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL}\ (\text{in k}\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/μs. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to 0.1V/μs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS-423A. Approximations for cable length and data rate are given by:

Max. data rate (in kb/s) = 300/t

Cable length (in feet) = 100 × t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS-423A and RS-232C. The high output mode meets the specifications of RS-232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the −MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

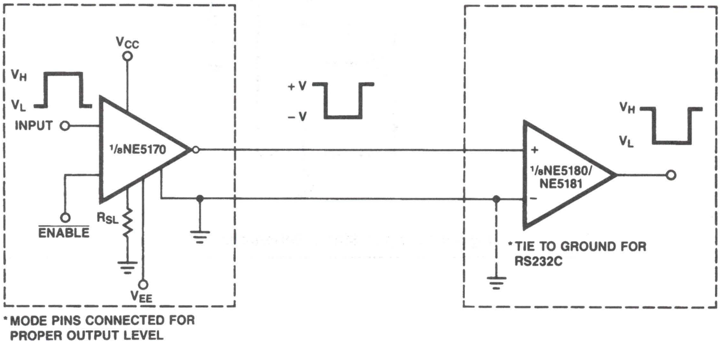


Figure 1. RS-232C/RS-423A Data Transmission

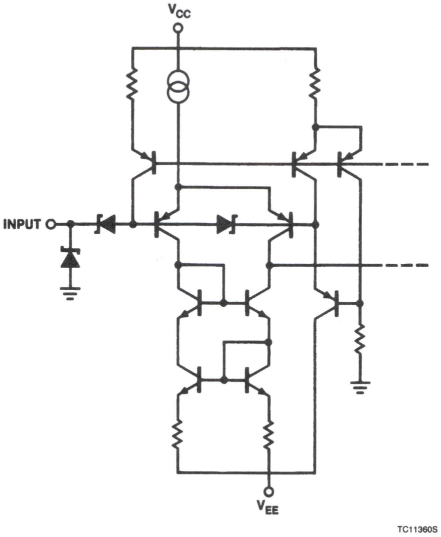

V_{CC}
INPUT
V_{EE}
TC11360S

Figure 2. Input Stage Schematic

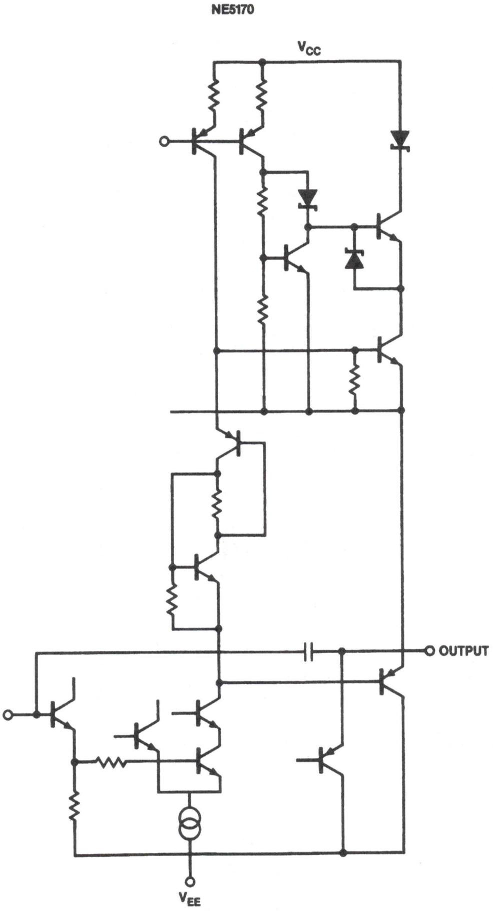

NE5170
V_{CC}
OUTPUT
V_{EE}
TC11370S

Figure 3. Output Stage Schematic

Octal Line Driver

NE5170

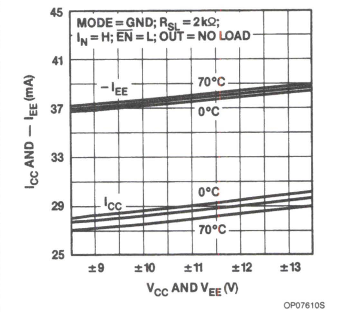


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

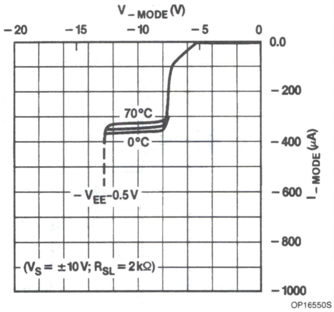


Figure 7. Typical −MODE Current vs −MODE Voltage

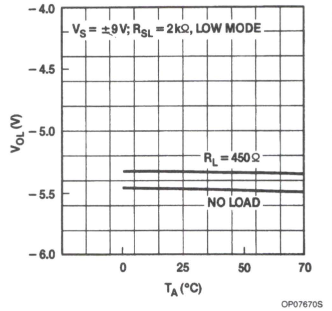


Figure 10. Typical Output Low Voltage vs Temperature

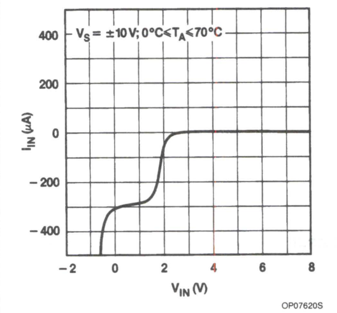


Figure 5. Typical Input Current vs Input Voltage

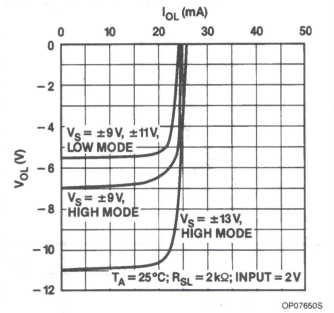


Figure 8. Typical Output Low Voltage vs Load Current

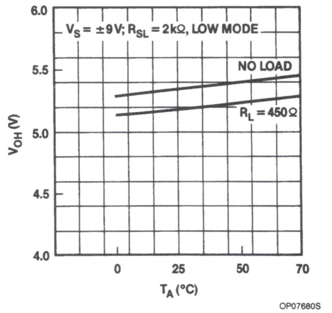


Figure 11. Typical Output High Voltage vs Temperature

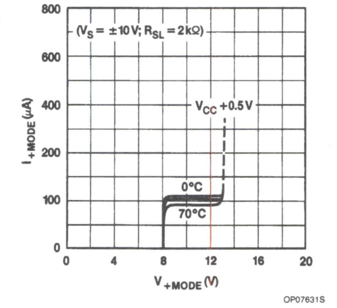


Figure 6. Typical +MODE Current vs +MODE Voltage

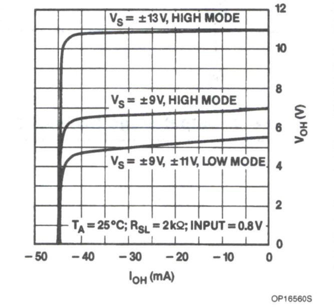


Figure 9. Typical Output High Voltage vs Load Current

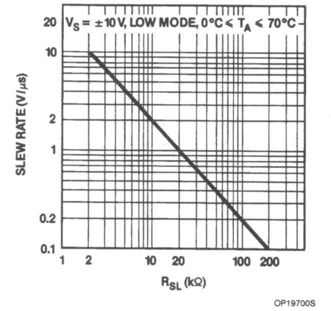


Figure 12. Typical Slew Rate vs R_{SL}

Signetics

NE5180/NE5181
Octal Differential Line Receivers

Preliminary Specification

Linear Products

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

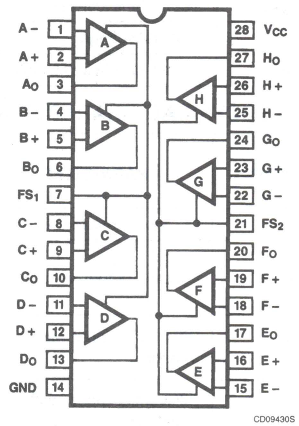
- **Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28**
- **Single +5V supply — TTL compatible outputs**
- **Differential inputs withstand ±25V**
- **Failsafe feature**
- **Input noise filter (NE5180 only)**
- **Internal hysteresis**
- **Available in SMD PLCC**

APPLICATIONS

- **High-speed modems**
- **High-speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

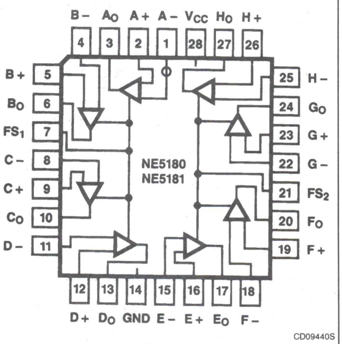
PIN CONFIGURATIONS

N Package


A− 1
A+ 2
AO 3
B− 4
B+ 5
BO 6
FS1 7
C− 8
C+ 9
CO 10
D− 11
D+ 12
DO 13
GND 14
28 VCC
27 HO
26 H+
25 H−
24 GO
23 G+
22 G−
21 FS2
20 FO
19 F+
18 F−
17 EO
16 E+
15 E−
A
B
C
D
E
F
G
H
CD09430S

TOP VIEW

A Package


B− AO A+ A− VCC HO H+
4 3 2 1 28 27 26
B+ 5
BO 6
FS1 7
C− 8
C+ 9
CO 10
D− 11
25 H−
24 GO
23 G+
22 G−
21 FS2
20 FO
19 F+
12 13 14 15 16 17 18
D+ DO GND E− E+ EO F−
NE5180
NE5181
CD09440S

TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} > 200\text{mV}$[1]	X	H
$V_{ID} < -200\text{mV}$[1]	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:

1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5180N
28-Pin Plastic DIP	0 to +70°C	NE5181N
28-Pin PLCC	0 to +70°C	NE5180A
28-Pin PLCC	0 to +70°C	NE5181A

Octal Differential Line Receivers

NE5180/NE5181

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$

SYMBOL	PARAMETER	RATING	UNIT
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common-mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Output sink current	50	mA
V_{FS}	Failsafe voltage	−0.3 to V_{CC}	V
I_{OS}	Output short-circuit time	1	sec

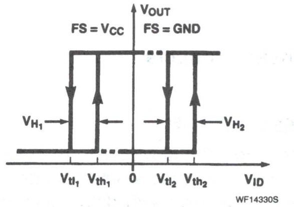


Figure 1. V_{tl}, V_{th}, V_H Definitions

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V \pm 5\%$, $0°C \leq T_A \leq +70°C$, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNIT
				Min	Max	Min	Max	
R_{IN}	DC input resistance	$3V \leq \lvert V_{IN} \rvert \leq 25V$		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	$0 \leq I_{OUT} \leq 8mA$, $V_{failsafe} = 0V$		0.45		0.45	V
			$0 \geq I_{OUT} \geq -400\mu A$, $V_{failsafe} = V_{CC}$	2.7		2.7		
V_{TH}	Differential input high[4] threshold	$V_{OUT} \geq 2.7V$, $I_{OUT} = -440\mu A$	$R_S = 0$[1]		0.2		0.2	V
			$R_S = 50$[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	$V_{OUT} \leq 0.45V$, $I_{OUT} = 8mA$	$R_S = 0$[1]	−0.2		−0.2		V
			$R_S = 50$[1]	−0.4		−0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance				30		30	pF
V_{OH}	High level output voltage	$V_{ID} = 1V$, $I_{OUT} = -440\mu A$		2.7		2.7		V
V_{OL}	Low level output voltage	$V_{ID} = -1V$	$I_{OUT} = 4mA$[2]		0.4		0.4	V
			$I_{OUT} = 8mA$[2]		0.45		0.45	
I_{OS}	Short-circuit output current	$V_{ID} = 1V$, Note 3		20	100	20	100	mA
I_{CC}	Supply current	$4.75V \leq V_{CC} \leq 5.25V$, $V_{ID} = -1V$; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	$V_{IN} = +10V$		3.25		3.25	mA
			$V_{IN} = -10V$	−3.25		−3.25		

NOTES
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V \pm 5\%$, $0°C \leq T_A \leq +70°C$

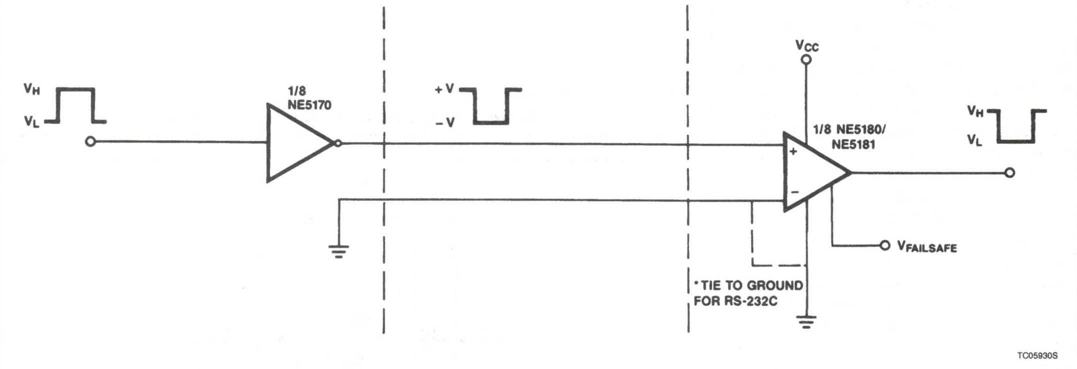
SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay — low to high	$C_L = 50pF$, $V_{ID} = \pm 1V$		500		100	ns
t_{PHL}	Propagation delay — high to low	$C_L = 50pF$, $V_{ID} = \pm 1V$		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, $V_{ID} = \pm 200mV$[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, $V_{ID} = \pm 500mV$	5.5		NA		MHz

NOTE:
1. $V_{ID} = \pm 1V$ for NE5181.

FAILSAFE OPERATION

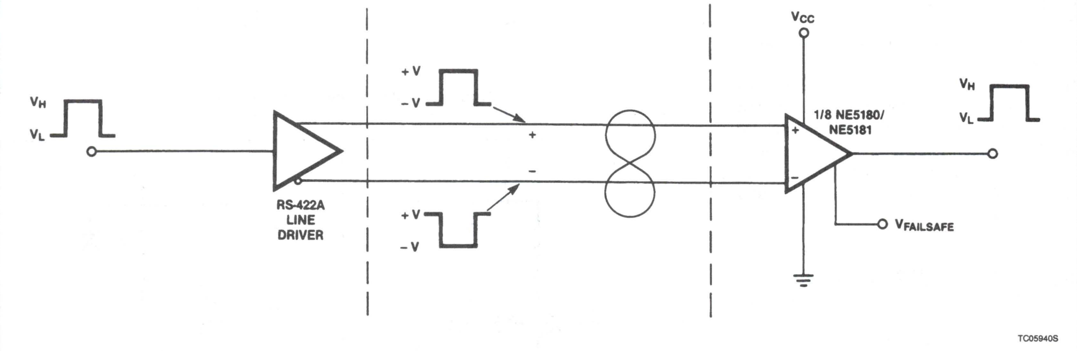
These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides

APPLICATIONS



VH
VL
1/8
NE5170
+V
−V
VCC
1/8 NE5180/
NE5181
+
−
VH
VL
VFAILSAFE
*TIE TO GROUND
FOR RS-232C
TC05930S

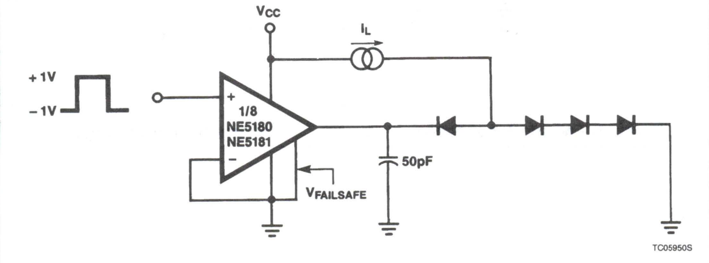
RS-232C/RS-423C Data Transmission



VH
VL
+V
−V
+
−
RS-422A
LINE
DRIVER
+V
−V
VCC
1/8 NE5180/
NE5181
+
−
VH
VL
VFAILSAFE
TC05940S

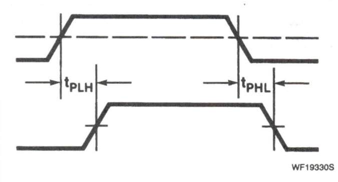
RS-422A Data Transmission

AC TEST CIRCUIT



VCC
IL
+1V
−1V
+
1/8
NE5180
NE5181
−
VFAILSAFE
50pF
TC05950S

VOLTAGE WAVEFORMS



tPLH
tPHL
WF19330S

Octal Differential Line Receivers NE5180/NE5181

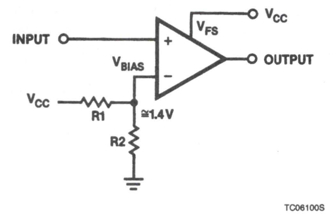
a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).



NOTE:
Two silicon diodes may be used in place of R2.

Figure 2. Single-Input Failsafe Programming

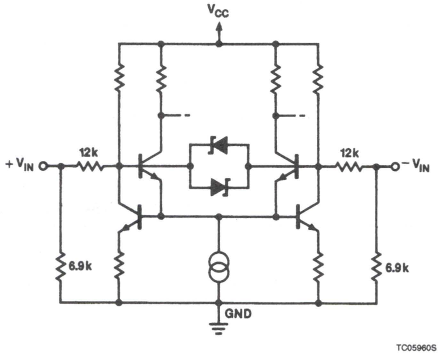


Figure 3. Differential Input Stage

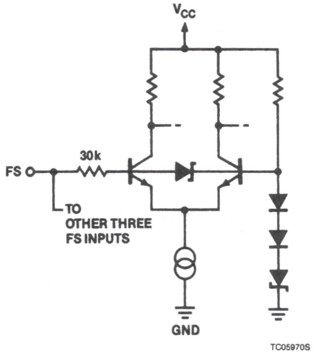


Figure 4. Failsafe Input Stage

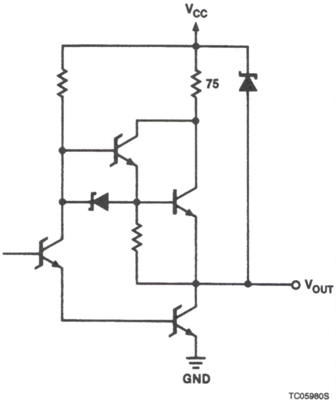


Figure 5. Output Stage

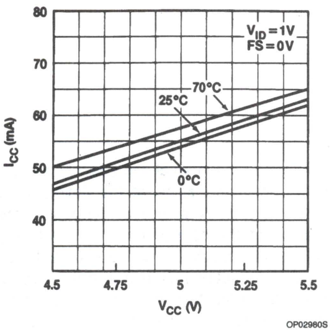


Figure 6. Typical Supply Current vs Supply Voltage

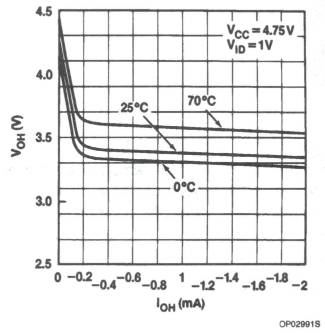


Figure 7. Typical High Level Output Voltage vs Output Current

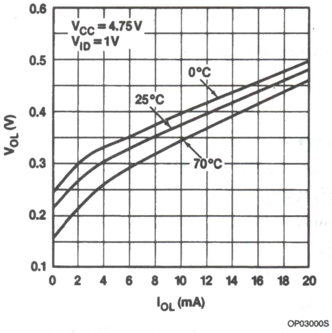
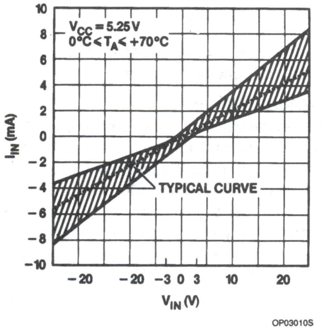


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

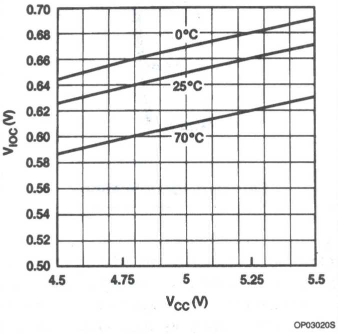


Figure 10. Typical V_{IOC} vs V_{CC}

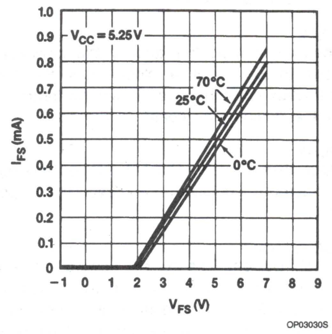


Figure 11. Typical FS Input Current vs FS Applied Voltage

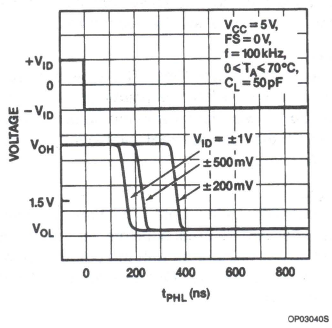


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

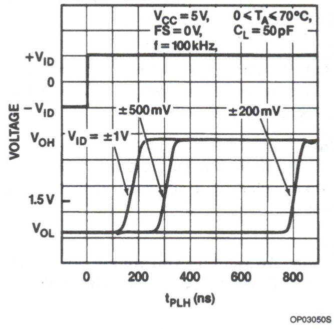


Figure 13. NE5180: Propagation Delay at Various Input Amplitudes

Signetics

Symbols and Definitions for Peripheral and Display Drivers

Linear Products

BCD
Binary Coded Decimal.

$\overline{BI}$/RBO
Blanking Input or Ripple Blanking Output.

CE
Chip Enable.

CLR
Clear. Clear command will preset all internal circuits to a predetermined state.

Duty Cycle
Ratio of time on to time off. Generally expressed in percentage.

f_{MAX}
The maximum clock frequency; the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

I_{BIAS}
Input Bias Current. Current into an analog circuit input, specified at a particular voltage level.

I_{CC} $(-I_{CC})$
Supply Current. The current flowing into the $+V_{CC}$ $(-V_{CC})$ supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{IH}
Input High Current. The current flowing into or out of an input when a specified HIGH level voltage is applied to that input.

I_{IL}
Input Low Current. The current flowing out of an input when a specified LOW level voltage is applied to that input.

I_{OH}
Output Current Source the device can supply while maintaining a specified voltage output level.

I_{OL}
Output Low Current. The current flowing into an output when it is in the LOW state.

I_{OS}
Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is shorted to ground.

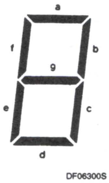
I_S
Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

I_{SEG}
Segment Current. The amount of current supplied to each segment as a display. Current ratios are generally compared to segment 'b'.

LED
Light-Emitting Diode.

$\overline{RBI}$
Ripple Blanking Input.

Segment Identification



Segment Identification

t_H
Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_{PHL}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{REC}
Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_S
Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

Truth Tables
0 = logic level LOW

1 = logic level HIGH

x = don't care condition; has no effect under circuit conditions listed.

Typical Value
The typical value of a particular parameter at 25°C determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min/max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

V_{BR}
Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{CC} $(-V_{CC})$
Supply Voltage. The range of power supply voltage over which the device will operate safely.

V_F
Forward voltage drop of a device at a specified current level.

V_{IH}
Input High Voltage. The range of input voltages recognized by the device as a logic HIGH.

V_{IL}
Input Low Voltage. The range of input voltages recognized by the device as a logic LOW.

Symbols and Definitions for Peripheral and Display Drivers

V_{IN}
The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OH}
Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}
Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{OUT}
The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

V_S
Source Voltage. A separate V_{CC} line depending on part type.

$\overline{XX}$
Negate Bar. When it appears over a function indicates that the "true" or valid condition of that function is a logic LOW level;
i.e., LE would require a logic HIGH level to cause a latch enable;
$\overline{LE}$ would require a logic LOW level to cause a latch enable.

Signetics

NE5090
Addressable Relay Driver

Product Specification

Linear Products

DESCRIPTION

The NE5090 addressable relay driver is a high-current latched driver, similar in function to the 9934 address decoder. The device has 8 open-collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{\text{CE}}$ input line which also serves the function of further address decoding. A common clear input, $\overline{\text{CLR}}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16-pin plastic or Cerdip package.

FEATURES

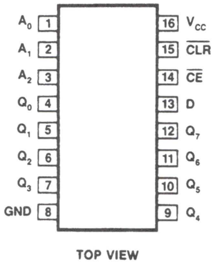
- **8 high-current outputs**
- **Low-loading bus-compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin-compatible with 9334 (Siliconix or Fairchild)**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

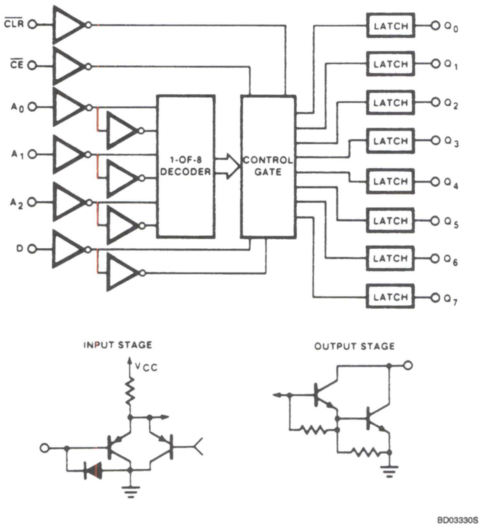
D[1], F, N Packages


A0 1
A1 2
A2 3
Q0 4
Q1 5
Q2 6
Q3 7
GND 8
16 VCC
15 CLR
14 CE
13 D
12 Q7
11 Q6
10 Q5
9 Q4
TOP VIEW

CD10060S

NOTE:
1. SOL-Released in Large SO package only.

BLOCK DIAGRAM


CLR
CE
A0
A1
A2
D
1-OF-8 DECODER
CONTROL GATE
LATCH
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
INPUT STAGE
VCC
OUTPUT STAGE

BD03330S

Addressable Relay Driver NE5090

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 – 3	$A_0 - A_2$	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4 – 7, 9 – 12	$Q_0 - Q_7$	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input condition.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE5090D
16-Pin Plastic DIP	0 to +70°C	NE5090N
16-Pin Cerdip	0 to +70°C	NE5090F

TRUTH TABLE

<table>
<tr><th colspan="6">INPUTS</th><th colspan="8">OUTPUTS</th><th>MODE</th></tr>
<tr><th>$\overline{CLR}$</th><th>$\overline{CE}$</th><th>D</th><th>A_0</th><th>A_1</th><th>A_2</th><th>Q_0</th><th>Q_1</th><th>Q_2</th><th>Q_3</th><th>Q_4</th><th>Q_5</th><th>Q_6</th><th>Q_7</th><th></th></tr>
<tr><td>L</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>Clear</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td rowspan="6">Demultiplex</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td></tr>
<tr><td>H</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="8">$Q_{N-1} \longrightarrow$</td><td>Memory</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td colspan="7">$Q_{N-1} \longrightarrow$</td><td rowspan="6">Addressable Latch</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td colspan="7">$Q_{N-1} \longrightarrow$</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>Q_{N-1}</td><td>H</td><td colspan="6">$Q_{N-1} \longrightarrow$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>Q_{N-1}</td><td>L</td><td colspan="6">Q_{N-1}</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td colspan="7">$Q_{N-1} \longrightarrow$</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td colspan="7">$Q_{N-1} \longrightarrow$</td><td>L</td></tr>
</table>

NOTES:
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

Addressable Relay Driver NE5090

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage	−0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 1388 1712 1315	 mW mW mW
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec. max)	300	°C

NOTE:

1. Derate above 25°C at the following rates:
   F package at 11.1mW/°C.
   N package at 13.7mW/°C.
   D package at 10.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75V$ to $5.25V$, $0°C \leqslant T_A \leqslant +70°C$, unless otherwise specified.[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
 V_{IH} V_{IL}	Input voltage High Low		 2.0 		 0.8	V
V_{OL}	Output voltage Low	$I_{OL} = 150mA$, $T_A = 25°C$ Over temperature		1.05	1.30 1.50	V
 I_{IH} I_{IL}	Input current High Low	 $V_{IN} = V_{CC}$ $V_{IN} = 0V$		 < 1.0 −3.0	 10 −250	μA
I_{OH}	Leakage current	$V_{OUT} = 28V$,		5	250	μA
 I_{CCL} I_{CCH}	Supply current All outputs low All outputs high	$V_{CC} = 5.25V$		 35 22	 60 50	mA
P_D	Power dissipation	No output load			315	mW

NOTE:

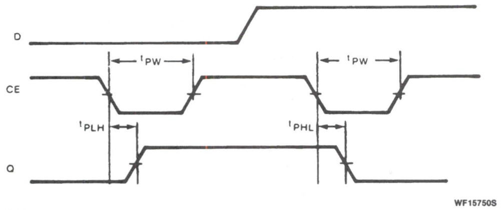
1. All typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $V_{OUT} = 5V$, $I_{OUT} = 100mA$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$.

SYMBOL	PARAMETER	TO	FROM	MIN	TYP	MAX	UNIT
	Propagation delay time						
t_{PLH} t_{PHL}	Low-to-high[1] High-to-low[1]	Output	$\overline{CE}$		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low-to-high[2] High-to-low[2]	Output	Data		920 130	1850 260	ns
t_{PLH} t_{PHL}	Low-to-high[3] High-to-low[3]	Output	Address		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low-to-high[4] High-to-low[4]	Output	$\overline{CLR}$		920	1850	ns
Switching setup requirements							
$t_{S(H)}$[5] $t_{S(L)}$[5]	Setup time high Setup time low	Chip enable Chip enable	High data Low data	40 50			ns
$t_{S(A)}$[6]	Address setup time	Chip enable	Address	40			ns
$t_{H(H)}$[5] $t_{H(L)}$[5]	Hold time high Hold time low	Chip enable Chip enable	High data Low data	10 10			ns
$t_{PW(E)}$[1]	Chip enable pulse width[1]			40			ns

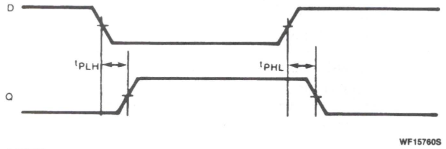
NOTES:
1. See Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data-to-Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address-to-Output timing diagram.
4. See Turn-Off Delay, Clear-to-Output timing diagram.
5. See Setup and Hold Time, Data-to-Enable timing diagram.
6. See Setup Time, Address-to-Enable timing diagram.

TIMING DIAGRAMS


D
CE
tPW
tPW
tPLH
tPHL
Q
WF15750S

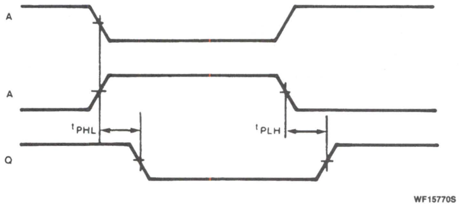
NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width


D
tPLH
tPHL
Q
WF15760S

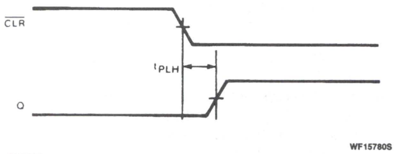
NOTE:
Other Inputs: $\overline{CE}$ = I, $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Data-to-Output


A
A
tPHL
tPLH
Q
WF15770S

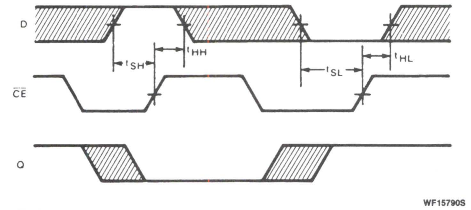
NOTE:
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

Turn-On and Turn-Off Delays, Address-to-Output


$\overline{CLR}$
tPLH
Q
WF15780S

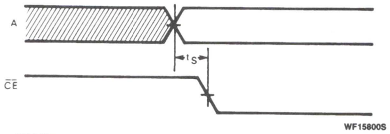
NOTE:
Other Inputs: $\overline{CE}$ = H

Turn-Off Delay, Clear-to-Output


D
tSH
tHH
tSL
tHL
$\overline{CE}$
Q
WF15790S

NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

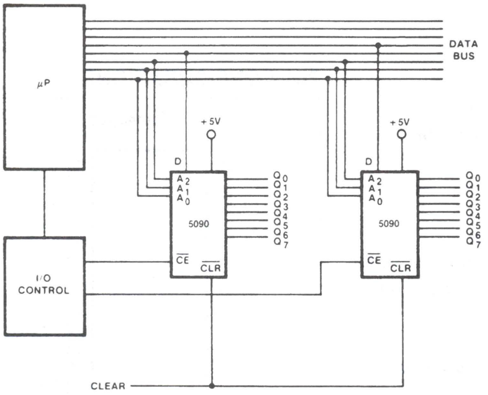
Setup and Hold Time, Data-to-Enable


A
tS
$\overline{CE}$
WF15800S

NOTE:
Other Inputs: $\overline{CLR}$ = H

Setup Time, Address-to-Enable

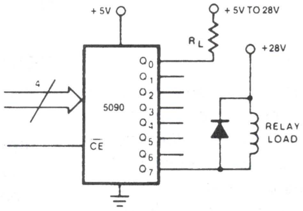
TYPICAL APPLICATIONS


μP
DATA
BUS
+5V
D
A_2
A_1
A_0
5090
$\overline{CE}$
$\overline{CLR}$
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
I/O
CONTROL
CLEAR

LD06040S

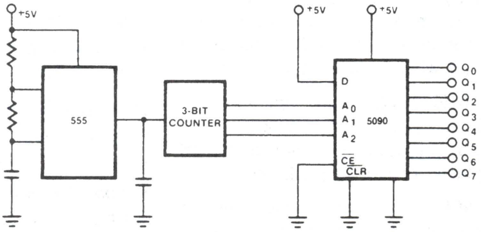
NOTE:
A_0, A_1, A_2 may be connected to the address bus if permitted by system design.

Interfacing With a Microprocessor System


+5V
+5V TO 28V
R_L
+28V
4
5090
$\overline{CE}$
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
RELAY
LOAD

TC10871S

Driving Simple Loads

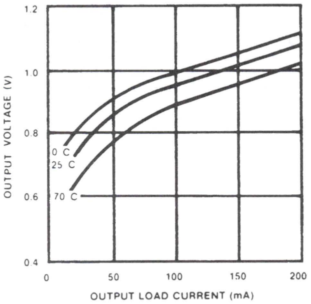

+5V
555
3-BIT
COUNTER
+5V
+5V
D
A_0
A_1
A_2
5090
$\overline{CE}$
$\overline{CLR}$
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7

TC10880S

Operating in Demultiplex Mode

TYPICAL PERFORMANCE CHARACTERISITCS

Output Voltage vs Load Current



OP06770S

Signetics

NE590/NE591
Addressable Peripheral Drivers

Product Specification

Linear Products

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has eight Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has eight open-collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin plastic or Cerdip package.

The NE591 has eight open-emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5V V_{CC} supply. The device is packaged in an 18-pin plastic or Cerdip package.

FEATURES

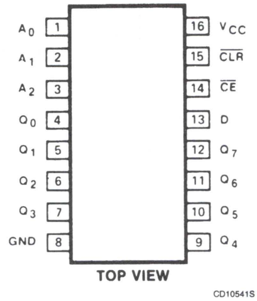
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 54/74LS259**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

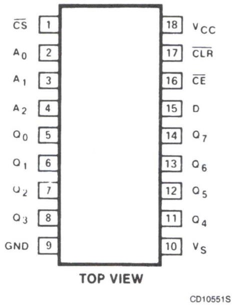
PIN CONFIGURATIONS

F, N Packages



A0 1
A1 2
A2 3
Q0 4
Q1 5
Q2 6
Q3 7
GND 8
16 VCC
15 CLR
14 CE
13 D
12 Q7
11 Q6
10 Q5
9 Q4
TOP VIEW
CD10541S

F, N Packages



CS 1
A0 2
A1 3
A2 4
Q0 5
Q1 6
Q2 7
Q3 8
GND 9
18 VCC
17 CLR
16 CE
15 D
14 Q7
13 Q6
12 Q5
11 Q4
10 VS
TOP VIEW
CD10551S

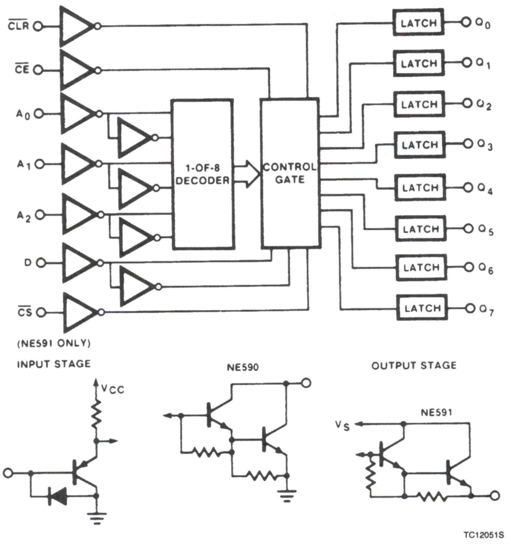
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE590F
16-Pin Plastic	0 to +70°C	NE590N
18-Pin Cerdip	0 to +70°C	NE591F
18-Pin Plastic	0 to +70°C	NE591N

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1 – 3	2 – 4	$A_0 - A_2$	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4 – 7, 9 – 12	5 – 8, 11 – 14	$Q_0 - Q_7$	The 8 device outputs. The NE590 has open-collector Darlington outputs. The NE591 has open emitter-follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
–	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
–	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

BLOCK DIAGRAM


CLR
CE
A0
A1
A2
D
CS
(NE591 ONLY)
1-OF-8 DECODER
CONTROL GATE
LATCH
LATCH
LATCH
LATCH
LATCH
LATCH
LATCH
LATCH
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
INPUT STAGE
VCC
NE590
OUTPUT STAGE
NE591
VS
TC12051S

TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1} →								Memory
H	H	L	X	X	X	X	Q_{N-1} →								
H	L	H	X	X	X	X	Q_{N-1} →								
H	L	L	L	L	L	L	L	Q_{N-1} →							Addressable Latch
H	L	L	H	L	L	L	H	Q_{N-1} →							
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	L	H	H	H	Q_{N-1} →							L	
H	L	L	H	H	H	H	Q_{N-1} →							H	

NOTES:
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"OFF" output state
H = High voltage level/"ON" output state

Addressable Peripheral Drivers NE590/NE591

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage NE590 NE591	 0 to +7 0 to V_{CC}	V
V_S	Source bus voltage NE591 only	-0.5 to +7	V
V_S-V_{CC}	Source/supply differential voltage NE591 only	-5 to +2	V
I_{OUT}	Output current Each output All outputs	 300 1000	mA
P_D	Maximum power dissipation $T_A=25°C$ (still air) NE590[1] F package N package NE591[2] F package N package	 1190 1450 1500 1690	mW
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	165	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C.
   N package at 11.6mW/°C.
2. Derate above 25°C at the following rates:
   F package at 12mW/°C.
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 to 5.25V, 0°C ⩾ T_A ⩽ 70°C, unless otherwise specified. [1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	
	Output voltage					
V_{OL}	Low (NE590 only)	I_{OL} = 250mA, T_A = 25°C		1.0	1.3	
		Over temperature			1.5	V
V_{OH}	High (NE591 only)	I_{OH} = −250mA, V_{CC} = V_S = 5V	2.9			
	Input current					
I_{IH}	High	V_{IN} = V_{CC}		0.1	10	
I_{IL}	Low	V_{IN} = 0V				
	$\overline{CE}$ input			−25	−60	μA
	All other inputs			−15	−50	
I_{OH}	Leakage current	V_{OUT} = 5.25V		10	250	μA
	Supply current[3]	V_S = V_{CC} = 5V				
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					mA
	NE590			15	50	
	NE591			30	50	
P_D	Power dissipation	No output load			350	mW

NOTES:

1. All typical values are at V_{CC} = 5V and T_A = 25°C.
2. For the NE591 V_S = V_{CC} in all tests.
3. Supply current for the NE591 is measured with no output load.

Addressable Peripheral Drivers

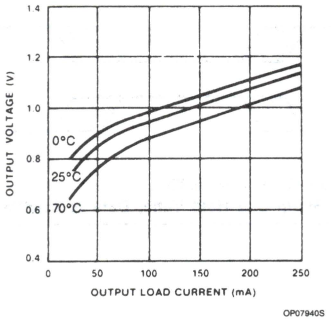
NE590/NE591

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$.

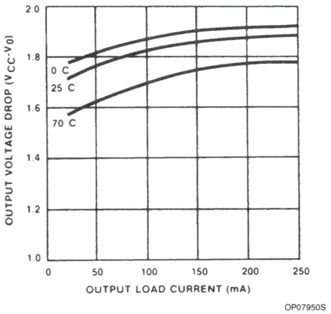
SYMBOL	PARAMETER	TO	FROM	NE590			NE591			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Propagation delay time									
t_{PLH}	Low-to-High[1]	Output	$\overline{CE}$		65	150		50	80	ns
t_{PHL}	High-to-Low[1]				115	230		70	120	
t_{PLH}	Low-to-High[2]	Output	Data		65	130		45	70	ns
t_{PHL}	High-to-Low[2]				120	240		65	100	
t_{PLH}	Low-to-High[3]	Output	Address		100	200		45	80	ns
t_{PHL}	High-to-Low[3]				130	260		75	140	
t_{PLH}	Low-to-High[4]	Output	$\overline{CLR}$		65	130				ns
t_{PHL}	High-to-Low[4]							45	140	
t_{PLH}	Low-to-High[1]	Output	$\overline{CS}$					40	80	ns
t_{PHL}	High-to-Low[1]							70	120	
Switching setup requirements										
$t_{S(H)}$[5]		Chip enable	High data	210			100			ns
$t_{S(L)}$[5]		Chip enable	Low data	210			100			ns
$t_{S(A)}$[6]		Chip enable	Address	30			30			ns
$t_{H(H)}$[5]		Chip enable	High data	40			10			ns
$t_{H(L)}$[5]		Chip enable	Low data	30			10			ns
$t_{S(CS)}$[5]		Chip enable	Low chip select				100			ns
$t_{PW(E)}$	Chip enable pulse width[1]			120			120			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

TYPICAL PERFORMANCE CHARACTERISTICS

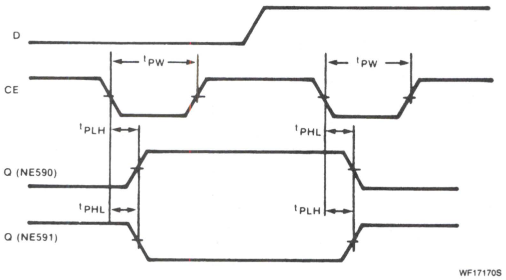


Output Voltage vs Load Current (NE590)



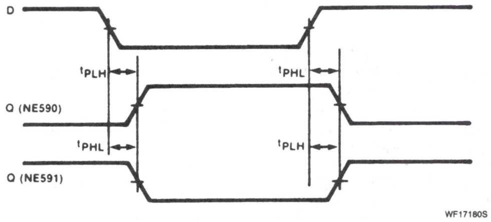
Output Voltage Drop vs Load Current (NE591)

TIMING DIAGRAMS


D
CE
tPW
tPW
tPLH
tPHL
Q (NE590)
tPHL
tPLH
Q (NE591)
WF17170S

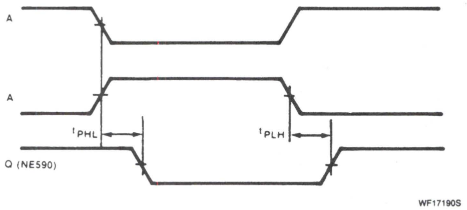
NOTE:
Other Inputs $\overline{CLR}$ = H. A = Stable. $\overline{CS}$ = L.

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width


D
tPLH
tPHL
Q (NE590)
tPHL
tPLH
Q (NE591)
WF17180S

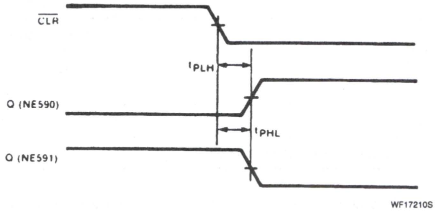
NOTE:
Other Inputs $\overline{CE}$ $\overline{CS}$ = L. $\overline{CLR}$ = H. A = Stable.

Turn-On and Turn-Off Delays, Data-to-Output


A
A
tPHL
tPLH
Q (NE590)
WF17190S

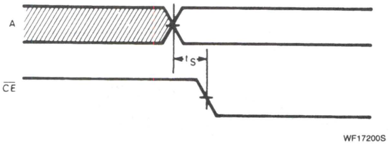
NOTE:
Other Inputs: $\overline{CE}$ = L. $\overline{CLR}$ = L. D = H.

Turn-On and Turn-Off Delays, Address to Output


$\overline{CLR}$
tPLH
Q (NE590)
tPHL
Q (NE591)
WF17210S

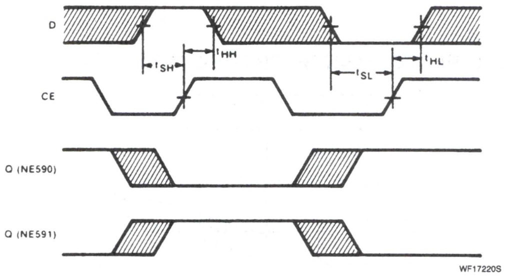
NOTE:
Other Inpputs: $\overline{CE}$ = H. $\overline{CS}$ = H.

Turn-Off Delay, Clear to Output


A
tS
$\overline{CE}$
WF17200S

NOTE:
Other Inputs: $\overline{CLR}$=H. $\overline{CS}$=L.

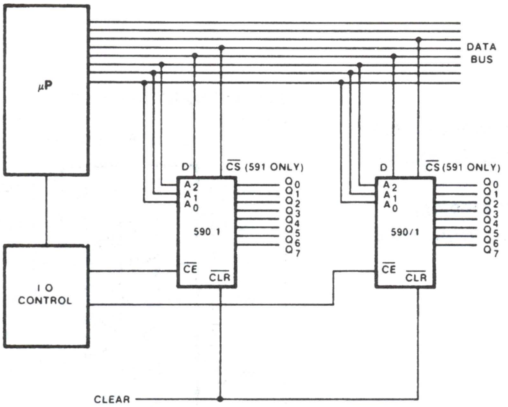
Setup Time, Address to Enable


D
tSH
tHH
tSL
tHL
CE
Q (NE590)
Q (NE591)
WF17220S

NOTE:
Other Inputs: $\overline{CLR}$=H. A=Stable. $\overline{CS}$=L.

Setup and Hold Time, Data to Enable

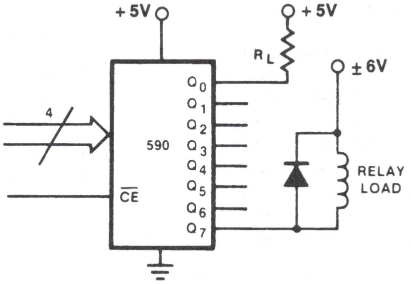
TYPICAL APPLICATIONS


μP
DATA BUS
D
$\overline{CS}$ (591 ONLY)
A2
A1
A0
590 1
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
$\overline{CE}$
$\overline{CLR}$
D
$\overline{CS}$ (591 ONLY)
A2
A1
A0
590/1
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
$\overline{CE}$
$\overline{CLR}$
I O CONTROL
CLEAR

LD06180S

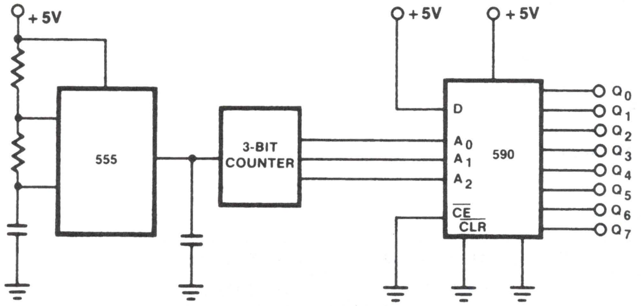
NOTE:
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

Interfacing the 590/591 With a Microprocessor System


+5V
+5V
R_L
±6V
4
590
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
$\overline{CE}$
RELAY LOAD

TC12061S

NE590 Driving Simple Loads


+5V
555
3-BIT COUNTER
+5V
+5V
D
A0
A1
A2
590
$\overline{CE}$
$\overline{CLR}$
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

TC12070S

NE590 Operating in Demultiplex Mode

ULN2003/04

High Voltage/High Current Darlington Transistor Arrays

Product Specification

Linear Products

DESCRIPTION

These high voltage, high current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open-collector outputs and integral suppression diodes for inductive loads. Peak in-rush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps, also.

The Type ULN2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS 5V supply voltage.

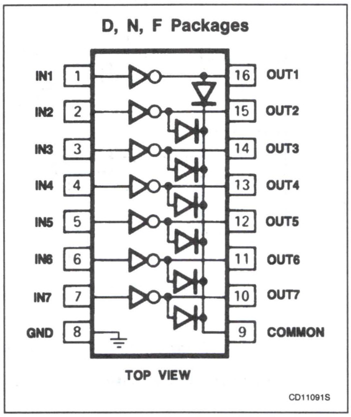
The Type ULN2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN2003.

In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic package.

FEATURES

- **Peak in-rush current 600mA**
- **Protected internally against inductive loads**
- **Open-collector topology**
- **Compatible with most logic technologies**

PIN CONFIGURATION

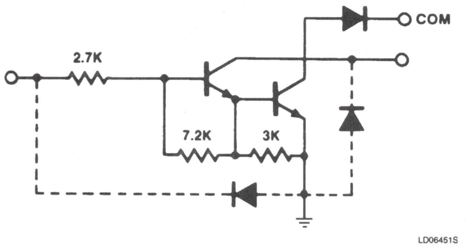


ORDERING INFORMATION

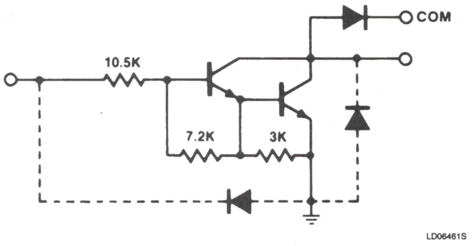
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	ULN2003N
16-Pin Plastic DIP	0 to +70°C	ULN2004N
16-Pin Cerdip	0 to +70°C	ULN2003F
16-Pin Cerdip	0 to +70°C	ULN2004F
16-Pin Plastic SO	0 to +70°C	ULN2003D
16-Pin Plastic SO	0 to +70°C	ULN2004D

High Voltage/High Current Darlington Transistor Arrays ULN2003/04

EQUIVALENT SCHEMATICS



Type ULN2003
(each driver)



Type ULN2004
(each driver)

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ free air temperature for any one Darlington pair unless otherwise specified.[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CE}	Output voltage	50	V
V_{IN}	Input voltage	30	V
V_{EBO}	Emitter base voltage	6	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_D	Maximum power dissipation[2] F package N package D package	 1190 1450 1090	 mW mW mW
T_J	Operating junction temperature	150	°C
T_A	Operating ambient temperature range	0 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTES:

1. Under normal operating conditions, these units will sustain 350mA per output with $V_{CE(SAT)} = 1.6V$ at 70°C with a pulse width of 20ms and a duty cycle of 30%.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

High Voltage/High Current Darlington Transistor Arrays ULN2003/04

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	TEST FIG.	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
I_{CEX}	Output leakage current	$V_{CE} = 50V$, $T_A = 70°C$	1A			100	µA
	Type ULN2004	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 1V$	1B			500	µA
$V_{CE(SAT)}$	Collector-emitter	$I_C = 350mA$, $I_B = 500\mu A$	2		1.25	1.6	V
	Saturation voltage	$I_C = 200mA$, $I_B = 350\mu A$	2		1.1	1.3	V
		$I_C = 100mA$, $I_B = 250\mu A$	2		0.9	1.1	V
$I_{IN(ON)}$	Input current						
	Type ULN2003	$V_{IN} = 3.85V$	3		0.93	1.35	mA
	Type ULN2004	$V_{IN} = 5V$	3		0.35	0.5	mA
		$V_{IN} = 12V$	3		1.0	1.45	mA
$I_{IN(OFF)}$	Input current	$I_C = 500\mu A$, $T_A = 70°C$	4	50	65		µA
$V_{IN(ON)}$	Input voltage						
	Type ULN2003	$V_{CE} = 2V$, $I_C = 200mA$	5			2.4	V
		$V_{CE} = 2V$, $I_C = 250mA$	5			2.7	V
		$V_{CE} = 2V$, $I_C = 300mA$	5			3.0	V
	Type ULN2004	$V_{CE} = 2V$, $I_C = 125mA$	5			5.0	V
		$V_{CE} = 2V$, $I_C = 200mA$	5			6.0	V
		$V_{CE} = 2V$, $I_C = 275mA$	5			7.0	V
		$V_{CE} = 2V$, $I_C = 350mA$	5			8.0	V
C_{IN}	Input capacitance				15	30	pF
I_R	Clamp diode leakage current	$V_R = 50V$	6			50	µA
V_F	Clamp diode forward voltage	$I_F = 350mA$	7		1.7	2	V

NOTES:

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.[1, 2, 3]

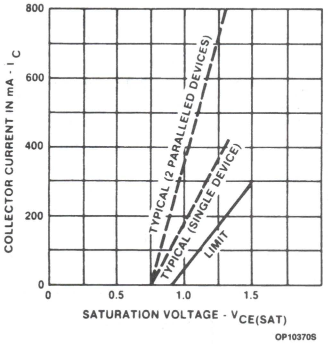
SYMBOL	PARAMETER	TEST CONDITIONS	TEST FIG.	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{PLH}	Turn-on delay	0.5 E_{IN} to 0.5 E_{OUT}			1.0	5	µs
t_{PHL}	Turn-off delay	0.5 E_{IN} to 0.5 E_{OUT}			1.0	5	µs

NOTES:

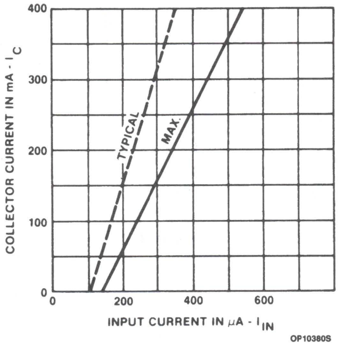
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

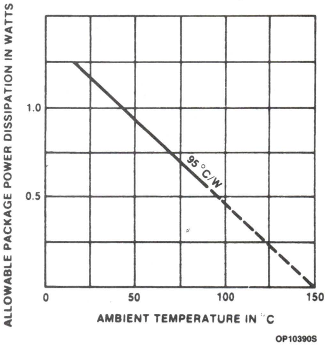
Collector Current as a Function of Saturation Voltage



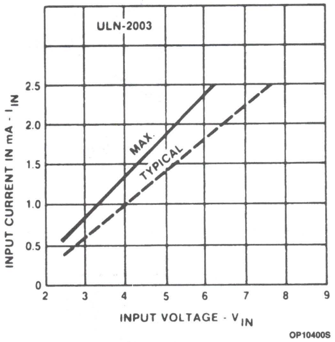
Collector Current as a Function of Input Current



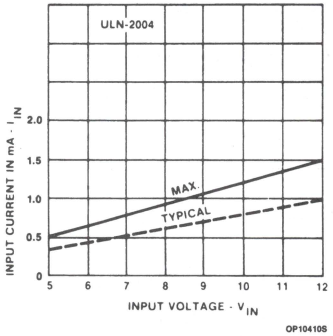
Allowable Average Package Power Dissipation as a Function of Ambient Temperature



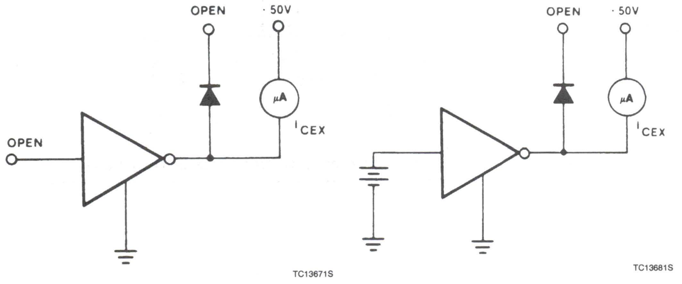
Input Current as a Function of Input Voltage for ULN2003



Input Current as a Function of Input Voltage for ULN2004



TEST CIRCUITS


OPEN
· 50V
OPEN
μA
I_{CEX}
TC13671S
OPEN
· 50V
μA
I_{CEX}
TC13681S

a. b.

Figure 1

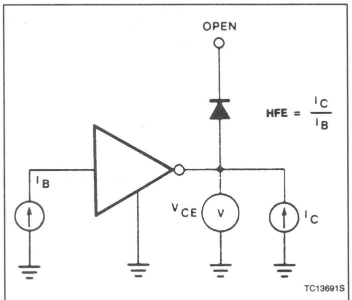

OPEN
HFE = $\frac{I_C}{I_B}$
I_B
V_{CE}
V
I_C
TC13691S

Figure 2

High Voltage/High Current Darlington Transistor Arrays ULN2003/04

TEST CIRCUITS (Continued)

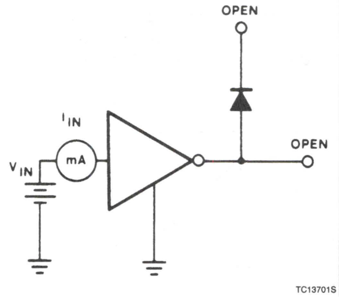

OPEN
I_{IN}
OPEN
V_{IN}
mA
TC13701S

Figure 3

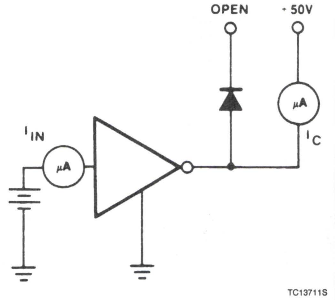

OPEN
+50V
μA
I_{IN}
I_C
μA
TC13711S

Figure 4

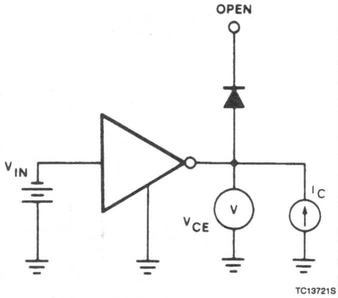

OPEN
V_{IN}
I_C
V
V_{CE}
TC13721S

Figure 5

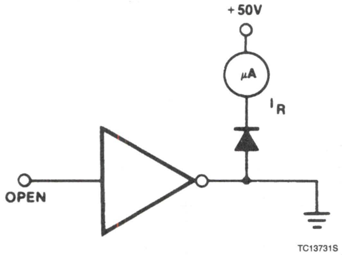

+50V
μA
I_R
OPEN
TC13731S

Figure 6

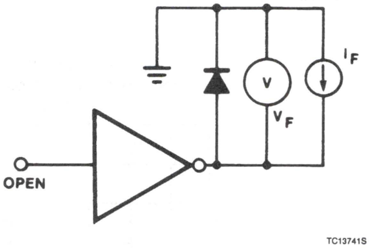
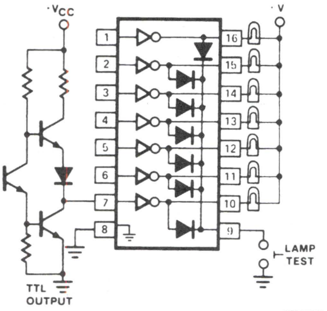
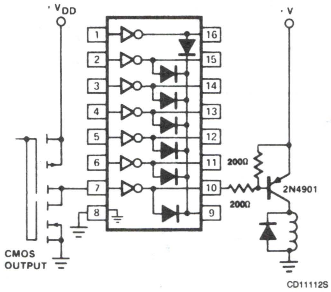

I_F
V
V_F
OPEN
TC13741S

Figure 7

TYPICAL APPLICATIONS


+VCC
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
LAMP TEST
TTL OUTPUT
CD11102S

TTL-to-Load ULN2003


+VDD
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
200Ω
200Ω
2N4901
CMOS OUTPUT
CD11112S

Buffer for Higher Current Loads ULN 2004

Signetics

Symbols and Definitions for Peripheral and Display Drivers

Linear Products

BCD
Binary Coded Decimal.

$\overline{BI}$/RBO
Blanking Input or Ripple Blanking Output.

CE
Chip Enable.

CLR
Clear. Clear command will preset all internal circuits to a predetermined state.

Duty Cycle
Ratio of time on to time off. Generally expressed in percentage.

f_{MAX}
The maximum clock frequency; the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

I_{BIAS}
Input Bias Current. Current into an analog circuit input, specified at a particular voltage level.

I_{CC} ($-I_{CC}$)
Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{IH}
Input High Current. The current flowing into or out of an input when a specified HIGH level voltage is applied to that input.

I_{IL}
Input Low Current. The current flowing out of an input when a specified LOW level voltage is applied to that input.

I_{OH}
Output Current Source the device can supply while maintaining a specified voltage output level.

I_{OL}
Output Low Current. The current flowing into an output when it is in the LOW state.

I_{OS}
Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is shorted to ground.

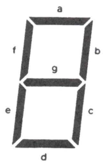
I_S
Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

I_{SEG}
Segment Current. The amount of current supplied to each segment as a display. Current ratios are generally compared to segment 'b'.

LED
Light-Emitting Diode.

$\overline{RBI}$
Ripple Blanking Input.

Segment Identification



DF06300S

Segment Identification

t_H
Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_{PHL}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{REC}
Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_S
Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

Truth Tables
0 = logic level LOW

1 = logic level HIGH

x = don't care condition; has no effect under circuit conditions listed.

Typical Value
The typical value of a particular parameter at 25°C determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min/max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

V_{BR}
Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{CC} ($-V_{CC}$)
Supply Voltage. The range of power supply voltage over which the device will operate safely.

V_F
Forward voltage drop of a device at a specified current level.

V_{IH}
Input High Voltage. The range of input voltages recognized by the device as a logic HIGH.

V_{IL}
Input Low Voltage. The range of input voltages recognized by the device as a logic LOW.

Symbols and Definitions for Peripheral and Display Drivers

V_{IN}
The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OH}
Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}
Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{OUT}
The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

V_S
Source Voltage. A separate V_{CC} line depending on part type.

$\overline{XX}$
Negate Bar. When it appears over a function indicates that the "true" or valid condition of that function is a logic LOW level;
i.e., LE would require a logic HIGH level to cause a latch enable;
$\overline{LE}$ would require a logic LOW level to cause a latch enable.

Signetics

NE587
LED Decoder/Driver

Preliminary Specification

Linear Products

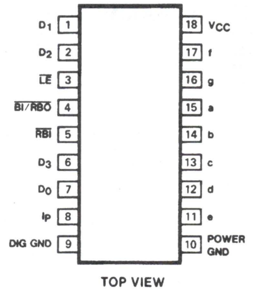
DESCRIPTION
The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES
- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading- and/or trailing-edge zeros**

APPLICATIONS
- **Digital panel motors**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

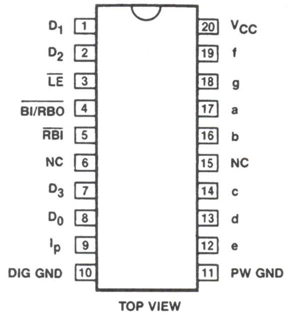
PIN CONFIGURATIONS

F, N Packages


D1 1
D2 2
$\overline{LE}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
D3 6
D0 7
Ip 8
DIG GND 9
18 VCC
17 f
16 g
15 a
14 b
13 c
12 d
11 e
10 POWER GND
TOP VIEW

CD09990S

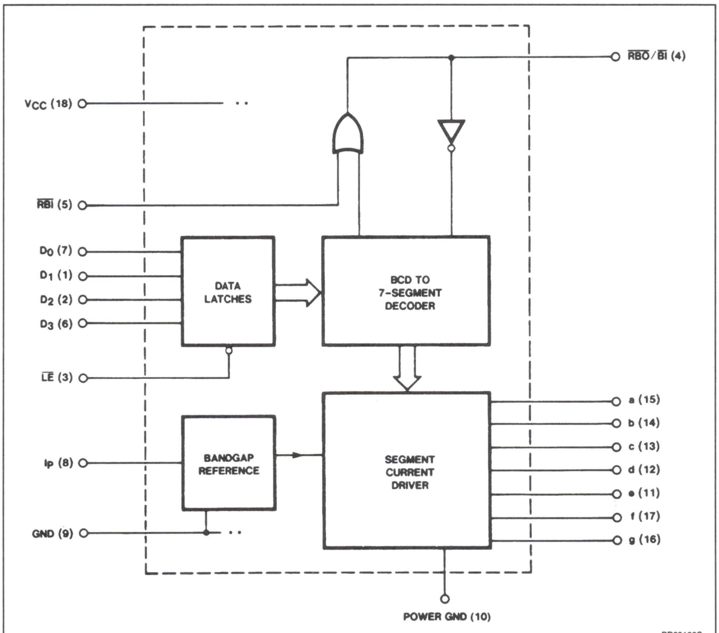
D Package[1]


D1 1
D2 2
$\overline{LE}$ 3
$\overline{BI}/RBO$ 4
$\overline{RBI}$ 5
NC 6
D3 7
D0 8
Ip 9
DIG GND 10
20 VCC
19 f
18 g
17 a
16 b
15 NC
14 c
13 d
12 e
11 PW GND
TOP VIEW

CD10000S

NOTE:
1. SOL and non-standard pinout.

BLOCK DIAGRAM


$\overline{RBO}/\overline{BI}$ (4)
VCC (18)
$\overline{RBI}$ (5)
D0 (7)
D1 (1)
D2 (2)
D3 (6)
DATA LATCHES
BCD TO 7-SEGMENT DECODER
$\overline{LE}$ (3)
Ip (8)
BANDGAP REFERENCE
SEGMENT CURRENT DRIVER
GND (9)
a (15)
b (14)
c (13)
d (12)
e (11)
f (17)
g (16)
POWER GND (10)

BD03130S

LED Decoder/Driver NE587

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE587D[1]
18-Pin Plastic DIP	0 to +70°C	NE587N
18-Pin Cerdip	0 to +70°C	NE587F

NOTE:
1. SOL and non-standard pinout

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage ($D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a − g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Soldering temperature (10sec max)	300	°C

NOTE:
1. Derate power dissipation as indicated
   N package — 95°C/W above 55°C
   F package — 100°C/W above 50°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (± 1%), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All inputs except $\overline{BI}$	2.0		15	V
		$\overline{BI}$	2.0		5.5	
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	$I_{IN} = -12mA$, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$				µA
		V_{IN} = 2.4V		1.0	10	
		V_{IN} = 15V		15	15	
		Input $\overline{BI}$ (Pin 4) $\overline{RBI}$ = H $V_{IN} = V_{CC}$ = 5.25V		10	100	µA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs $D_0 - D_3$		−5		
		$\overline{LE}$, $\overline{RBI}$		−200		µA
		Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{OUT} = 3.0mA		0.2	0.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ $I_{OUT} = -50\mu A$ $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" through "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" through "g" V_{OUT} = 5.0V		20	250	µA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		33	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		50	70	mA

NOTE:

NE587 Programming:

The NE587 output current can be programmed, provided a program resistor, R_P, be connected between I_P (Pin 8) and Ground (Pin 9). The voltage at I_P (Pin 8) is constant (≈1.3V). Thus, a current through R_P is $I_P \approx \frac{1.3V}{R_P}$, as shown in Figure 5. $\frac{I_O}{I_P}$ is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$, $T_A = 25°C$, $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{DAV}	Propagation delay Figure 2	From data to output		135		ns
t_{DAV}	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		30			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	20			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

NOTE:
$t_{DAV} = \frac{1}{2}(t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE							**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	–
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	Blank
**BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	Blank

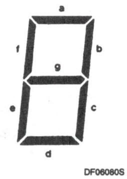
NOTES:
H = HIGH voltage level, output is "OFF"
L = LOW voltage level, output is "ON"
X = Don't care
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO/BI}$ used as an input overrides all other input conditions.

LED Decoder/Driver NE587

NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between R_P (Pin 8) and GND (Pin 9). The voltage at R_P (Pin 8) is constant (≈ 1.40V). A partial schematic of the voltage reference used in the NE587 is shown in Figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high-impedance source such as an I_{OUT} DAC used to control display brightness.



Segment Identification

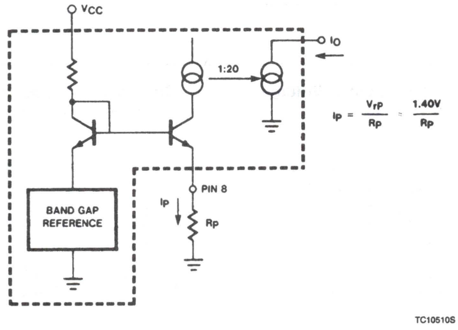


Figure 1

TIMING DIAGRAMS

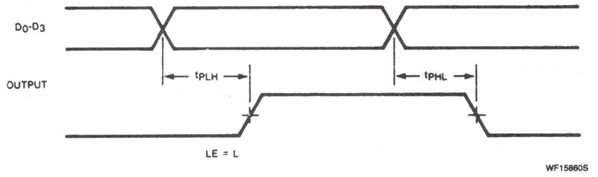


Figure 2. Propagation Delay, Data-to-Output

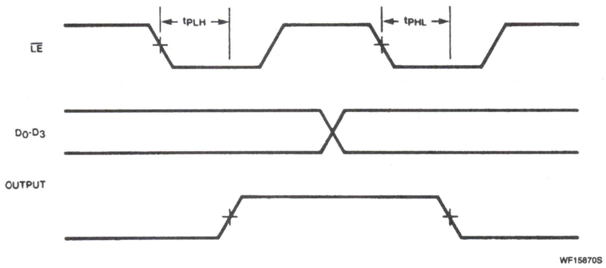


Figure 3. Propagation Delay, Latch Enable-to-Output

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation; but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large-size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant-current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible, consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to Figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC}	Supply voltage to driver
V_S	Supply voltage to display
I_{CC}	Quiescent supply current of driver
I_{SEG}	LED segment current
V_F	LED segment forward voltage at I_{SEG}
K_{DC}	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

LED Decoder/Driver NE587

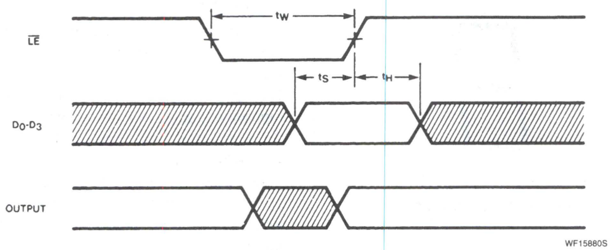


Figure 4

These voltages are all for single-diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus, a maximum power dissipation calculation when all segments are on, is:

$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC} \text{mW}$$

Assuming $V_S = V_{CC} = 5.25V$

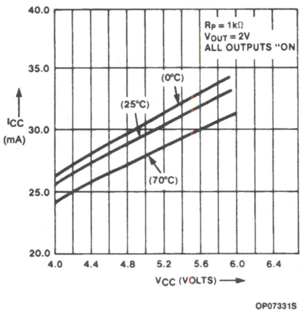
$V_F = 2.0V$

$K_{DC} = 100\%$

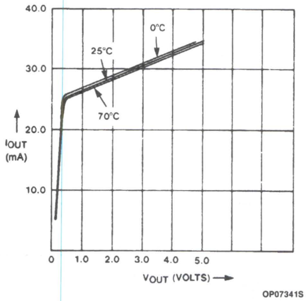
$$P_{D\ MAX} = 5.25 \times 50 + 3.25 \times 7 \times 30\text{mW} = 945\text{mW}$$

TYPICAL PERFORMANCE CURVES

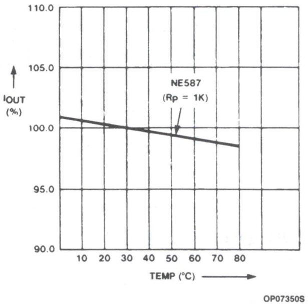
Supply Current vs Supply Voltage



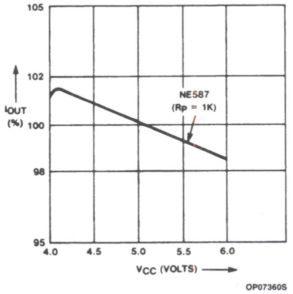
Output Current vs Output Voltage $R_P = 1k\Omega$



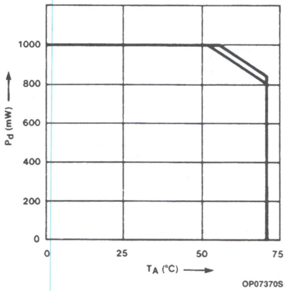
Normalized Output Current vs Temperature $V_{CC} = 5.0V$



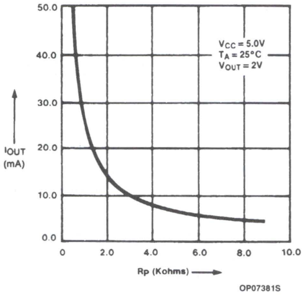
Normalized Output Current vs Supply Voltage $V_O = 2V$, $T_A = 25°C$

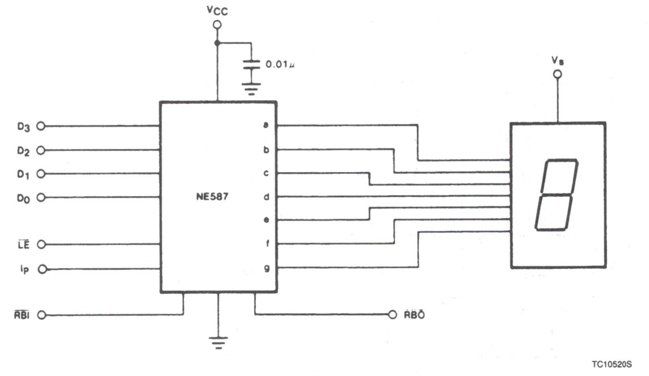


Maximum Power Dissipation vs Temperature



Output Current vs Program Resistor





NOTE:
Decoupling capacitor on V_{CC} should be 0.01µF ceramic.

Figure 6. Driving a Single Digit

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{D\ MAX} = 5.0 \times 30 + 3.00 \times 5 \times 25\text{mW} = 525\text{mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics.)

However, a major portion of this power dissipation ($P_{D\ MAX}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{SEG}} \simeq 10\Omega\ (\tfrac{1}{2}\text{W rating})$$

assuming worst case I_{SEG} of 30mA.

Hence now

$$\begin{aligned} P_{D\ MAX} &= V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{SEG}) \times 7 \times I_{SEG} \times K_{DC} \\ &= 5.25 \times 50 + 1.25 \times 7 \times 30\text{mW} \\ &= 525\text{mW} \end{aligned}$$

and

$$P_{D\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306\text{ mW}.$$

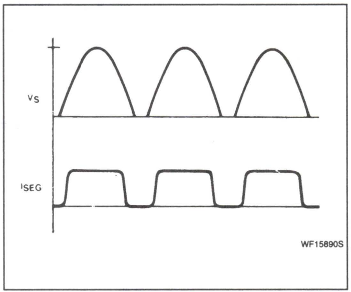
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d,\ V_D \simeq 0.8\text{V}$$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 9. For example a Darlington PNP or NPN emitter-follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact, a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about $3 - 4.5V_{RMS}$ works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
$V_S = 4.9\text{V}$ peak
$V_F = 2.0\text{V}$

The duty cycle is approximately 60%.

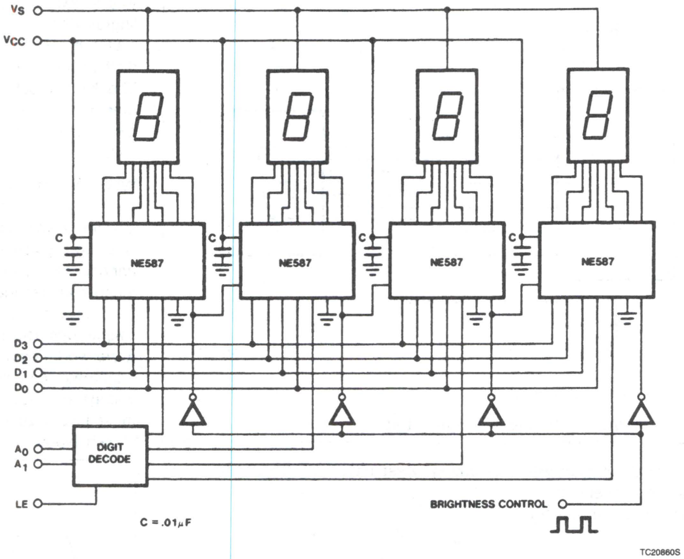

V_S
V_{CC}
C
NE587
NE587
NE587
NE587
D_3
D_2
D_1
D_0
A_0
A_1
DIGIT DECODE
LE
C = .01μF
BRIGHTNESS CONTROL
TC20860S

Figure 7. 4-Digit Display With Brightness Control and Leading-Edge Ripple Blanking

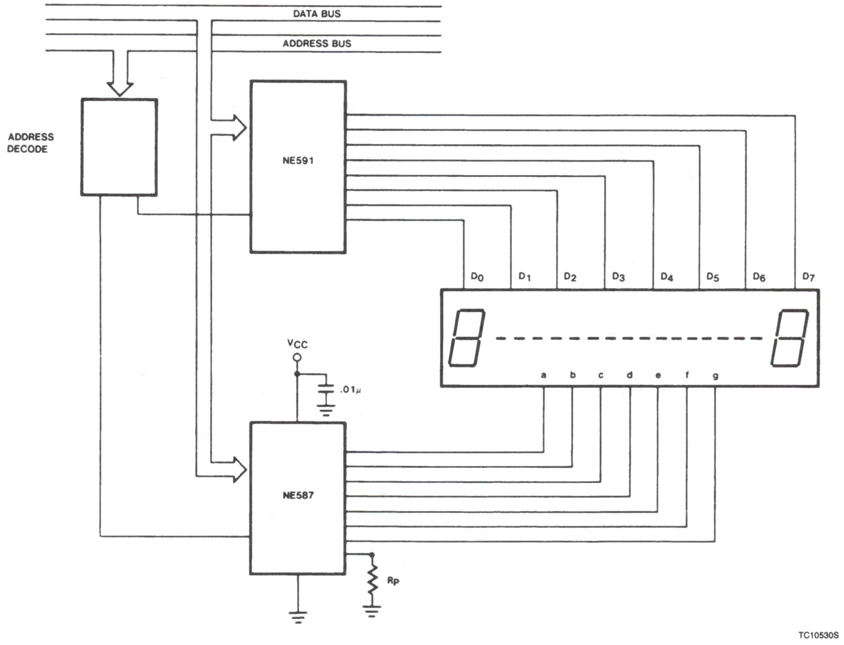

DATA BUS
ADDRESS BUS
ADDRESS DECODE
NE591
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
a
b
c
d
e
f
g
V_{CC}
.01μ
NE587
R_P
TC10530S

Figure 8. Interfacing 8-Digit LED Display With μP Bus

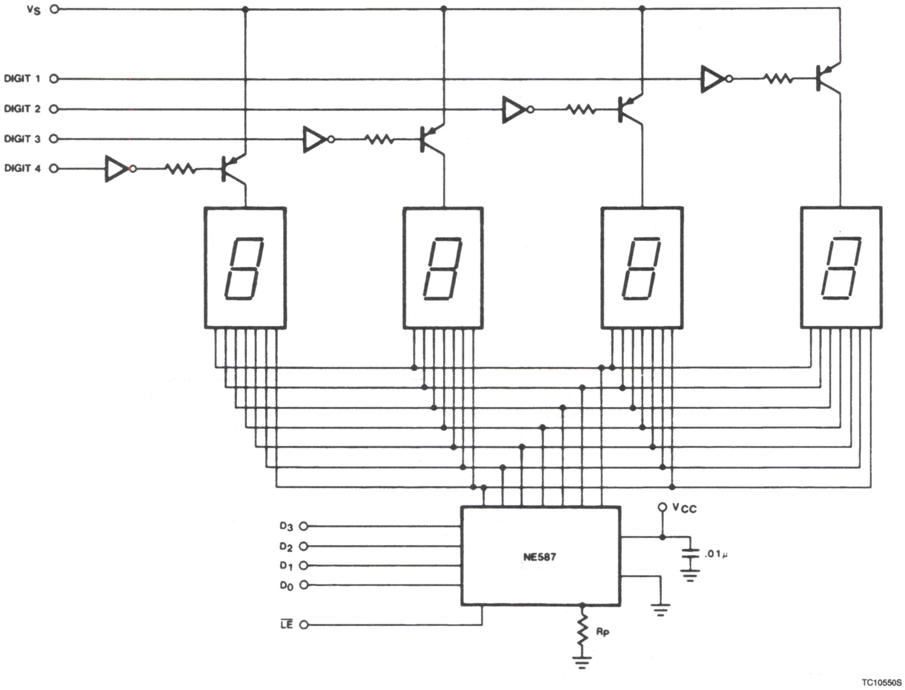

VS
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
D3
D2
D1
D0
LE
NE587
VCC
.01μ
RP
TC10550S

Figure 9. 4-Digit Multiplexed LED Display

Signetics

NE589
LED Decoder/Driver

Product Specification

Linear Products

DESCRIPTION

The NE589 is a latch/decoder/driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

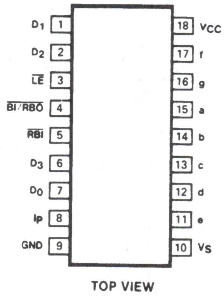
- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing-edge zeroes**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

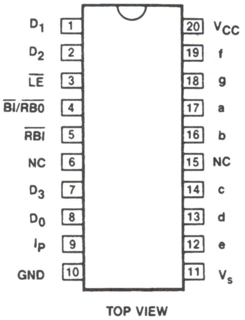
PIN CONFIGURATIONS

N Package


D1 1
D2 2
LE 3
BI/RBO 4
RBI 5
D3 6
D0 7
IP 8
GND 9
18 VCC
17 f
16 g
15 a
14 b
13 c
12 d
11 e
10 VS
TOP VIEW

CD10520S

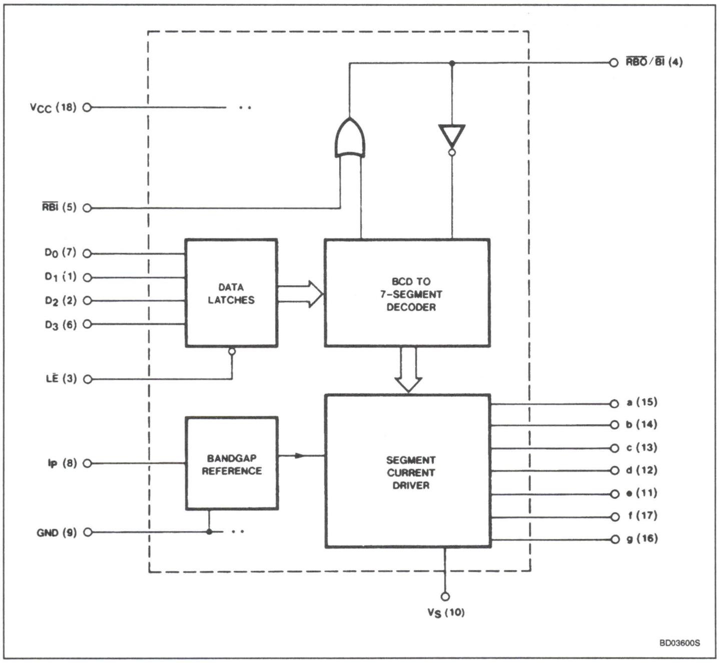
D Package[1]


D1 1
D2 2
LE 3
BI/RBO 4
RBI 5
NC 6
D3 7
D0 8
IP 9
GND 10
20 VCC
19 f
18 g
17 a
16 b
15 NC
14 c
13 d
12 e
11 VS
TOP VIEW

CD10530S

NOTE:
1. SOL and non-standard pinout.

BLOCK DIAGRAM


RBO/BI (4)
VCC (18)
RBI (5)
D0 (7)
D1 (1)
D2 (2)
D3 (6)
DATA LATCHES
BCD TO 7-SEGMENT DECODER
LE (3)
IP (8)
BANDGAP REFERENCE
SEGMENT CURRENT DRIVER
GND (9)
a (15)
b (14)
c (13)
d (12)
e (11)
f (17)
g (16)
VS (10)

BD03600S

LED Decoder/Driver NE589

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL, non-standard	0 to +70°C	NE589D
18-Pin Plastic DIP	0 to +70°C	NE589N

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_S	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage ($D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a − g, RBO)	−0.5 to +7	V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] N package D package	 1690 1390	 mW mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at V_{CC} = V_S = 5V, T_A = 25°C, R_P = 7kΩ (±1%), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}, V_S	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V		 0.1 10	 10 15	 μA μA
I_{IH}	Input high current	Input $\overline{BI}$ (Pin 4) $\overline{RBI}$ = H V_{IN} = V_{CC} = 5.25V		10		μA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs $D_0 - D_3$ $\overline{LE}$, $\overline{RBI}$		−5 −200		μA
I_{IL}	Input low current	Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{OUT} = 3.0mA		0.2	0.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50μA $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" through "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	mA
I_{OFF}	Output segment "OFF" current	Outputs "a" through "g"		20	250	μA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		25	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		30	65	mA

AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_S = 5V$, $T_A = 25°C$, $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

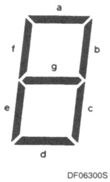
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation delay Figure 2	From data to output		135		ns
t_{PLH}, t_{PHL}	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE								STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	c
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	e
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	f
**BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	blank

NOTES:

H = HIGH voltage level, output is "ON".
L = LOW voltage level, output is "OFF".
X = Don't care.
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO}/\overline{BI}$ used as an input overrides all other input conditions.



Segment Identification

NE589 PROGRAMMING

Output current can be programmed by using a programming resistor, R_P, connected between r_P (Pin 8) and GND (Pin 9). The voltage at r_P (Pin 8) is constant (≈1.3V). A partial schematic of the voltage reference used in the NE589 is shown in Figure 1.

Output current to program current ratio, I_O/I_P, is 120 in the 10mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high-impedance source such as an I_{OUT} DAC used to control display brightness.

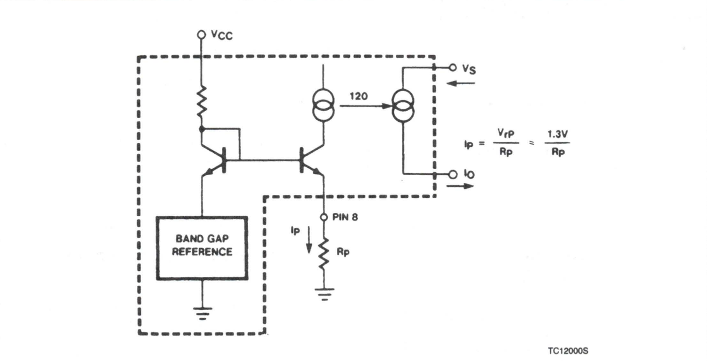


Figure 1

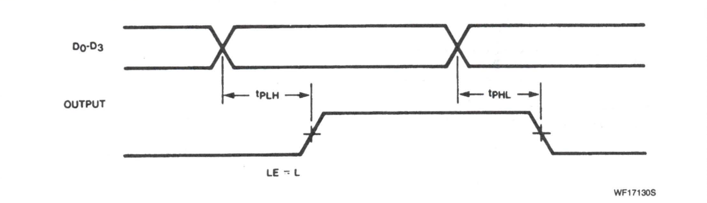


Figure 2. Propagation Delay, Data-to-Output

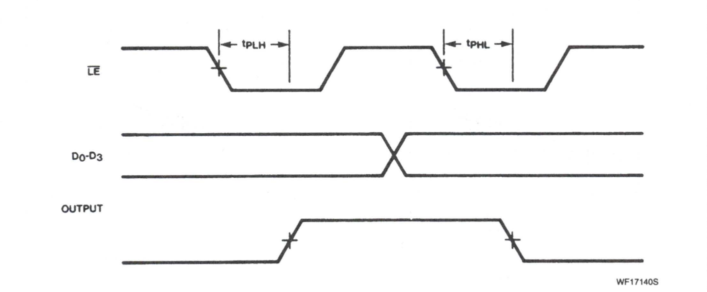


Figure 3. Propagation Delay, Latch Enable-to-Output

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant-current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to Figure 5, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC}	Supply voltage to driver
V_S	Supply voltage to display
I_{CC}	Quiescent supply current of driver
I_{SEG}	LED segment current
V_F	LED segment forward voltage at I_{SEG}
K_{DC}	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Continued)

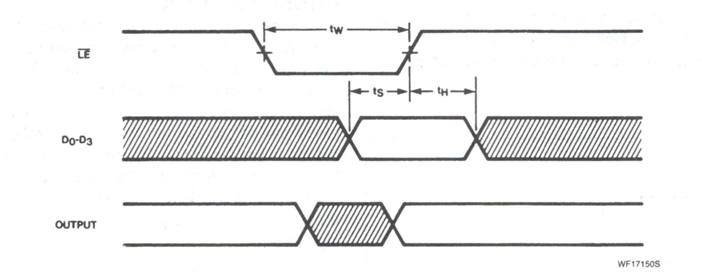


Figure 4. Latch Enable Pulse Width, Setup and Hold Times

These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation, when all segments are on, is:

$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC} \text{mW}$$

Assuming $V_S = V_{CC} = 5.25V$

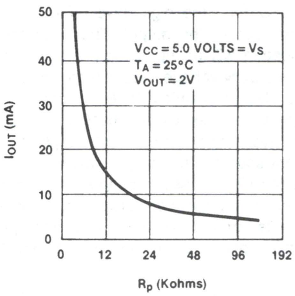
$V_F = 2.0V$

$K_{DC} = 100\%$

$$P_D \text{ max} = 5.25 \times 50 + 3.25 \times 7 \times 30\text{mW} = 945\text{mW}$$

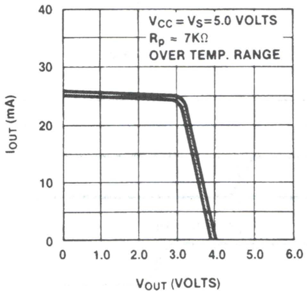
TYPICAL PERFORMANCE CURVES

Output Current vs Program Resistor



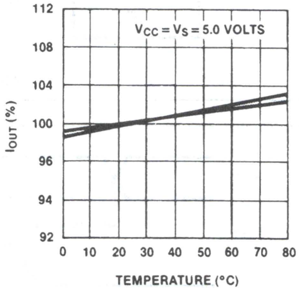
OP07880S

Output Current vs Output Voltage



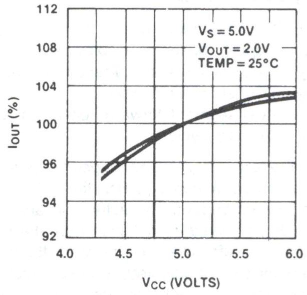
OP07890S

Normalized Output Current vs Temperature



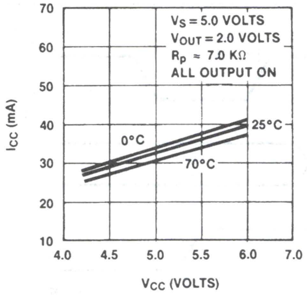
OP07900S

Normalized Output Current vs Supply Voltage



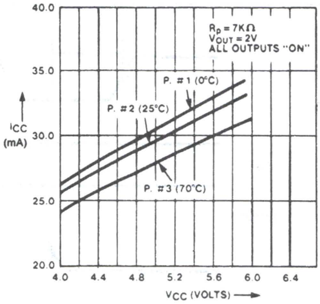
OP07910S

Supply Current vs Supply Voltage

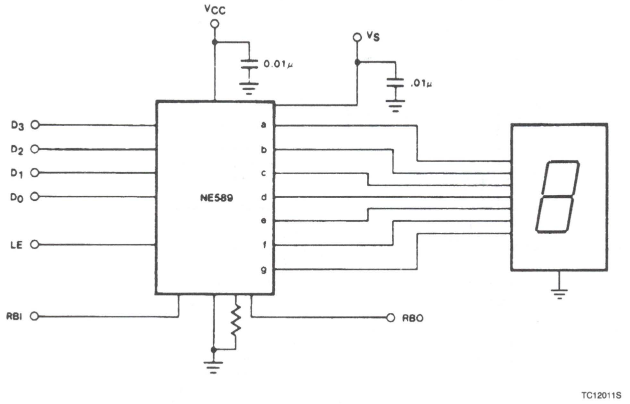


OP07920S

Supply Current vs Supply Voltage



OP07932S



NOTE:
Decoupling capacitor on V_{CC} should be 0.0μF ceramic.

Figure 5. Driving a Single Digit

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{DAV} = 5.0 \times 30 + 3.00 \times 5 \times 25\text{mW} = 525\text{mW}$$

A major portion of this power dissipation (P_D max) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{SEG}} \simeq 10\Omega \text{ (½W rating)}$$

assuming worst-case I_{SEG} of 30mA

Hence now

$$P_D \max = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{SEG}) \times 7 \times XI_{SEG} \times K_{DC}$$
$$= 5.25 \times 50 + 1.25 \times 7 \times 30\text{mW}$$
$$= 525\text{mW}$$

and

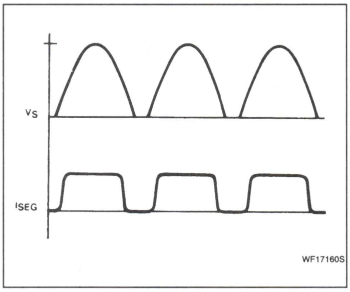
$$P_{DAV} = 5.0 \times 30 + 1.25 \times 5 \times 25$$
$$= 306\text{mW}$$

If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to $V_S - V_F - nV_D$, $V_D \simeq 0.8\text{V}$

Where "n" is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 8. For example a Darlington PNP or NPN emitter-follower may be preferable. Figure 7 shows the NE590 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated A transformer voltage of about 3 – 4.5V_{RMS} works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver. With

$$V_S = 4.9V_{pk}$$
$$V_F = 2.0\text{V}$$

The duty cycle is approximately 60%.

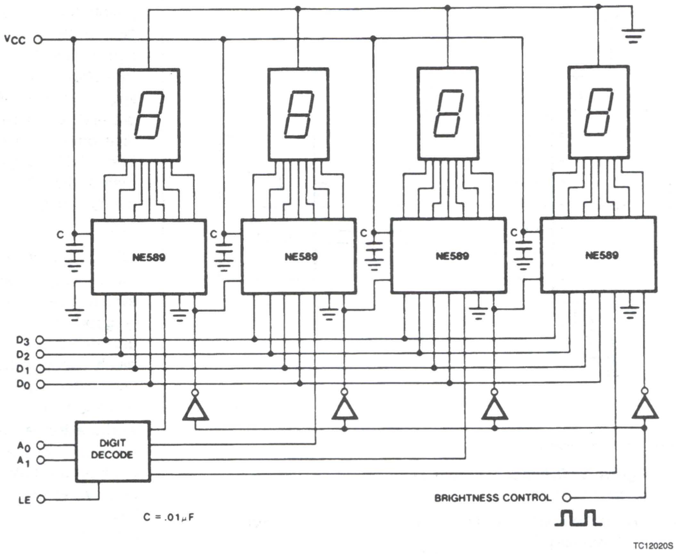

VCC
C
NE589
NE589
NE589
NE589
D3
D2
D1
D0
A0
A1
DIGIT DECODE
LE
C = .01μF
BRIGHTNESS CONTROL
TC12020S

Figure 6. 4-Digit Display With Brightness Control and Leading Edge Ripple Blanking

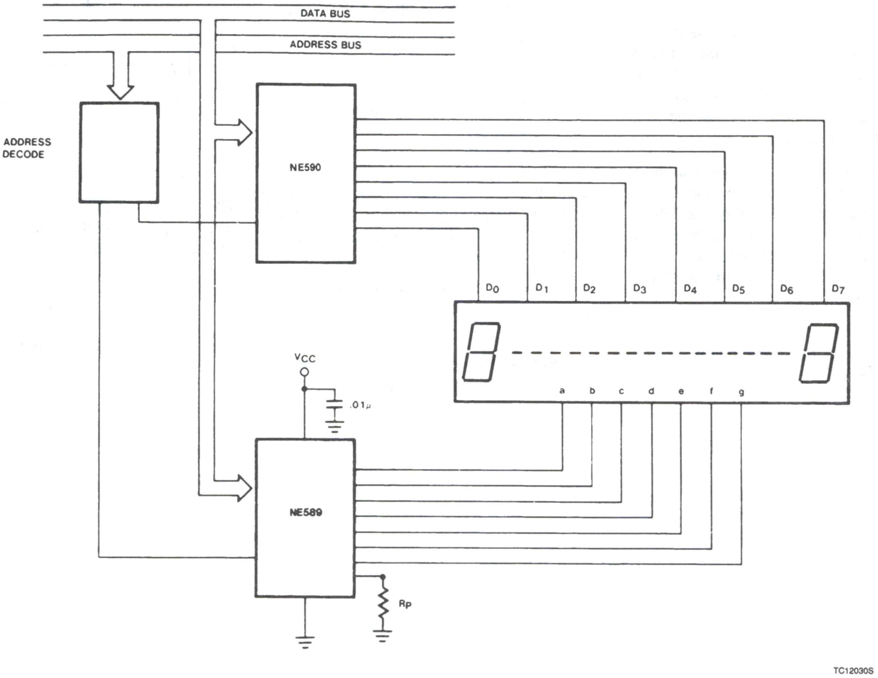

DATA BUS
ADDRESS BUS
ADDRESS DECODE
NE590
D0
D1
D2
D3
D4
D5
D6
D7
a
b
c
d
e
f
g
VCC
.01μ
NE589
Rp
TC12030S

Figure 7. Interfacing 8-Digit LED Display With μP Bus

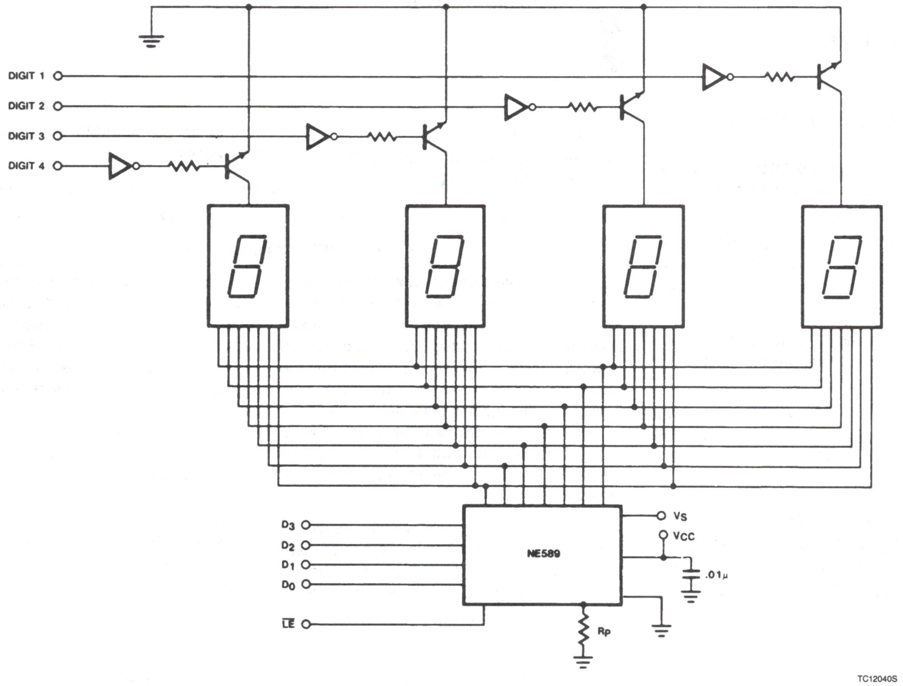

DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
D3
D2
D1
D0
LE
NE589
VS
VCC
.01μ
RP
TC12040S

Figure 8. 4-Digit Multiplexed LED Display

Signetics

Linear Products

AN112

LED Decoder Drivers: Using the NE587 and NE589

Application Note

LED DECODER DRIVER NE587 AND 589

The NE587 and 589 are latchable decoder drivers for LED displays. Figure 1 provides a summary of their features.

The programmable constant-current supplies (fixed or adjustable) are essentially independent of output voltage, power supply voltage, and temperature.

The data (BCD) and $\overline{LE}$ (latch enable) inputs are low loading and thus are compatible with a data bus system.

Figure 2 shows a block diagram of the NE587/589. Seven-segment decoding is implemented using a ROM.

LED DRIVERS AND POWER DISSIPATION CONSIDERATION

The following discussion refers to the NE587, but is also applicable for the 589.

- **Strobed latch**
- **Inputs compatible with NMOS, CMOS, DMOS, TTL**
- **Single 5V supply**
- **Inputs are compatible with microprocessor bus**
- **BCD inputs — hexadecimal outputs**
- **Programmable segment current**

Figure 1. NE587/589 LED Drivers

LED displays are power hungry devices, and, inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the NE587 output is a constant programmed current source, all the remaining supply voltage which is not dropped across the LED (and the digit driver, if used) will appear across the output of the NE587. Thus, the power dissipation in the NE587 will go up sharply if the display power supply voltage rises. Clearly then, it is good design practice to keep the display supply voltage as low as possible, consistent with proper operation of the output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, total system power remains the same.

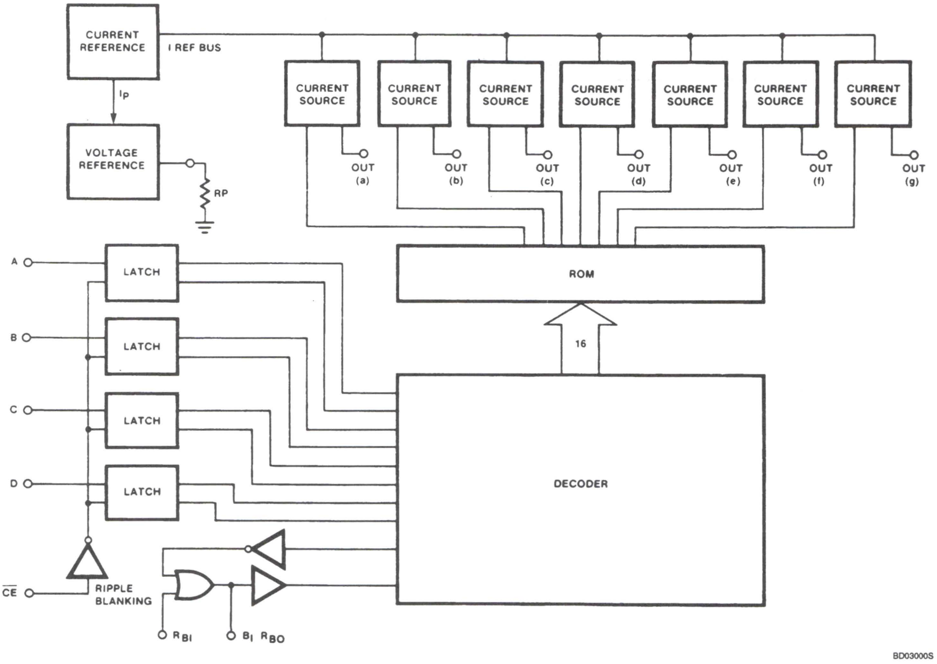

CURRENT REFERENCE
I REF BUS
Ip
VOLTAGE REFERENCE
RP
CURRENT SOURCE
CURRENT SOURCE
CURRENT SOURCE
CURRENT SOURCE
CURRENT SOURCE
CURRENT SOURCE
CURRENT SOURCE
OUT (a)
OUT (b)
OUT (c)
OUT (d)
OUT (e)
OUT (f)
OUT (g)
A
B
C
D
LATCH
LATCH
LATCH
LATCH
ROM
16
DECODER
$\overline{CE}$
RIPPLE BLANKING
RBI
BI RBO
BD03000S

Figure 2. NE587/589 LED Drivers Block Diagram

LED Decoder Drivers: Using the NE587 and NE589

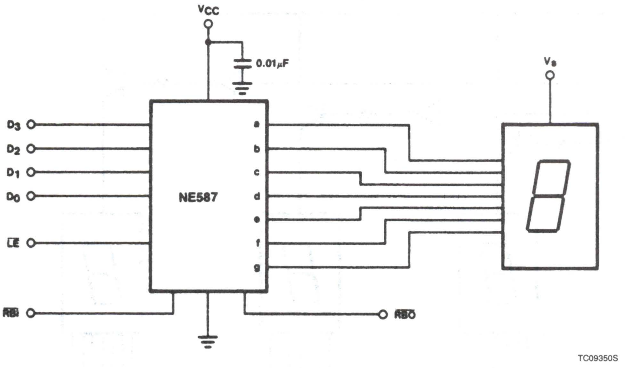


Figure 3. Typical Applications Driving a Single Digit

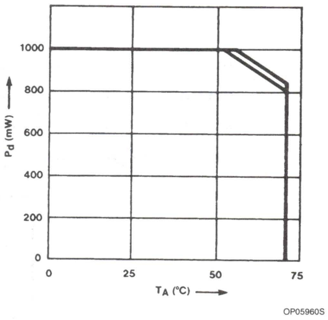


Figure 4. Maximum Power Dissipation vs Temperature

Power dissipation within the NE587 may be calculated as follows. Referring to Figure 3, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

- V_{CC} Supply voltage to driver
- V_S Supply voltage to display
- I_{CC} Quiescent supply current of driver
- I_{SEG} LED segment current
- V_F LED segment forward voltage at I_{SEG}
- K_{DC} % Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected. However, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment, hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC} \text{ mW} \quad (1)$$

Assuming $V_S = V_{CC} = 5.25V$

$V_F = 2.0V$

$K_{DC} = 100\%$

$I_{SEG} = 30mA$

$$P_{D\ MAX} = 5.25 \times 50 + 3.25 \times 7 \times 30mW = 945mW$$

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{D\ AV} = 5.0 \times 30 + 3.00 \times 5 \times 25mW = 525\ mW$$

Operating temperature range limitations can be deduced from the power dissipation graph in Figure 4.

However, a major portion of this power dissipation ($P_{D\ MAX}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_F for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by using equation 2.

$$R_S = \frac{V_{DROP}}{I_{SEG} \times \#\text{ of SEG}} \quad (2)$$

or

$$R_S = \frac{2.0}{7 \times I_{SEG}} \simeq 10\Omega \text{ (1/2W rating)}$$

assuming worst-case I_{SEG} of 30mA, now:

$$P_{D\ MAX} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{SEG}) \times 7 \times I_{SEG} \times K_{DC}$$
$$= 5.25 \times 50 + 1.25 \times 7 \times 30mW = 525mW \quad (3)$$

and $P_{D\ AV} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306mW$

If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$V_S - V_F - nV_D$, $V_D \simeq 0.8V$

Where n is the number of diodes used, and so power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 5. For example, a Darlington PNP or NPN emitter-follower may be preferable. Figure 6 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V, which means that the power dissipation is evenly distributed between the two integrated circuits.

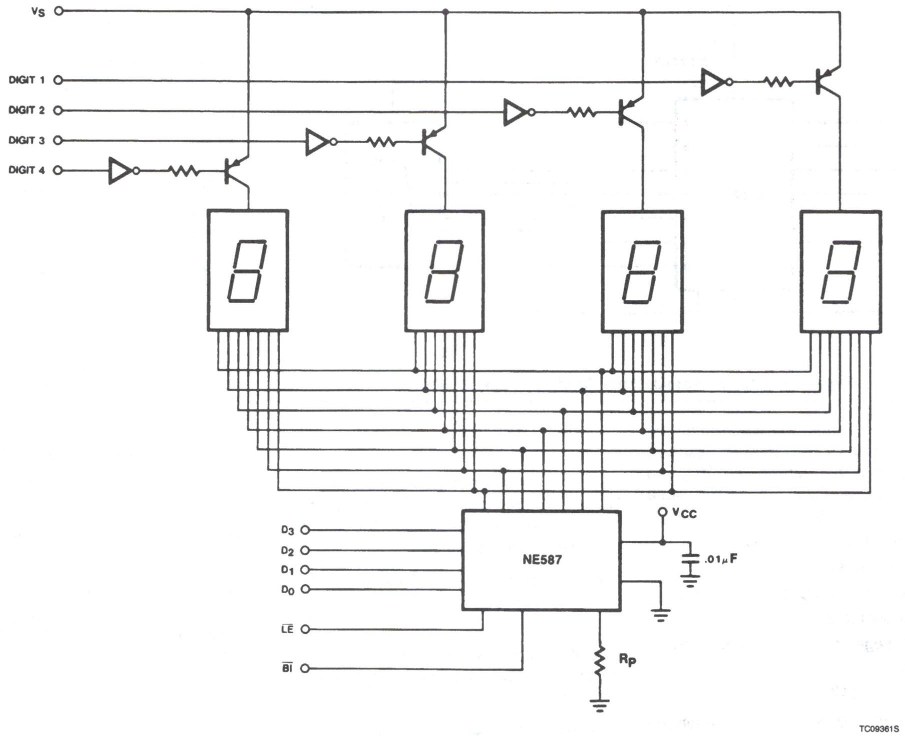

V_S
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
NE587
V_CC
.01μF
D3
D2
D1
D0
LE
BI
R_P
TC09361S

Figure 5. 4-Digit Multiplexed LED Display

LED Decoder Drivers: Using the NE587 and NE589

AN112

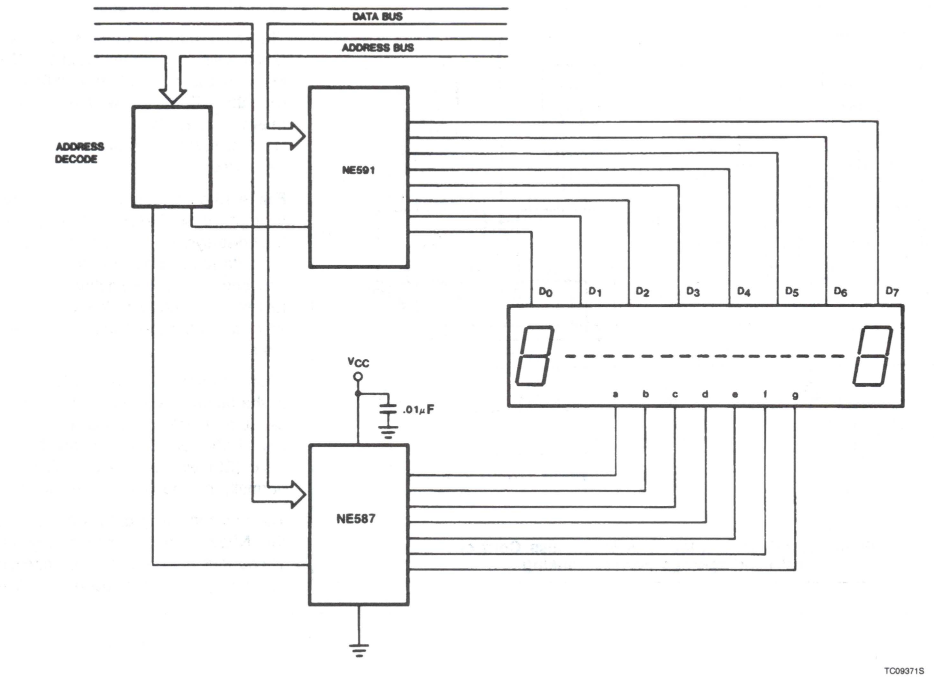


Figure 6. Interfacing 8-Digit LED Display With Microprocessor Bus

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact, a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3 – 4.5V_{RMS} works well in most LED display systems. Waveforms are shown in Figure 7.

The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With $V_S = 4.9V$ peak
$V_F = 2.0V$

The duty cycle is approximately 60%.

V_S in this example was derived by the circuit shown in Figure 7. Remember that the forward voltage drop of the rectifying diode must be subtracted to arrive at the exact peak of the V_S voltage.

Figure 8 shows other typical application schemes for multiplexing LED displays.

ADDRESSABLE PERIPHERAL DRIVERS SUPPORT MICROPROCESSOR-BASED SYSTEMS

The Signetics NE590, NE5090 and NE591 addressable peripheral drivers (APDs) greatly facilitate interfacing a variety of support circuits to microprocessor-based systems.

The APDs are designed to eliminate the need for many of the buffers, latches, TTL ICs, and discrete transistors currently needed to drive peripheral devices.

Figure 9 shows that each driver includes a set of input latches, a 1-of-8 demultiplexer, and a set of high current drive outputs together with the assorted chip enable and clear logic.

The low loading inputs of these drivers (typically $I_{IL} = 15\mu A$ and $I_{IH} = 1\mu A$) allow direct interfacing to the microprocessor bus. Eight addressable latches, which are addressed by a three bit binary code and (set/reset) by a single binary bit, allow storage of each output condition (ON/OFF), allowing the microprocessor to continue processing after the APD has been addressed.

Driver selection is accomplished with a low active chip enable which may be derived from the I/O decoder common to all I/O devices. A low active master clear is also provided to reset all outputs simultaneously. This signal

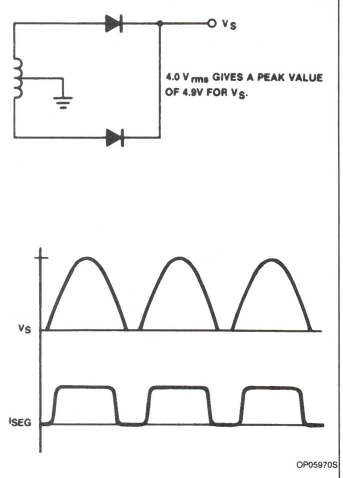


Figure 7

LED Decoder Drivers: Using the NE587 and NE589 AN112

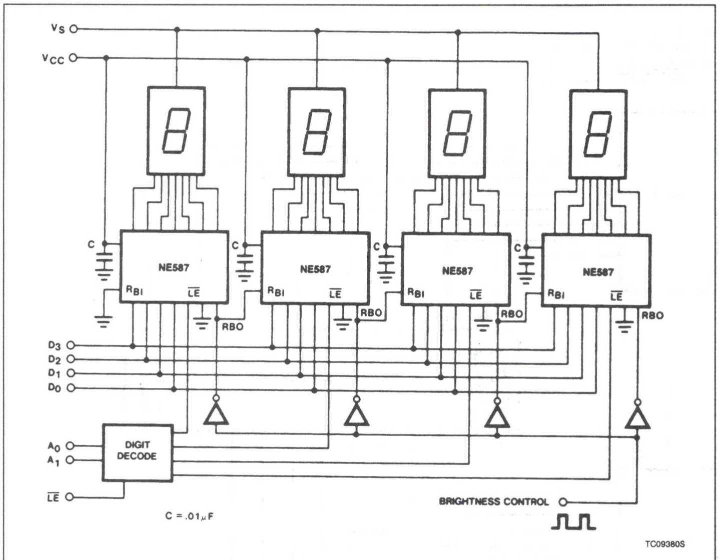

VS
VCC
C
NE587
RBI
LE
RBO
D3
D2
D1
D0
A0
A1
DIGIT DECODE
LE
C = .01μF
BRIGHTNESS CONTROL
TC09380S

Figure 8. 4-Digit Display With Brightness Control and Leading-Edge Ripple Blanking

may be generated from the I/O decoder or set high when not required.

The high current outputs of the drivers (250mA sinking with the NE590, 150mA sinking with the NE5090 and 250mA sourcing with the NE591) allow direct interfacing to relays, motors, lamps, LEDs, and other devices or systems requiring high current drive capabilities.

Figure 10 demonstrates the use of APDs in a microprocessor-based system. When driving LED displays, a single 8-bit word contains all the data required for defining both digit location and segment selection. The APD uses four bits — three to address one of 8 outputs and one to set the output to an ON or OFF state.

When using the NE590 or NE5090, ON refers to the output low state in which the output is capable of sinking a maximum of 250mA for the NE590, or 150mA for the NE5090. The clear ($\overline{CL}$) pin may be tied high and would normally not be required in this application.

The four remaining data bits are required by the NE587 which supplies segment data. These four BCD data bits are converted into seven-segment data used for driving the

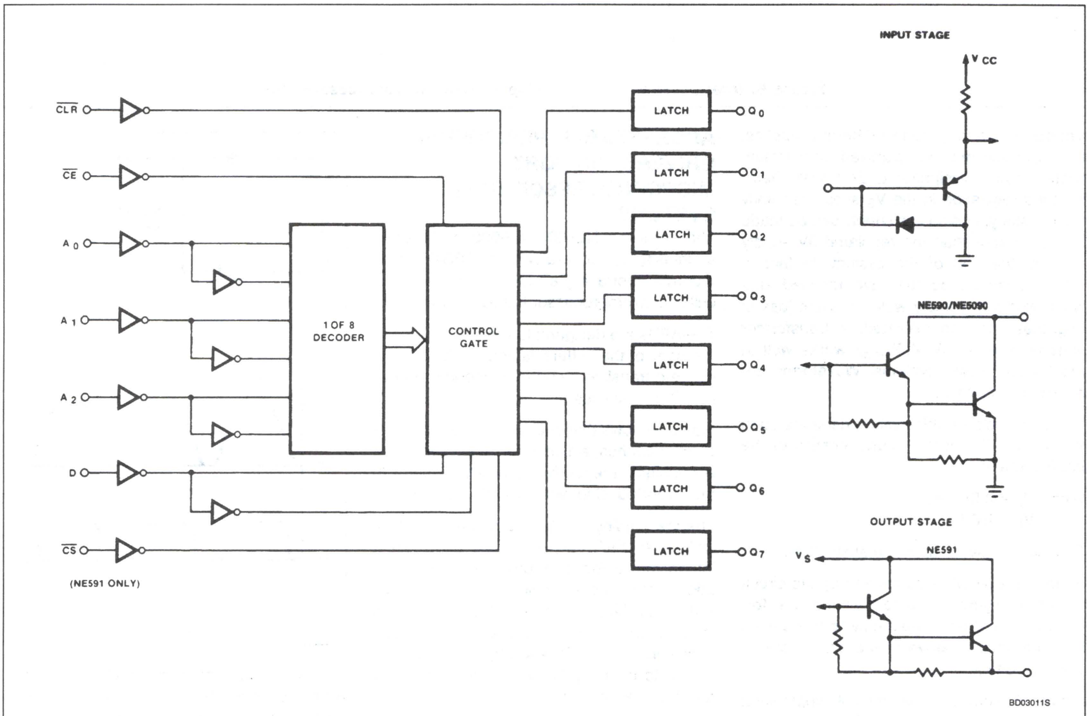

CLR
CE
A0
A1
A2
D
CS
(NE591 ONLY)
1 OF 8 DECODER
CONTROL GATE
LATCH
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
INPUT STAGE
VCC
NE590/NE5090
OUTPUT STAGE
NE591
VS
BD03011S

Figure 9. NE590/591/5090 Block Diagram

LED Decoder Drivers: Using the NE587 and NE589 AN112

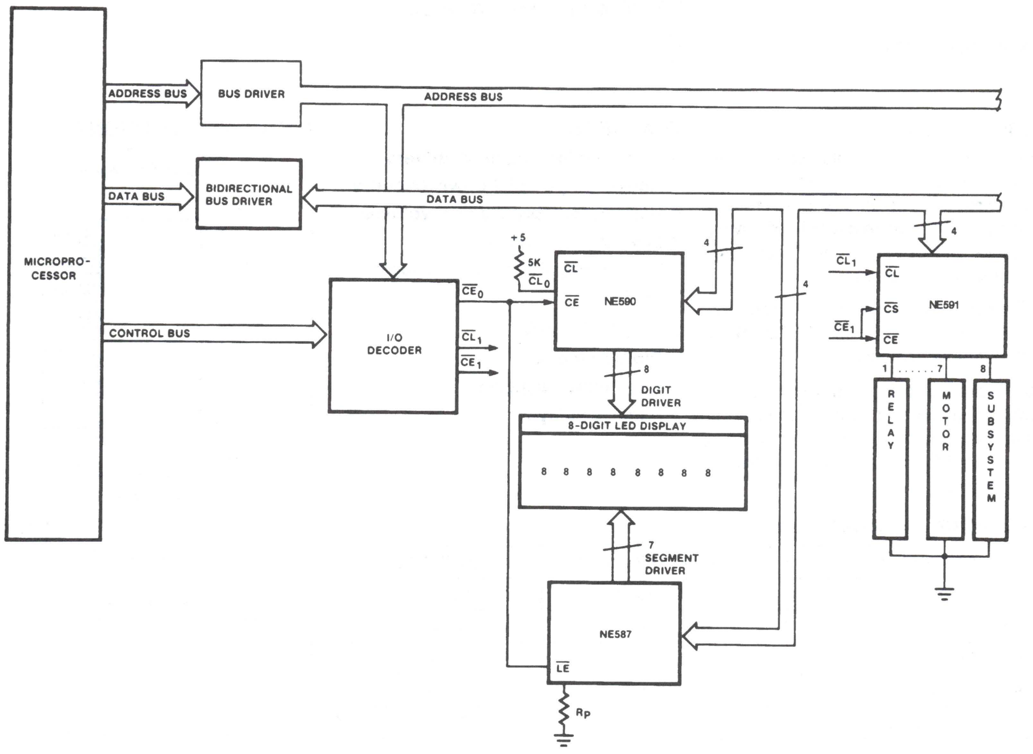

MICROPRO-CESSOR
ADDRESS BUS
BUS DRIVER
ADDRESS BUS
DATA BUS
BIDIRECTIONAL BUS DRIVER
DATA BUS
CONTROL BUS
I/O DECODER
$\overline{CE}_0$
$\overline{CL}_1$
$\overline{CE}_1$
+5
5K
$\overline{CL}_0$
$\overline{CL}$
$\overline{CE}$
NE590
4
4
8
DIGIT DRIVER
8-DIGIT LED DISPLAY
8 8 8 8 8 8 8 8
7
SEGMENT DRIVER
NE587
$\overline{LE}$
R_P
$\overline{CL}_1$
$\overline{CE}_1$
$\overline{CL}$
$\overline{CS}$
$\overline{CE}$
NE591
4
1 ...... 7 8
RELAY
MOTOR
SUBSYSTEM
BD03021S

Figure 10. Microprocessor-Based System

anodes of the LEDs. Data is strobed into the latches by the LATCH ENABLE INPUT at the same time that information is being supplied to the NE590. Since the NE587 provides a constant-current sink, uniform brightness is obtained from each segment in the display. The NE587 is capable of supplying up to 50mA/segment. Segment currents are set by a single programming resistor.

Figure 10 shows several devices connected to the NE591: a relay, a motor, and a D-C subsystem. Each device is selected in the same manner as the LED digits; that is, three bits are used to select the output and one bit is used to turn the output ON or OFF.

An output may be cleared in one of two ways:

1) By direct selection and clearing of the individual latch,
or

2) By clearing all outputs through the use of the clear input.

The latter method does not require addressing.

The examples shown in Figure 10 clearly demonstrate the advantages that can be derived from using the NE590 and NE591 APDs in microprocessor-based systems. These devices provide easy interfacing and minimize the number of interfacing components; they also provide the logic interface to the microprocessor and the switch function and high current drive required by the peripheral units.

Signetics

Linear Products

NE/SA594
Vacuum Fluorescent Display Driver

Product Specification

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network, and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

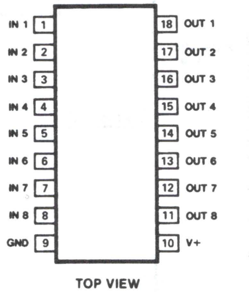
- **Digit and/or segment drivers**
- **Active output pull-down circuitry**
- **High output breakdown voltage**
- **Low supply voltage**
- **Input compatible with all logic outputs**

APPLICATIONS

- **Digital clocks**
- **Dashboard displays**
- **Panel displays**

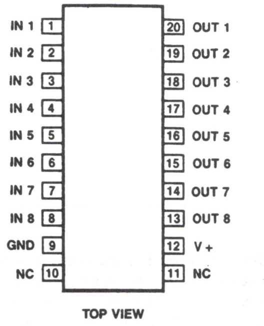
PIN CONFIGURATIONS

N, F Packages


IN 1 1
IN 2 2
IN 3 3
IN 4 4
IN 5 5
IN 6 6
IN 7 7
IN 8 8
GND 9
18 OUT 1
17 OUT 2
16 OUT 3
15 OUT 4
14 OUT 5
13 OUT 6
12 OUT 7
11 OUT 8
10 V+
TOP VIEW

CD11640S

D Package[1]


IN 1 1
IN 2 2
IN 3 3
IN 4 4
IN 5 5
IN 6 6
IN 7 7
IN 8 8
GND 9
NC 10
20 OUT 1
19 OUT 2
18 OUT 3
17 OUT 4
16 OUT 5
15 OUT 6
14 OUT 7
13 OUT 8
12 V+
11 NC
TOP VIEW

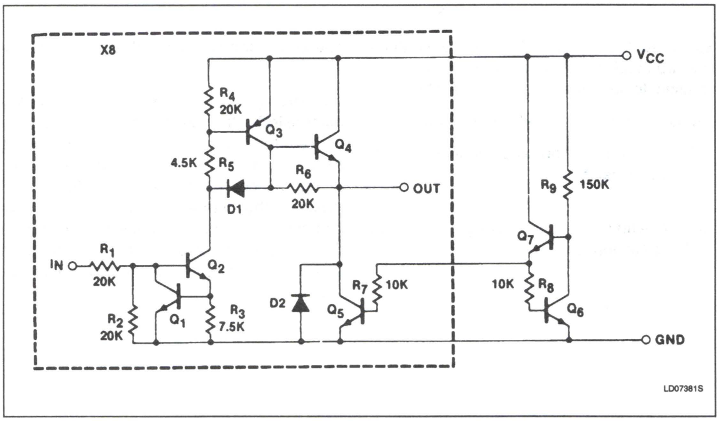
CD11650S

NOTE:
1. SOL – Released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP	0 to +70°C	NE594N
18-Pin Ceramic DIP	0 to +70°C	NE594F
20-Pin Plastic SO	0 to +70°C	NE594D
18-Pin Plastic DIP	-40°C to +85°C	SA594N
18-Pin Ceramic DIP	-40°C to +85°C	SA594F

EQUIVALENT SCHEMATIC


X8
R4 20K
Q3
Q4
4.5K R5
R6 20K
D1
OUT
VCC
R9 150K
Q7
IN
R1 20K
Q2
Q1
R2 20K
R3 7.5K
D2
Q5
R7 10K
10K R8
Q6
GND
LD07381S

Vacuum Fluorescent Display Driver NE/SA594

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	−0.3, +20	V
I_{OUT}	Output current Each output All outputs	 50 200	 mA mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 1500 1690 1390	 mW mW mW
T_A	Operating ambient temperature range NE594 SA594	 0 to 70 −40 to +85	 °C °C
T_{STG}	Storage temperature range	+65 to +150	°C
T_J	Maximum junction temperature	−150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 12.0mW/°C
   N package at 13.5mW/°C
   D package at 11.1mW/°C

Vacuum Fluorescent Display Driver NE/SA594

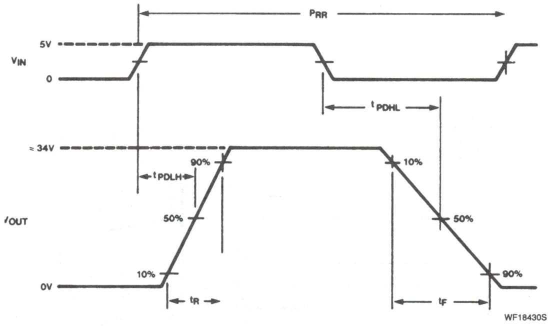
DC ELECTRICAL CHARACTERISTICS V_{CC} = +4.75 to +40V, T_A = 0 to 70°C (NE), T_A = −40 to +85°C (SA), unless otherwise stated.

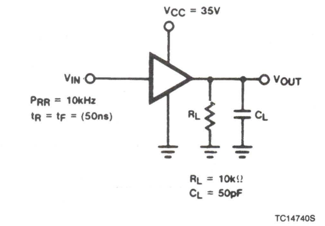
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	V_{CC} = 40V, V_{IN} = 3.5V		3	6	mA
I_{CCL}	Supply current (all outputs low)	V_{CC} = 40V, V_{IN} = 0.4V		0.4	1	mA
V_{IN}	Input voltage range		0		15	V
V_{IH}	Input voltage to ensure logic '1'		2.6			V
V_{IL}	Input voltage to ensure logic '0'				0.8	V
I_{IH}	Input current to ensure logic '1'		100			µA
I_{IL}	Input current to ensure logic '0'				10	µA
I_{IN}	Input current	V_{IN} = 2.6V		60	130	µA
		V_{IN} = 5.0V		180	330	µA
		V_{IN} = 15.0V		.68	1.3	mA
V_{OH}	Output high voltage	V_{IN} = 3.5V, I_{OUT} = −25mA, T_A = 25°C	V_{CC}−1.5	V_{CC}−1.1		V
		V_{IN} = 3.5V, I_{OUT} = −25mA, Over temp.	V_{CC}−2	V_{CC}−1.3		V
		V_{OUT} with respect to V_{CC}				
V_{OH}	Output high, no load voltage	V_{IN} = 3.5V, I_{OUT} = 0, T_A = 25°C, V_{OUT} with respect to V_{CC}	V_{CC}−1	V_{CC}−0.8		V
V_{OFF}	Output 'OFF' voltage level	V_{IN} = 0.8V, I_{OUT} = 0		10	200	mV
I_{OH}	Available output current	V_{CC} = 35V, V_{IN} = 3.5V, V_{OUT} = 30V, T_A = 25°C	−35			mA
I_{OUT}	Output pulldown current	V_{CC} = V_{OUT} = 35V, Inputs open	100	200	400	µA
I_{CEX}	Output leakage current	T_A = 25°C, V_{IN} = 0.4V V_{CC} = 40V, V_{OUT} = 0V		−1 −1		µA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 35V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{PLH}	Propagation delay — low-to-high output transition	50% V_{IN} to 50% V_{OUT}		1	5	µs
t_{PHL}	Propagation delay — high-to-low output transition	50% V_{IN} to 50% V_{OUT}		3	10	µs
t_R	Output rise time	10% V_{OUT} to 90% V_{OUT}		0.5	3	µs
t_F	Output fall time	90% V_{OUT} to 10% V_{OUT}		1.5	5	µs

SWITCHING TIMES OF DRIVERS

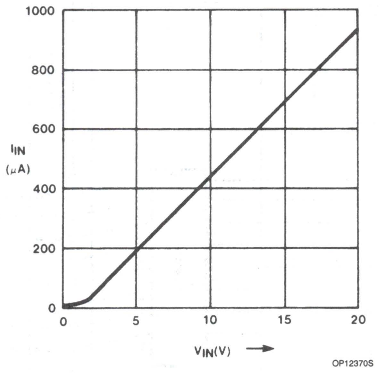

PRR
5V
VIN
0
tPDHL
≈ 34V
90%
10%
tPDLH
VOUT
50%
50%
10%
90%
0V
tR
tF
WF18430S


VCC = 35V
VIN
VOUT
PRR = 10kHz
tR = tF = (50ns)
RL
CL
RL = 10kΩ
CL = 50pF
TC14740S

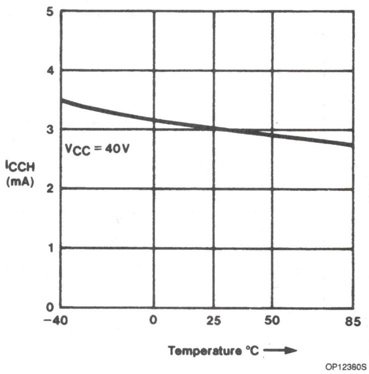
NOTE:
Includes probe and fixture capacitance.

Figure 1. Test Circuit

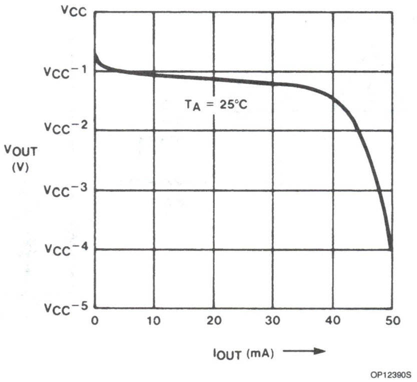
TYPICAL PERFORMANCE CHARACTERISTICS



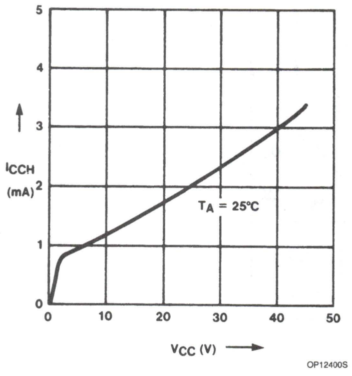
I_{IN} vs V_{IN}



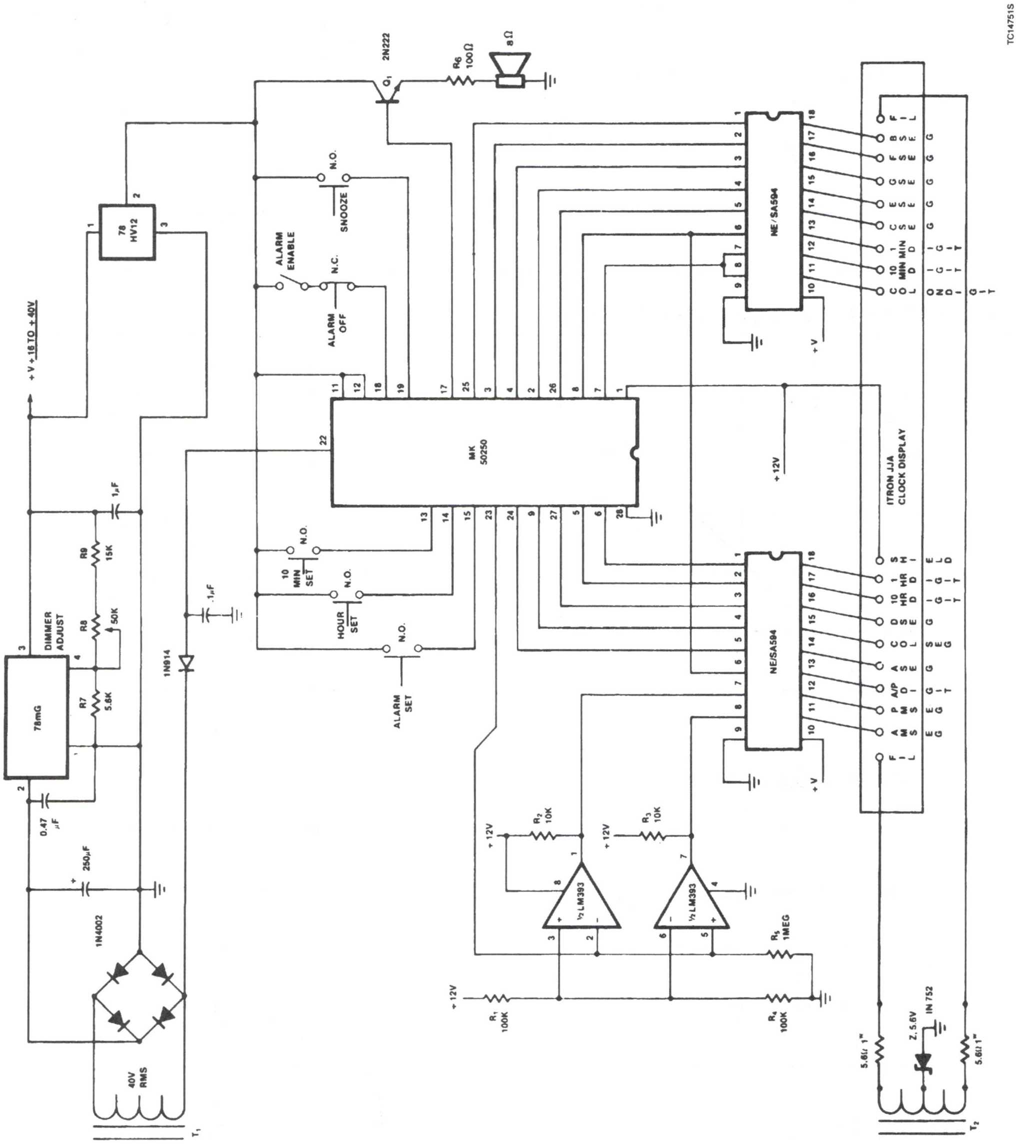
I_{CCH} vs Temperature



Output Voltage vs Output Current



I_{CC} vs V_{CC} (All inputs High)



TC14751S
+V +16 TO +40V
78
HV12
78mG
DIMMER ADJUST
R9 15K
R8 50K
R7 5.6K
1μF
.1μF
0.47 μF
250μF
1N4002
1N914
40V RMS
T1
2N222
Q1
R6 100Ω
8Ω
N.O.
SNOOZE
ALARM ENABLE
N.C.
ALARM OFF
10 MIN SET
HOUR SET
ALARM SET
MK 50250
NE/SA594
NE/SA594
+V
+12V
ITRON JJA CLOCK DISPLAY
½ LM393
½ LM393
R1 100K
R2 10K
R3 10K
R4 100K
R5 1MEG
Z, 5.6V
IN 752
5.6Ω 1W
5.6Ω 1W
T2
FIL
BSEG
FSEG
GSEG
ESEG
CSEG
1 MIN DIGIT
10 MIN DIGIT
COL
ON DIGIT
SHELD
1 HR DIGIT
10 HR DIGIT
DSEG
COLSEG
ASEG
A/P DIGIT
PM SEG
AM SEG
FIL

Figure 2. Typical Application: Digital Clock With Alarm

Signetics

PCF1303T
18-Element Bar Graph LCD Driver

Preliminary Specification

Linear Products

DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_C) when in pointer or thermometer mode.

FEATURES

- **18-element drive capability**
- **Low current consumption**
- **Pointer and thermometer modes**

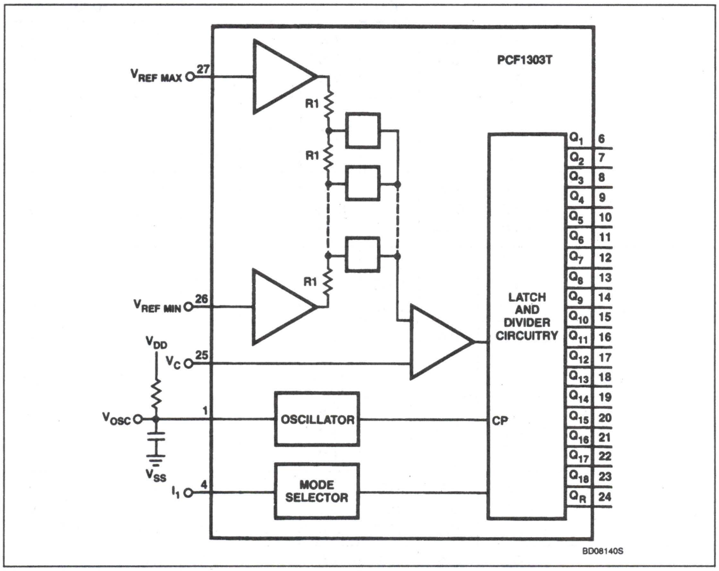
APPLICATION

- **LCD displays**

ORDERING INFORMATION

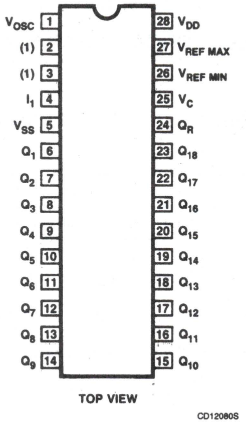
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic SO (SO-28; SOT-136A)	-40°C to 85°C	PCF1303TD

BLOCK DIAGRAM


PCF1303T
$V_{REF\ MAX}$ 27
R1
R1
R1
$V_{REF\ MIN}$ 26
V_{DD}
V_C 25
V_{OSC}
1
V_{SS}
I_1 4
OSCILLATOR
MODE SELECTOR
LATCH AND DIVIDER CIRCUITRY
CP
Q_1 6
Q_2 7
Q_3 8
Q_4 9
Q_5 10
Q_6 11
Q_7 12
Q_8 13
Q_9 14
Q_{10} 15
Q_{11} 16
Q_{12} 17
Q_{13} 18
Q_{14} 19
Q_{15} 20
Q_{16} 21
Q_{17} 22
Q_{18} 23
Q_R 24
BD08140S

PIN CONFIGURATION

D Package


V_{OSC} 1
(1) 2
(1) 3
I_1 4
V_{SS} 5
Q_1 6
Q_2 7
Q_3 8
Q_4 9
Q_5 10
Q_6 11
Q_7 12
Q_8 13
Q_9 14
28 V_{DD}
27 $V_{REF\ MAX}$
26 $V_{REF\ MIN}$
25 V_C
24 Q_R
23 Q_{18}
22 Q_{17}
21 Q_{16}
20 Q_{15}
19 Q_{14}
18 Q_{13}
17 Q_{12}
16 Q_{11}
15 Q_{10}
TOP VIEW
CD12080S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{OSC}	Oscillator pin
4	I_1	Mode select input
5	V_{SS}	Ground (0V)
6	Q_1	Segment outputs
7	Q_2	
8	Q_3	
9	Q_4	
10	Q_5	
11	Q_6	
12	Q_7	
13	Q_8	
14	Q_9	
15	Q_{10}	
16	Q_{11}	
17	Q_{12}	
18	Q_{13}	
19	Q_{14}	
20	Q_{15}	
21	Q_{16}	
22	Q_{17}	
23	Q_{18}	
24	Q_R	Backplane output
25	V_C	Control voltage
26	$V_{REF\ MIN}$	Reference voltage inputs
27	$V_{REF\ MAX}$	
28	V_{DD}	Positive supply voltage

NOTE:
1. Pins 2 and 3 should be connected to V_{SS}.

18-Element Bar Graph LCD Driver PCF1303T

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	−0.5 to +15	V
V_I	Voltage on any input	−0.5 to V_{DD} +0.5	V
$\pm I_I$	DC current into any input or output	Max. 10	mA
T_{STG}	Storage temperature range	−25 to +125	°C
T_A	Operating ambient temperature range	−40 to +85	°C

DC ELECTRICAL CHARACTERISTICS $V_{SS} = 0V$.

SYMBOL	PARAMETER	V_{DD} V	T_A (°C)							UNIT
			−40		+25			+85		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent device current[1]	10.0		1200			1200		1200	µA
I_{DD}	Operating supply current	8.2		2.0			2.0		2.0	mA
$\pm I_I$	Input leakage current[2]	6.0		300			300		1000	nA
		8.2		300			300		1000	nA
		10.0		300			300		1000	nA
V_{IH}	HIGH level input voltage select input I_1	6.0	4.2		4.2			4.2		V
		8.2	5.8		5.8			5.8		V
		10.0	7.0		7.0			7.0		V
V_{IL}	LOW level input voltage select input I_1	6.0		1.8			1.8		1.8	V
		8.2		2.4	2.4		2.4			V
		10.0		3.0			3.0		3.0	V
V_{OH}	HIGH level output voltage[3]	6.0	5.95		5.95			5.95		V
		8.2	8.15		8.15			8.15		V
		10.0	9.95		9.95			9.95		V
V_{OL}	LOW level output voltage[3]	6.0		0.05			0.05		0.05	V
		8.2		0.05			0.05		0.05	V
		10.0		0.05			0.05		0.05	V
$-I_{OH}$	Output current HIGH[4]	6.0	0.6		0.5			0.35		mA
		8.2	0.85		0.7			0.45		mA
		10.0	1.0		0.85			0.6		mA
I_{OL}	Output current LOW[5]	6.0	0.65		0.5			0.4		mA
		8.2	1.0		0.8			0.6		mA
		10.0	1.3		1.0			0.8		mA
V_{IC}	Input voltage control input V_C	6.0	0.0	6.0	0.0		6.0	0.0	6.0	V
		8.2	0.0	8.2	0.0		8.2	0.0	8.2	V
		10.0	0.0	10.0	0.0		10.0	0.0	10.0	V
$V_{IR\ MAX}$	Input voltage $V_{REF\ MAX}$ input	6.0	3.6	5.5	3.6		5.5	3.6	5.5	V
		8.2	3.6	7.7	3.6		7.7	3.6	7.7	V
		10.0	3.6	9.5	3.6		9.5	3.6	9.5	V
$V_{IR\ MIN}$	Input voltage $V_{REF\ MIN}$ input	6.0	0.5	1.0	0.5		1.0	0.5	1.0	V
		8.2	0.5	4.5	0.5		4.5	0.5	4.5	V
		10.0	0.5	6.0	0.5		6.0	0.5	6.0	V
ΔV_I	$V_{REF\ MAX} - V_{REF\ MIN}$	6.0	3.0		3.0			3.0		V
		8.2	3.0		3.0			3.0		V
		10.0	3.0		3.0			3.0		V
$\pm V_{BP}$	DC component bar output to backplane output[6]	8.2		25		10	25		25	mV

18-Element Bar Graph LCD Driver PCF1303T

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{SS} = 0V$.

SYMBOL	PARAMETER	V_{DD} V	T_A (°C)							UNIT
			−40		+25			+85		
			Min	Max	Min	Typ	Max	Min	Max	
f_{BP}	Backplane frequency[7]	8.2	90	110		100		90	110	Hz
$\pm V_{IO}$	Input offset voltage[8]	8.2		120			120		120	mV
$\pm \Delta V_{STEP}$	Step voltage variable[9]	8.2		50			50		50	mV
SR	Input voltage slew rate V_C input[10]	6.0 8.2 10.0		50 50 50			50 50 50		50 50 50	V/s V/s V/s

NOTES:

1. $V_{REF\ MIN} = 0.5V$, $V_{REF\ MAX} = 9.5V$, $V_C = V_{OSC} = 0V$, I_1 at V_{SS} or V_{DD}.
2. Pin under test at V_{SS} or V_{DD}. All other inputs simultaneously at V_{SS} or V_{DD}.
3. $I_O = 0$, all inputs at V_{SS} or V_{DD}.
4. $V_{OH} = V_{DD} - 0.5V$, all inputs at V_{SS} or V_{DD}.
5. $V_{OL} = 0.4V$, all inputs at V_{SS} or V_{DD}.
6. $f_{BP} = 100Hz$, load segment outputs to backplane output.
   $C_1 - C_{18} \leqslant 0.01\mu F$, $C_{BP} = C_1 + C_2 + \ldots C_{18} \leqslant 0.05\mu F$, $R_1 - R_{18} \geqslant 2M\Omega$.
7. $R_{OSC} = 0.1M\Omega$, $C_{OSC} = 390pF$.
8. Number of segments 2 or 18.
   For n = 2:

$$V_{IO} = V_C - V_{REF\ MIN} - \frac{(V_{REF\ MAX}) - (V_{REF\ MIN})}{18} \pm V_H$$

   For n = 18:

$$V_{IO} = V_C - V_{REF\ MAX} + \frac{(V_{REF\ MAX}) - (V_{REF\ MIN})}{18} \pm V_H$$

9. See Equation 1.
10. Condition applies with clock oscillator such that $f_{BP} = 100Hz$.

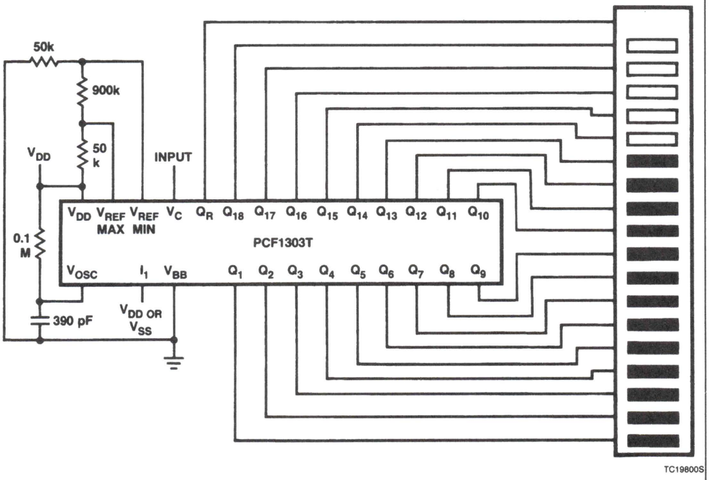

50k
900k
50 k
V_{DD}
INPUT
0.1 M
390 pF
V_{DD} V_{REF} MAX V_{REF} MIN V_C Q_R Q_{18} Q_{17} Q_{16} Q_{15} Q_{14} Q_{13} Q_{12} Q_{11} Q_{10}
PCF1303T
V_{OSC} I_1 V_{BB} Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
V_{DD} OR V_{SS}
TC19800S

Figure 1. Typical Application

18-Element Bar Graph LCD Driver PCF1303T

FUNCTION TABLE

I_1	MODE
L	Pointer
H	Thermometer

NOTES:
H = HIGH voltage level
L = LOW voltage level

FUNCTIONAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to the control voltage when in pointer or thermometer mode.

The first segment will energize when the control voltage is less than the trigger voltage ($V_{T(bar)2}$) (see Equation 3).

The circuit has analog and digital sections.

The analog section consists of a comparator with the inverting input coupled to the input control voltage. The non-inverting input of the comparator is connected via 17 analog switches to the nodes of an 18-element resistor divider. The extremities of the resistor divider are coupled via high input impedance amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The control input functions with Schmitt trigger action.

The digital section has one reference output (Q_R) to drive the backplane and 18 outputs (Q_1 to Q_{18}) to drive the segments.

The segment outputs incorporate two latches and some gates.

The circuit is driven by an on-chip oscillator with external resistors and capacitors. The outputs are driven at typically 100Hz.[1]

LINEARITY

$$V_{STEP} = V_{STEP}' \pm \Delta V_{STEP} \qquad (1)$$

$V_{STEP'}$ is the voltage drop (internal) across the resistor-ladder network, ΔV_{STEP} is the differential on V_{STEP}.

$$V_{STEP'} = \frac{(V_{REF\ MAX} \pm \Delta V_{2'} - (V_{REF\ MIN} \pm \Delta V_2)}{18} \qquad (2)$$

ΔV_2 and $\Delta V_{2'}$ are the maximum offset voltage spread of the on-chip voltage followers.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_C pin is $V_{T(bar)n}$:

$$V_{T(bar)n} = (V_{REF\ MIN} \pm \Delta V_2{}^1) + \{(n - 1)V_{STEP'} \pm \Delta V_R\} \pm \Delta V_1 \pm V_H \qquad (3)$$

n = number of segments; $2 \leqslant n \leqslant 18$.

ΔV_R is the voltage deviation at step n of the resistor-ladder network (for $n = 2$ or 18, $\Delta V_R = \Delta V_{STEP}$).

ΔV_1 is the offset voltage for the on-chip comparator.

V_H is the hysteresis voltage: $30\%\ V_{STEP} \geqslant V_H \geqslant 10\%\ V_{STEP}$.

NOTE:
1. The same sign (+ or −) should be used in Equation 2.

Signetics

PCF2100
LCD Duplex Driver

Product Specification

Linear Products

DESCRIPTION

The PCF2100 is a single-chip, silicon-gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 40 segments in a duplex manner, especially for low-voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

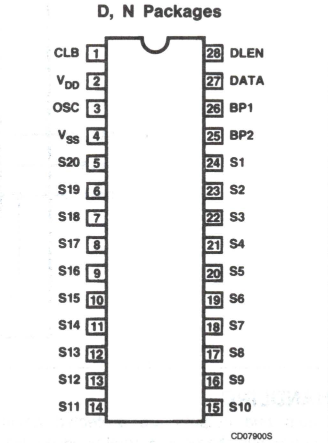
FEATURES

- **40 LCD segment drive capability**
- **Supply voltage 2.25 to 6.5V**
- **Low current consumption**
- **Serial data input**
- **CBUS control**
- **One-point built-in oscillator**
- **Expansion possibility**

APPLICATIONS

- **LCD displays**
- **Gauges**
- **Level/volume indicators**
- **Thermometers**

PIN CONFIGURATION


D, N Packages
CLB 1
VDD 2
OSC 3
VSS 4
S20 5
S19 6
S18 7
S17 8
S16 9
S15 10
S14 11
S13 12
S12 13
S11 14
28 DLEN
27 DATA
26 BP1
25 BP2
24 S1
23 S2
22 S3
21 S4
20 S5
19 S6
18 S7
17 S8
16 S9
15 S10
CD07900S

PIN NO.	SYMBOL	DESCRIPTION	
Supply			
2	V_{DD}	Positive supply	
4	V_{SS}	Negative supply	
Inputs			
3	OSC	Oscillator input	
27	DATA	Data line	CBUS
28	DLEN	Data line enable	
1	CLB	Clock burst	
Outputs			
26	BP1	Backplane drivers	
25	BP2	(common of LCD)	
S1 to S20		LCD driver outputs	

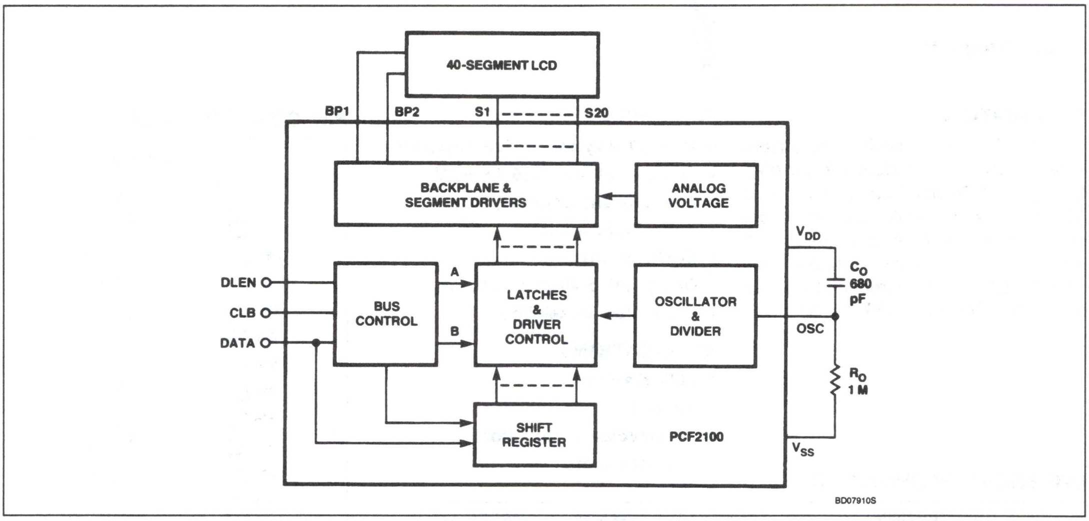
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	−40°C to +85°C	PCF2100PN
28-Pin Plastic SO package (SO-28; SOT-136A)	−40°C to +85°C	PCF2100TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage with respect to V_{SS}	−0.3 to 8	V
V_N	Voltage on any pin	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM


40-SEGMENT LCD
BP1
BP2
S1
S20
BACKPLANE & SEGMENT DRIVERS
ANALOG VOLTAGE
V_{DD}
C_O 680 pF
DLEN
CLB
DATA
BUS CONTROL
A
B
LATCHES & DRIVER CONTROL
OSCILLATOR & DIVIDER
OSC
R_O 1 M
SHIFT REGISTER
PCF2100
V_{SS}
BD07910S

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.25 to 6.5 V; V_{SS} = 0 V; T_A = −40 to +85°C; R_O = 1MΩ; C_O = 680pF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{DD}	Supply current	No external load		10	50	μA
I_{DD}	Supply current	No external load; T_A = −25 to +85°C			30	μA
f_{LCD}	Display frequency	See Figure 7; T = 680μs	60	80	100	Hz
V_{BP}	DC component of LCD drive	With respect to V_{SX}		±10		mV
	Load on each segment driver				10 500	MΩ pF
	Load on each backplane driver				1 5	MΩ nF
V_{IH}	Input voltage HIGH	See Figure 8	2			V
V_{IL}	Input voltage LOW	See Figure 8			0.6	V
t_R	Rise time V_{BP} to V_{SX}	Maximum load		20		μs
Inputs CLB, DATA, DLEN[1]						
t_R, t_F	Rise and fall times	See Figure 1			10	μs
t_{WH}	CLB pulse width HIGH	See Figure 1	1			μs
t_{WL}	CLB pulse width LOW	See Figure 1	9			μs
t_{SUDA}	Data setup time DATA → CLB	See Figure 1	8			μs
t_{HDDA}	Data hold time DATA → CLB	See Figure 1	8			μs
t_{SUEN}	Enable setup time DLEN → CLB	See Figure 1	1			μs
t_{SUDI}	Disable setup time CLB → DLEN	See Figure 1	8			μs
t_{SULD}	Setup time (load pulse) DLEN → CLB	See Figure 1	8			μs
t_{BUSY}	Busy-time from load pulse to next start of transmission	See Figure 1	8			μs
t_{SULZ}	Setup time (leading zero) DATA → CLB	See Figure 1	8			μs

NOTE:

1. All timing values are referred to V_{IHmin} and V_{ILmax} (see Figure 1). If external resistors are used in the bus lines (see Figure 8), the extra time constant has to be added.

LCD Duplex Driver PCF2100

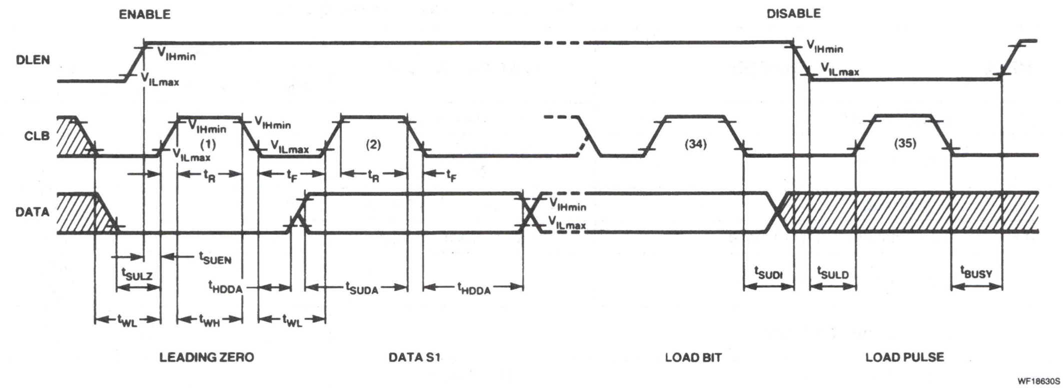
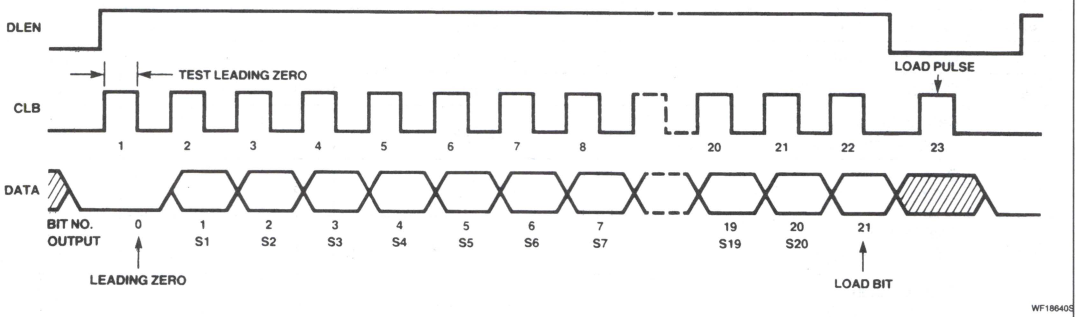

ENABLE
DISABLE
DLEN
CLB
DATA
V_{IHmin}
V_{ILmax}
(1)
(2)
(34)
(35)
tR
tF
tSULZ
tSUEN
tHDDA
tSUDA
tSUDI
tSULD
tBUSY
tWL
tWH
LEADING ZERO
DATA S1
LOAD BIT
LOAD PULSE
WF18630S

Figure 1. CBUS Timing


DLEN
TEST LEADING ZERO
LOAD PULSE
CLB
1 2 3 4 5 6 7 8 20 21 22 23
DATA
BIT NO. 0 1 2 3 4 5 6 7 19 20 21
OUTPUT S1 S2 S3 S4 S5 S6 S7 S19 S20
LEADING ZERO
LOAD BIT
WF18640S

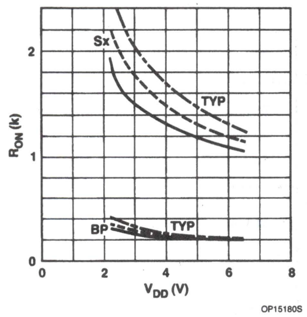
NOTES:
An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded.
When DATA-bit 21 is LOW, the B-latches (BP2) are loaded.
CLB-pulse 23 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

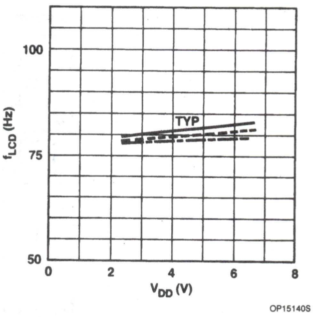
If one of the test conditions is not fulfilled, no action follows the load conditions (load pulse width DLEN is LOW) and the driver is ready to receive new data.

Figure 2. CBUS Data Format



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-·- $T_A = +85°C$

Figure 3. Output Resistance of Backplane and Segments



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-·- $T_A = +85°C$

Figure 4. Display Frequency as a Function of Supply Voltage; $R_OC_O = 680\mu s$

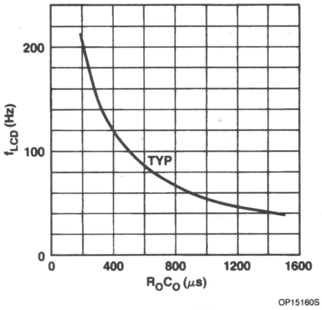
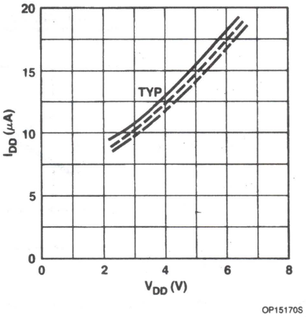


Figure 5. Display Frequency as a Function of $R_O \times C_O$ Time; $T_A = 25°C$



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-·- $T_A = +85°C$

Figure 6. Supply Current as a Function of Supply Voltage

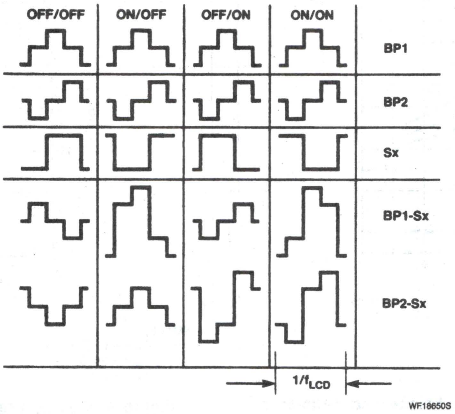
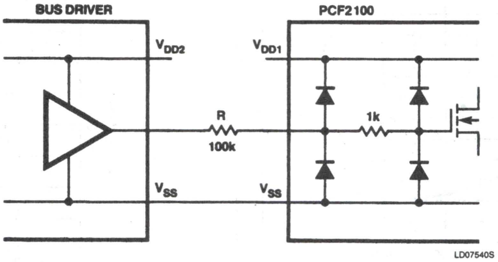

OFF/OFF
ON/OFF
OFF/ON
ON/ON
BP1
BP2
Sx
BP1-Sx
BP2-Sx
$1/f_{LCD}$
WF18650S

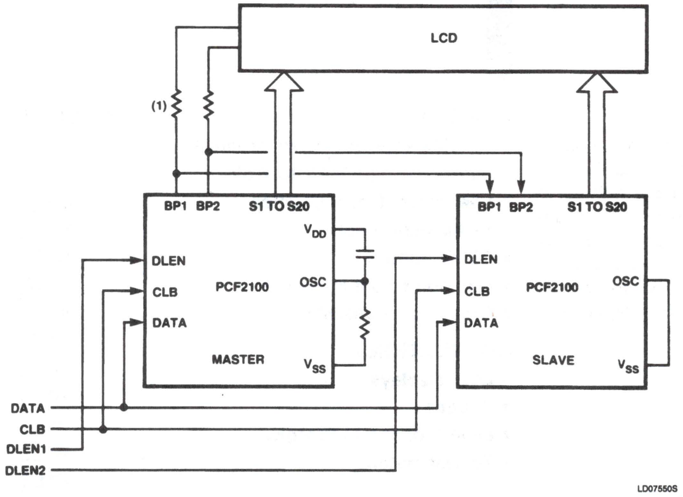
Figure 7. Timing Diagram


BUS DRIVER
PCF2100
V_{DD2}
V_{DD1}
R
100k
1k
V_{SS}
V_{SS}
LD07540S

NOTES:

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5V$, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current ≤ 40 μA.

Figure 8. Input Circuitry


LCD
(1)
BP1 BP2 S1 TO S20
VDD
DLEN
CLB
DATA
PCF2100
OSC
MASTER
VSS
BP1 BP2 S1 TO S20
DLEN
CLB
DATA
PCF2100
OSC
SLAVE
VSS
DATA
CLB
DLEN1
DLEN2
LD07550S

NOTES:

1. In the slave mode, the serial resistors between BP1 and BP2 of the PCF2100 and the backplane of the LCD must be > 2.7kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.
   By connecting the OSC to V_{SS}, the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, and PCF2100 ICs up to the BP drive capability of the master.

PCF2111 is a 64 LCD-segment driver.

Figure 9. Diagram Showing Expansion Possibility

Signetics

PCF2111
LCD Duplex Driver

Product Specification

Linear Products

DESCRIPTION

The PCF2111 is a single-chip, silicon-gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; especially for low-voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

FEATURES

- **64 LCD segment drive capability**
- **Supply voltage 2.25 to 6.5V**
- **Low current consumption**
- **Serial data input**
- **CBUS control**
- **One-point built-in oscillator**
- **Expansion possibility**

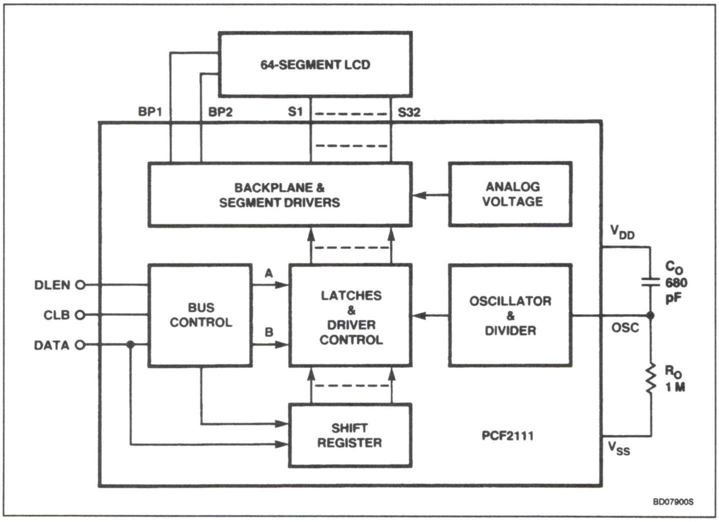
APPLICATIONS

- **LCD displays**
- **Gauges**
- **Level/volume indicators**
- **Thermometers**

ORDERING INFORMATION

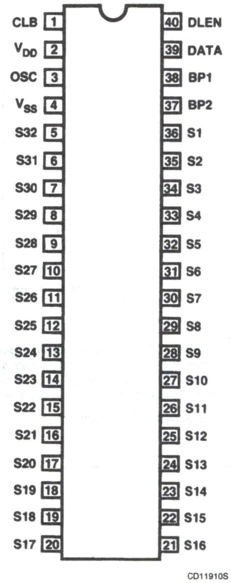
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
40-Pin Plastic DIP (SOT-129)	−40°C to +85°C	PCF2111PN
40-Pin Plastic SO (VSO-40; SOT-158A)	−40°C to +85°C	PCF2111TD

BLOCK DIAGRAM


64-SEGMENT LCD
BP1
BP2
S1
S32
BACKPLANE & SEGMENT DRIVERS
ANALOG VOLTAGE
V_DD
C_O 680 pF
DLEN
CLB
DATA
BUS CONTROL
A
B
LATCHES & DRIVER CONTROL
OSCILLATOR & DIVIDER
OSC
R_O 1 M
SHIFT REGISTER
PCF2111
V_SS
BD07900S

PIN CONFIGURATION

N, D Packages


CLB 1
V_DD 2
OSC 3
V_SS 4
S32 5
S31 6
S30 7
S29 8
S28 9
S27 10
S26 11
S25 12
S24 13
S23 14
S22 15
S21 16
S20 17
S19 18
S18 19
S17 20
40 DLEN
39 DATA
38 BP1
37 BP2
36 S1
35 S2
34 S3
33 S4
32 S5
31 S6
30 S7
29 S8
28 S9
27 S10
26 S11
25 S12
24 S13
23 S14
22 S15
21 S16
CD11910S

PIN NO.	SYMBOL	DESCRIPTION	
Supply			
2	V_{DD}	Positive supply	
4	V_{SS}	Negative supply	
Inputs			
3	OSC	Oscillator input	
1	CLB	Clock burst	CBUS
39	DATA	Data line	
40	DLEN	Data line enable	
Outputs			
5 to 36	S1 to S32	LCD driver outputs	
38	BP1	Backplane drivers (common of LCD)	
37	BP2		

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage with respect to V_{SS}	-0.3 to 8	V
V_n	Voltage on any pin	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.25 to 6.5V; V_{SS} = 0V; T_A = −40°C to +85°C; R_O = 1MΩ; C_O = 680 pF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{DD}	Supply current	No external load		10	50	μA
I_{DD}	Supply current	No external load; T_A = −25 to +85°C			30	μA
f_{LCD}	Display frequency	See Figure 7; T = 680μs	60	80	100	Hz
V_{BP}	DC component of LCD drive	With respect to V_{SX}		±10		mV
	Load on each segment driver				10 500	MΩ pF
	Load on each backplane driver				1 5	MΩ nF
V_{IH}	Input voltage HIGH	See Figure 8	2			V
V_{IL}	Input voltage LOW				0.6	V
t_R	Rise time V_{BP} to V_{SX}	Maximum load		20		μs
Inputs CLB, DATA, DLEN[1]						
C_{IN} C_{IN}	Input capacitance	For SOT-129 package For SOT-158A package			10 5	pF pF
t_R, t_F	Rise and fall times	See Figure 1			10	μs
t_{WH}	CLB pulse width HIGH	See Figure 1	1			μs
t_{WL}	CLB pulse width LOW	See Figure 1	9			μs
t_{SUDA}	Data setup time DATA → CLB	See Figure 1	8			μs
t_{HDDA}	Data hold time DATA → CLB	See Figure 1	8			μs
t_{SUEN}	Enable setup time DLEN → CLB	See Figure 1	1			μs
t_{SUDI}	Disable setup time CLB → DLEN	See Figure 1	8			μs
t_{SULD}	Setup time (load pulse) DLEN → CLB	See Figure 1	8			μs
t_{BUSY}	Busy-time from load pulse to next start of transmission	See Figure 1	8			μs
t_{SULZ}	Setup time (leading zero) DATA → CLB	See Figure 1	8			μs

NOTE:

1. All timing values are referred to V_{IHmin} and V_{ILmin} (see Figure 1). If external resistors are used in the bus lines (see Figure 8), the extra time constant has to be added.

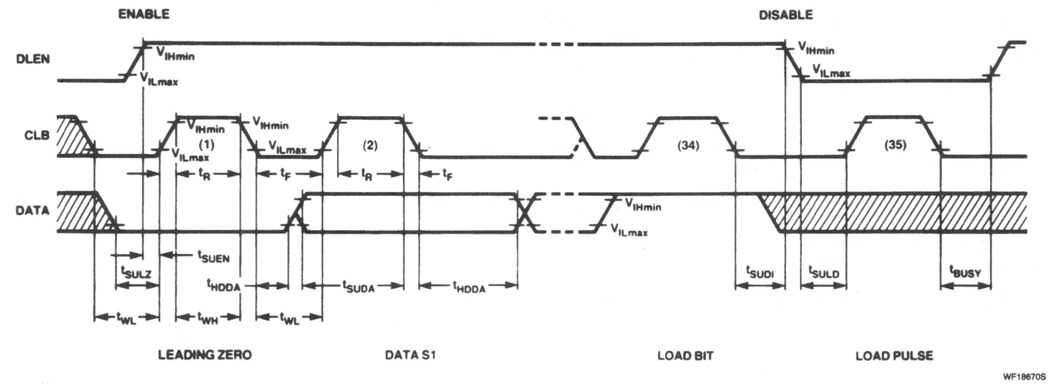
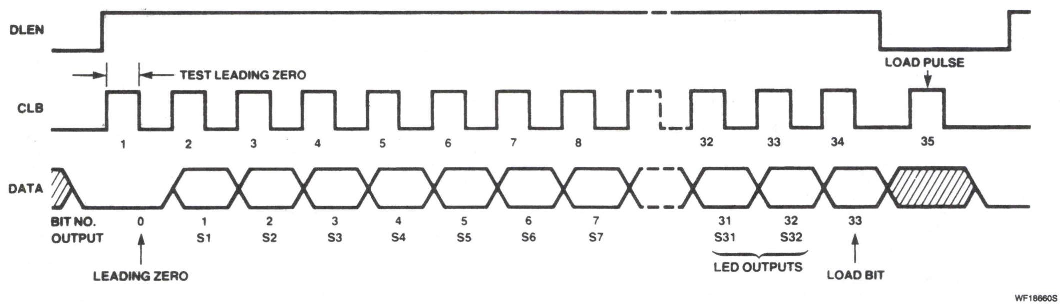

ENABLE
DISABLE
DLEN
CLB
DATA
V_IHmin
V_ILmax
(1)
(2)
(34)
(35)
t_R
t_F
t_SUEN
t_SULZ
t_HDDA
t_SUDA
t_WL
t_WH
t_SUDI
t_SULD
t_BUSY
LEADING ZERO
DATA S1
LOAD BIT
LOAD PULSE
WF18670S

Figure 1. CBUS Timing


DLEN
TEST LEADING ZERO
LOAD PULSE
CLB
1
2
3
4
5
6
7
8
32
33
34
35
DATA
BIT NO.
OUTPUT
0
1
2
3
4
5
6
7
31
32
33
S1
S2
S3
S4
S5
S6
S7
S31
S32
LEADING ZERO
LED OUTPUTS
LOAD BIT
WF18660S

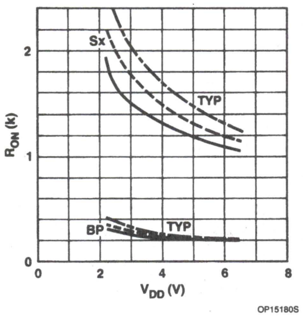
NOTES:

An LCD segment is activated when the corresponding DATA bit is HIGH.
When DATA bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:
a. Test on leading zero.
b. Test on number of DATA bits.
c. Test of disturbed DLEN and DATA signals during transmission.

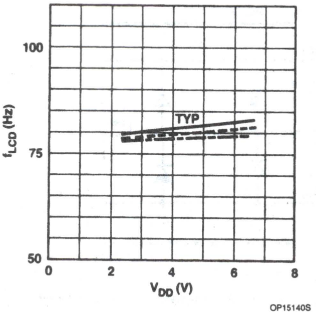
If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

Figure 2. CBUS Data Format



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-·- $T_A = +85°C$

Figure 3. Output Resistance of Backplane and Segments



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-·- $T_A = +85°C$

Figure 4. Display Frequency as a Function of Supply Voltage $R_OC_O = 680\mu s$

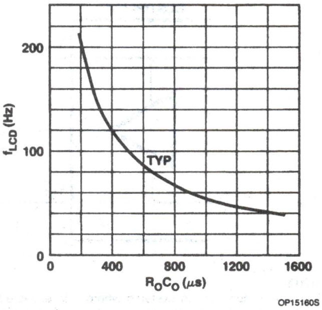
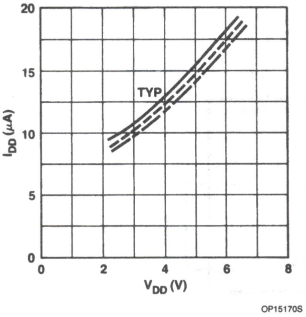


Figure 5. Display Frequency as a Function of $R_O \times C_O$ Time $T_A = 25°C$



NOTES:
—— $T_A = -40°C$
- - - $T_A = +25°C$
-·-·- $T_A = +85°C$

Figure 6. Supply Current as a Function of Supply Voltage

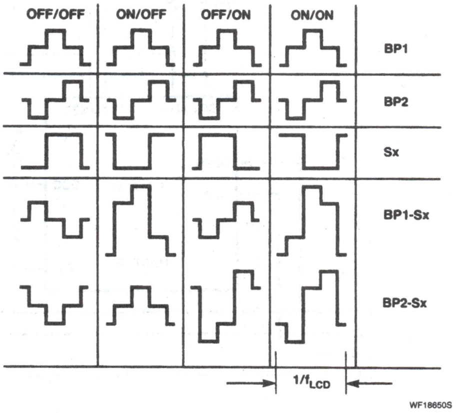
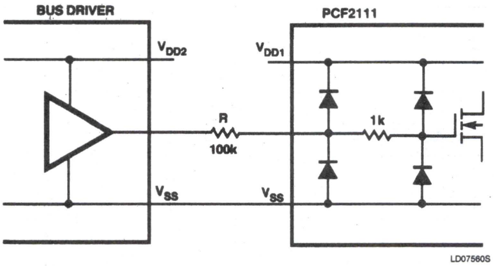
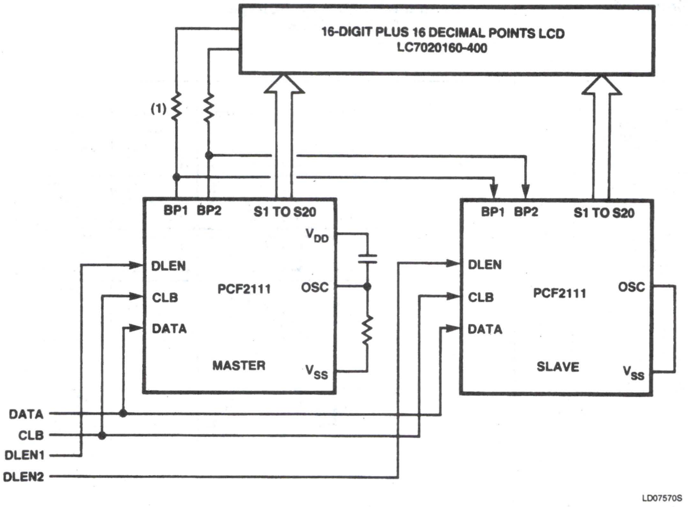

OFF/OFF
ON/OFF
OFF/ON
ON/ON
BP1
BP2
Sx
BP1-Sx
BP2-Sx
$1/f_{LCD}$
WF18650S

Figure 7. Timing Diagram


BUS DRIVER
PCF2111
V_{DD2}
V_{DD1}
R
100k
1k
V_{SS}
V_{SS}
LD07560S

NOTE:
V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5V$, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current ≤ 40μA.

Figure 8. Input Circuitry


16-DIGIT PLUS 16 DECIMAL POINTS LCD
LC7020160-400
(1)
BP1 BP2 S1 TO S20
V_{DD}
DLEN
CLB
DATA
PCF2111
OSC
MASTER
V_{SS}
BP1 BP2 S1 TO S20
DLEN
CLB
DATA
PCF2111
OSC
SLAVE
V_{SS}
DATA
CLB
DLEN1
DLEN2
LD07570S

NOTES:

1. In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be > 2.7 kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

By connecting OSC to V_{SS} the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110, and PCF2100 ICs up to the BP drive capability of the master.

PCF2100 is a 40 LCD segment driver.
PCF2110 is a 60 LCD segment driver plus 2 LED driver outputs.

Figure 9. Diagram Showing Expansion Possibility for a 16-digit Plus 16 Decimal Points LCD

Signetics

PCF2112
LCD Driver

Product Specification

Linear Products

DESCRIPTION

The PCF2112 is a single-chip, silicon-gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 32 segments in direct drive; especially for low-voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

FEATURES

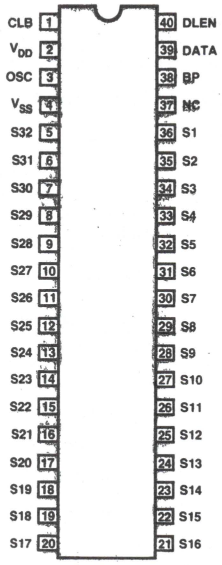
- **32 LCD segment drive capability**
- **Supply voltage 2.25 to 6.5V**
- **Low current consumption**
- **Serial data input**
- **CBUS control**
- **One-point built-in oscillator**
- **Expansion possibility**

APPLICATIONS

- **LCD displays**
- **Gauges**
- **Level/Volume indicators**
- **Thermometers**

PIN CONFIGURATION

D, N Packages



CLB 1
V_DD 2
OSC 3
V_SS 4
S32 5
S31 6
S30 7
S29 8
S28 9
S27 10
S26 11
S25 12
S24 13
S23 14
S22 15
S21 16
S20 17
S19 18
S18 19
S17 20
40 DLEN
39 DATA
38 BP
37 NC
36 S1
35 S2
34 S3
33 S4
32 S5
31 S6
30 S7
29 S8
28 S9
27 S10
26 S11
25 S12
24 S13
23 S14
22 S15
21 S16

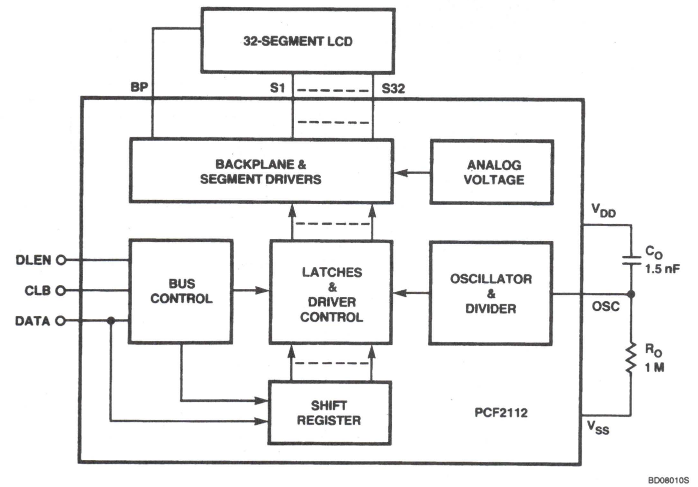
CD11920S

PIN NO.	SYMBOL	DESCRIPTION	
Supply			
2	V_{DD}	Positive supply	
4	V_{SS}	Negative supply	
Inputs			
3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	
1	CLB	Clock burst	
Outputs			
38	BP	Backplane driver (common of LCD)	
5-36	S1 to S32	LCD driver outputs	
37	NC	Not connected	

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
40-Pin Plastic DIP (SOT-129)	−40°C to +85°C	PCF2112PN
40-Pin Plastic SO (VSO-40; SOT-158A)	−40°C to +85°C	PCF2112TD

BLOCK DIAGRAM



32-SEGMENT LCD
BP
S1
S32
BACKPLANE & SEGMENT DRIVERS
ANALOG VOLTAGE
V_DD
C_O 1.5 nF
DLEN
CLB
DATA
BUS CONTROL
LATCHES & DRIVER CONTROL
OSCILLATOR & DIVIDER
OSC
R_O 1 M
SHIFT REGISTER
PCF2112
V_SS

BD08010S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage with respect to V_{SS}	−0.3 to 8	V
V_n	Voltage on any pin	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.25 to 6.5V; V_{SS} = 0V; T_A = −40°C to +85°C; R_O = 1MΩ; C_O = 1.5nF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{DD}	Supply current	No external load		10	50	µA
I_{DD}	Supply current	No external load; T_A = −25°C to +85°C			30	µA
f_{LCD}	Display frequency	T = 1.5ms	30	40	50	Hz
R_S	Output resistance of each segment	I_O = µA			10	kΩ
R_{BP}	Output resistance of backplane				2	kΩ
V_{IH}	Input voltage HIGH	see Figure 7	2			V
V_{IL}	Input voltage LOW				0.6	V
Inputs CLB, DATA, DLEN[1]						
C_{IN} C_{IN}	Input capacitance	For SOT-129 package For SOT-158A package			10 5	pF pF
t_R, t_F	Rise and fall times	see Figure 1			10	µs
t_{WH}	CLB pulse width HIGH	see Figure 1	1			µs
t_{WL}	CLB pulse width LOW	see Figure 1	9			µs
t_{SUDA}	Data setup time DATA → CLB	see Figure 1	8			µs
t_{HDDA}	Data hold time DATA → CLB	see Figure 1	8			µs
t_{SUEN}	Enable setup time DLEN → CLB	see Figure 1	1			µs
t_{SUDI}	Disable setup time CLB → DLEN	see Figure 1	8			µs
t_{SULD}	Setup time (load pulse) DLEN → CLB	see Figure 1	8			µs
t_{BUSY}	Busy-time from load pulse to next start of transmission	see Figure 1	8			µs
t_{SULZ}	Setup time (leading zero) DATA → CLB	see Figure 1	8			µs

NOTE:

1. All timing values are referred to V_{IHmin} and V_{ILmax} (see Figure 1). If external resistors are used in the ← bus lines (see Figure 7), an extra time constant has to be added.

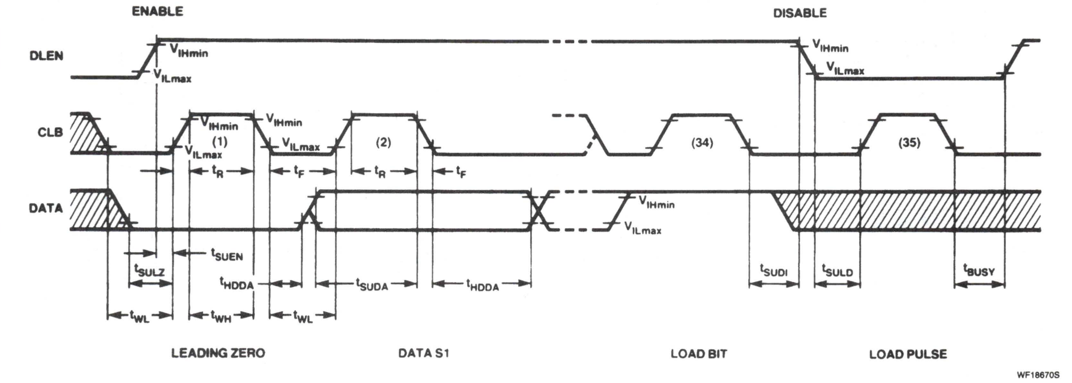
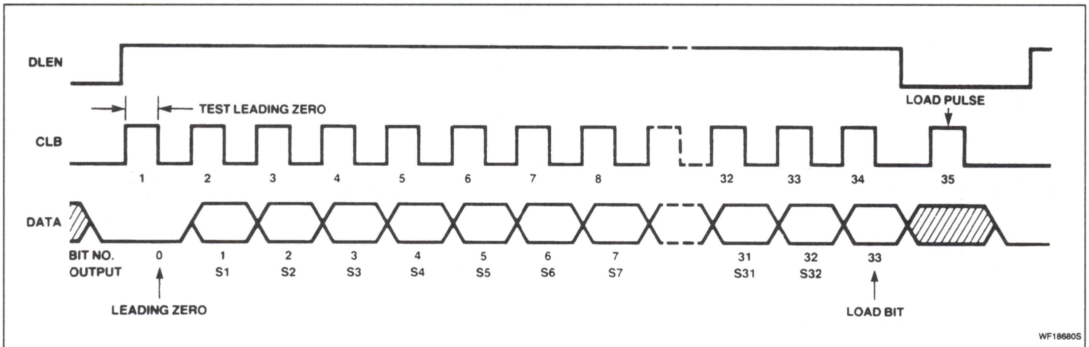

ENABLE
DISABLE
DLEN
CLB
DATA
V_{IHmin}
V_{ILmax}
(1)
(2)
(34)
(35)
t_R
t_F
t_{SULZ}
t_{SUEN}
t_{HDDA}
t_{SUDA}
t_{SUDI}
t_{SULD}
t_{BUSY}
t_{WL}
t_{WH}
LEADING ZERO
DATA S1
LOAD BIT
LOAD PULSE
WF18670S

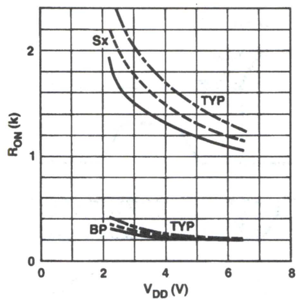
Figure 1. CBUS Timing


DLEN
TEST LEADING ZERO
LOAD PULSE
CLB
1
2
3
4
5
6
7
8
32
33
34
35
DATA
BIT NO.
OUTPUT
0
1
2
3
4
5
6
7
31
32
33
S1
S2
S3
S4
S5
S6
S7
S31
S32
LEADING ZERO
LOAD BIT
WF18680S

NOTES:

An LCD segment is activated when the corresponding DATA bit is HIGH.
When DATA bit 33 is HIGH, the latches are loaded. CLB pulse 35 transfers data from shift register to latches.
The following tests are carried out by the bus control logic:
a. Test on leading zero.
b. Test on number of DATA bits.
c. Test of disturbed DLEN and DATA signals during transmission.
If one of the tests conditions is not filled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

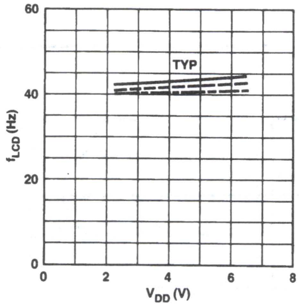
Figure 2. Data Format



OP15180S

NOTES:
——— $T_A = -40°C$
- - - $T_A = +25°C$
—·— $T_A = +85°C$

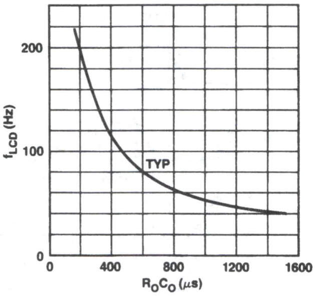
Figure 3. Output Resistance of Backplane and Segments



OP15190S

NOTES:
$R_OC_O = 1.5ms$
——— $T_A = -40°C$
- - - $T_A = +25°C$
—·— $T_A = +85°C$

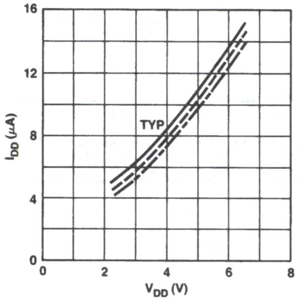
Figure 4. Display Frequency as a Function of Supply Voltage



OP15200S

NOTE:
$T_A = +25°C$

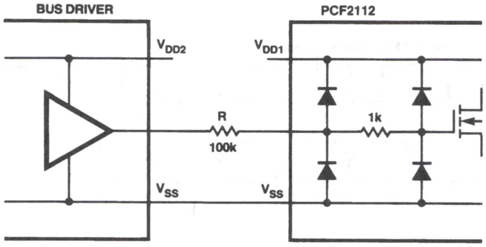
Figure 5. Display Frequency as a Function of $R_O \times C_O$ Time



OP15210S

NOTES:
——— $T_A = -40°C$
- - - $T_A = +25°C$
—·— $T_A = +85°C$

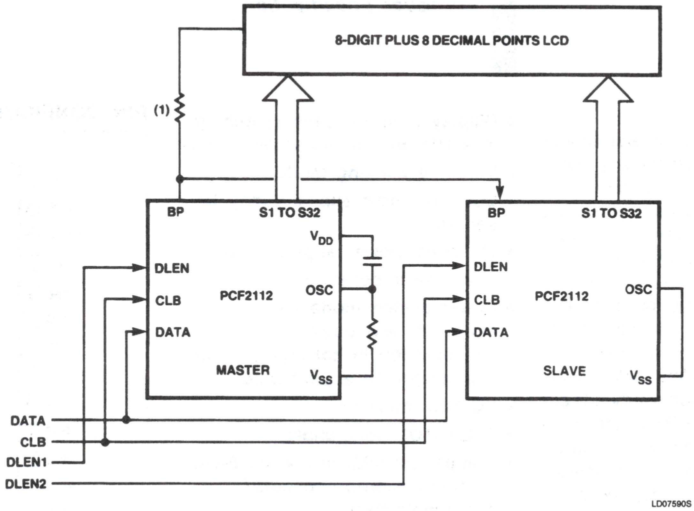
Figure 6. Supply Current as a Function of Supply Voltage



LD07580S

NOTE:
V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5V$, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\mu A$.

Figure 7. Input Circuitry


8-DIGIT PLUS 8 DECIMAL POINTS LCD
(1)
BP
S1 TO S32
V_DD
DLEN
CLB
PCF2112
OSC
DATA
MASTER
V_SS
BP
S1 TO S32
DLEN
CLB
PCF2112
OSC
DATA
SLAVE
V_SS
DATA
CLB
DLEN1
DLEN2
LD07590S

NOTES:

1. In the slave mode, the serial resistor between BP of the PCF2112 and the backplane of the LCD must be > 2.7kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.
   By connecting OSC to V_{SS} the BP pin becomes input and generates signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2112 ICs up to the BP drive capability of the master.

Figure 8. Diagram Showing Expansion Possibility for an 8-Digit Plus 8 Decimal Points LCD

PCF8566
Universal LCD Driver for Low Multiplex Rates

Product Specification

DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware sub-addressing, and by display memory switching (static and duplex drive modes).

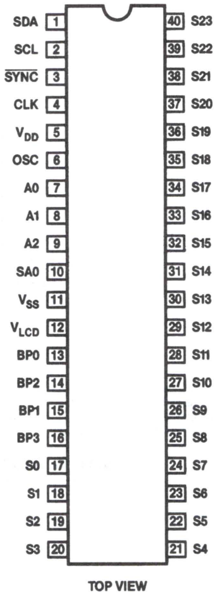
FEATURES

- **Single-chip LCD controller/driver**
- **Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing**
- **Selectable display bias configuration: static, ½, or ⅓**
- **Internal LCD bias generation with voltage-follower buffers**
- **24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements**
- **24 × 4-Bit RAM for display data storage**
- **Auto-incremented display data loading across device subaddress boundaries**
- **Display memory bank switching in static and duplex drive modes**
- **Versatile blinking modes**
- **LCD and logic supplies may be separated**
- **3V to 6V power supply range**
- **Low power consumption**
- **Power saving mode for extremely low power consumption in battery-operated and telephone applications**
- **I^2C bus interface**
- **TTL/CMOS compatible**
- **Compatible with any 4-bit, 8-bit, or 16-bit microprocessors/microcontrollers**
- **May be cascaded for large LCD applications (up to 1536 segments possible)**
- **Cascadable with the 40-segment LCD driver PFC8576**
- **Optimized pinning for single plane wiring in both single and multiple PCF8566 applications**
- **Space-saving 40-pin plastic SO**
- **No external components required (even in multiple device applications)**
- **Manufactured in silicon-gate CMOS process**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
40-Pin Plastic DIP (SOT-129)	−40°C to +85°C	PCF8566PN
40-Pin Plastic SO (VSO-40; SOT-158A)	−40°C to +85°C	PCF8566TD

PIN CONFIGURATION

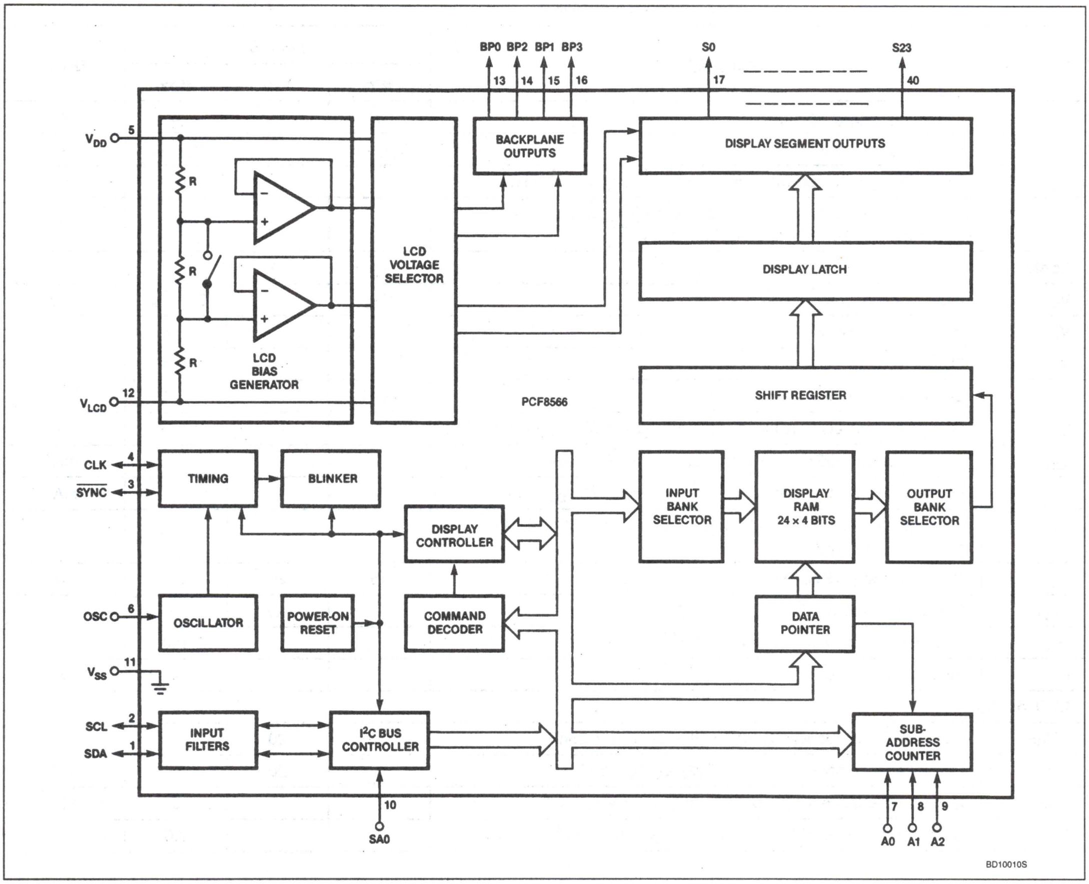


CD13730S

PIN NO.	SYMBOL	DESCRIPTION
1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{\text{SYNC}}$	Cascade synchronization input/output
4	CLK	External clock input/output
5	V_{DD}	Positive supply voltage
6	OSC	Oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address Bit 0 input
11	V_{SS}	Logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 40	S0 to S23	LCD segment outputs

Universal LCD Driver for Low Multiplex Rates PCF8566

BLOCK DIAGRAM


BP0 BP2 BP1 BP3
13 14 15 16
S0
17
S23
40
BACKPLANE OUTPUTS
DISPLAY SEGMENT OUTPUTS
V_{DD} 5
R
R
R
LCD VOLTAGE SELECTOR
DISPLAY LATCH
LCD BIAS GENERATOR
V_{LCD} 12
PCF8566
SHIFT REGISTER
CLK 4
$\overline{SYNC}$ 3
TIMING
BLINKER
DISPLAY CONTROLLER
INPUT BANK SELECTOR
DISPLAY RAM 24 x 4 BITS
OUTPUT BANK SELECTOR
OSC 6
OSCILLATOR
POWER-ON RESET
COMMAND DECODER
DATA POINTER
V_{SS} 11
SCL 2
SDA 1
INPUT FILTERS
I²C BUS CONTROLLER
SUB-ADDRESS COUNTER
10
SA0
7 8 9
A0 A1 A2
BD10010S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power voltage range; see note	−0.5 to +7	V
V_{LCD}	LCD supply voltage range	$V_{DD}-7$ to V_{DD}	V
V_I	Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
V_O	Output voltage range (S0 to S23; BP0 to BP3)	$V_{LCD}-0.5$ to $V_{DD}+0.5$	V
$\pm I_I$	DC input current	20	mA
$\pm I_O$	DC output current	25	mA
$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	V_{DD}, V_{SS}, or V_{LCD} current	50	mA
P_{TOT}	Power dissipation per package	400	mW
P_O	Power dissipation per output	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; V_{DD} = 3 to 6V; V_{LCD} = V_{DD} −3 to V_{DD} −6V; T_A = −40 to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Operating supply voltage	3		6	V
V_{LCD}	LCD supply voltage	$V_{DD}-6$		$V_{DD}-3$	V
I_{DD}	Operating supply current (normal mode) at f_{CLK} = 200kHz[1]			180	μA
I_{LP}	Power-saving mode supply current at V_{DD} = 3.5V; V_{LCD} = 0V; f_{CLK} = 35kHz; A0, A1, and A2 tied to V_{SS} [1]			60	μA
Logic					
V_{IL}	Input voltage LOW	V_{SS}		0.3 V_{DD}	V
V_{IH}	Input voltage HIGH	0.7 V_{DD}		V_{DD}	V
V_{OL}	Output voltage LOW at I_O = 0mA			0.05	V
V_{OH}	Output voltage HIGH at I_O = 0mA	$V_{DD}-0.05$			V
I_{OL1}	Output current LOW (CLK, $\overline{\text{SYNC}}$) at V_{OL} = 1.0V; V_{DD} = 5V	1			mA
I_{OH}	Output current HIGH (CLK) at V_{OH} = 4.0V; V_{DD} = 5V			−1	mA
I_{OL2}	Output current LOW (SDA; SCL) at V_{OL} = 0.4V; V_{DD} = 5V	3			mA
$\pm I_L$	Leakage current (SAO, CLK, OSC, A0, A1, A2, SCL, SDA) at V_I = V_{SS} or V_{DD}			1	μA
R_{SYNC}	Pull-up resistor ($\overline{\text{SYNC}}$)	15	25	60	kΩ
V_{REF}	Power-on reset level[2]		1.3	1.8	V
t_{SW}	Tolerable spike width on bus			100	ns
C_I	Input capacitance[3]			7	pF
LCD outputs					
$\pm V_{BP}$	DC voltage component (BP0 to BP3) at C_{BP} = 35nF		20		mV
$\pm V_S$	DC voltage component (S0 to S23) at C_S = 5nF		20		mV
R_{BP}	Output impedance (BP0 to BP3) at V_{LCD} = $V_{DD}-5V$[4]			5	kΩ
R_S	Output impedance (S0 to S23) at V_{LCD} = $V_{DD}-5V$[4]			7.0	kΩ

AC ELECTRICAL CHARACTERISTICS $V_{SS} = 0V$; $V_{DD} = 3$ to $6V$; $V_{LCD} = V_{DD} - 3$ to $V_{DD} - 6V$; $T_A = -40$ to $+85°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{CLK}	Oscillator frequency (normal mode)[6]	125	200	315	kHz
f_{CLKLP}	Oscillator frequency (power-saving mode) at $V_{DD} = 3.5V$	21	31	48	kHz
t_{CLKH}	CLK HIGH time	1			μs
t_{CLKL}	CLK LOW time	1			μs
t_{PSYNC}	$\overline{\text{SYNC}}$ propagation delay			400	ns
t_{SYNCL}	$\overline{\text{SYNC}}$ LOW time	1			μs
t_{PLCD}	Driver delays with test loads at $V_{LCD} = V_{DD} - 5V$			30	μs
I^2C bus					
t_{BUF}	Bus free time	4.7			μs
t_{HD}, t_{STA}	Start condition hold time	4			μs
t_{LOW}	SCL LOW time	4.7			μs
t_{HIGH}	SCL HIGH time	4			μs
t_{SU}, t_{STA}	Start condition setup time (repeated start code only)	4.7			μs
t_{HD}, t_{DAT}	Data hold time	0			μs
t_{SU}, t_{DAT}	Data setup time	250			ns
t_R	Rise time			1	μs
t_F	Fall time			300	ns
t_{SU}, t_{STO}	Stop condition setup time	4.7			μs

NOTES:

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125kHz$, I^2C bus maximum transmission speed is derated.

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Figure 1. The host microprocessor/microcontroller maintains the two-line I^{2}C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (Pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and to the LCD panel chosen for the application.

Power-On Reset

At power-on, the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1:4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^{2}C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^{2}C bus should be avoided for 1ms following power-on to allow completion of the reset action.

LCD Bias Generation

The full-scale LCD voltage (V_{OP}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature-compensated externally through the V_{LCD} supply to Pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The center resistor can be switched out of circuit to provide a ½ bias voltage level for the 1:2 multiplex configuration.

LCD Voltage Selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{OP} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{OP} is determined by equating $V_{OFF(RMS)}$ with a defined LCD threshold voltage (V_{TH}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode, a suitable choice is $V_{OP} \gtrsim 3V_{TH}$.

Multiplex drive ratios of 1:3 and 1:4 with ½ bias are possible, but the discrimination and, hence, the contrast ratios, are smaller ($\sqrt{3} = 1.732$ for 1:3 multiplex or $\sqrt{21}/3 = 1.528$ for 1:4 multiplex). The advantage of these modes is a reduction of the LCD full-scale voltage V_{OP} as follows:

1:3 multiplex (½ bias):
$V_{OP} = \sqrt{6}V_{OFF(RMS)} = 2.449V_{OFF(RMS)}$

1:4 multiplex (½ bias):
$V_{OP} = 4\sqrt{3}/3V_{OFF(RMS)} = 2.309V_{OFF(RMS)}$

These compare with $V_{OP} = 3V_{OFF(RMS)}$ when ⅓ bias is used.

Table 1. Selection of Display Configurations

ACTIVE BACKPLANE OUTPUTS	NO OF SEGMENTS	7-SEGMENT NUMERIC	14-SEGMENT ALPHANUMERIC	DOT MATRIX
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 × 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 × 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 × 24)
1	24	3 digits + 3 indicator symbols	1 character + 10 indicator symbols	24 dots

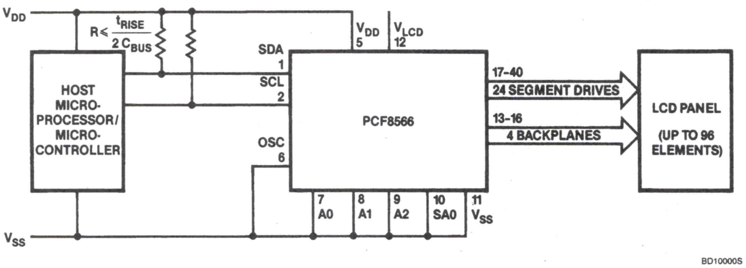


Figure 1. Typical System Configuration

Universal LCD Driver for Low Multiplex Rates PCF8566

Table 2. Preferred LCD Drive Modes: Summary of Characteristics

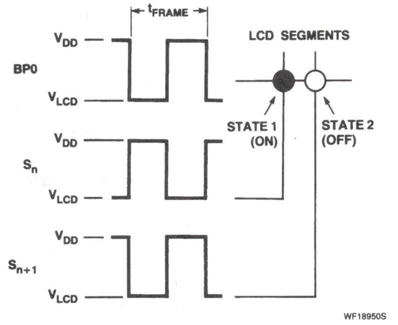
LCD DRIVE MODE	LCD BIAS CONFIGURATION	$\frac{V_{OFF(RMS)}}{V_{OP}}$	$\frac{V_{ON(RMS)}}{V_{OP}}$	$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}}$
static (1BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0.354$	$\sqrt{10}/4 = 0.791$	$\sqrt{5} = 2.236$
1 : 2 MUX (2BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{5}/3 = 0.745$	$\sqrt{5} = 2.236$
1 : 3 MUX (3BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{33}/9 = 0.638$	$\sqrt{33}/3 = 1.915$
1 : 4 MUX (4BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{3}/3 = 0.577$	$\sqrt{3} = 1.732$

LCD Drive Mode Waveforms

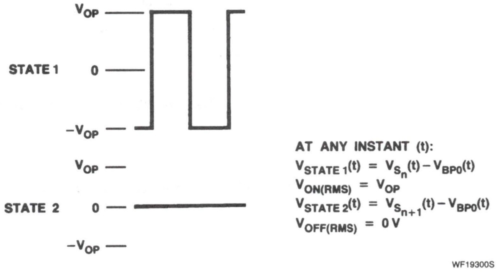
The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 2.

When two backplanes are provided in the LCD, the 1:2 multiplex drive mode applies. The PCF8566 allows use of ½ or ⅓ bias in this mode as shown in Figures 3 and 4.

The backplane and segment drive wavefront for the 1:3 multiplex drive mode (three LCD backplanes) and for the 1:4 multiplex drive mode (four LCD backplanes) are shown in Figures 5 and 6, respectively.



a. Waveforms at Driver



AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{ON(RMS)} = V_{OP}$

$V_{STATE\,2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

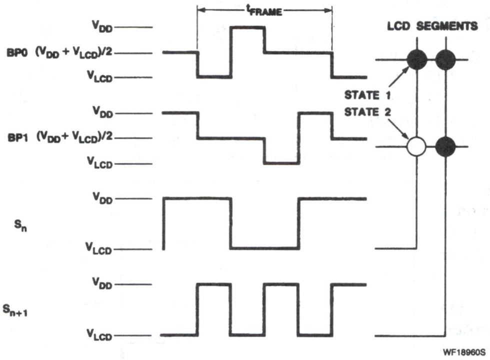
$V_{OFF(RMS)} = 0\,V$

b. Resultant Waveforms at LCD Segment

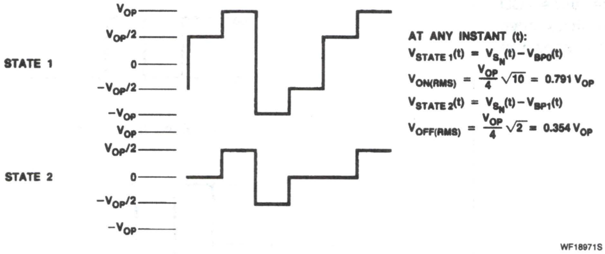
NOTE:
$V_{OP} = V_{DD} - V_{LCD}$.

Figure 2. Static Drive Mode Waveforms

LCD Drive Mode Waveforms (Continued)


t_{FRAME}
LCD SEGMENTS
V_{DD}
BP0 $(V_{DD} + V_{LCD})/2$
V_{LCD}
STATE 1
STATE 2
V_{DD}
BP1 $(V_{DD} + V_{LCD})/2$
V_{LCD}
V_{DD}
S_n
V_{LCD}
V_{DD}
S_{n+1}
V_{LCD}
WF18960S

a. Waveforms at Driver


STATE 1
V_{OP}
$V_{OP}/2$
0
$-V_{OP}/2$
$-V_{OP}$
STATE 2
V_{OP}
$V_{OP}/2$
0
$-V_{OP}/2$
$-V_{OP}$
WF18971S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_N}(t) - V_{BP0}(t)$

$V_{ON(RMS)} = \frac{V_{OP}}{4}\sqrt{10} = 0.791\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_N}(t) - V_{BP1}(t)$

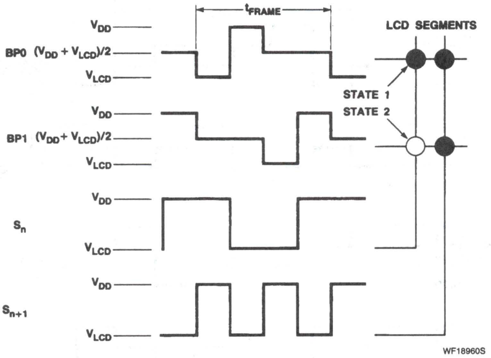
$V_{OFF(RMS)} = \frac{V_{OP}}{4}\sqrt{2} = 0.354\,V_{OP}$

b. Resultant Waveforms at LCD Segment

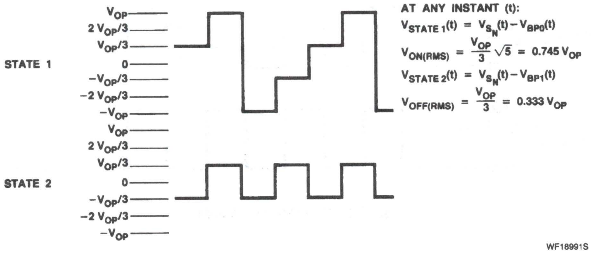
NOTE:
$V_{OP} = V_{DD} - V_{LCD}$

Figure 3. Waveforms for 1 : 2 Multiplex Drive Mode With ½ Bias

LCD Drive Mode Waveforms (Continued)


t_{FRAME}
LCD SEGMENTS
V_{DD}
BP0 $(V_{DD}+V_{LCD})/2$
V_{LCD}
STATE 1
STATE 2
V_{DD}
BP1 $(V_{DD}+V_{LCD})/2$
V_{LCD}
V_{DD}
S_n
V_{LCD}
V_{DD}
S_{n+1}
V_{LCD}
WF18960S

a. Waveforms at Driver


STATE 1
V_{OP}
$2\,V_{OP}/3$
$V_{OP}/3$
0
$-V_{OP}/3$
$-2\,V_{OP}/3$
$-V_{OP}$
STATE 2
V_{OP}
$2\,V_{OP}/3$
$V_{OP}/3$
0
$-V_{OP}/3$
$-2\,V_{OP}/3$
$-V_{OP}$
WF18991S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_N}(t) - V_{BP0}(t)$

$V_{ON(RMS)} = \frac{V_{OP}}{3}\sqrt{5} = 0.745\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_N}(t) - V_{BP1}(t)$

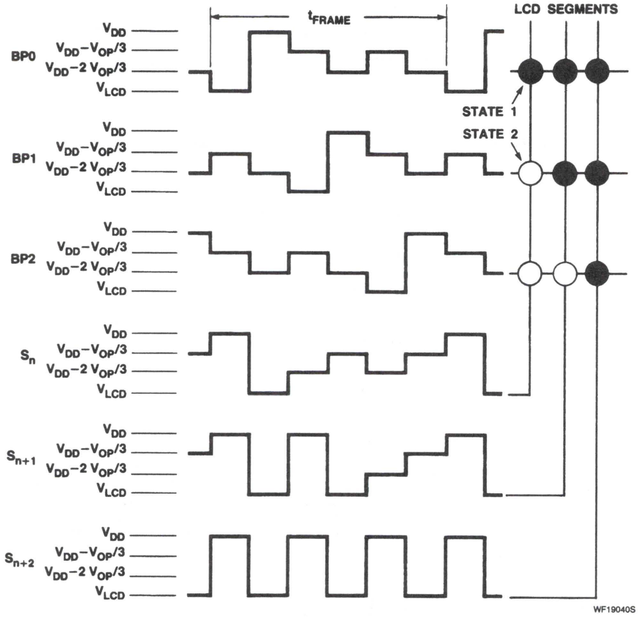
$V_{OFF(RMS)} = \frac{V_{OP}}{3} = 0.333\,V_{OP}$

b. Resultant Waveforms at LCD Segment

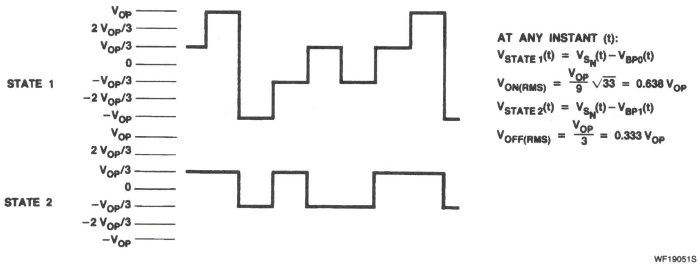
NOTE:
$V_{OP} = V_{DD} - V_{LCD}$

Figure 4. Waveforms for 1 : 2 Multiplex Drive Mode With ⅓ Bias

LCD Drive Mode Waveforms (Continued)


t_FRAME
LCD SEGMENTS
STATE 1
STATE 2
BP0
BP1
BP2
S_n
S_n+1
S_n+2
V_DD
V_DD−V_OP/3
V_DD−2 V_OP/3
V_LCD
WF19040S

a. Waveforms at Driver


STATE 1
STATE 2
V_OP
2 V_OP/3
V_OP/3
0
−V_OP/3
−2 V_OP/3
−V_OP
WF19051S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_N}(t) - V_{BP0}(t)$

$V_{ON(RMS)} = \frac{V_{OP}}{9}\sqrt{33} = 0.638\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_N}(t) - V_{BP1}(t)$

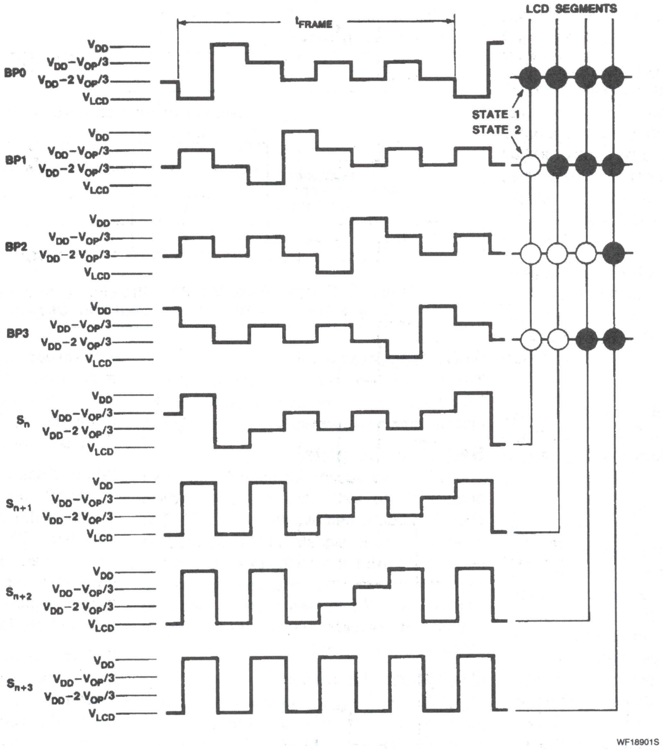
$V_{OFF(RMS)} = \frac{V_{OP}}{3} = 0.333\,V_{OP}$

b. Resultant Waveforms at LCD Segment

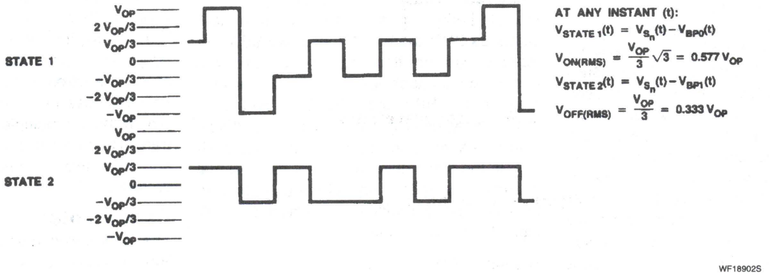
NOTE:
$V_{OP} = V_{DD} - V_{LCD}$

Figure 5. Waveforms for 1 : 3 Multiplex Drive Mode

LCD Drive Mode Waveforms (Continued)


LCD SEGMENTS
t_{FRAME}
STATE 1
STATE 2
BP0
BP1
BP2
BP3
S_n
S_{n+1}
S_{n+2}
S_{n+3}
V_{DD}
$V_{DD}-V_{OP}/3$
$V_{DD}-2\,V_{OP}/3$
V_{LCD}
WF18901S

a. Waveforms at Driver


STATE 1
STATE 2
V_{OP}
$2\,V_{OP}/3$
$V_{OP}/3$
0
$-V_{OP}/3$
$-2\,V_{OP}/3$
$-V_{OP}$
WF18902S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{ON(RMS)} = \frac{V_{OP}}{3}\sqrt{3} = 0.577\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{OFF(RMS)} = \frac{V_{OP}}{3} = 0.333\,V_{OP}$

b. Resultant Waveforms at LCD Segment

NOTE:
$V_{OP} = V_{DD} - V_{LCD}$

Figure 6. Waveforms for 1 : 4 Multiplex Drive Mode

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100kHz, f_{CLK} should be chosen to be above 125kHz. A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal Clock

When the internal oscillator is used, OSC (Pin 6) should be tied to V_{SS}. In this case, the output from CLK (Pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External Clock

The condition for external clock is made by tying OSC (Pin 6) to V_{DD}; CLK (Pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency, which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to Pin 4 when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode, the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus, but no data loss occurs.

Display Latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs, and one column of the display RAM.

Table 3. LCD Frame Frequencies

PCF8566 MODE	f_{FRAME}	NOMINAL f_{FRAME} (Hz)
Normal mode	$f_{CLK}/2880$	64
Power-saving mode	$f_{CLK}/480$	64

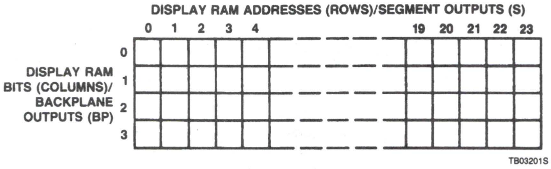

DISPLAY RAM ADDRESSES (ROWS)/SEGMENT OUTPUTS (S)
0 1 2 3 4
19 20 21 22 23
0
1
2
3
DISPLAY RAM BITS (COLUMNS)/ BACKPLANE OUTPUTS (BP)
TB03201S

Figure 7. Display RAM Bit-Map Showing Direct Relationship Between Display RAM Addresses and Segment Outputs, and Between Bi

Shift Register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

Segment Outputs

The LCD drive section includes 24 segment outputs S0 to S23 (Pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required, the unused segment outputs should be left open.

Backplane Outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open. In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1; therefore, these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3, respectively, carry the same signals, and may also be paired to increase the drive capabilities. In the static drive mode, the same signal is carried by all four backplane outputs, and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, a logic 0 indicates the "off" state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Figure 7). In multiplexed LCD applications, the segment data of the second, third, and fourth column of the display RAM are time-multiplexed with BP1, BP2, and BP3, respectively.

When display data is transmitted to the PCF8566, the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 8; the RAM filling organization depicted applies equally to other LCD types.

With reference to Figure 8, in the static drive mode the eight transmitted data bits are placed in Bit 0 of eight successive display RAM addresses. In the 1:2 multiplex drive mode, the eight transmitted data bits are placed in Bits 0 and 1 of four successive display RAM addresses. In the 1:3 multiplex drive mode, these bits are placed in Bits 0, 1, and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1:4 multiplex drive mode, the eight transmitted data bits are placed in Bits 0, 1, 2, and 3 of two successive display RAM addresses.

Data Pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer, thereby observing the filling order shown in Figure 8. The data pointer is automatically incremented according to the LCD configura-

Table 4. Blinking Frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY f_{BLINK} (Hz)
off			blinking_{off}
2Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0.5Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0.5

tion chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1:2 multiplex drive mode), by three (1:3 multiplex drive mode) or by two (1:4 multiplex drive mode).

Subaddress Counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1, and A2 (Pins 7, 8, and 9). A0, A1, and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree, then data storage is inhibited, but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

Output Bank Selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1:4 multiplex, all RAM addresses of Bit 0 are the first to be selected; these are followed by the contents of Bit 1, Bit 2, and then Bit 3. Similarly in 1:3 multiplex, Bits 0, 1, and 2 are selected sequentially. In 1:2 multiplex, Bits 0 then 1 are selected and, in the static mode, Bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of Bit 2 to be selected for display instead of Bit 0 contents. In the 1:2 drive mode, the contents of Bits 2 and 3 may be selected instead of Bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input Bank Selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in Bit 2 in static drive mode or in Bits 2 and 3 in 1:2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable Bit E at the required rate using the MODE SET command.

CHARACTERISTICS OF THE I^{2}C BUS

The I^{2}C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System Configuration

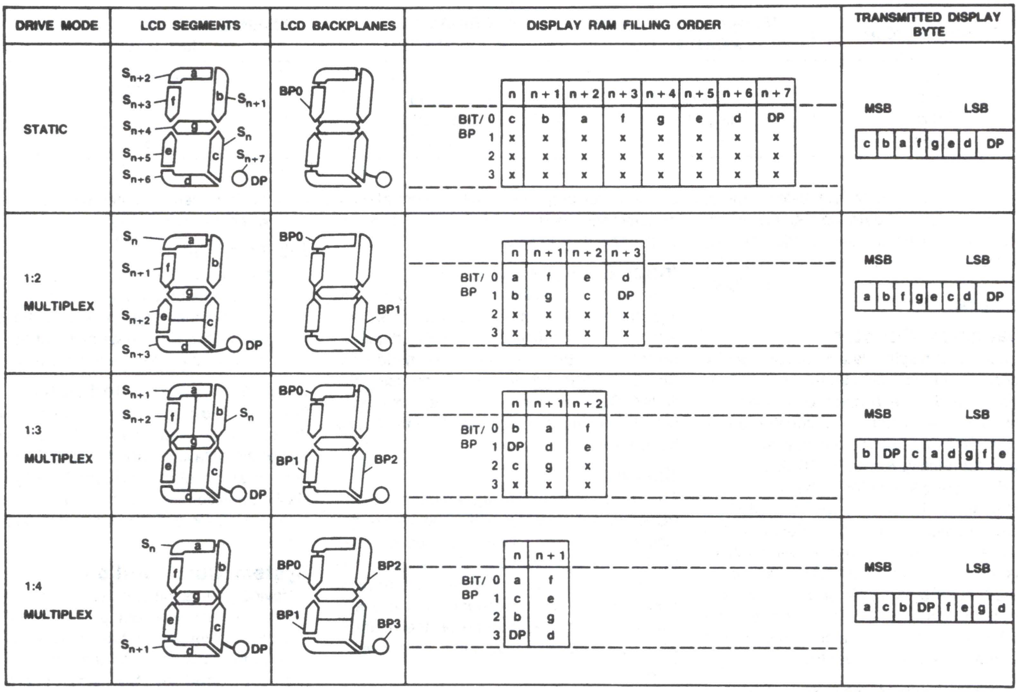
A device generating a message is a "transmitter"; a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse, and setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

PCF8566 I^{2}C Bus Controller

The PCF8566 acts as an I^{2}C slave receiver. It does not initiate I^{2}C bus transfers or transmit data to an I^{2}C master receiver. The only data


DRIVE MODE
LCD SEGMENTS
LCD BACKPLANES
DISPLAY RAM FILLING ORDER
TRANSMITTED DISPLAY BYTE
STATIC
1:2 MULTIPLEX
1:3 MULTIPLEX
1:4 MULTIPLEX
S_{n+2}
S_{n+3}
S_{n+4}
S_{n+5}
S_{n+6}
S_{n+1}
S_n
S_{n+7}
a
b
c
d
e
f
g
DP
BP0
BP1
BP2
BP3
MSB
LSB
TB03210S

STATIC

BIT/BP	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
0	c	b	a	f	g	e	d	DP
1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

MSB LSB: c b a f g e d DP

1:2 MULTIPLEX

BIT/BP	n	n + 1	n + 2	n + 3
0	a	f	e	d
1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

MSB LSB: a b f g e c d DP

1:3 MULTIPLEX

BIT/BP	n	n + 1	n + 2
0	b	a	f
1	DP	d	e
2	c	g	x
3	x	x	x

MSB LSB: b DP c a d g f e

1:4 MULTIPLEX

BIT/BP	n	n + 1
0	a	f
1	c	e
2	b	g
3	DP	d

MSB LSB: a c b DP f e g d

Figure 8. Relationships Between LCD Layout, Drive Mode, Display RAM Filling Order and Display Data Transmitted Over the I^2C Bus (x = Data Bit Unchanged)

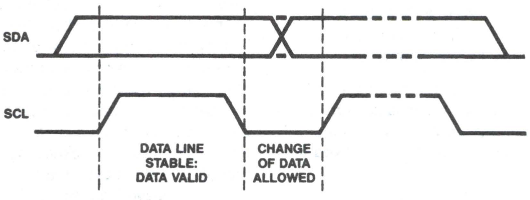

SDA
SCL
DATA LINE STABLE: DATA VALID
CHANGE OF DATA ALLOWED
WF20050S

Figure 9. Bit Transfer

output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I^2C bus slave address, on the transferred command data, and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2, are normally left open or tied to V_{SS}, which defines the hardware subaddress 0. In multiple device applications, A0, A1, and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I^2C slave address have the same hardware sub-address.

In the power-saving mode, it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line Low until its internal operations are completed. This is known as the "clock synchronization feature" of the I^2C bus and serves to slow down fast transmitters. Data loss does not occur.

Input Filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I^2C Bus Protocol

Two I^2C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (Pin 10). Therefore, two types of PCF8566 can be distinguished on the same I^2C bus, which allows:

(a) up to 16 PCF8566s on the same I^2C bus for very large LCD applications

(b) the use of two types of LCD multiplex on the same I^2C bus

The I^2C bus protocol is shown in Figure 13. The sequence is initiated with a start condition (S) from the I^2C bus master, which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address, but all PCF8566s with the alternative SA0 level ignore the whole I^2C bus transfer. After acknowledgement, one or

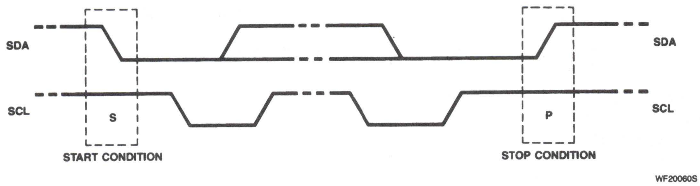

SDA
SCL
S
START CONDITION
SDA
SCL
P
STOP CONDITION
WF20060S

Figure 10. Definition of Start and Stop Conditions

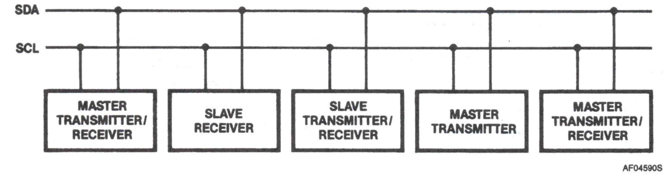

SDA
SCL
MASTER TRANSMITTER/ RECEIVER
SLAVE RECEIVER
SLAVE TRANSMITTER/ RECEIVER
MASTER TRANSMITTER
MASTER TRANSMITTER/ RECEIVER
AF04590S

Figure 11. System Configuration

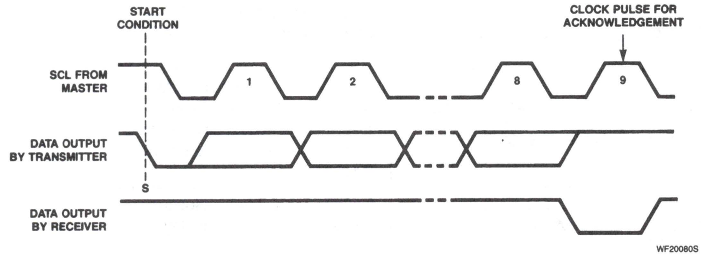

START CONDITION
CLOCK PULSE FOR ACKNOWLEDGEMENT
SCL FROM MASTER
1
2
8
9
DATA OUTPUT BY TRANSMITTER
S
DATA OUTPUT BY RECEIVER
WF20080S

Figure 12. Acknowledgement on the I^{2}C Bus

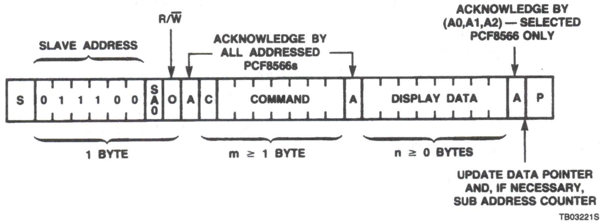

R/W̄
SLAVE ADDRESS
ACKNOWLEDGE BY ALL ADDRESSED PCF8566s
ACKNOWLEDGE BY (A0,A1,A2) — SELECTED PCF8566 ONLY
S
0 1 1 1 0 0
SA0
0
A
C
COMMAND
A
DISPLAY DATA
A
P
1 BYTE
m ≥ 1 BYTE
n ≥ 0 BYTES
UPDATE DATA POINTER AND, IF NECESSARY, SUB ADDRESS COUNTER
TB03221S

Figure 13. I^{2}C Bus Protocol

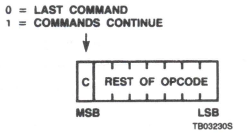

0 = LAST COMMAND
1 = COMMANDS CONTINUE
C
REST OF OPCODE
MSB
LSB
TB03230S

Figure 14. General Format of Command Byte

more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation Bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the sub-address counter. Both data pointer and sub-address counter are automatically updated and the data is directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I^{2}C bus master issues a stop condition (P).

Command Decoder

The command decoder identifies command bytes that arrive on the I^{2}C bus. All available commands carry a continuation Bit C in their most-significant bit position (Figure 14). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8566 are defined in Table 5.

Table 5. Definition of PCF8566 Commands

COMMAND/OPCODE	OPTIONS			DESCRIPTION
MODE SET C 1 0 LP E B M1 M0	**LCD Drive Mode**		**Bits M1 M0**	Defines LCD drive mode.
	static (1BP)		0 1	
	1:2 MUX (2BP)		1 0	
	1:3 MUX (3BP)		1 1	
	1:4 MUX (4BP)		0 0	
	LCD Bias		**Bit B**	Defines LCD bias configuration.
	1/3 bias		0	
	1/2 bias		1	
	Display Status		**Bit E**	Defines display status. The possibility of disabling the display allows implementation of blinking under external control.
	disabled (blank)		0	
	enabled		1	
	Mode		**Bit LP**	Defines power dissipation mode.
	normal mode		0	
	power-saving mode		1	
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	Bits P4 P3 P2 P1 P0			Five bits of immediate data, Bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses.
	5-Bit binary value of 0 to 23			
DEVICE SELECT C 1 1 0 0 A2 A1 A0	Bits		A0 A1 A2	Three bits of immediate data, Bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses.
	3-Bit binary value of 0 to 7			
BANK SELECT C 1 1 1 1 0 I O	**Static**	**1:2 MUX**	**Bit I**	Defines input bank selection (storage of arriving display data).
	RAM Bit 0	RAM Bits 0, 1	0	
	RAM Bit 2	RAM Bits 2, 3	1	
	Static	**1:2 MUX**	**Bit O**	Defines output bank selection (retrieval of LCD display data).
	RAM Bit 0	RAM Bits 0, 1	0	
	RAM Bit 2	RAM Bits 2, 3	1	The BANK SELECT command has no effect in 1:3 and 1:4 multiplex drive modes.
BLINK C 1 1 1 0 A BF1 BF0	**Blink Frequency**		**Bits BF1 BF0**	Defines the blinking frequency.
	off		0 0	
	2Hz		0 1	
	1Hz		1 0	
	0.5Hz		1 1	
	Blink Mode		**Bit A**	Selects the blinking mode; normal operation with frequency set by Bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1:3 and 1:4 multiplex drive modes.
	normal blinking		0	
	alternation blinking		1	

Display Controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded Operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs, but their backplane outputs are left open (Figure 15).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g., by noise in adverse electrical environments, or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin, the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Figure 16. The waveforms are identical to the parent device PCF8576. Cascadability between PCF8566s and PCF8576s is possible, giving cost-effective LCD applications.

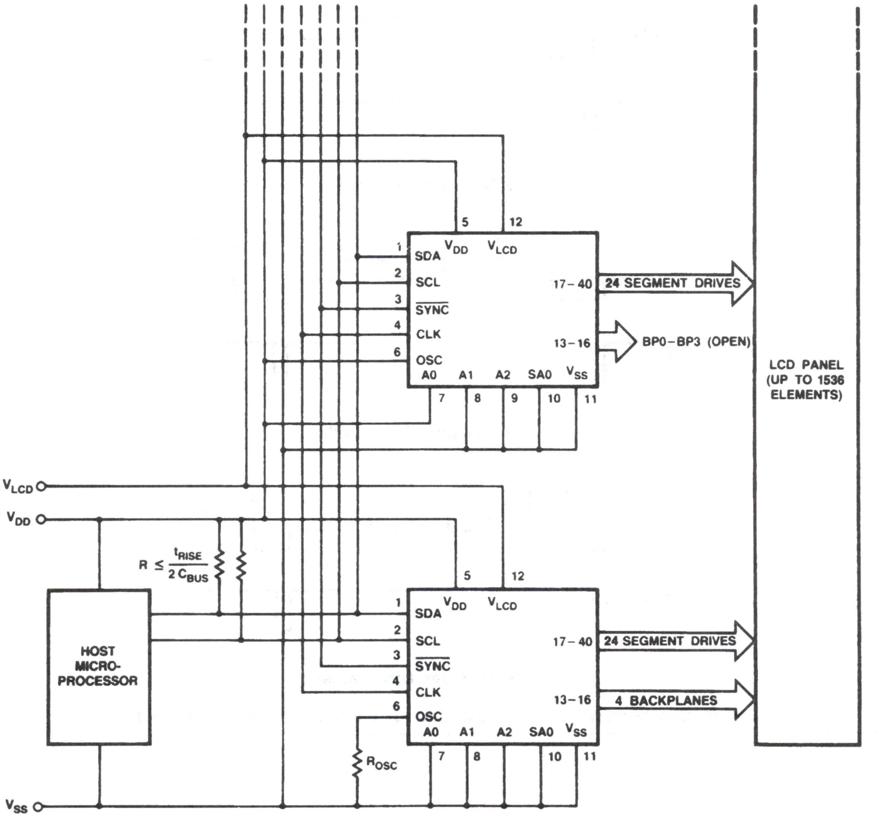
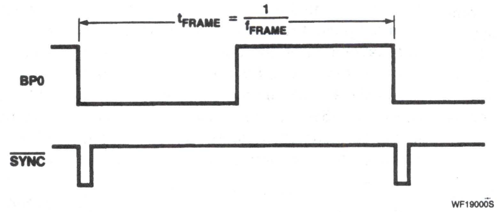
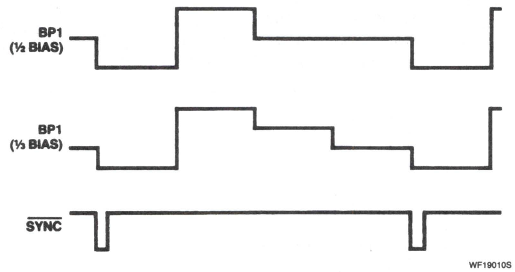


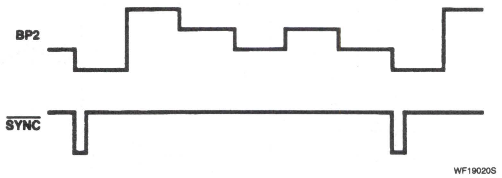
Figure 15. Cascaded PCF8566 Configuration


$t_{FRAME} = \frac{1}{f_{FRAME}}$
BP0
$\overline{\text{SYNC}}$
WF19000S

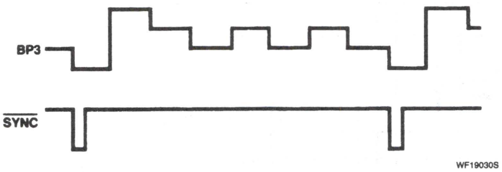
a. Static Drive Mode


BP1
(½ BIAS)
BP1
(⅓ BIAS)
$\overline{\text{SYNC}}$
WF19010S

b. 1:2 Multiplex Drive Mode


BP2
$\overline{\text{SYNC}}$
WF19020S

c. 1:3 Multiplex Drive Mode


BP3
$\overline{\text{SYNC}}$
WF19030S

d. 1:4 Multiplex Drive Mode

Figure 16. Synchronization of the Cascade for the Various PCF8566 Drive Modes

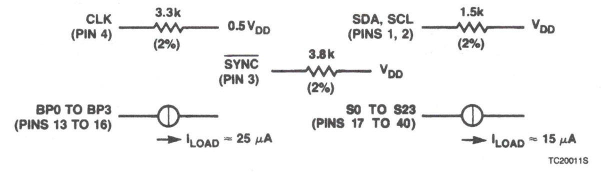

CLK
(PIN 4)
3.3k
(2%)
0.5 V_{DD}
SDA, SCL
(PINS 1, 2)
1.5k
(2%)
V_{DD}
SYNC
(PIN 3)
3.8k
(2%)
V_{DD}
BP0 TO BP3
(PINS 13 TO 16)
I_{LOAD} ≈ 25 μA
S0 TO S23
(PINS 17 TO 40)
I_{LOAD} ≈ 15 μA
TC20011S

Figure 17. Test Loads

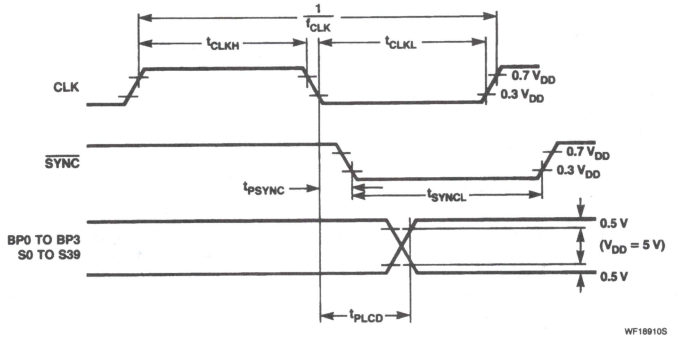

1/t_{CLK}
t_{CLKH}
t_{CLKL}
CLK
0.7 V_{DD}
0.3 V_{DD}
SYNC
0.7 V_{DD}
0.3 V_{DD}
t_{PSYNC}
t_{SYNCL}
BP0 TO BP3
S0 TO S39
0.5 V
(V_{DD} = 5 V)
0.5 V
t_{PLCD}
WF18910S

Figure 18. Driver Timing Waveforms

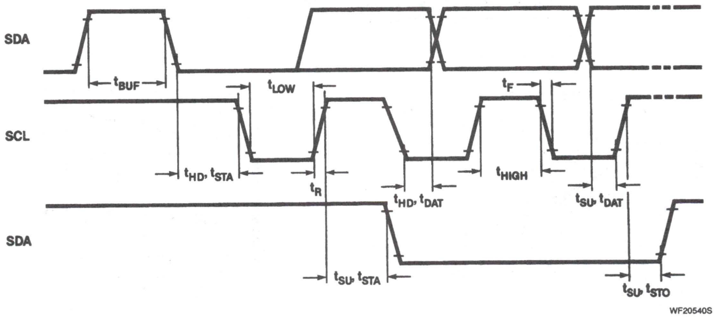
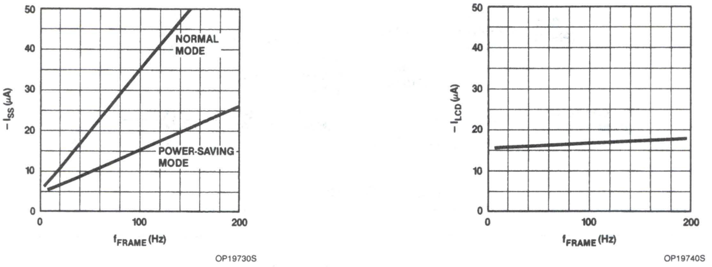
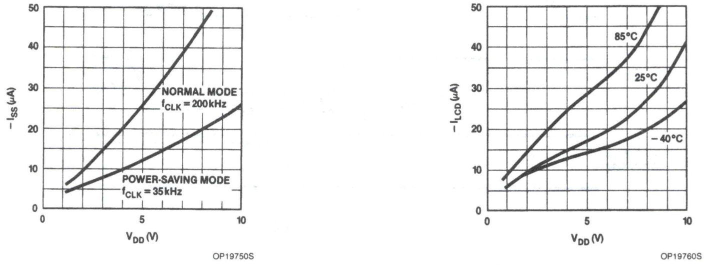

SDA
t_{BUF}
t_{LOW}
t_F
SCL
t_{HD}, t_{STA}
t_R
t_{HIGH}
t_{HD}, t_{DAT}
t_{SU}, t_{DAT}
SDA
t_{SU}, t_{STA}
t_{SU}, t_{STO}
WF20540S

Figure 19. I^2C Bus Timing Waveforms



a. $V_{DD} = 5V$; $V_{LCD} = 0V$; $T_A = 25°C$

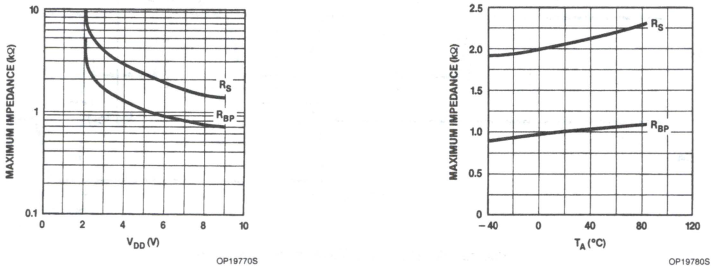
b. $V_{DD} = 5V$; $V_{LCD} = 0V$; $T_A = 25°C$



c. $V_{LCD} = 0V$; External Clock; $T_A = -40$ to $+85°C$

d. $V_{LCD} = 0V$; External Clock; f_{CLK} = Nominal Frequency

Figure 20. Typical Supply Current Characteristics



a. $V_{LCD} = 0V$; $T_A = 25°C$

b. $V_{DD} = 5V$; $V_{LCD} = 0V$

Figure 21. Typical Characteristics of LCD Outputs

Universal LCD Driver for Low Multiplex Rates PCF8566

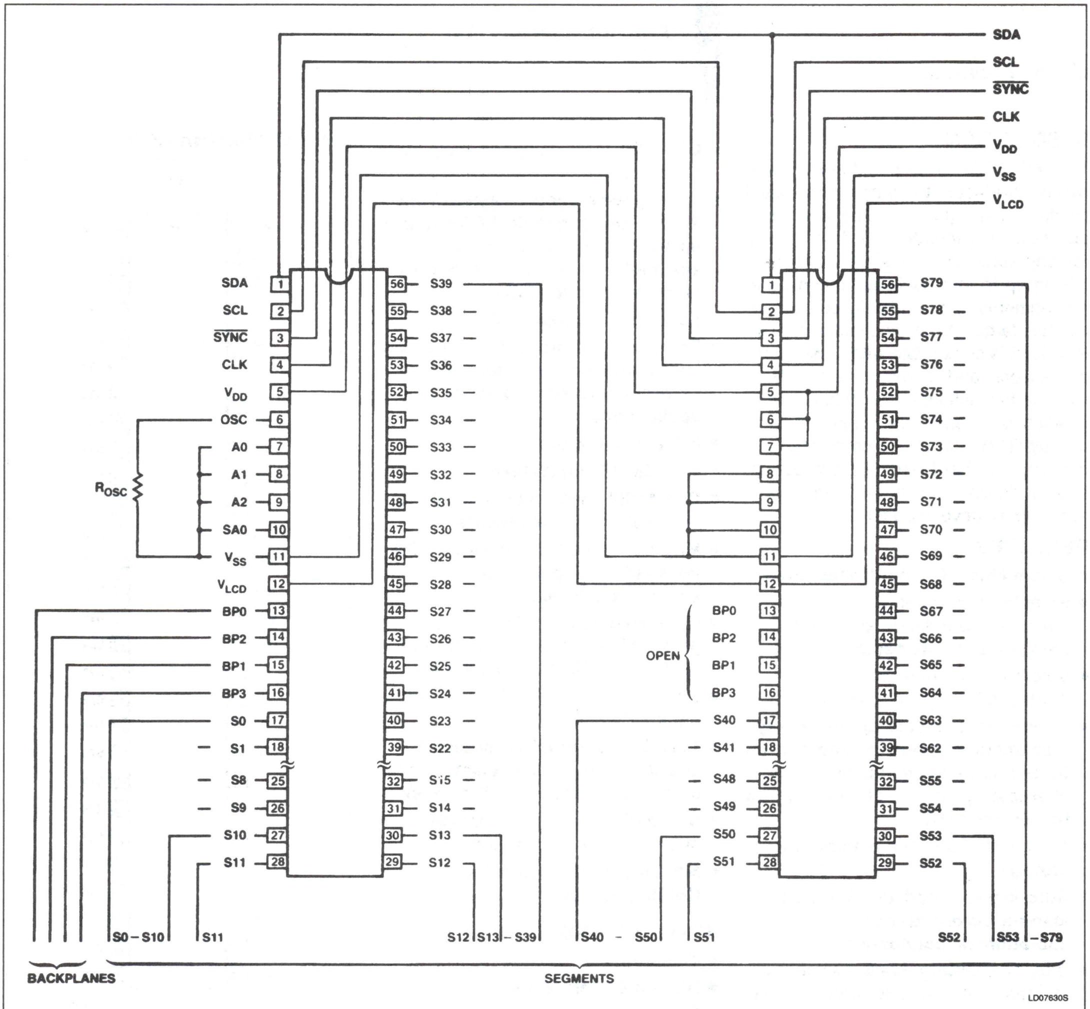

SDA
SCL
SYNC
CLK
V_DD
V_SS
V_LCD
SDA 1
SCL 2
SYNC 3
CLK 4
V_DD 5
OSC 6
A0 7
A1 8
A2 9
SA0 10
V_SS 11
V_LCD 12
BP0 13
BP2 14
BP1 15
BP3 16
S0 17
S1 18
S8 25
S9 26
S10 27
S11 28
R_OSC
56 S39
55 S38
54 S37
53 S36
52 S35
51 S34
50 S33
49 S32
48 S31
47 S30
46 S29
45 S28
44 S27
43 S26
42 S25
41 S24
40 S23
39 S22
32 S15
31 S14
30 S13
29 S12
OPEN
BP0 13
BP2 14
BP1 15
BP3 16
S40 17
S41 18
S48 25
S49 26
S50 27
S51 28
56 S79
55 S78
54 S77
53 S76
52 S75
51 S74
50 S73
49 S72
48 S71
47 S70
46 S69
45 S68
44 S67
43 S66
42 S65
41 S64
40 S63
39 S62
32 S55
31 S54
30 S53
29 S52
S0 – S10
S11
S12
S13 – S39
S40 - S50
S51
S52
S53 – S79
BACKPLANES
SEGMENTS
LD07630S

Figure 22. Single-Plane Wiring of Packaged PCF8566s

Signetics

PCF8576

Universal LCD Driver for Low Multiplex Rates

Product Specification

Linear Products

DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware sub-addressing, and by display memory switching (static and duplex drive modes).

FEATURES

- **Single-chip LCD controller/driver**
- **Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing**
- **Selectable display bias configuration: static, ½, or ⅓**
- **40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements**
- **40 × 4-bit RAM for display data storage**
- **Auto-incremented display data loading across device sub-address boundaries**
- **Display memory bank switching in static and duplex drive modes**
- **Versatile blinking modes**
- **LCD and logic supplies may be separated**
- **Wide power supply range: from 2V for low-threshold LCDs and up to 9V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs**
- **Low power consumption**
- **Power-saving mode for extremely low power consumption in battery-operated and telephone applications**
- **I^2C bus interface**
- **TTL/CMOS compatible**
- **Compatible with any 4-bit, 8-bit, or 16-bit microprocessors**
- **May be cascaded for large LCD applications (up to 2560 segments possible)**
- **Optimized pinning for single plane wiring in both single and multiple PCF8576 applications**
- **Space-saving 56-lead plastic mini-pack (VSO-56)**
- **Very low external component count (at most one resistor, even in multiple device applications)**
- **Compatible with Philips/Videlec chip-on-glass technology**
- **Manufactured in silicon-gate CMOS process**

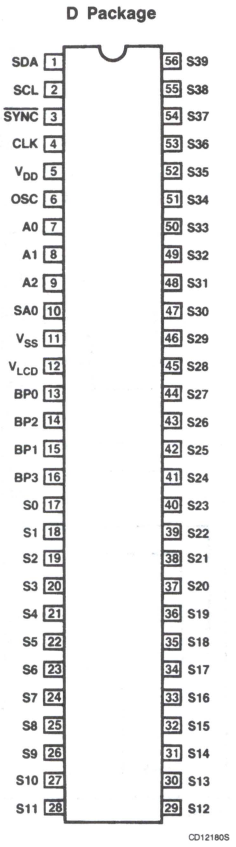
APPLICATIONS

- **Telephony**
- **Hand-held terminals**
- **General instrumentation**
- **Car dashboard displays**

ORDERING INFORMATION

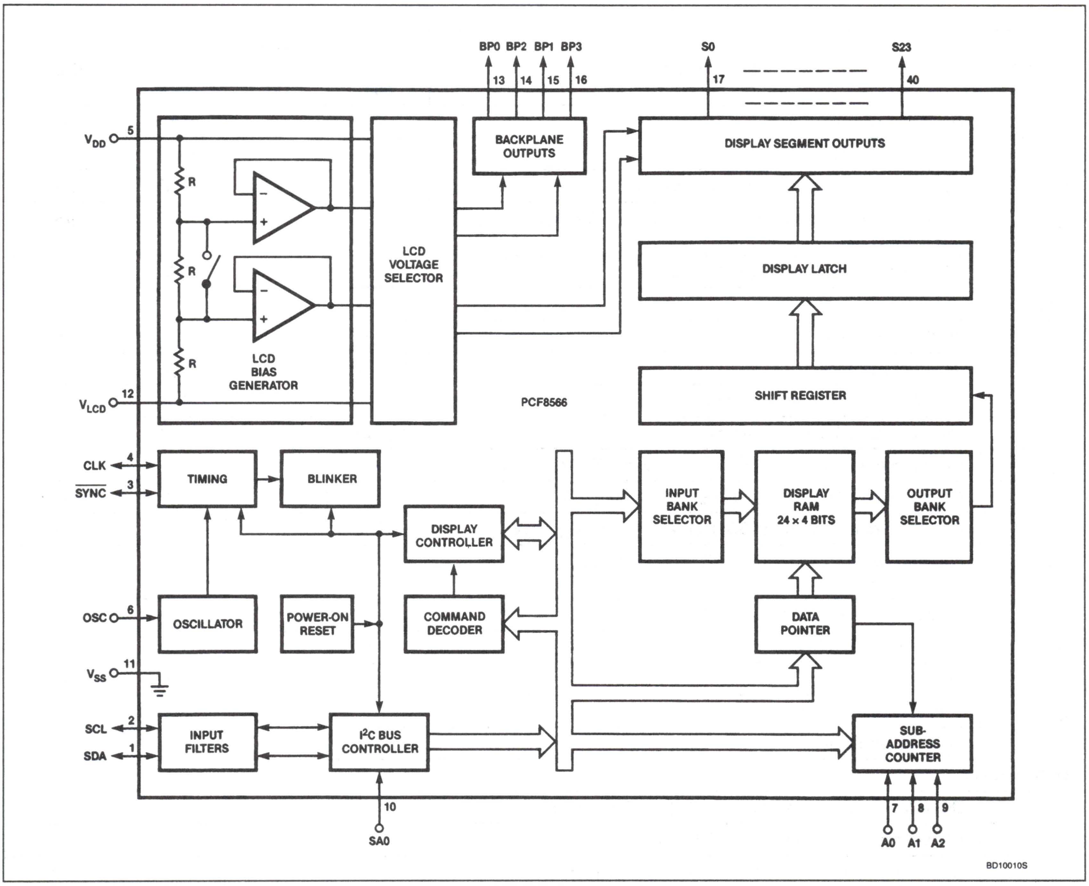
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
56-Pin Plastic SO (VSO-56; SOT-190)	−40°C to +85°C	PCF8576TD

PIN CONFIGURATION


D Package
SDA 1
SCL 2
SYNC 3
CLK 4
VDD 5
OSC 6
A0 7
A1 8
A2 9
SA0 10
VSS 11
VLCD 12
BP0 13
BP2 14
BP1 15
BP3 16
S0 17
S1 18
S2 19
S3 20
S4 21
S5 22
S6 23
S7 24
S8 25
S9 26
S10 27
S11 28
56 S39
55 S38
54 S37
53 S36
52 S35
51 S34
50 S33
49 S32
48 S31
47 S30
46 S29
45 S28
44 S27
43 S26
42 S25
41 S24
40 S23
39 S22
38 S21
37 S20
36 S19
35 S18
34 S17
33 S16
32 S15
31 S14
30 S13
29 S12
CD12180S

PIN NO.	SYMBOL	DESCRIPTION
1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	Cascade synchronization input/output
4	CLK	External clock input/output
5	V_{DD}	Positive supply voltage
6	OSC	Oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	Logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

BLOCK DIAGRAM


BP0 BP2 BP1 BP3
13 14 15 16
S0
17
S23
40
BACKPLANE OUTPUTS
DISPLAY SEGMENT OUTPUTS
VDD
5
R
R
R
LCD VOLTAGE SELECTOR
DISPLAY LATCH
LCD BIAS GENERATOR
VLCD
12
PCF8566
SHIFT REGISTER
CLK
4
SYNC
3
TIMING
BLINKER
DISPLAY CONTROLLER
INPUT BANK SELECTOR
DISPLAY RAM 24 × 4 BITS
OUTPUT BANK SELECTOR
OSC
6
OSCILLATOR
POWER-ON RESET
COMMAND DECODER
DATA POINTER
VSS
11
SCL
2
SDA
1
INPUT FILTERS
I²C BUS CONTROLLER
SUB-ADDRESS COUNTER
10
SA0
7 8 9
A0 A1 A2
BD10010S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to +11	V
V_{LCD}	LCD supply voltage range	V_{DD} −11 to V_{DD}	V
V_I	Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_{SS} −0.5 to V_{DD} +0.5	V
V_O	Output voltage range (S0 to S39; BP0 to BP3)	V_{LCD} −0.5 to V_{DD} +0.5	V
$\pm I_I$	DC input current	20	mA
$\pm I_O$	DC output current	25	mA
$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	V_{DD}, V_{SS}, or V_{LCD} current	50	mA
P_{TOT}	Power dissipation per package	400	mW
P_O	Power dissipation per output	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

V_{SS} = 0V; V_{DD} = 2 to 9V; V_{LCD} = V_{DD}−2 to V_{DD}−9V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Operating supply voltage	2		9	V
V_{LCD}	LCD supply voltage[1]	V_{DD}−9		V_{DD}−2	V
I_{DD}	Operating supply current at f_{CLK} = 200kHz[2]			TBD	μA
I_{LP}	Power-saving mode supply current at V_{DD} = 3.5V; V_{LCD} = 0V; f_{CLK} = 35kHz[2]			TBD	μA
I_{LCD}	LCD supply current at f_{CLK} = 200kHz[2]			TBD	μA
Logic					
V_{IL}	Input voltage Low	V_{SS}		0.3V_{DD}	V
V_{IH}	Input voltage High	0.7 V_{DD}		V_{DD}	V
V_{OL}	Output voltage Low at I_O = 0mA			0.05	V
V_{OH}	Output voltage High at I_O = 0mA	V_{DD}−0.05			V
I_{OL1}	Output current Low (CLK, $\overline{SYNC}$) at V_{OL} = 1.0V; V_{DD} = 5V	1			mA
I_{OH}	Output current High (CLK) at V_{OH} = 4.0V; V_{DD} = 5V			−1	mA
I_{OL2}	Output current Low (SDA; SCL) at V_{OL} = 0.4V; V_{DD} = 5V	3			mA
± I_{L1}	Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}			1	μA
± I_{L2}	Leakage current (OSC) at V_I = V_{DD}			1	μA
R_{SYNC}	Pull-up resistor ($\overline{SYNC}$)	30	60	100	kΩ
V_{REF}	Power-on reset level[3]	0.8	1.2	1.6	V
t_{SW}	Tolerable spike width on bus			100	ns
C_I	Input capacitance[4]			7	pF
LCD outputs					
± V_{BP}	DC voltage component (BP0 to BP3) at C_{BP} = 35nF		20		mV
± V_S	DC voltage component (S0 to S39) at C_S = 5nF		20		mV
R_{BP}	Output impedance (BP0 to BP3) at V_{LCD} = V_{DD}−5V[5]			5	kΩ
R_S	Output impedance (S0 to S39) at V_{LCD} = V_{DD}−5V[5]			7.0	kΩ

AC ELECTRICAL CHARACTERISTICS $V_{SS} = 0V$; $V_{DD} = 2$ to 9V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9V$; $T_A = -40°C$ to $+85°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{CLK}	Oscillator frequency (normal mode) at $V_{DD} = 5V$; $R_{OSC} = 200k\Omega^7$	125	185	288	kHz
f_{CLKLP}	Oscillator frequency (power-saving mode) at $V_{DD} = 3.5V$; $R_{OSC} = 1.2M\Omega$	21	31	48	kHz
t_{CLKH}	CLK High time	1			μs
t_{CLKL}	CLK Low time	1			μs
t_{PSYNC}	$\overline{SYNC}$ propagation delay			200	ns
t_{SYNCL}	$\overline{SYNC}$ Low time	1			μs
t_{PLCD}	Driver delays with test loads at $V_{LCD} = V_{DD}-5V$			30	μs
I^2C bus high-speed mode					
t_{BUF}	Bus free time	4.7			μs
t_{HD}, t_{STA}	Start condition hold time	4			μs
t_{LOW}	SCL Low time	4.7			μs
t_{HIGH}	SCL High time	4			μs
t_{SU}, t_{STA}	Start condition setup time (repeated start code only)	4.7			μs
t_{HD}, t_{DAT}	Data hold time	0			μs
t_{SU}, t_{DAT}	Data setup time	250			ns
t_R	Rise time			1	μs
t_F	Fall time			300	ns
t_{SU}, t_{STO}	Stop condition setup time	4.7			μs
I^2C bus low-speed mode					
t_{BUF}	Bus free time	105			μs
t_{HD}, t_{STA}	Start condition hold time	365			μs
t_{LOW}	SCL Low time	105		155	μs
t_{HIGH}	SCL High time	365		415	μs
t_{SU}, t_{STA}	Start condition setup time (repeated start code only)	105		155	μs
t_{HD}, t_{DAT}	Data hold time	0			μs
t_{SU}, t_{DAT}	Data setup time	250			ns
t_R	Rise time			1	μs
t_F	Fall time			300	ns
t_{SU}, t_{STO}	Stop condition setup time	105		155	μs

NOTES:

1. $V_{LCD} < V_{DD}-3V$ for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty cycle; I^2C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125kHz$, I^2C bus maximum transmission speed is derated.

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Figure 1. The host microprocessor maintains the 2-line I^2C bus communication channel with the PCF8576. A resistor connected between OSC (Pin 6) and V_{SS} (Pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and to the LCD panel chosen for the application.

Table 1. Selection of Display Configurations

ACTIVE BACKPLANE OUTPUTS	NUMBER OF SEGMENTS	7-SEGMENT NUMERIC	14-SEGMENT ALPHANUMERIC	DOT MATRIX
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4×40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3×40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2×40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

Power-On Reset

At power-on, the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with ⅓ bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1ms following power-on to allow completion of the reset action.

LCD Bias Generator

The full-scale LCD voltage (V_{OP}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to Pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The center resistor can be switched out of circuit to provide a ½ bias voltage level for the 1:2 multiplex configuration.

LCD Voltage Selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{OP} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2. Preferred LCD Drive Modes: Summary of Characteristics

LCD DRIVE MODE	LCD BIAS CONFIGURATION	$\frac{V_{OFF(RMS)}}{V_{OP}}$	$\frac{V_{ON\,(RMS)}}{V_{OP}}$	$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}}$
Static (1BP)	Static (2 levels)	0	1	∞
1:2 MUX (2BP)	½ (3 levels)	$\sqrt{2}/4 = 0.354$	$\sqrt{10}/4 = 0.791$	$\sqrt{5} = 2.236$
1:2 MUX (2BP)	⅓ (4 levels)	⅓ = 0.333	$\sqrt{5}/3 = 0.745$	$\sqrt{5} = 2.236$
1:3 MUX (3BP)	⅓ (4 levels)	⅓ = 0.333	$\sqrt{33}/9 = 0.638$	$\sqrt{33}/3 = 1.915$
1:4 MUX (4BP)	⅓ (4 levels)	⅓ = 0.333	$\sqrt{3}/3 = 0.577$	$\sqrt{3} = 1.732$

A practical value for V_{OP} is determined by equating $V_{OFF(RMS)}$ with a defined LCD threshold voltage ($V_{TH\,LCD}$), typically when the LCD exhibits approximately 10% contrast. In the static drive mode, a itable choice is $V_{OP} \gtrsim 3V_{TH\,LCD}$.

Multiplex drive ratios of 1:3 and 1:4 with ½ bias are possible, but the discrimination and, therefore, the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1:3 multiplex or $\sqrt{21}/3 = 1.528$ for 1:4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{OP} as follows:

1:3 multiplex (½ bias):
$V_{OP} = \sqrt{6}V_{OFF(RMS)} = 2.449V_{OFF(RMS)}$

1:4 multiplex (½ bias): $V_{OP} = 4\sqrt{3}/3V_{OFF(RMS)} = 2.309V_{OFF(RMS)}$ These compare with $V_{OP} = 3V_{OFF(RMS)}$ when ⅓ bias is used.

LCD Drive Mode Waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 2.

When two backplanes are provided in the LCD, the 1:2 multiplex drive mode applies. The PCF8576 allows use of ½ or ⅓ bias in this mode as shown in Figures 3 and 4.

Universal LCD Driver for Low Multiplex Rates **PCF8576**

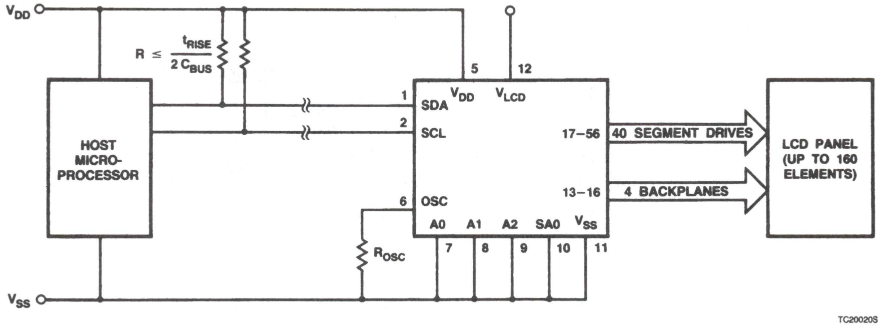
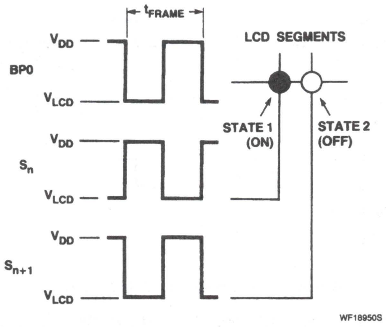
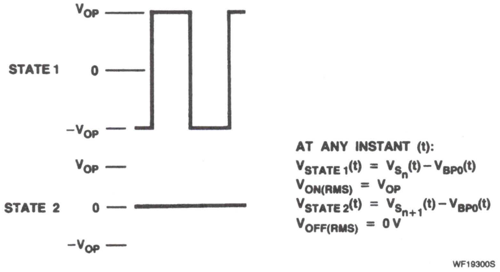

VDD
VSS
R ≤ tRISE / 2 CBUS
HOST MICRO-PROCESSOR
5
12
1
2
6
SDA
SCL
OSC
VDD
VLCD
17–56
13–16
A0
A1
A2
SA0
VSS
7
8
9
10
11
ROSC
40 SEGMENT DRIVES
4 BACKPLANES
LCD PANEL (UP TO 160 ELEMENTS)
TC20020S

Figure 1. Typical System Configuration


tFRAME
VDD
BP0
VLCD
VDD
Sn
VLCD
VDD
Sn+1
VLCD
LCD SEGMENTS
STATE 1 (ON)
STATE 2 (OFF)
WF18950S

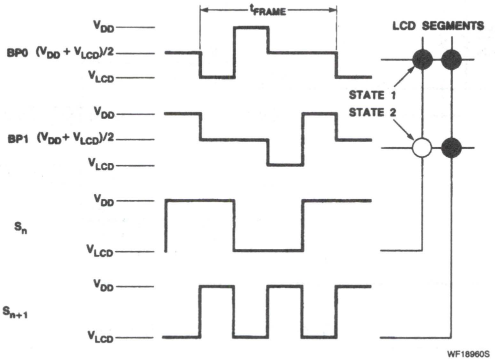
a. Waveforms at Driver


VOP
STATE 1
0
−VOP
VOP
STATE 2
0
−VOP
AT ANY INSTANT (t):
VSTATE 1(t) = VSn(t) − VBP0(t)
VON(RMS) = VOP
VSTATE 2(t) = VSn+1(t) − VBP0(t)
VOFF(RMS) = 0 V
WF19300S

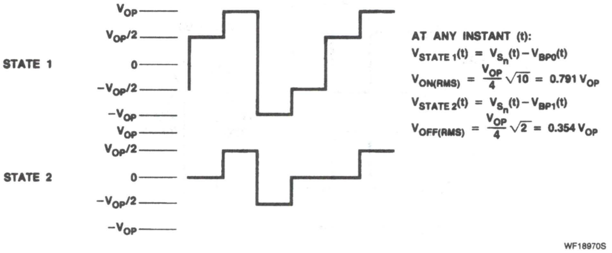
b. Resultant Waveforms at LCD Segment

Figure 2. Static Drive Mode Waveforms: $V_{OP} = V_{DD} - V_{LCD}$

6


t_{FRAME}
V_{DD}
BP0 $(V_{DD} + V_{LCD})/2$
V_{LCD}
LCD SEGMENTS
STATE 1
STATE 2
V_{DD}
BP1 $(V_{DD} + V_{LCD})/2$
V_{LCD}
V_{DD}
S_n
V_{LCD}
V_{DD}
S_{n+1}
V_{LCD}
WF18960S

a. Waveforms at Driver


V_{OP}
$V_{OP}/2$
STATE 1
0
$-V_{OP}/2$
$-V_{OP}$
V_{OP}
$V_{OP}/2$
STATE 2
0
$-V_{OP}/2$
$-V_{OP}$
WF18970S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_n}(t) - V_{BP0}(t)$

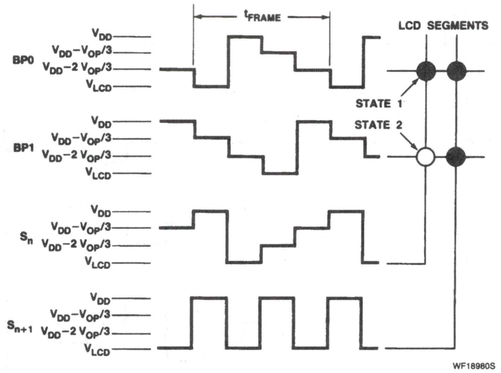
$V_{ON(RMS)} = \frac{V_{OP}}{4}\sqrt{10} = 0.791\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_n}(t) - V_{BP1}(t)$

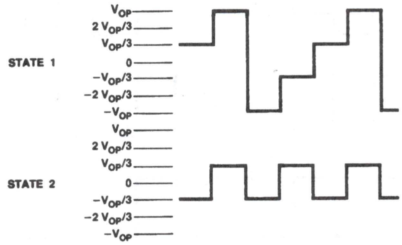
$V_{OFF(RMS)} = \frac{V_{OP}}{4}\sqrt{2} = 0.354\,V_{OP}$

b. Resultant Waveforms at LCD Segment

Figure 3. Waveforms for 1:2 Multiplex Drive Mode With ½ Bias: $V_{OP} = V_{DD} - V_{LCD}$


tFRAME
LCD SEGMENTS
BP0
BP1
S_n
S_{n+1}
V_{DD}
$V_{DD}-V_{OP}/3$
$V_{DD}-2V_{OP}/3$
V_{LCD}
STATE 1
STATE 2
WF18980S

a. Waveforms at Drive


STATE 1
STATE 2
V_{OP}
$2V_{OP}/3$
$V_{OP}/3$
0
$-V_{OP}/3$
$-2V_{OP}/3$
$-V_{OP}$
WF18990S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{ON(RMS)} = \frac{V_{OP}}{3}\sqrt{5} = 0.745\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_n}(t) - V_{BP1}(t)$

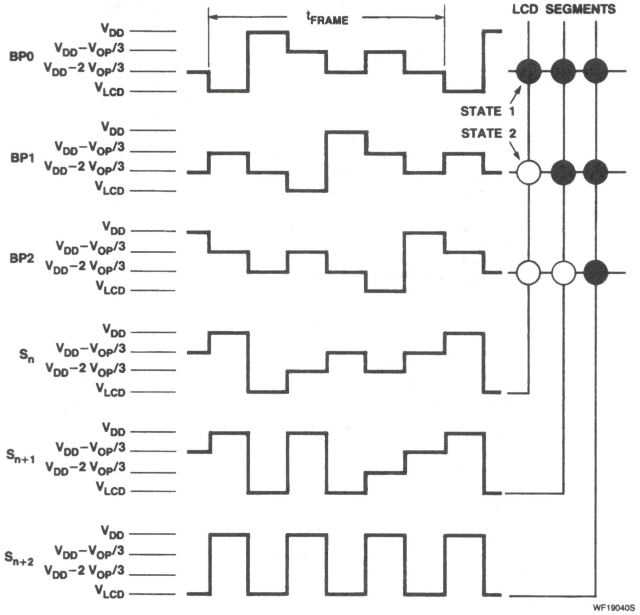
$V_{OFF(RMS)} = \frac{V_{OP}}{3} = 0.333\,V_{OP}$

b. Resultant Waveforms at LCD Segment

Figure 4. Waveforms for 1:2 Multiplex Drive Mode With ⅓ Bias: $V_{OP} = V_{DD} - V_{LCD}$

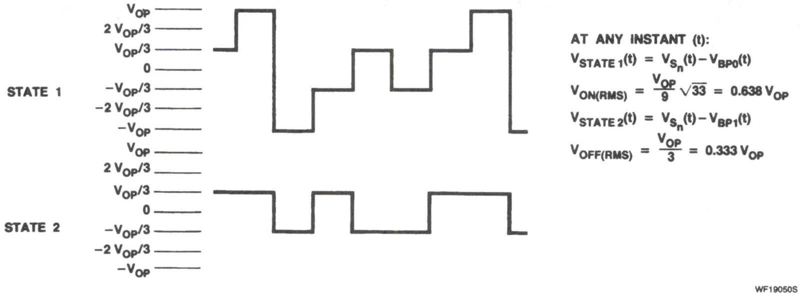
Universal LCD Driver for Low Multiplex Rates PCF8576

The backplane and segment drive wavefront for the 1:3 multiplex drive mode (three LCD backplanes) and for the 1:4 multiplex drive mode (four LCD backplanes) are shown in Figures 5 and 6, respectively.



t_{FRAME}
LCD SEGMENTS
BP0
BP1
BP2
S_n
S_{n+1}
S_{n+2}
V_{DD}
$V_{DD}-V_{OP}/3$
$V_{DD}-2\,V_{OP}/3$
V_{LCD}
STATE 1
STATE 2
WF19040S

a. Waveforms at Driver



STATE 1
STATE 2
V_{OP}
$2\,V_{OP}/3$
$V_{OP}/3$
0
$-V_{OP}/3$
$-2\,V_{OP}/3$
$-V_{OP}$
WF19050S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_n}(t) - V_{BP0}(t)$

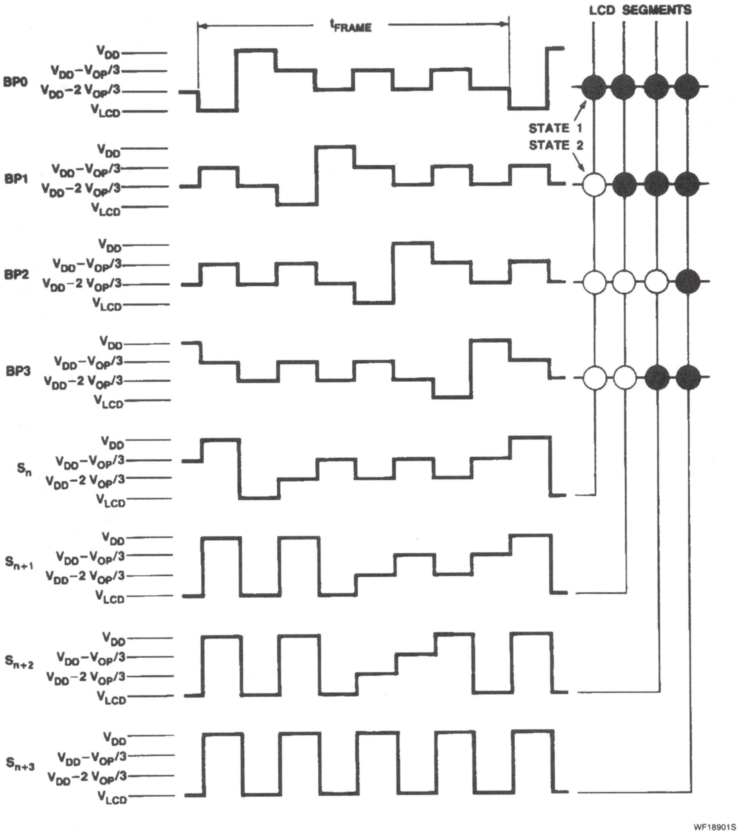
$V_{ON(RMS)} = \frac{V_{OP}}{9}\sqrt{33} = 0.638\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_n}(t) - V_{BP1}(t)$

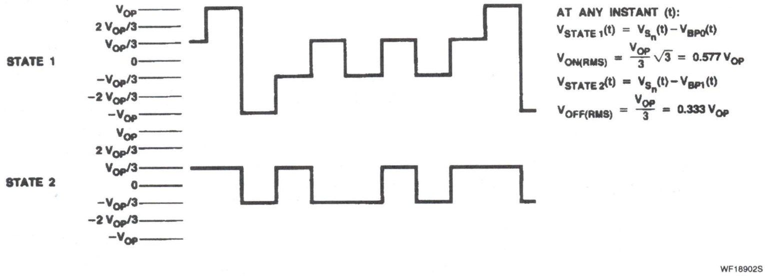
$V_{OFF(RMS)} = \frac{V_{OP}}{3} = 0.333\,V_{OP}$

b. Resultant Waveforms at LCD Segment

Figure 5. Waveforms for 1:3 Multiplex Drive Mode: $V_{OP} = V_{DD} - V_{LCD}$


LCD SEGMENTS
tFRAME
BP0
BP1
BP2
BP3
Sn
Sn+1
Sn+2
Sn+3
VDD
VDD−VOP/3
VDD−2 VOP/3
VLCD
STATE 1
STATE 2
WF18901S

a. Waveforms at Driver


STATE 1
STATE 2
VOP
2 VOP/3
VOP/3
0
−VOP/3
−2 VOP/3
−VOP
WF18902S

AT ANY INSTANT (t):

$V_{STATE\,1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{ON(RMS)} = \frac{V_{OP}}{3}\sqrt{3} = 0.577\,V_{OP}$

$V_{STATE\,2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{OFF(RMS)} = \frac{V_{OP}}{3} = 0.333\,V_{OP}$

b. Resultant Waveforms at LCD Segment

Figure 6. Waveforms for 1:4 Multiplex Drive Mode: $V_{OP} = V_{DD} - V_{LCD}$

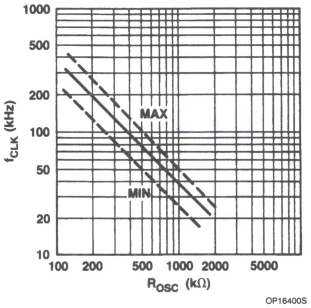


Figure 7. Oscillator Frequency as a Function of R_{OSC}: $f_{CLK} \approx (3.6 \times 10^7 / R_{OSC})$ kHz·Ω

Oscillator

Internal Clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (Pin 6) and V_{SS} (Pin 11) as shown in Figure 7. In this case, the output from CLK (Pin 4) provides the clock signal for cascaded PCF8576s in the system.

External Clock

The condition for external clock is made by tying OSC (Pin 6) to V_{DD}; CLK (Pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100kHz, f_{CLK} should be chosen to be above 125kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{\text{SYNC}}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{OSC} when internal clock is used, or by the frequency applied to Pin 4 when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 200kΩ will result in the nominal frame frequency. In the power-saving mode, the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and, for the same frame frequency, R_{OSC} will be 1.2MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line Low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus, but no data loss occurs.

Display Latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs, and one column of the display RAM.

Shift Register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

Segment Outputs

The LCD drive section includes 40 segment outputs S0 to S39 (Pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required, the unused segment outputs should be left open.

Backplane Outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open. In the 1:3 multiplex drive mode BP3 carries the same signal as BP1; therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3, respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Figure 8). In multiplexed LCD applications, the segment data of the second, third, and fourth column of the display RAM are time-multiplexed with BP1, BP2, and BP3, respectively.

When display data is transmitted to the PCF8576, the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 9; the RAM filling organization depicted applies equally to other LCD types.

With reference to Figure 9, in the static drive mode, the eight transmitted data bits are placed in Bit 0 of eight successive display RAM addresses. In the 1:2 multiplex drive mode, the eight transmitted data bits are placed in Bits 0 and 1 of four successive display RAM addresses. In the 1:3 multiplex drive mode, these bits are placed in Bits 0, 1, and 2 of three successive addresses, with Bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1:4 multiplex drive mode, the eight transmitted data bits are placed in Bits 0, 1, 2, and 3 of two successive display RAM addresses.

Data Pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer, thereby observing the filling order shown in Figure 9. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1:2 multiplex drive mode), by three (1:3 multiplex drive mode) or by two (1:4 multiplex drive mode).

Sub-Address Counter

The storage of display data is conditioned by the contents of the sub-address counter. Storage is allowed to take place only when the contents of the sub-address counter

Table 3. LCD Frame Frequencies

PCF8576 MODE	RECOMMENDED R_{OSC} (kΩ)	f_{FRAME}	NOMINAL f_{FRAME} (Hz)
Normal mode	200	$f_{CLK}/2880$	64
Power-saving mode	1200	$f_{CLK}/480$	64

Table 4. Blinking Frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY f_{BLINK} (Hz)
Off			Blinking off
2Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0.5Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0.5

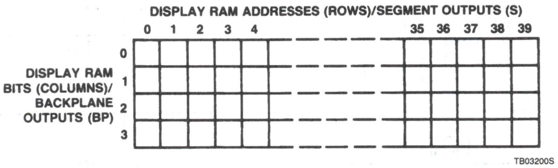

DISPLAY RAM ADDRESSES (ROWS)/SEGMENT OUTPUTS (S)
0 1 2 3 4
35 36 37 38 39
DISPLAY RAM BITS (COLUMNS)/ BACKPLANE OUTPUTS (BP)
0
1
2
3
TB03200S

Figure 8. Display RAM Bit Map Showing Direct Relationship Between Display RAM Addresses and Segment Outputs, and Between Bits in a RAM Word and Backplane Outputs

agree with the hardware sub-address applied to A0, A1, and A2 (Pins 7, 8, and 9). The sub-address counter value is defined by the DEVICE SELECT command. If the contents of the sub-address counter and the hardware sub-address do not agree, data storage is inhibited, but the data pointer is incremented as if data storage had taken place. The sub-address counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Sub-addressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1:3 multiplex mode).

Output Bank Selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1:4 multiplex, all RAM addresses of Bit 0 are the first to be selected. These are followed by the contents of Bit 1, Bit 2, and then Bit 3. Similarly, in 1:3 multiplex, Bits 0, 1, and 2 are selected sequentially. In 1:2 multiplex, Bits 0 then 1 are selected and; in the static mode, Bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of Bit 2 to be selected for display instead of Bit 0 contents. In the 1:2 drive mode, the contents of Bits 2 and 3 may be selected instead of Bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input Bank Selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in Bit 2 in static drive mode or in Bits 2 and 3 in 1:2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

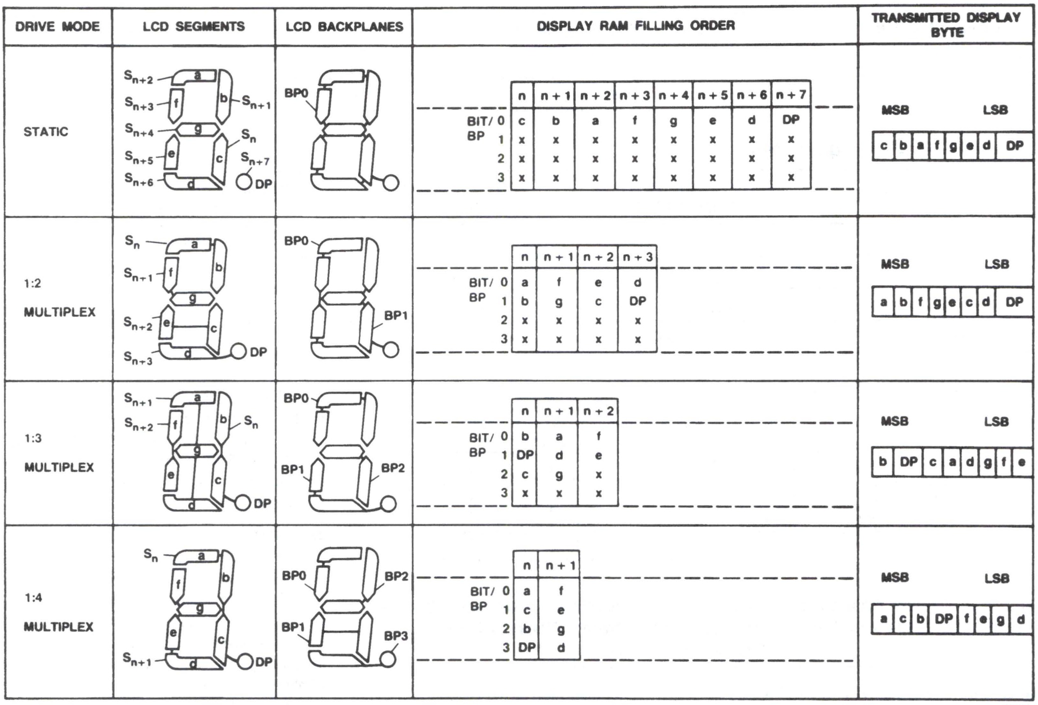
Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the Display Enable Bit E at the required rate using the MODE SET command.


DRIVE MODE
LCD SEGMENTS
LCD BACKPLANES
DISPLAY RAM FILLING ORDER
TRANSMITTED DISPLAY BYTE
STATIC
S_{n+2} a
S_{n+3} f
b S_{n+1}
S_{n+4} g
S_n
S_{n+5} e
c S_{n+7}
S_{n+6} d
DP
BP0
1:2 MULTIPLEX
S_n a
S_{n+1} f
b
g
S_{n+2} e
c
S_{n+3} d
DP
BP0
BP1
1:3 MULTIPLEX
S_{n+1} a
S_{n+2} f
b S_n
g
e
c
d
DP
BP0
BP1
BP2
1:4 MULTIPLEX
S_n a
f
b
g
e
c
S_{n+1} d
DP
BP0
BP2
BP1
BP3
TB03210S

STATIC

BIT/BP	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
0	c	b	a	f	g	e	d	DP
1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

Transmitted display byte (MSB … LSB): c b a f g e d DP

1:2 MULTIPLEX

BIT/BP	n	n+1	n+2	n+3
0	a	f	e	d
1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

Transmitted display byte (MSB … LSB): a b f g e c d DP

1:3 MULTIPLEX

BIT/BP	n	n+1	n+2
0	b	a	f
1	DP	d	e
2	c	g	x
3	x	x	x

Transmitted display byte (MSB … LSB): b DP c a d g f e

1:4 MULTIPLEX

BIT/BP	n	n+1
0	a	f
1	c	e
2	b	g
3	DP	d

Transmitted display byte (MSB … LSB): a c b DP f e g d

Figure 9. Relationships Between LCD Layout, Drive Mode, Display Data Transmitted Over the I²C Bus (x = Data Bit Unchanged)

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the High period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and Stop Conditions

Both data and clock lines remain High when the bus is not busy. A High-to-Low transition of the data line while the clock is High is defined as the start condition (S). A Low-to-High transition of the data line while the clock is High is defined as the stop condition (P).

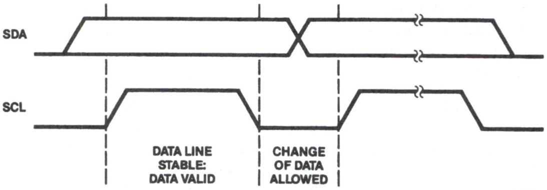

SDA
SCL
DATA LINE STABLE: DATA VALID
CHANGE OF DATA ALLOWED
WF18500S

Figure 10. Bit Transfer

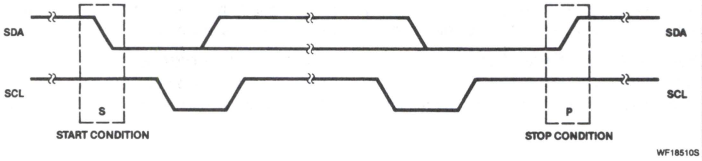

SDA
SCL
S
START CONDITION
P
STOP CONDITION
SDA
SCL
WF18510S

Figure 11. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a High level put on the bus by the transmitter, whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable Low during the High period of the acknowledge-related clock pulse; setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line High to enable the master to generate a stop condition.

PCF8576 I^{2}C Bus Controller

The PCF8576 acts as an I^{2}C slave receiver. It does not initiate I^{2}C bus transfers or transmit data to an I^{2}C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I^{2}C bus slave address, on the transferred command data, and on the hardware sub-address.

In single device applications, the hardware sub-address inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware sub-address 0. In multiple device applications. A0, A1, and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I^{2}C slave address have the same hardware sub-address.

In the power-saving mode, it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line Low until its internal operations are completed. This is known as the "clock synchronization feature" of the I^{2}C bus and serves to slow down fast transmitters. Data loss does not occur.

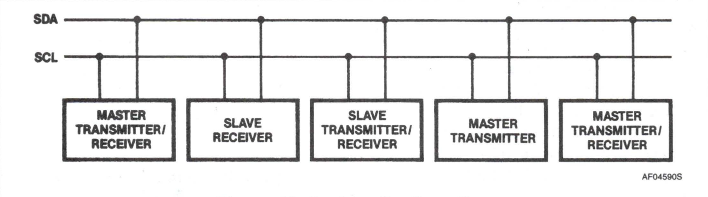

SDA
SCL
MASTER TRANSMITTER/ RECEIVER
SLAVE RECEIVER
SLAVE TRANSMITTER/ RECEIVER
MASTER TRANSMITTER
MASTER TRANSMITTER/ RECEIVER
AF04590S

Figure 12. System Configuration

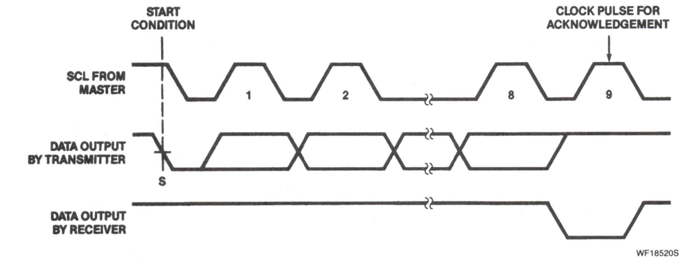

START CONDITION
CLOCK PULSE FOR ACKNOWLEDGEMENT
SCL FROM MASTER
1
2
8
9
DATA OUTPUT BY TRANSMITTER
S
DATA OUTPUT BY RECEIVER
WF18520S

Figure 13. Acknowledgement on the I^{2}C Bus

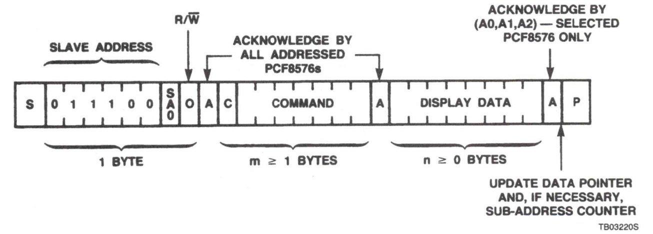

R/W̄
ACKNOWLEDGE BY (A0,A1,A2) — SELECTED PCF8576 ONLY
SLAVE ADDRESS
ACKNOWLEDGE BY ALL ADDRESSED PCF8576s
S
0 1 1 1 0 0
S A 0
0
A
C
COMMAND
A
DISPLAY DATA
A
P
1 BYTE
m ≥ 1 BYTES
n ≥ 0 BYTES
UPDATE DATA POINTER AND, IF NECESSARY, SUB-ADDRESS COUNTER
TB03220S

Figure 14. I^{2}C Bus Protocol

Input Filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I^{2}C Bus Protocol

Two I^{2}C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (Pin 10). Therefore, two types of PCF8576 can be distinguished on the same I^{2}C bus which allows:

a. up to 16 PCF8576s on the same I^{2}C bus for very large LCD applications;

b. the use of two types of LCD multiplex on the same I^{2}C bus.

The I^{2}C bus protocol is shown in Figure 14. The sequence is initiated with a start condition (S) from the I^{2}C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address, but all PCF8576s with the alternative SA0 level ignore the whole I^{2}C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the sub-address counter. Both data pointer and sub-address counter are automatically updated and the data is directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF 8576. After the last display byte, the I^{2}C bus master issues a stop condition (P).

Command Decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Figure 15). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data. The five commands available to the PCF8576 are defined in Table 5.

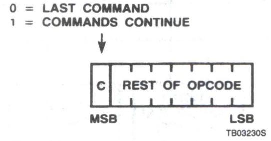


Figure 15. General Format of Command Byte

Table 5. Definition of PCF8576 Commands

COMMAND/OPCODE	OPTIONS				DESCRIPTION
MODE SET C 1 0 LP E B M1 M0	LCD drive mode	Bits	M1	M0	Defines LCD drive mode
	Static (1 BP)		0	1	
	1:2 MUX (2 BP)		1	0	
	1:3 MUX (3 BP)		1	1	
	1:4 MUX (4 BP)		0	0	
	LCD bias	Bit	B		Defines LCD bias configuration
	1/3 bias		0		
	1/2		1		
	Display status	Bit	E		Defines display status The possibility to disable the display allows implementation of blinking under external control
	Disabled (blank)		0		
	Enabled		1		
	Mode	Bit	LP		Defines power dissipation mode
	Normal mode		0		
	Power-saving mode		1		
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	Bits P5 P4 P3 P2 P1 P0				Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
	6-bit binary value of 0 to 39				
DEVICE SELECT C 1 1 0 0 A2 A1 A0	Bits	A0	A1	A2	Three bits of immediate data, bits A0 to A2, are transferred to the sub-address counter to define one of eight hardware sub-addresses
	3-bit binary value of 0 to 7				

Table 5. Definition of PCF8576 Commands (Continued)

COMMAND/OPCODE	OPTIONS			DESCRIPTION
BANK SELECT c 1 1 1 1 0 I 0	static	1:2 MUX	bit I	Defines input bank selection (storage of arriving display data)
	RAM bit 0	RAM bits 0, 1	0	
	RAM bit 2	RAM bits 2, 3	1	
	static	1:2 MUX	bit 0	Defines output bank selection (retrieval of LCD display data)
	RAM bit 0	RAM bits 0, 1	0	
	RAM bit 2	RAM bits 2, 3	1	
				The BANK SELECTION command has no effect in 1:3 and 1:4 multiplex drive modes
BLINK C 1 1 1 0 A BF1 BF0	blink frequency	bits BF1	BF0	Defines the blinking frequency
	off	0	0	
	2 Hz	0	1	
	1 Hz	1	0	
	0.5 Hz	1	1	
	blink mode		bit A	Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alteration of display RAM banks. Alteration blinking does not apply in 1:3 and 1:4 multiplex drive modes
	normal blinking		0	
	alteration blinking		1	

Display Controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded Operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I^{2}C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I^{2}C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs, but their backplane outputs are left open (Figure 16).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g., by noise in adverse electrical environment, or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Figure 17.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see application information.

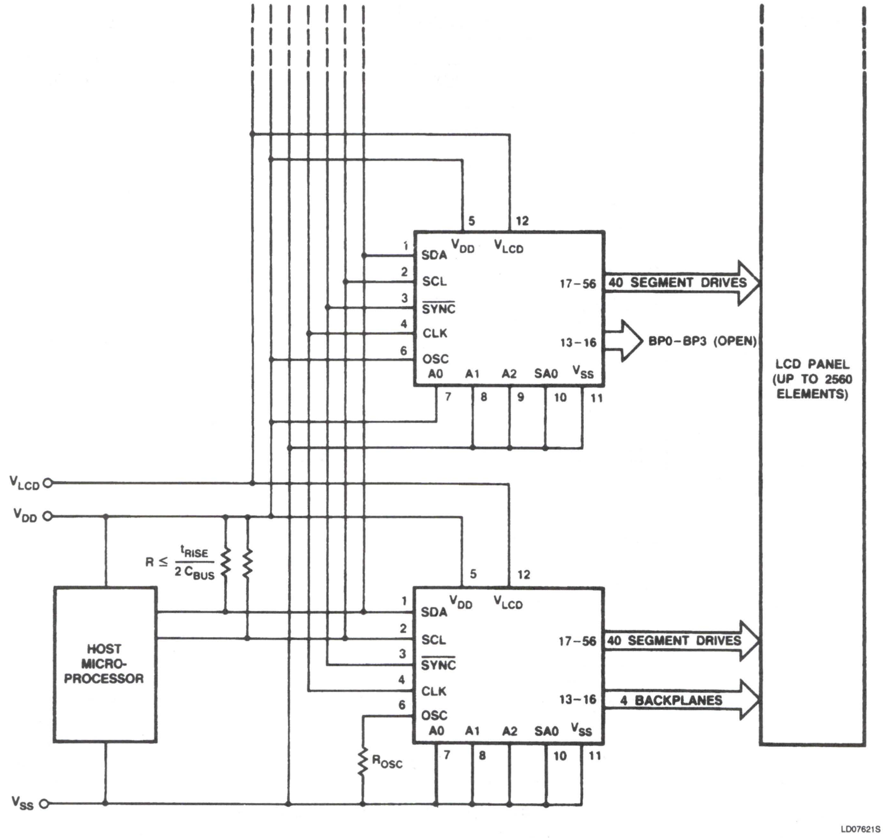
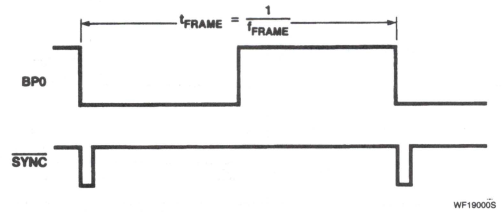
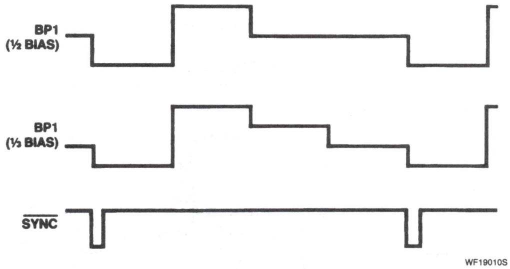

5
12
1
SDA
V_{DD}
V_{LCD}
2
SCL
17–56
40 SEGMENT DRIVES
3
SYNC
4
CLK
13–16
BP0–BP3 (OPEN)
6
OSC
A0 A1 A2 SA0 V_{SS}
7 8 9 10 11
LCD PANEL (UP TO 2560 ELEMENTS)
V_{LCD}
V_{DD}
$R \leq \frac{t_{RISE}}{2\,C_{BUS}}$
HOST MICRO-PROCESSOR
4 BACKPLANES
R_{OSC}
V_{SS}
LD07621S

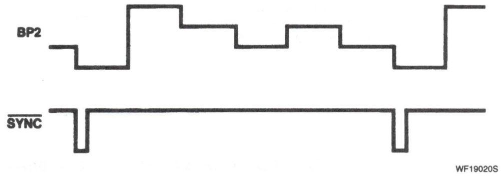
Figure 16. Cascaded PCF8576 Configuration


$t_{FRAME} = \frac{1}{f_{FRAME}}$
BP0
SYNC
WF19000S

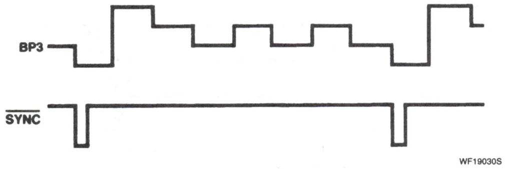
a. Static Drive Mode


BP1
(½ BIAS)
BP1
(⅓ BIAS)
SYNC
WF19010S

b. 1:2 Multiplex Drive Mode


BP2
SYNC
WF19020S

c. 1:3 Multiplex Drive Mode


BP3
SYNC
WF19030S

d. 1:4 Multiplex Drive Mode

Figure 17. Synchronization of the Cascade for the Various PCF8576 Drive Modes

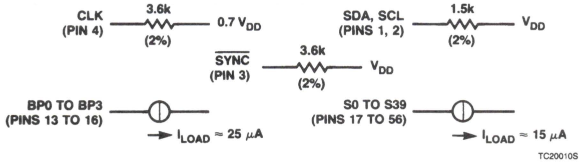

CLK
(PIN 4)
3.6k
(2%)
0.7 V_{DD}
SDA, SCL
(PINS 1, 2)
1.5k
(2%)
V_{DD}
SYNC
(PIN 3)
3.6k
(2%)
V_{DD}
BP0 TO BP3
(PINS 13 TO 16)
$I_{LOAD} \approx 25\ \mu A$
S0 TO S39
(PINS 17 TO 56)
$I_{LOAD} \approx 15\ \mu A$
TC20010S

Figure 18. Test Loads

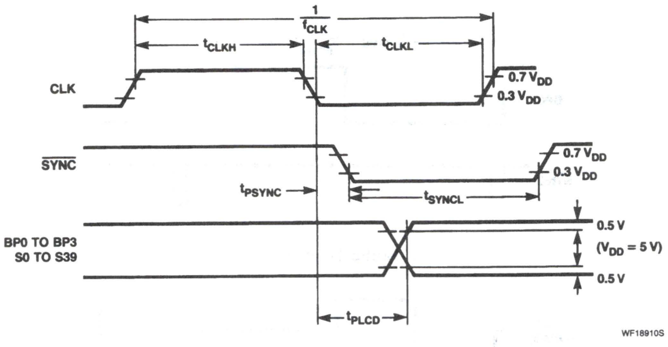

$\frac{1}{f_{CLK}}$
t_{CLKH}
t_{CLKL}
CLK
0.7 V_{DD}
0.3 V_{DD}
$\overline{SYNC}$
0.7 V_{DD}
0.3 V_{DD}
t_{PSYNC}
t_{SYNCL}
BP0 TO BP3
S0 TO S39
0.5 V
(V_{DD} = 5 V)
0.5 V
t_{PLCD}
WF18910S

Figure 19. Driver Timing Waveforms

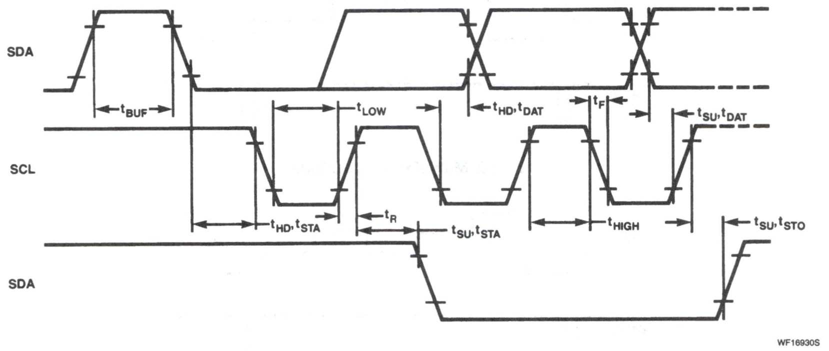

SDA
t_{BUF}
t_{LOW}
t_{HD}, t_{DAT}
t_F
t_{SU}, t_{DAT}
SCL
t_{HD}, t_{STA}
t_R
t_{SU}, t_{STA}
t_{HIGH}
t_{SU}, t_{STO}
SDA
WF16930S

Figure 20. I^2C Bus High-Speed Mode Timing Waveforms

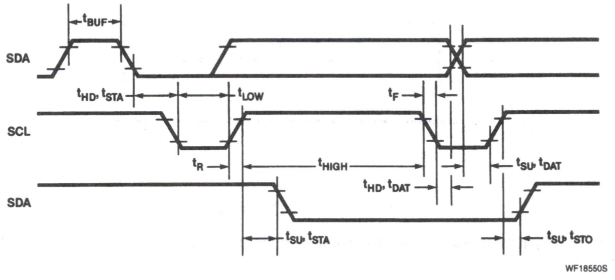

t_{BUF}
SDA
t_{HD}, t_{STA}
t_{LOW}
t_F
SCL
t_R
t_{HIGH}
t_{SU}, t_{DAT}
t_{HD}, t_{DAT}
SDA
t_{SU}, t_{STA}
t_{SU}, t_{STO}
WF18550S

Figure 21. I^2C Bus Low-Speed Mode Timing Waveforms

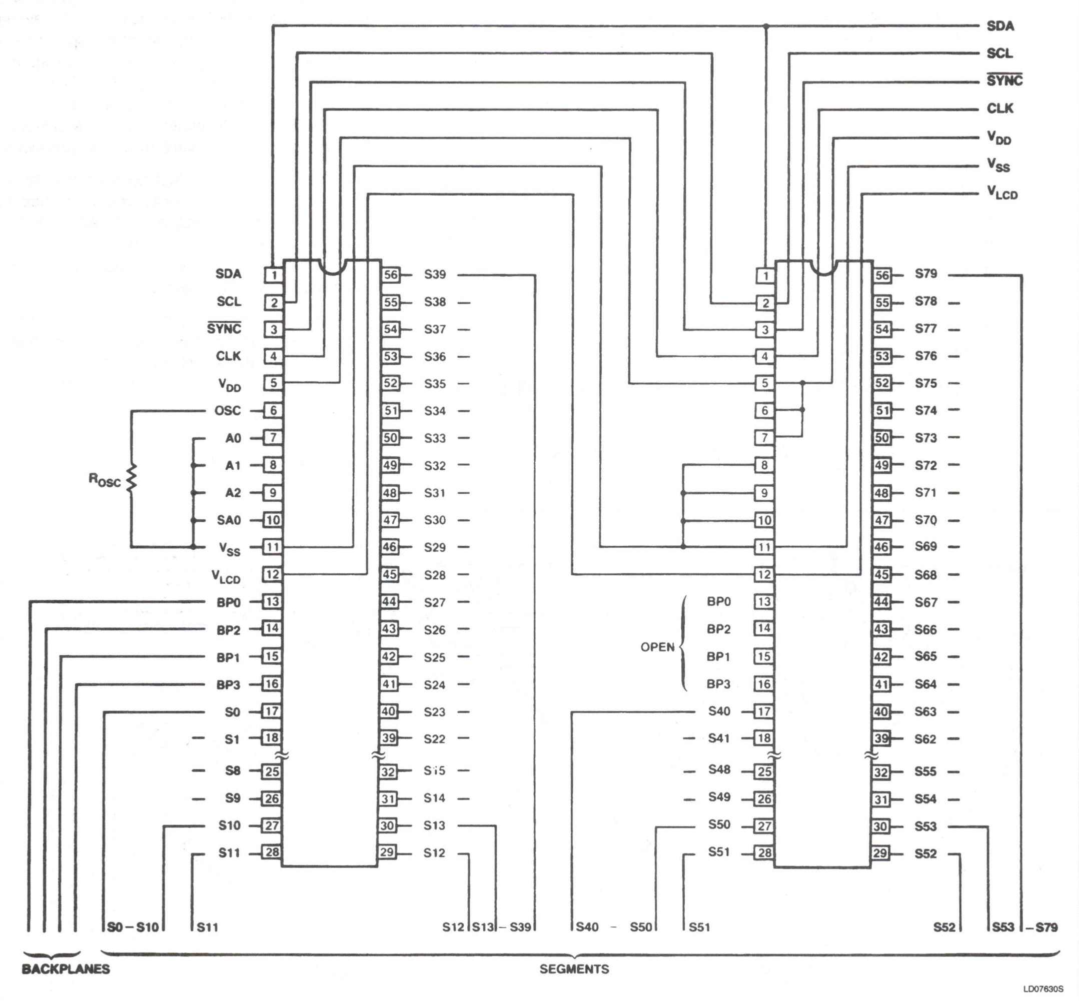

SDA
SCL
SYNC
CLK
V_{DD}
V_{SS}
V_{LCD}
SDA
SCL
SYNC
CLK
V_{DD}
OSC
A0
A1
A2
SA0
V_{SS}
V_{LCD}
BP0
BP2
BP1
BP3
S0
S1
S8
S9
S10
S11
R_{OSC}
S39
S38
S37
S36
S35
S34
S33
S32
S31
S30
S29
S28
S27
S26
S25
S24
S23
S22
S15
S14
S13
S12
OPEN
BP0
BP2
BP1
BP3
S40
S41
S48
S49
S50
S51
S79
S78
S77
S76
S75
S74
S73
S72
S71
S70
S69
S68
S67
S66
S65
S64
S63
S62
S55
S54
S53
S52
S0 – S10
S11
S12
S13 – S39
S40 – S50
S51
S52
S53 – S79
BACKPLANES
SEGMENTS
LD07630S

Figure 22. Single Plane Wiring of Packaged PCF8576s

APPLICATION INFORMATION

Chip-on-Glass Cascadability in Single Plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Figure 23). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, CLK, SCL, SDA, and $\overline{\text{SYNC}}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade center. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Universal LCD Driver for Low Multiplex Rates PCF8576

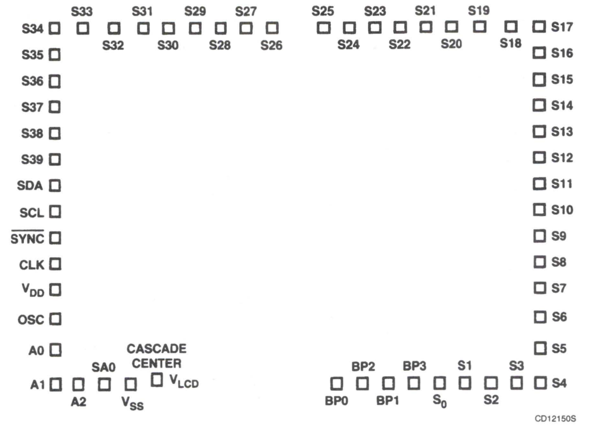

S33
S31
S29
S27
S25
S23
S21
S19
S34
S32
S30
S28
S26
S24
S22
S20
S18
S17
S35
S16
S36
S15
S37
S14
S38
S13
S39
S12
SDA
S11
SCL
S10
SYNC
S9
CLK
S8
V_{DD}
S7
OSC
S6
A0
CASCADE CENTER
S5
SA0
BP2
BP3
S1
S3
A1
V_{LCD}
S4
A2
V_{SS}
BP0
BP1
S_0
S2
CD12150S

Figure 23. PCF8576 Bonding Pad Layout

Figure 24 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA, and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2, and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress, and slave address.

Videlec is a joint venture of BBC Brown Boveri and Philips specializing in liquid crystal display technology to meet the requirements of original equipment manufacturers.

Videlec AG
Hardstrasse 5
Lenzburg CH5600
Switzerland.

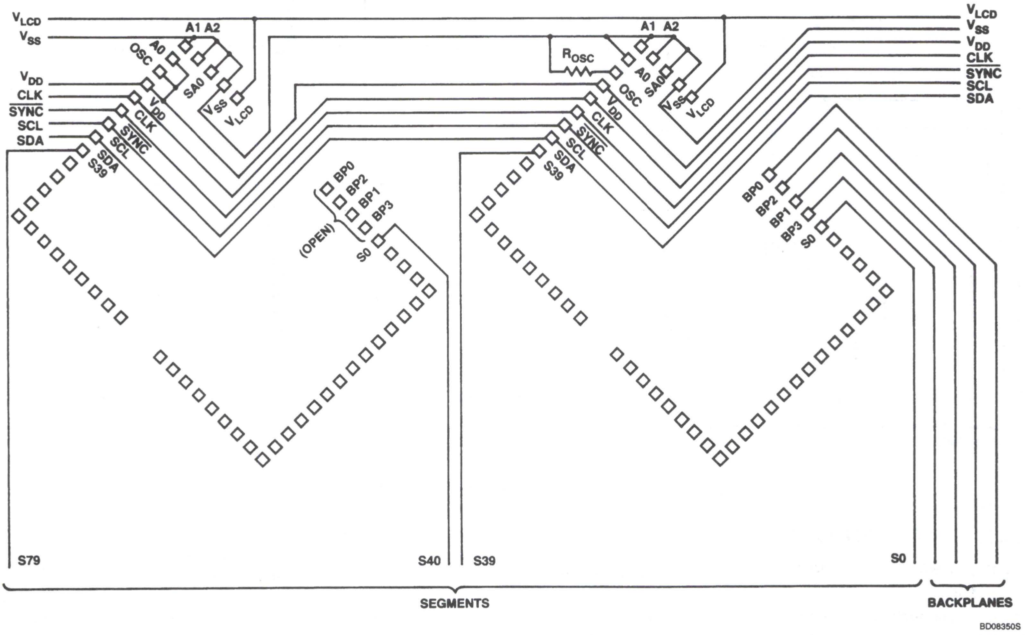

V_{LCD}
V_{SS}
V_{DD}
CLK
SYNC
SCL
SDA
A1 A2
A0
OSC
SA0
V_{SS}
V_{LCD}
V_{DD}
CLK
SYNC
SCL
SDA
S39
BP0
BP2
BP1
BP3
(OPEN)
S0
R_{OSC}
A1 A2
A0
OSC
SA0
V_{SS}
V_{LCD}
V_{DD}
CLK
SYNC
SCL
SDA
S39
BP0
BP2
BP1
BP3
S0
V_{LCD}
V_{SS}
V_{DD}
CLK
SYNC
SCL
SDA
S79
S40
S39
S0
SEGMENTS
BACKPLANES
BD08350S

Figure 24. Chip-on-Glass Application; Cascaded PCF8576s With Single-Plane Wiring (Viewed From Back of Chip)

Signetics

Linear Products

PCF8577

32-/64-Segment LCD Driver for Automotive

Product Specification

DESCRIPTION

The PCF8577 is a single-chip, silicon-gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I^{2}C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing, and display memory switching (direct drive mode).

FEATURES

- **Direct-/duplex-drive modes with up to 32-/64-segment LCD drive capability per device**
- **Operating supply voltage: 2.5 to 9V**
- **Low power consumption**
- **I^{2}C bus interface**
- **Optimized pinning for single plane wiring**
- **Single-pin built-in oscillator**
- **Auto-incremented loading across device sub-address boundaries**
- **Display memory switching in direct-drive mode**
- **May be used for I^{2}C bus output expander**
- **System expansion up to 256 segments**
- **Power-on reset sets all segments off (to blank)**

APPLICATIONS

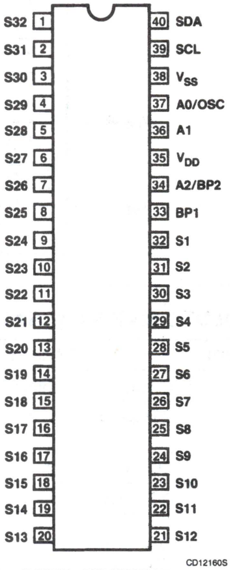
- **Telephony**
- **Car dashboards**
- **General instrumentation**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
40-Pin Plastic DIP (SOT-129)	−40°C to +85°C	PCF8577PN
40-Pin Plastic SO (VSO-40; SOT-158A)	−40°C to +85°C	PCF8577TD

PIN CONFIGURATION

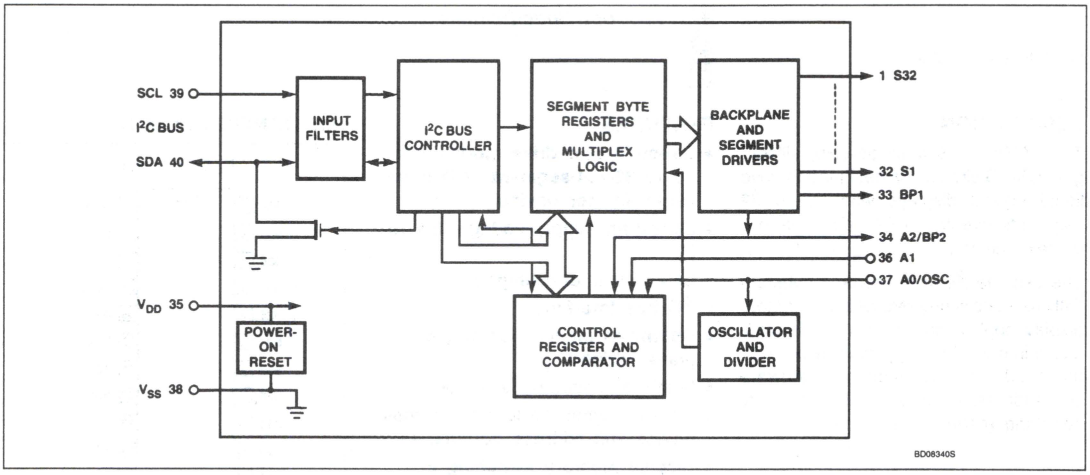
N, D Packages


S32 1
S31 2
S30 3
S29 4
S28 5
S27 6
S26 7
S25 8
S24 9
S23 10
S22 11
S21 12
S20 13
S19 14
S18 15
S17 16
S16 17
S15 18
S14 19
S13 20
40 SDA
39 SCL
38 V_{SS}
37 A0/OSC
36 A1
35 V_{DD}
34 A2/BP2
33 BP1
32 S1
31 S2
30 S3
29 S4
28 S5
27 S6
26 S7
25 S8
24 S9
23 S10
22 S11
21 S12
CD12160S

PIN NO.	SYMBOL	DESCRIPTION
Supply		
35	V_{DD}	Positive supply
38	V_{SS}	Negative supply
I^{2}C bus		
40	SDA	I^{2}C bus data line
39	SCL	I^{2}C bus clock line
Inputs		
36	A1	Hardware address line
37	A0/OSC	Hardware address line/oscillator pin
Outputs		
1 – 32	S1 – S32	Segment outputs
Input – Output		
34	A2/BP2	Hardware address line/cascade sync input/backplane output
33	BP1	Cascade sync input/backplane output

32-/64-Segment LCD Driver for Automotive PCF8577

BLOCK DIAGRAM


SCL 39
I²C BUS
SDA 40
INPUT FILTERS
I²C BUS CONTROLLER
SEGMENT BYTE REGISTERS AND MULTIPLEX LOGIC
BACKPLANE AND SEGMENT DRIVERS
1 S32
32 S1
33 BP1
34 A2/BP2
36 A1
37 A0/OSC
VDD 35
POWER-ON RESET
VSS 38
CONTROL REGISTER AND COMPARATOR
OSCILLATOR AND DIVIDER
BD08340S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to 11	V
V_I	Voltage on any pin	$V_{SS} - 0.8$ to $V_{DD} + 0.8$	V
$\pm I_I$	DC input current	20	mA
$\pm I_O$	DC output current	25	mA
$\pm I_{DD}$, I_{SS}	V_{DD} or V_{SS} current	50	mA
P_{TOT}	Power dissipation per package	500[1]	mW
P_D	Power dissipation per output	100	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Derate 7.7mW/°C when $T_A > 60°C$.

32-/64-Segment LCD Driver for Automotive PCF8577

DC AND AC ELECTRICAL CHARACTERISTICS $V_{DD} = 2.5$ to 9V; $V_{SS} = 0V$; $T_A = -40°C$ to $+85°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Supply voltage	2.5		9.0	V
I_{DD}	Supply current at $f_{SCL} = 100kHz$, no load, $R_{OSC} = 1M\Omega$			250	μA
V_{REF}	Power-on reset level[1]	0.9	1.3	2.0	V
	Input SCL; input/output SDA				
V_{IL}	input voltage Low	0		0.8	V
V_{IH}	input voltage High	2.0		9.0	V
I_{OL}	output current Low at $V_{OL} = 0.4V$	3.0			mA
I_{OH}	output leakage current High at $V_{OH} = V_{DD}$			100	nA
t_{SW}	tolerable spike width on bus			100	ns
C_I	input capacitance at $V_I = V_{SS}$			7	pF
I_I	A1 input leakage current at $V_I = V_{SS}$ or V_{DD}			100	nA
I_I	A2/BP2 input current at $V_I = V_{DD}$		5.0		μA
$\pm I_I$	A0/OSC input current at $V_I = V_{SS}$ or V_{DD}		5.0		μA
$\pm V_{BP}$	DC component of LCD driver		20		mV
C_{SX}	Segment loads			5	nF
R_{SX}		1			MΩ
I_{OL}	Segment output current at $V_{OL} = 0.4V$; $V_{DD} = 5V$	0.3			mA
$-I_{OH}$	Segment output current at $V_{OH} = V_{DD} - 0.4V$; $V_{DD} = 5V$	0.3			mA
C_{BP}	Backplane load (direct drive)			50	nF
R_{BP}		100			kΩ
C_{BP}	Backplane loads (duplex drive)			35	nF
R_{BP}		100			kΩ
t_R, t_F	Rise and fall times ($V_{BP} - V_{SX}$) at maximum load			200	μs
f_{LCD}	Display frequency at $C_{OSC} = 680pF$; $R_{OSC} = 1M\Omega$	65	90	120	Hz

NOTE:

1. The power-on reset circuit resets the I^2C bus logic with $V_{DD} < V_{REF}$.

32-/64-Segment LCD Driver for Automotive

PCF8577

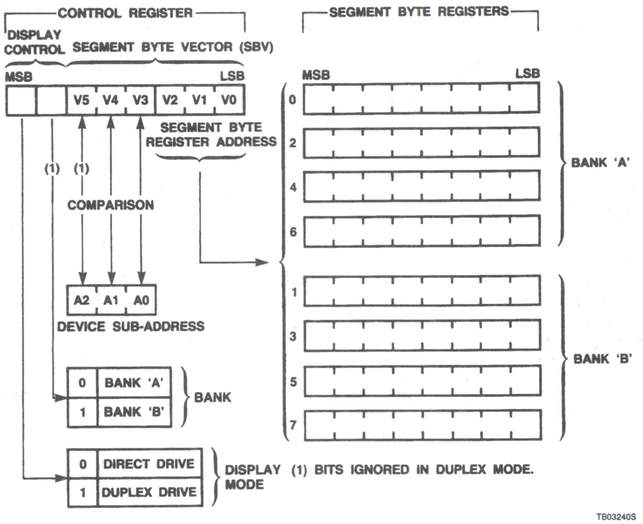


Figure 1. PCF8577 Register Organization

FUNCTIONAL DESCRIPTION

Hardware Sub-Address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2, respectively, to reduce pinout requirements.

A0/OSC	Line A0 is defined as Low (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as High (logic 1) when connected to V_{DD}.
A1	Line A1 must be defined as Low (logic 0) or as High (logic 1) by connection to V_{SS} or V_{DD}, respectively.
A2/BP2	In the direct drive mode, the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as Low (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as High (logic 1) when connected to V_{DD}.

In the duplex drive mode, the second backplane signal BP2 is required, and the A2 signal is undefined. In this mode, device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577, the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode, each PCF8577 is synchronized from the backplane signal(s).

User-Accessible Registers

There are nine user-accessible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even-numbered segment byte registers is called BANK A. Odd-numbered segment byte registers are called BANK B.

All PCF8577 have the same slave address (see Figure 12). All devices load the second byte into the control register, and each device maintains an identical copy of the control byte in the control register at all times (see I^2C bus protocol Figure 13).

The control register is shown in more detail in Figure 1. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1, and A0. If they are the same, then the device is enabled for loading; if not, the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct- or duplex-drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-Incremented Loading

After each segment byte is loaded, the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct-Drive Mode

The PCF8577 is set to the direct-drive mode by loading the MODE control bit with logic 0. In this mode, only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct-drive mode, the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded regardless of which bank is being displayed. Direct-drive output waveforms are shown in Figure 2.

Duplex Mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode, a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore, A2 and its equivalent SBV Bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

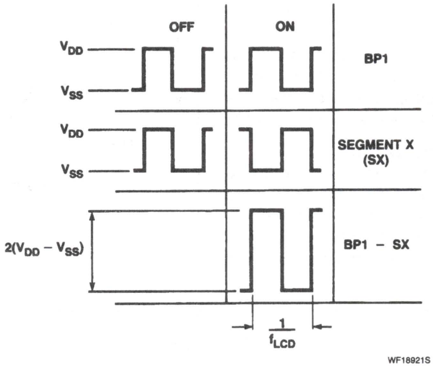
Duplex mode output waveforms are shown in Figure 3.

CHARACTERISTICS OF THE I^{2}C BUS

The I^{2}C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

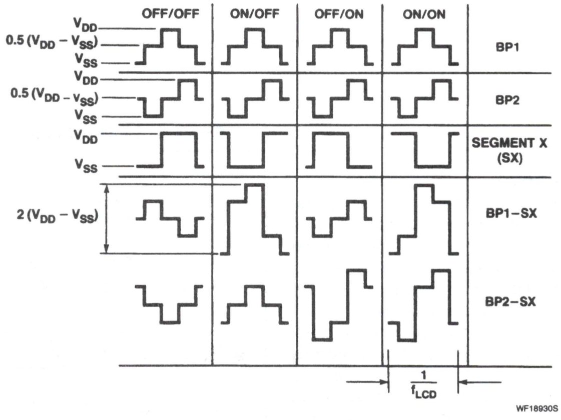
Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the High period of the clock pulse as changes in the data line at this time will be interpreted as control signals.


OFF
ON
V_DD
V_SS
BP1
V_DD
V_SS
SEGMENT X (SX)
2(V_DD − V_SS)
BP1 − SX
1/f_LCD
WF18921S

NOTES:
$V_{ON} = V_{DD} - V_{SS}$
$V_{OFF} = 0$

Figure 2. Direct-Drive Mode Display Output Waveforms


OFF/OFF
ON/OFF
OFF/ON
ON/ON
V_DD
0.5 (V_DD − V_SS)
V_SS
BP1
V_DD
0.5 (V_DD − V_SS)
V_SS
BP2
V_DD
V_SS
SEGMENT X (SX)
2 (V_DD − V_SS)
BP1−SX
BP2−SX
1/f_LCD
WF18930S

NOTES:
$V_{ON} = 0.79\ (V_{DD} - V_{SS})$
$V_{OFF} = 0.35\ (V_{DD} - V_{SS})$
$\frac{V_{ON}}{V_{OFF}} = 2.26$

Figure 3. Duplex Mode Display Output Waveforms

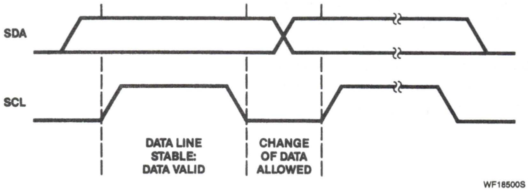

SDA
SCL
DATA LINE STABLE: DATA VALID
CHANGE OF DATA ALLOWED
WF18500S

Figure 4. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain High when the bus is not busy. A High-to-Low transition of the data line while the clock is High is defined as the start condition (S). A Low-to-High transition of the data line while the clock is High is defined as the stop condition (P).

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

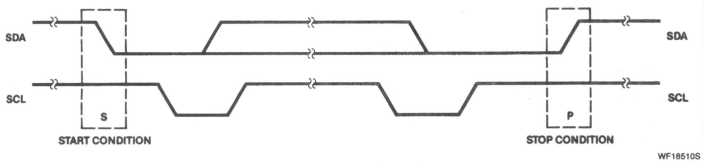

SDA
SCL
S
START CONDITION
SDA
SCL
P
STOP CONDITION
WF18510S

Figure 5. Definition of Start and Stop Conditions

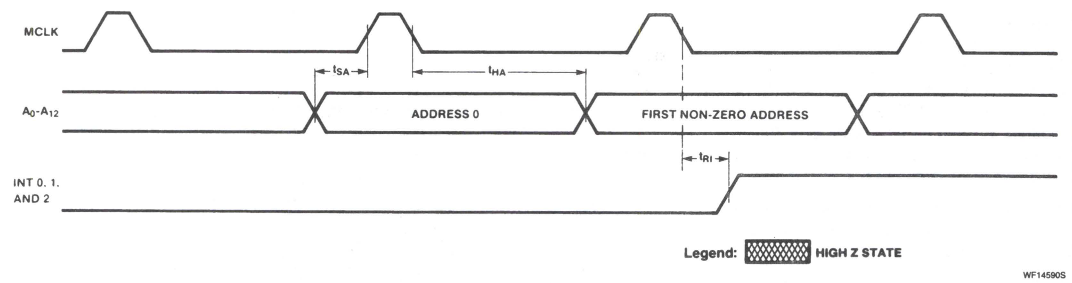

MCLK
t_{SA}
t_{HA}
A_0-A_{12}
ADDRESS 0
FIRST NON-ZERO ADDRESS
t_{RI}
INT 0, 1, AND 2
Legend: ▩ HIGH Z STATE
WF14590S

Figure 6. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a High level put on the bus by the transmitter, whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable Low during the High period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line High to enable the master to generate a stop condition.

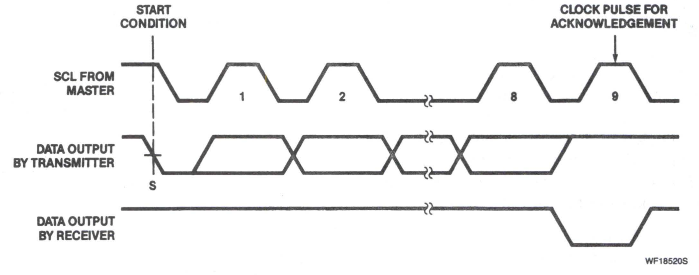

START CONDITION
CLOCK PULSE FOR ACKNOWLEDGEMENT
SCL FROM MASTER
1
2
8
9
DATA OUTPUT BY TRANSMITTER
S
DATA OUTPUT BY RECEIVER
WF18520S

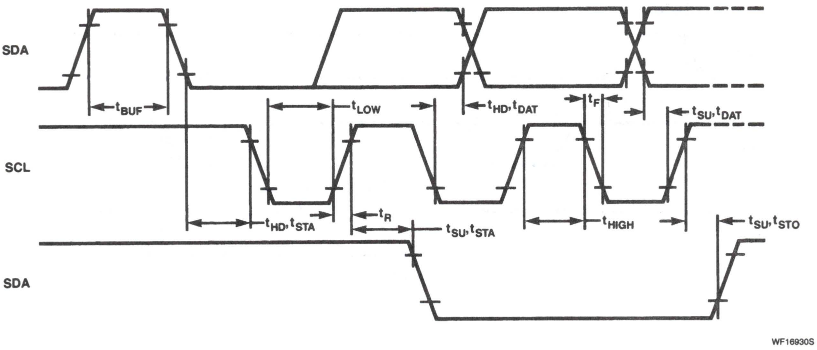
Figure 7. Acknowledgement on the I^2C Bus

Timing Specifications

Within the I²C bus specifications, a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes. The timing requirements are as follows:

High-Speed Mode

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 8.

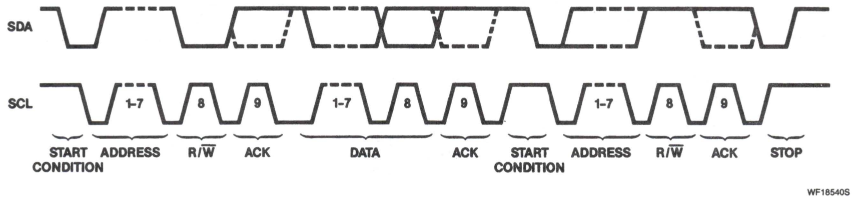

SDA
SCL
SDA
t_{BUF}
t_{LOW}
t_{HD}, t_{DAT}
t_F
t_{SU}, t_{DAT}
t_{HD}, t_{STA}
t_R
t_{SU}, t_{STA}
t_{HIGH}
t_{SU}, t_{STO}
WF16930S

Where:

t_{BUF}	$t \geqslant t_{LOW\ min}$	The minimum time the bus must be free before a new transmission can start
$t_{HD};\ t_{STA}$	$t \geqslant t_{HIGH\ min}$	Start condition hold time
t_{LOWmin}	4.7µs	Clock Low period
$t_{HIGHmin}$	4µs	Clock High period
$t_{SU};\ t_{STA}$	$t \geqslant t_{LOW\ min}$	Start condition setup time; only valid for repeated start code
$t_{HD};\ t_{DAT}$	$t \geqslant 0\mu s$	Data hold time
$t_{SU};\ t_{DAT}$	$t \geqslant 250ns$	Data setup time
t_R	$t \leqslant 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300ns$	Fall time of both the SDA and SCL line
$t_{SU};\ t_{STO}$	$t \geqslant t_{LOW\ min}$	Stop condition setup time

NOTE:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 8. Timing of the High-Speed Mode


SDA
SCL
1-7
8
9
1-7
8
9
1-7
8
9
START CONDITION
ADDRESS
R/W̄
ACK
DATA
ACK
START CONDITION
ADDRESS
R/W̄
ACK
STOP
WF18540S

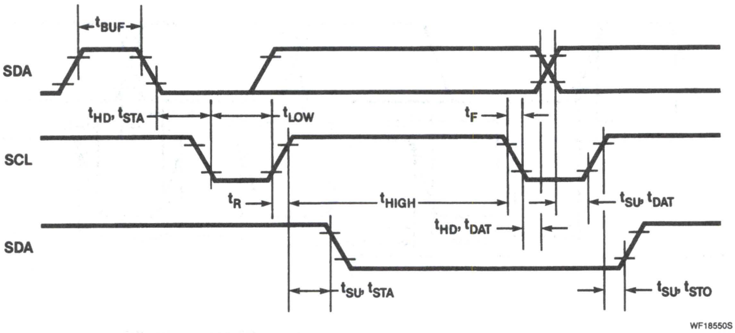
Where:

Clock t_{LOWmin}	4.7µs
$t_{HIGHmin}$	4µs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (Low-to-High)
Maximum number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Figure 9. Complete Data Transfer in the High-Speed Mode

32-/64-Segment LCD Driver for Automotive PCF8577

Low-Speed Mode
Masters generate a bus clock with a maximum frequency of 2kHz; a minimum Low period of 105µs and a minimum High period of 365µs. The mark-to-space ratio is 1:3 Low-to-High. Detailed timing is shown in Figure 10.

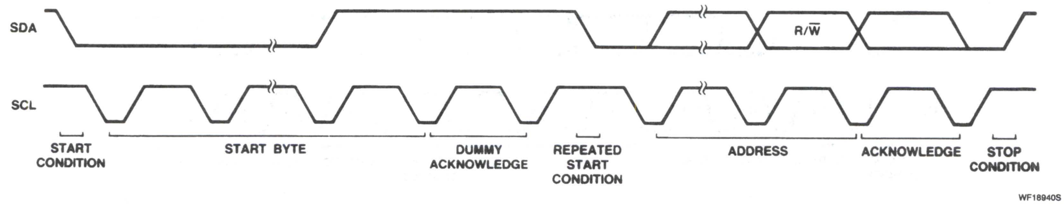

t_{BUF}
SDA
t_{HD}, t_{STA}
t_{LOW}
t_F
SCL
t_R
t_{HIGH}
t_{SU}, t_{DAT}
t_{HD}, t_{DAT}
SDA
t_{SU}, t_{STA}
t_{SU}, t_{STO}
WF18550S

Where:

t_{BUF}	$t \geq 105\mu s$ ($t_{LOW\,MIN}$)
$t_{HD;}\ t_{STA}$	$t \geq 365\mu s$ ($t_{HIGH\,MIN}$)
t_{LOW}	$130\mu s \pm 25\mu s$
t_{HIGH}	$390\mu s \pm 25\mu s$
$t_{SU;}\ t_{STA}$	$130\mu s \pm 25\mu s$*
$t_{HD;}\ t_{DAT}$	$t \geq 0\mu s$
$t_{SU;}\ t_{DAT}$	$t \geq 250ns$
t_R	$t \leq 1\mu s$
t_F	$t \leq 300ns$
$t_{SU;}\ t_{STO}$	$130\mu s \pm 25\mu s$

NOTE:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see High-Speed Mode.
* Only valid for repeated start code.

Figure 10. Timing of the Low-Speed Mode


SDA
R/W̄
SCL
START CONDITION
START BYTE
DUMMY ACKNOWLEDGE
REPEATED START CONDITION
ADDRESS
ACKNOWLEDGE
STOP CONDITION
WF18940S

Where:

Clock t_{LOWmin}	$130\mu s \pm 25\mu s$
$t_{HIGHmin}$	$390\mu s \pm 25\mu s$
Mark-to-space ratio	1:3 (Low-to-High)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	Not allowed
Acknowledge clock bit	Must be provided by master

Figure 11. Complete Data Transfer in the Low-Speed Mode

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave Address

The slave address for PCF8577 is shown in Figure 12.

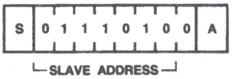

S
0 1 1 1 0 1 0 0
A
SLAVE ADDRESS
TB03250S

Figure 12. PCF8577 Slave Address

I²C Bus Protocol

The PCF8577 I²C bus protocol is shown in Figure 13.

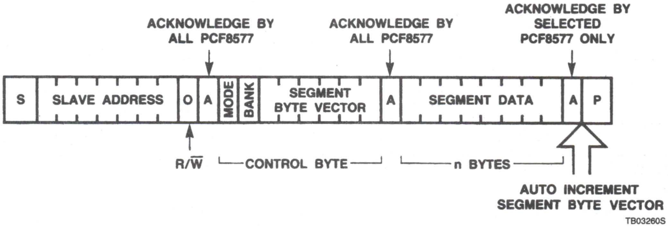

ACKNOWLEDGE BY ALL PCF8577
ACKNOWLEDGE BY ALL PCF8577
ACKNOWLEDGE BY SELECTED PCF8577 ONLY
S
SLAVE ADDRESS
O
A
MODE
BANK
SEGMENT BYTE VECTOR
A
SEGMENT DATA
A
P
R/W̄
CONTROL BYTE
n BYTES
AUTO INCREMENT SEGMENT BYTE VECTOR
TB03260S

Figure 13. I²C Bus Protocol

The PCF8577 is a slave receiver and has a fixed slave address (Figure 12). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge, the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data, only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct-drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0, even bytes (BANK A) are displayed; if BANK is set to logic 1, odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct-drive mode.

Table 1. Segment Byte — Segment Driver Mapping in the Direct-Drive Mode

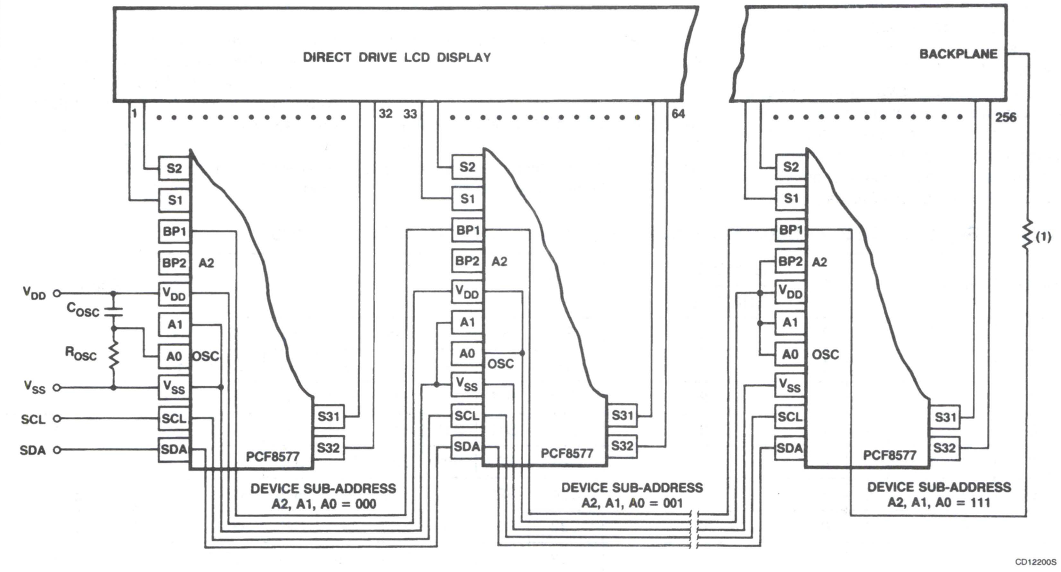
MODE	BANK	V2	V1	V0	SEGMENT	BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
					REGISTER										
0	0	0	0	0	0		S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1		S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2		S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3		S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4		S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5		S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6		S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7		S32	S31	S30	S29	S28	S27	S26	S25	BP1

NOTES:
Mapping example: Bit 0 of Register 7 controls the LCD segment S25 if BANK bit is a logic 1.
Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2. Segment Byte — Segment Driver Mapping in the Duplex Mode

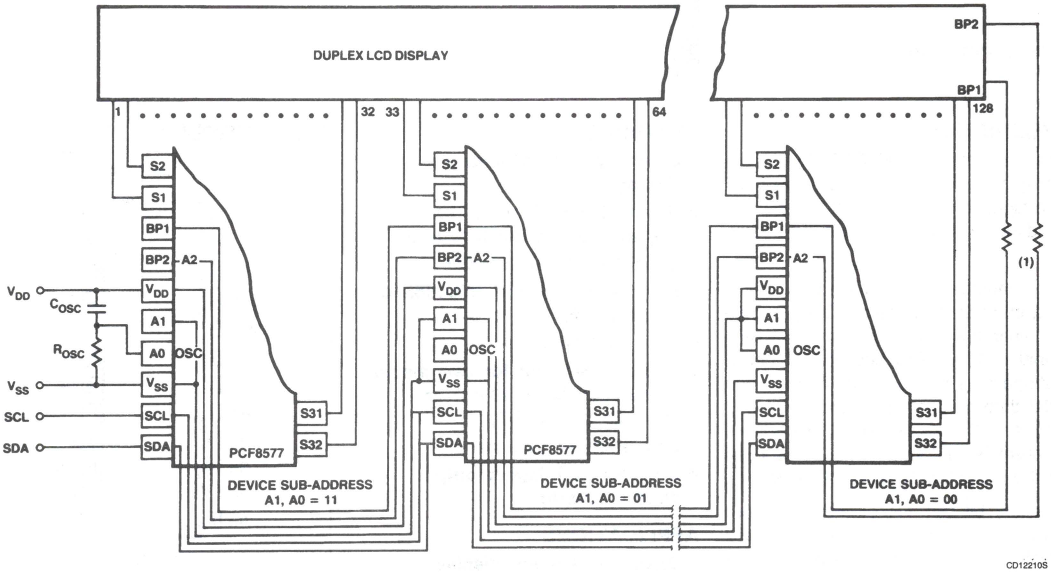
MODE	BANK	V2	V1	V0	SEGMENT REGISTER	BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
1	x	0	0	0	0		S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1		S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2		S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3		S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4		S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5		S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6		S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7		S32	S31	S30	S29	S28	S27	S26	S25	BP2

NOTES:
X = don't care.
Mapping example: Bit 7 of Register 5 controls the LCD segment S24/BP2.


DIRECT DRIVE LCD DISPLAY
BACKPLANE
1
32
33
64
256
S2
S1
BP1
BP2
A2
V_{DD}
A1
A0
OSC
V_{SS}
SCL
SDA
S31
S32
PCF8577
V_{DD}
C_{OSC}
R_{OSC}
V_{SS}
SCL
SDA
(1)
DEVICE SUB-ADDRESS
A2, A1, A0 = 000
DEVICE SUB-ADDRESS
A2, A1, A0 = 001
DEVICE SUB-ADDRESS
A2, A1, A0 = 111
CD12200S

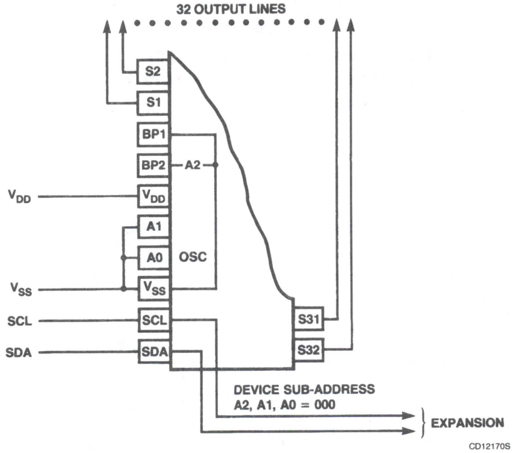
NOTE:
1. The series resistance of the display backplane must be greater than 1kΩ.

Figure 14. Direct-Drive Display; Expansion to 256 Segments Using Eight PCF8577s


DUPLEX LCD DISPLAY
BP2
BP1
1
32
33
64
128
S2
S1
BP1
BP2
A2
VDD
A1
A0
OSC
VSS
SCL
SDA
S31
S32
PCF8577
VDD
COSC
ROSC
VSS
SCL
SDA
DEVICE SUB-ADDRESS A1, A0 = 11
DEVICE SUB-ADDRESS A1, A0 = 01
DEVICE SUB-ADDRESS A1, A0 = 00
(1)
CD12210S

NOTE:
1. The series resistances of the display backplanes must be greater than 1kΩ.

Figure 15. Duplex Display; Expansion to 2 × 128 Segments Using Four PCF8577s


32 OUTPUT LINES
S2
S1
BP1
BP2
A2
VDD
A1
A0
OSC
VSS
SCL
SDA
S31
S32
VDD
VSS
SCL
SDA
DEVICE SUB-ADDRESS A2, A1, A0 = 000
EXPANSION
CD12170S

NOTES:
1. MODE bit must always be set to 0 (direct-drive).
2. BANK switching is permitted.
3. BP1 must always be connected to V_{SS} and A0/OSC must be connnected to either V_{DD} or V_{SS} (no LCD modulation).

Figure 16. Use of PCF8577 as 32-Bit Output Expander in I²C Bus Application

Signetics

SAA1060

LED Display/Interface Circuit

Product Specification

DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial-to-parallel decoder.

Data transmission is initiated by means of a burst of clock pulse (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading-zero. This allows different bus information to be supplied on the same bus lines for other circuits.

The last bit (Bit 17) of the data word contains the information that determines which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are NPN transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 × 2 segments can be connected in parallel.

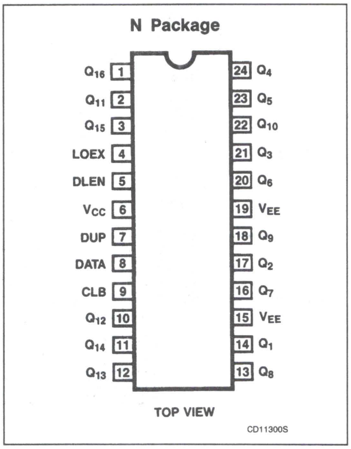
FEATURES

- **Driving 7-, 14-, 16-segment displays**
- **Driving linear displays, bar graph displays for analog functions**
- **Serial-to-parallel decoder**
- **Bus control for the selection of 18-bit words**
- **2 × 16-bit latch**
- **Duplex operation for two modes of output: static (16-bit) or dynamic (2 × 16-bit)**
- **Data transfer control**
- **2 outputs for higher output current (80mA)**

APPLICATIONS

- **Driving 7-segment displays**
- **Driving 14-segment displays**
- **Driving linear displays, e.g., pointer, bar graph**
- **Static output of switch functions**
- **Digital-to-analog converter, with external R-2R network**
- **Extension of the number of outputs for microprocessors or microcomputers**

PIN CONFIGURATION



ORDERING INFORMATION

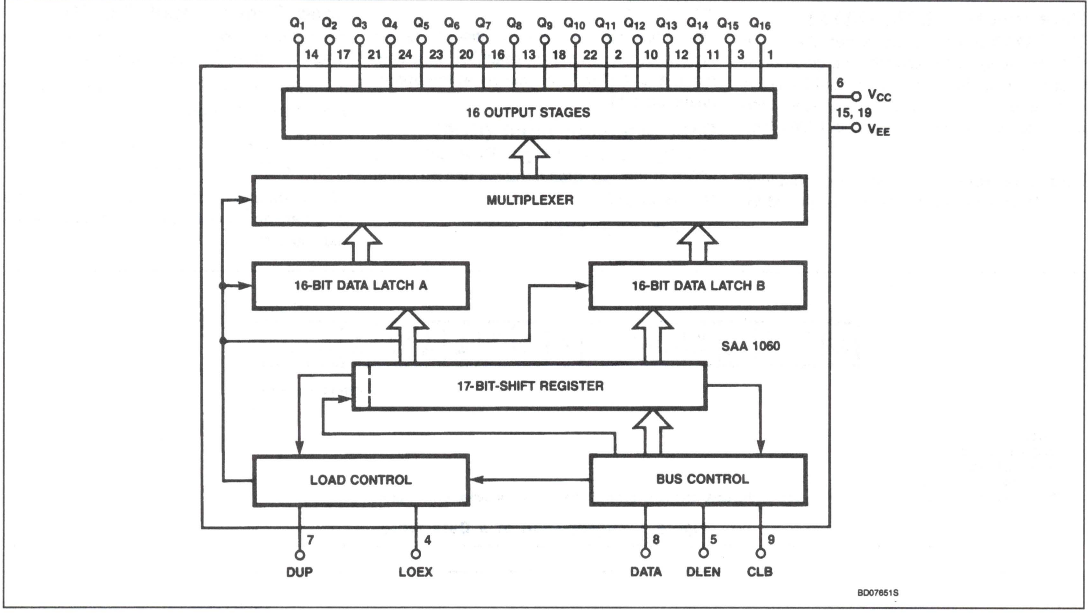
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP, (SOT-101A)	−20°C to +85°C	SAA1060N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.3 to +7	V
P_{TOT}	Total power dissipation	900	mW
T_A	Operating ambient temperature range	-20 to +80	°C
T_{STG}	Storage temperature range	-65 to +150	°C

LED Display/Interface Circuit SAA1060

BLOCK DIAGRAM


Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9 Q_{10} Q_{11} Q_{12} Q_{13} Q_{14} Q_{15} Q_{16}
14 17 21 24 23 20 16 13 18 22 2 10 12 11 3 1
6
V_{CC}
15, 19
V_{EE}
16 OUTPUT STAGES
MULTIPLEXER
16-BIT DATA LATCH A
16-BIT DATA LATCH B
SAA 1060
17-BIT-SHIFT REGISTER
LOAD CONTROL
BUS CONTROL
7
4
8
5
9
DUP
LOEX
DATA
DLEN
CLB
BD07651S

DC ELECTRICAL CHARACTERISTICS $V_{EE} = 0$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	V_{CC} (V)	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage			4	5	6	V
I_{CC}	Supply current	5			60		mA
	Inputs DATA, CLB, DLEN, LOEX						
V_{IH}	Input voltage HIGH	5		2		5	V
V_{IL}	Input voltage LOW	5				1	V
$-I_{IL}$	Input current LOW	5	$V_I = 0$			20	μA
f_I	Maximum input frequency	5			50		kHz
	Input DUP						
V_{IH}	Input voltage HIGH	5		0.8		12	V
V_{IL}	Input voltage LOW	5		−6		0.4	V
I_{IH}	Input current HIGH	5		0.01		12	mA
f_I	Maximum input frequency	5			50		kHz
	Outputs Q_1 to Q_7, Q_9 to Q_{15}						
V_{OH}	Output voltage HIGH	5	$I_{QH} = 0$			16.8	V
V_{OL}	Output voltage LOW	5	$I_{QL} = 40mA$			0.5	V
	Output current LOW						
I_{OL}	Duplex mode	5	Peak value at sinusoidal voltage			60	mA
I_{QL}	DC mode	5			20	40	mA
	Outputs Q_8 and Q_{16}						
V_{OH}	Output voltage HIGH	5	$I_{QL} = 0$			16.8	V
V_{OL}	Output voltage LOW	5	$I_{QL} = 80mA$			0.5	V
	Output current LOW						
I_{OL}	Duplex mode	5	Peak value at sinusoidal voltage			120	mA
I_{QL}	DC mode	5			40	80	mA

OPERATION DESCRIPTION

Data Inputs (DLEN, DATA)

The SAA1060 serially processes the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Figure 2).

Each data word must start with a leading-zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading-zero.

The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data Selection Input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents

1 = latch B contents

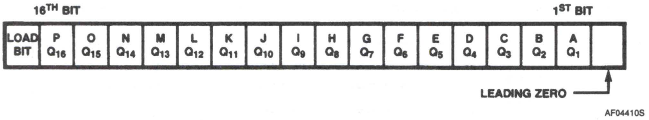
Load Control Input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e., output synchronized with the duplex signal

1 = DC mode, i.e., output direct from the by DUP selected data latch.

When operating in duplex mode at 50Hz, the time between two data words to be transmitted must be > 21ms.


16TH BIT
1ST BIT
LOAD BIT
P Q16
O Q15
N Q14
M Q13
L Q12
K Q11
J Q10
I Q9
H Q8
G Q7
F Q6
E Q5
D Q4
C Q3
B Q2
A Q1
LEADING ZERO
AF04410S

NOTES:
Condition for 17th bit:
0 = load data latch B
1 = load data latch A
The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

Figure 1. Organization of a Data Word

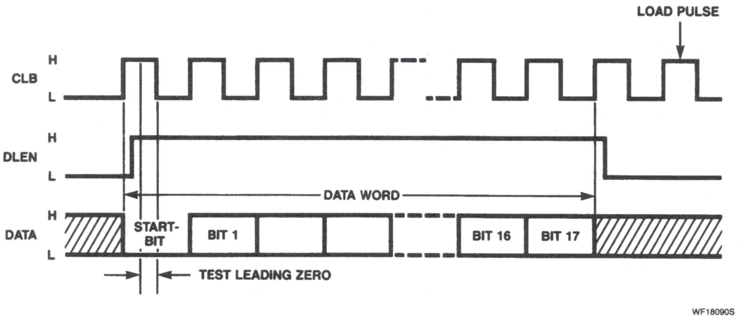

LOAD PULSE
CLB
H
L
DLEN
H
L
DATA WORD
DATA
H
L
START-BIT
BIT 1
BIT 16
BIT 17
TEST LEADING ZERO
WF18090S

Figure 2. Pulse Diagram of the 16-Bit Data Transmission

Signetics

SAA1061
Output Port Expander

Product Specification

Linear Products

DESCRIPTION

The SAA1061 is an NMOS output port expander circuit, which converts serial input data into parallel output information. The IC is used in combination with a microcomputer.

The SAA1061 is an addressable output port expander for use in microcomputer-controlled systems. It converts serial input data into parallel output information. The circuit comprises a CBUS receiver, logic to check input format, a 16-bit serial/parallel converter, latches and drivers for the parallel outputs.

The data is transmitted via the 3-line CBUS from the microcomputer. If the data transmission is valid, the data is transferred by a load pulse via the latch to the driver output. Each data transmission is checked for word length (18-bit) by the on-chip word format control circuitry. This allows different bus information to be supplied on the same bus lines for other circuits.

The address inputs A_0 and A_1 determine four address possibilities. A data transmission only takes place if the programmed addresses correspond with the address bits S0 and S1.

FEATURES

- **Bus control for the selection of 18-bit words**
- **16-bit latch and low-ohmic driver outputs**
- **Pin compatible with the SAA1060, except the SAA1061 has no duplex mode**
- **Address selection inputs; up to four SAA1061 circuits can be operated from a common CBUS**

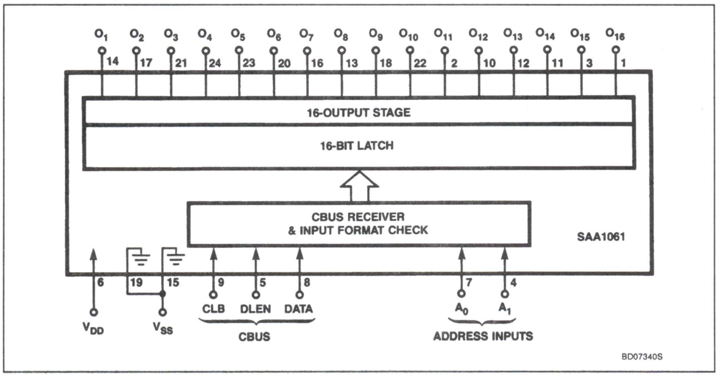
APPLICATIONS

- **LED driver**
- **μP output port expander**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	−20°C to +80°C	SAA1061N

BLOCK DIAGRAM

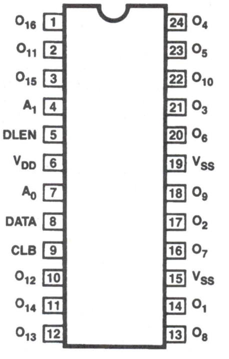


O1 O2 O3 O4 O5 O6 O7 O8 O9 O10 O11 O12 O13 O14 O15 O16
14 17 21 24 23 20 16 13 18 22 2 10 12 11 3 1
16-OUTPUT STAGE
16-BIT LATCH
CBUS RECEIVER & INPUT FORMAT CHECK
SAA1061
6 19 15 9 5 8 7 4
VDD
VSS
CLB DLEN DATA
CBUS
A0 A1
ADDRESS INPUTS

BD07340S

PIN CONFIGURATION

N Package



O16 1
O11 2
O15 3
A1 4
DLEN 5
VDD 6
A0 7
DATA 8
CLB 9
O12 10
O14 11
O13 12
24 O4
23 O5
22 O10
21 O3
20 O6
19 VSS
18 O9
17 O2
16 O7
15 VSS
14 O1
13 O8

TOP VIEW

CD10780S

PIN NO.	SYMBOL	DESCRIPTION	
6	V_{DD}	Positive supply (+5V)	
15, 19	V_{SS}	Ground (0V)	
Inputs			
4	A_1	Address bit S1	C BUS
5	DLEN	Data line enable	
7	A_0	Address bit S0	
8	DATA	Data word	
9	CLB	Clock burst	
Outputs			
1	O_{16}	Driver outputs O_1 to O_{16} corresponding with the data bits 1 to 16 of the data word.	
2	O_{11}		
3	O_{15}		
10	O_{12}		
11	O_{14}		
12	O_{13}		
13	O_8		
14	O_1		
16	O_7		
17	O_2		
18	O_9		
20	O_6		
21	O_3		
22	O_{10}		
23	O_5		
24	O_4		

Output Port Expander

SAA1061

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.3 to +7.5	V
V_{IN}	Input voltage range	−0.3 to +15	V
$\pm I_{IN}$	Input current	10	mA
V_{OUT}	Output voltage range	−0.3 to +16.5	V
$\pm I_{OUT}$	Output current per output	20	mA
P_O	Power dissipation per output	7.5	mW
P_{TOT}	Total power dissipation per package	300	mW
T_A	Operating ambient temperature range	−20 to +80	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $V_{SS} = 0V$; $V_{DD} = 5V$; $T_A = -20$ to $+80°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5	5.5	V
I_{DD}	Supply current				20	mA
Inputs CLB, DLEN, DATA, A_0, A_1						
V_{IL}	Input voltage LOW	$T_A = 25°C$	−0.3		0.8	V
V_{IH}	Input voltage HIGH		2.0		15	V
I_{IR}	Input leakage current	$V_I = -0.3$ to $+15V$			1	μA
Outputs O_1 to O_{16} (open-drain)						
V_{OL}	Output voltage LOW	$I_{OL} = 15mA$			0.65	V
I_{OH}	Output leakage current HIGH	$V_{OH} = 16.5V$			20	μA
t_R, t_F	Rise and fall times	$V_{OL} = 1.5V$; $V_{OH} = 13.5V$			10	μs
C BUS timing						
t_R, t_F	Rise and fall times	see Figure 1			2	μs
t_{SUDA}	Data setup time: DATA → CLB		400			ns
t_{HDDA}	Data hold time: DATA → CLB		250			ns
t_{SUEN}	Enable setup time: DLEN → CLB		400			ns
t_{SUDI}	Disable setup time: CLB → DLEN		600			ns
t_{SULD}	Setup time: DLEN → CLB (load pulse)		400			ns
t_{WH}, t_{WL}	CLB pulse width HIGH/LOW		450			ns

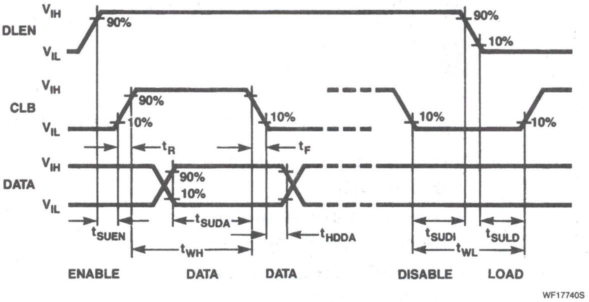

DLEN
V_IH
V_IL
90%
90%
10%
CLB
V_IH
V_IL
90%
10%
10%
10%
10%
t_R
t_F
DATA
V_IH
V_IL
90%
10%
t_SUEN
t_SUDA
t_WH
t_HDDA
t_SUDI
t_WL
t_SULD
ENABLE
DATA
DATA
DISABLE
LOAD
WF17740S

Figure 1. C BUS Timing

OPERATION DESCRIPTION

1. CBUS Transmission

The data words are entered via a serial CBUS interface. A clock burst of 18 clock periods is used to transmit the 16-bit data word, plus 2 identifier bits.

Serial data words, which are synchronized with the clock burst (CLB), are accepted if the enable input DLEN is HIGH at the same time. Each transmission is checked for word length (number of clock pulses during DLEN is HIGH) and the address bits S0 and S1.

The valid data flag is only set if:

1. Word length is correct; 2 address bits and 16 data bits.
2. Address bits S0 and S1 correspond with A_0 and A_1.

Loading the information into the selected latch register is done by the load pulse (first clock pulse after the HIGH-to-LOW transition of DLEN) if the address bits correspond with A_0 and A_1. The load pulse or a new LOW-to-HIGH transition of DLEN resets the valid data flag. Only after the valid data flag is reset, will new data be accepted.

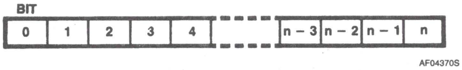

BIT
0
1
2
3
4
n − 3
n − 2
n − 1
n
AF04370S

Figure 2. Data Word Organization

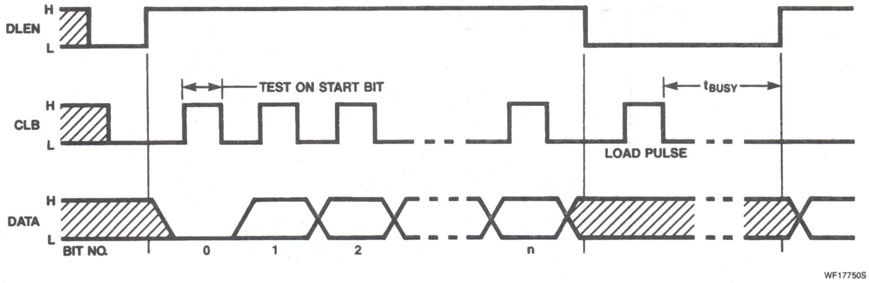

DLEN
H
L
CLB
H
L
TEST ON START BIT
t_BUSY
LOAD PULSE
DATA
H
L
BIT NO.
0
1
2
n
WF17750S

Figure 3. CBUS Data Transmission

Definitions to Figures 2 and 3:

- Word length: number of clock pulses during DLEN is active (HIGH); n + 1 bits = 18 bits.
- Bit number 0 is for the SAA1061 S0.
- Data bits: bit numbers 1 to n-1 (16-bits); bit no. n is S1.
- Load pulse: first clock pulse after DLEN returns to inactive (LOW).

2. Address Inputs A_0 and A_1

The 1st bit (bit S0) and the 18th bit (bit S1) of the data word are the address bits. Data is accepted only if the addresses correspond to the programmed addresses at inputs A_0 and A_1, that is for:

A_0 = S0 and A_1 = S1.

3. Data Outputs O_1 to O_{16}

The outputs O_1 to O_{16} correspond with the data bits 1 to n-1 (16-bits). The open-drain driver outputs (O_1 to O_{16}) are switched to ground (O_n = LOW), if the corresponding data bit is LOW.

4. Power-On Reset

The circuit generates internally a reset-cycle after switching on the supply and the outputs become high-ohmic (HIGH).

Signetics

Linear Products

TEA1017
13-Bit Serial-to-Parallel Converter

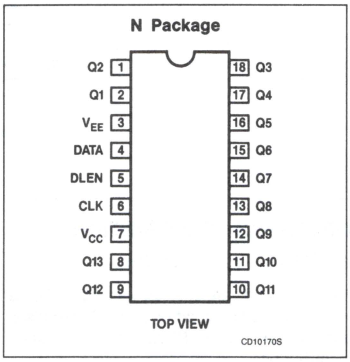
Product Specification

DESCRIPTION
The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays and small stepper motors. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

FEATURES
- **TTL and CMOS compatible inputs**
- **Outputs drive load in both directions**
- **Power-on reset makes outputs floating**
- **Wide supply voltage range**

APPLICATIONS
- **Driving stepper motors**
- **Driving triacs**
- **Used as a simple switch**
- **Driving mosaic printhead**
- **Electronic appliances; i.e., washing machines**
- **Electronic equipment; i.e., typewriters**
- **Relays**
- **Automotive industry**

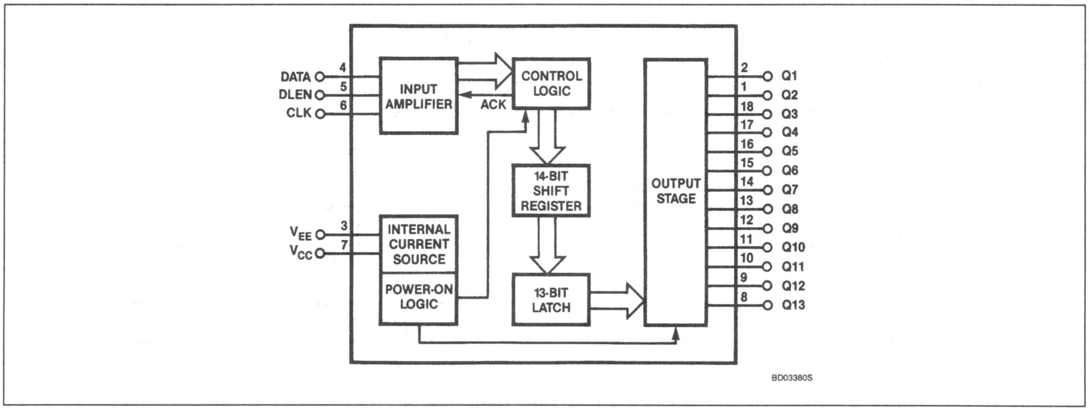
PIN CONFIGURATION


N Package
Q2 1
Q1 2
V_EE 3
DATA 4
DLEN 5
CLK 6
V_CC 7
Q13 8
Q12 9
18 Q3
17 Q4
16 Q5
15 Q6
14 Q7
13 Q8
12 Q9
11 Q10
10 Q11
TOP VIEW
CD10170S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−20°C to +80°C	TEA1017N

BLOCK DIAGRAM


DATA 4
DLEN 5
CLK 6
INPUT AMPLIFIER
CONTROL LOGIC
ACK
14-BIT SHIFT REGISTER
13-BIT LATCH
OUTPUT STAGE
V_EE 3
V_CC 7
INTERNAL CURRENT SOURCE
POWER-ON LOGIC
2 Q1
1 Q2
18 Q3
17 Q4
16 Q5
15 Q6
14 Q7
13 Q8
12 Q9
11 Q10
10 Q11
9 Q12
8 Q13
BD03380S

FUNCTIONAL DESCRIPTION

The control logic performs a key function in this device. It checks whether the input information has the correct format: a DLEN signal that has been HIGH during 14 clock pulses, and a DATA signal with its first bit LOW.

When the format is found to be correct, the 15th clock pulse makes the control logic generate a signal that loads the content of the first 13 bits of the shift register into 13 latches. These drive the output stages.

"Acknowledge" (Pin 4)

After the 15th clock pulse, an Acknowledge signal drives the DATA pin to LOW. To use this information, the DATA should be programmed HIGH and an open-collector device, or a series resistor should be used on the DATA input. This signal is valid until the next clock pulse, LOW-to-HIGH transition (see Figure 1).

Supply V_{CC} (Pin 7)

The supply current of the TEA1017, is regulated internally. This permits the circuit to be used over a very wide range of supply voltages (i.e., 4.5 to 18V) with little variation of supply current.

The circuit has a power-on reset arrangement that resets the circuit and brings the outputs in a high-impedance state. It requires a rise time of the supply larger than 3μs/V.

DATA Input (Pin 4)

The circuit requires input information on the DATA input consisting of 14 bits, the first bit being LOW. This information should be synchronous with the clock pulse. Data is loaded into the shift register at the HIGH-to-LOW transitions of the clock pulse.

Data Line Enable Input DLEN (Pin 5)

A HIGH level on the DLEN input enables the shift register. This HIGH level should have a duration of 14 clock pulses (see Figure 1).

After the DLEN input has returned to LOW the subsequent (15th) clock pulse transfers the content of the shift register to the latches and from there to the outputs.

Clock Input CLB (Pin 6)

The shift register shifts at the HIGH-to-LOW transitions of the clock pulse. The clock signal may be a continuously running clock or a clock burst of 15 clock pulses.

Outputs Q1 to Q13

The outputs are capable of supplying a load current in both directions; i.e., they can drive a load to the supply (V_{CC}) or to ground (V_{EE}).

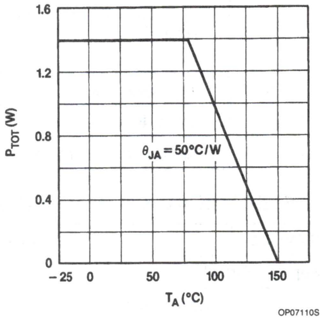


Figure 2. Derating Curve

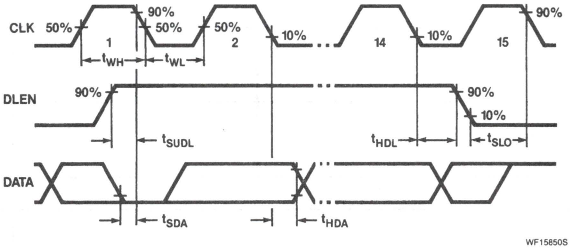


Figure 1. Bus Timing Characteristics

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
V_I	Input voltage range, all inputs	-0.3 to $V_{CC} = 0.3$	V
 $-I_{OH}$ I_{OL}	Output current, all outputs HIGH LOW	 150 150	 mA mA
P_{TOT}	Total power dissipation	1.4	W
T_{STG}	Storage temperature range	−40 to +150	°C
T_A	Operating ambient temperature range	−20 to +80	°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.5$ to 18V; $V_{EE} = 0V$; $T_A = -20°C$ to $+80°C$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Supply (Pin 7)					
  I_{CC} I_{CC}	Supply current during normal operation, unloaded at $V_{CC} = 4.5V$ at $V_{CC} = 18V$		 45 50	 60 70	 mA mA
 I_{CC} I_{CC}	during power-on blanking, unloaded at $V_{CC} = 4.5V$ at $V_{CC} = 18V$		 1.5 5	 2 7	 mA mA
	Supply voltage rise time to ensure power on reset	 3			 μs/V
Clock input CLK (Pin 6)					
 V_{IH} V_{IL}	Input voltage HIGH LOW	 2 		 0.8	 V V
 I_{IH} $-I_{IL}$	Input current HIGH at $V_{CLKH} = 2V$ LOW at $V_{CLKL} = 0.4V$			 10 10	 μA μA
DATA input (Pin 4)					
 V_{IH} V_{IL}	Input voltage HIGH LOW	 2 		 0.8	 V V
 I_{IH} $-I_{IL}$	Input current HIGH at $V_{IH} = 2V$ LOW at $V_{IL} = 0.4V$			 10 10	 μA μA
 I_{DACK}	DATA input in sink current ACKN = TRUE	 1			 mA
Data line enable input DLEN (Pin 5)					
 V_{IH} V_{IL}	Input voltage HIGH LOW	 2 		 0.8	 V V
 I_{IH} $-I_{IL}$	Input current HIGH at $V_{5-3} = 2V$ LOW at $V_{5-3} = 0.4V$			 10 10	 μA μA

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 4.5$ to 18V; $V_{EE} = 0V$; $T_A = -20°C$ to $+80°C$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Outputs Q1 to Q13					
	Output voltage during normal operation				
V_{OH}	HIGH at $-I_{OH} = 80mA$	V_{CC} −1.5			V
V_{OL}	LOW at $I_{OL} = 80mA$			1	V
	Output current during power-on reset				
$-I_{OH}$	HIGH			10	μA
I_{OL}	LOW			10	μA
	Rise and fall times: no maximum				
	Minimum times as V_{CC}=4.5V (See Figure 1)				

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.5$ to 18V; $V_{EE} = 0V$; $T_A = -20°C$ to $+80°C$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Clock input CLK (Pin 6)					
	Clock pulse duration				
t_{WH}	HIGH	8			μs
t_{WL}	LOW	10			μs
Outputs Q1 to Q13					
t_{SUDL}	Setup time ENABLE	2.8			μs
t_{HOL}	Hold time ENABLE	5.0			μs
t_{SDA}	Setup time DATA	0			μs
t_{HDA}	Hold time DATA	2.8			μs
t_{SLO}	Setup time LOAD	1.4			μs
t_{WL}	Pulse width LOW	10			μs
t_{WH}	Pulse width HIGH	8			μs
f_{MAX}	Max. clock input frequency = $1/(t_{WH} + t_{WL})$			50	kHz
t_{PCQ}	Propagation delay CL to output			8.5	μs
t_{PCA}	Propagation delay CL to ACKN			6	μs

APPLICATION INFORMATION

1. From the buffer-capacitors C1 of the power supply the supply connections to the TEA1017 and the loads should be separated. An extra capacitor of 10µF with good high-frequency characteristics should be mounted across the V_{CC} and V_{EE} connections as close as possible to the TEA1017.
2. If no use is made of the Acknowledge information it is advised to program the data output from the controller to LOW during the time ACKN is valid. To use the Acknowledge information, the data output must be programmed HIGH. When a push-pull controller device is used, a series resistor has to be connected in the data line between the controller and TEA1017. The ACKN may be sensed on the TEA1017 side of this resistor (see Figure 3).

NOTE:
ACKN is removed from the data line after the next LOW-to-HIGH transition of the clock line with a maximum delay of 6µs (t_{PCA} maximum).

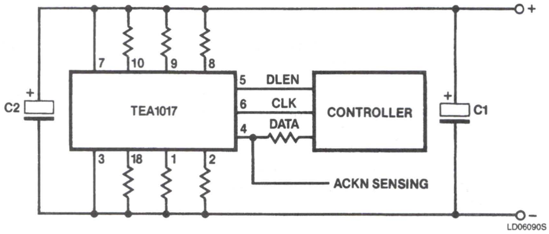


Figure 3. TEA1017 With 3 Loads to V_{CC} Q = 0 and 3 Loads to V_{EE} Q = 1

Signetics

AN103
13-Bit Serial-to-Parallel Converter: TEA1017

Application Note

Linear Products

The TEA1017 integrated circuit is a serial-to-parallel converter with 13 push-pull output stages, each capable of sourcing or sinking 80mA. Owing to its high output current, the TEA1017 can drive a variety of loads such as displays, triacs, relays and small stepping motors directly. Data enters the TEA1017 via a serial 3-line bus (CBUS), which can be controlled by virtually all microcontrollers. Additional features of the TEA1017 are:

- A wide supply voltage range, 4.5V to 18V
- Input data rate up to 50K baud
- Data acknowledgement
- Integrated flywheel diodes in the output stages.

Figure 1 is a block diagram of the TEA1017. The DATA, DLEN and CLK lines comprise the CBUS. Serial data from a microcontroller enters on the DATA input and is clocked into a shift register enabled by the DLEN (data line enable) signal. Internal control logic checks that the data has the correct format before it is latched and applied to the output stages. The output data can be updated every 320μs. At power-on, the power-on logic resets the control logic and leaves the outputs, Q1 to Q13, floating until the first data word is latched.

Table 1 gives brief data on the TEA1017.

INPUT AMPLIFIER

Figure 2 shows the input section of a TEA1017. A constant-current source I_1 supplies four transistors TR1 to TR4 of which TR2, TR3 and TR4 are the current sources for three differential amplifiers for the CBUS signals DATA, DLEN and CLK. TR1 supplies the drive current for the DATA acknowledge signal.

The DATA input is connected to the inverting input (base of TR5) of the first differential amplifier. The non-inverting input is connected to a voltage reference V_1 which sets a threshold of about $2V_{BE}$ for the DATA input.

The output of the first differential amplifier is a current mirror, TR7 and TR8, the inverse of the DATA input signal appearing at the collector of TR8. Inverse DLEN and CLK signals are generated in a similar way.

When the format of the incoming serial data is correct (see 'CBUS data transfer'), TR9 is turned on by a signal from the control logic after 14 data bits have been received, forcing the DATA input LOW. If the DATA input is pulled HIGH by the microcontroller; e.g., with a pull-up resistor, the microcontroller can read the DATA line acknowledgement from the TEA1017.

OUTPUT STAGE

Figure 3 shows one of the 13 output stages of a TEA1017. V_1 and V_2 are internally-derived reference voltages.

When the TEA1017 is connected to a supply voltage V_{CC}, the contents of the 13-bit latch will be random. To inhibit the output stage until the first valid data is latched, V_1 is set to zero during power-on reset. This makes the differential amplifier comprising transistors TR1 and TR2 inactive since neither transistor can be driven, and leaves the output floating.

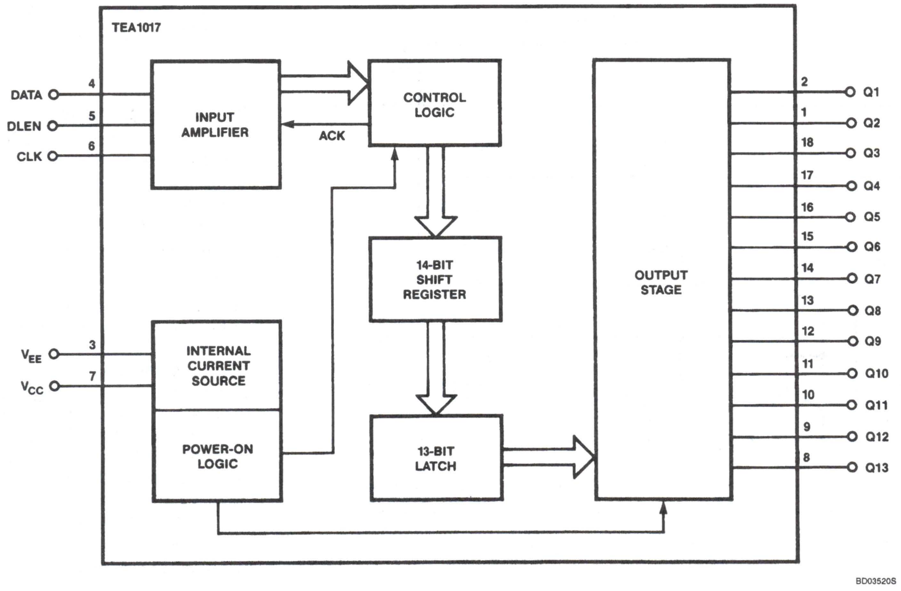


Figure 1. Block Diagram of the TEA1017. The IC is in a Standard 18-Pin DIP Package

Table 1. Brief Data on the TEA1017 V_{CC} = 4.5V to 18V; V_{EE} = 0V and T_A = 25°C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	4.5		18	V
I_{OL}; $-I_{OH}$	Max. output current per ouput	80		150	mA
	Output leakage current during power-on reset			10	μA
	Power dissipation, loaded				
P_{tot}	at V_{CC} = 5V		0.23	0.3	W
P_{tot}	at V_{CC} = 18V		0.9	1.26	W
	Input voltage for DATA, DLEN and CLK:				
V_{IH}	input voltage HIGH	2		V_{CC}+0.3	V
V_{IL}	input voltage LOW	−0.3		0.8	V
	Input current for DATA, DLEN and CLK:				
I_{IH}	input current HIGH (V_{IH} = 2V)			10	μA
$-I_{IL}$	input current LOW (V_{IL} = 0.4V)			10	μA
V_{OH}	Output voltage HIGH at $-I_{OH}$ = 80mA	V_{CC} − 1.5			V
V_{OL}	Output voltage LOW at I_{OL} = 80mA			1	V
I_{DACK}	Sink current at DATA input for acknowledge	1			mA
T_A	Operating ambient temperature range	0		+80	°C

The complementary output stage TR3 and TR4 has a low output impedance for both HIGH and LOW logic levels. Since TR3 is an emitter-follower, its saturation voltage is one V_{BE} higher than that of TR4, a common-emitter amplifier. This should be taken into account when calculating power dissipation. The maximum power dissipation of a TEA1017 up to 80°C is 1.4W. See Figure 4.

When an output is changing state, both TR3 and TR4 can conduct briefly. To supply the necessary through-current, it is essential to connect a 10μF capacitor between V_{CC} and V_{EE} as close as possible to the TEA1017. This capacitor decouples the TEA1017's supply from that for the load.

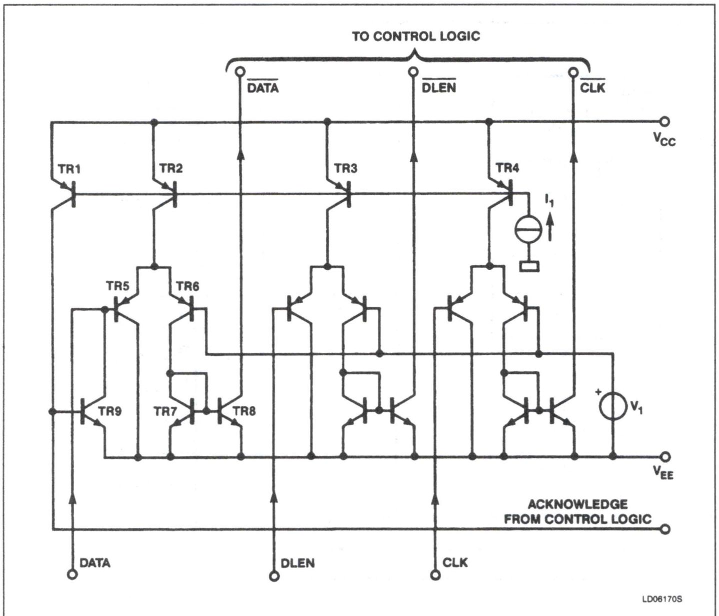


Figure 2. Input Stage

Flywheel diode D1 protects the output of TR3 when switching inductive loads. Diode D2 sinks the current I_1 from a HIGH input (from the input stage) into the voltage source V_2, limiting the voltage between the bases of TR1 and TR2.

CBUS DATA TRANSFER

Communication between a TEA1017 and a microcontroller is according to the CBUS format. As stated earlier, the CBUS comprises three lines:

- Data line DATA
- Data line enable DLEN
- Clock CLK.

Instead of an address, the length of the words on the DATA line is used to access different devices connected to a CBUS. For TEA1017s, the word length is 14 bits, the start and end of words being indicated by the DLEN signal. In addition, the first bit of each word must be a zero. Several TEA1017s on the same CBUS can be accessed individually by gating the DLEN signal. The CBUS clock can have a frequency up to 50kHz and may run continuously or operate in bursts of 15 clock periods.

Figure 5 and Table 2 show the CBUS timing for a TEA1017. Starting from the inactive state (DLEN LOW, CLK LOW and DATA

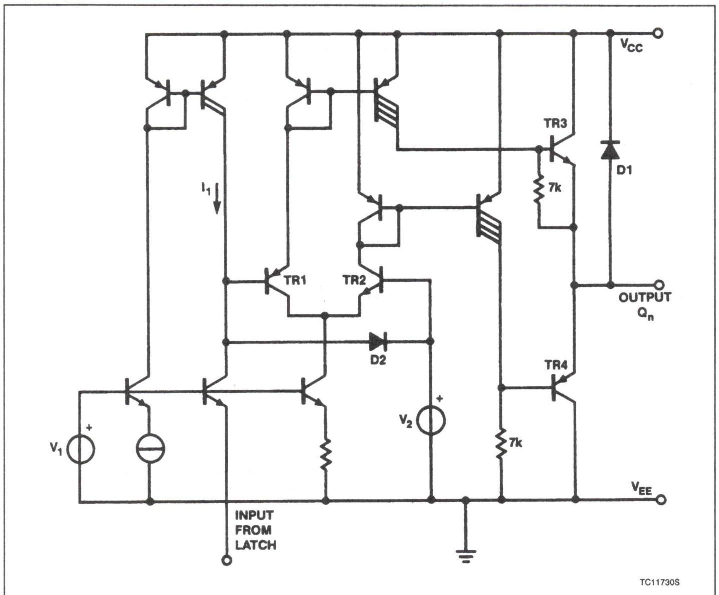


Figure 3. Output Stage

Table 2. CBUS Timing $V_{CC} = 4.5V$; $T_A = 25°C$

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{SUDL}	Setup time ENABLE	2.8		µs
t_{HDL}	Hold time ENABLE	5.0		µs
t_{SDA}	Setup time DATA	0		µs
t_{HDA}	Hold time DATA	2.8		µs
t_{SLO}	Setup time LOAD	1.4		µs
t_{WL}	Pulse width LOW	10		µs
t_{WH}	Pulse width HIGH	8		µs
f_{CLK}	Clock frequency (1/(t_{WH} + t_{WL})		50	kHz
	Propagation delay:			
t_{PCQ}	latch to outputs		8.5	µs
t_{PCA}	acknowledge		6	µs
t_{PCAR}	acknowledge release		6	µs

HIGH or LOW), DLEN goes HIGH, enabling an internal clock for a 14-bit shift register. The DATA line which should be synchronized to the CLK is read on the falling edges of CLK and the data is loaded into the shift register. After the fourteenth falling edge of the clock pulse, DLEN goes LOW, indicating the end of a word. On the falling edge of the fifteenth clock pulse:

- the contents of the shift register (apart from the first bit which is always a LOW for a TEA1017) are transferred to a 13-bit latch that drives the 13 output stages. The first significant bit read appears at output Q13, the last at Q1.
- the DATA line is pulled LOW, acknowledging the data transfer. On the rising edge of the sixteenth clock pulse (continuous clock) or of the next clock burst, the DATA line is released within 6µs (t_{PCAR}). To use this acknowledge signal, the microcontroller port connected to the DATA line should be programmed HIGH and be an open-collector output. When a microcontroller with push-pull outputs is used, a series resistor should be inserted in the DATA line. The acknowledge can be sensed on the TEA1017 side of the resistor.

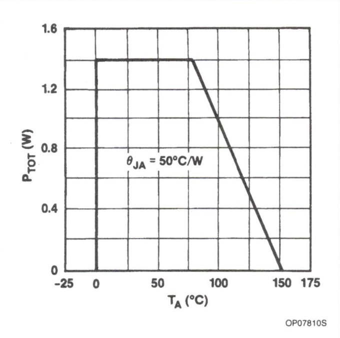


Figure 4. Power Derating Curve

If no use is made of the acknowledge signal, the microcontroller port connected to the DATA line should be programmed LOW while the acknowledge is valid.

Data words or DLEN signals not according to the CBUS format are detected by the internal control logic which prevents the word being latched, the existing word in the latch being held until the next valid word is generated.

APPLICATIONS

Switch

The simplest use for the TEA1017 is as a multipole switch. Because all switch states are latched in the TEA1017, its microcontroller only has to address the device when the state of a switch has to be altered.

Figure 6a shows a 13-level status indicator with 26 LEDs (off and on display). This circuit is extremely simple because the output voltage of a TEA1017 can switch almost between V_{CC} and V_{EE}.

After power-on reset, the outputs of the TEA1017 are floating, so both LEDs are lit at reduced brightness. After the first data transfer, only one diode is lit at each output.

The TEA1017 can be used to drive a relay directly, owing to the integrated flywheel diode in each output stage, see Figure 6b.

Driving Stepping Motors

The TEA1017 can drive a variety of small four-phase unipolar stepping motors, see Figure 7. Phase energization can be easily altered because the control data is stored in software in a microcontroller. Larger motors than that shown can be controlled by adding power transistors at the outputs of the TEA1017. Table 3 shows the output states for

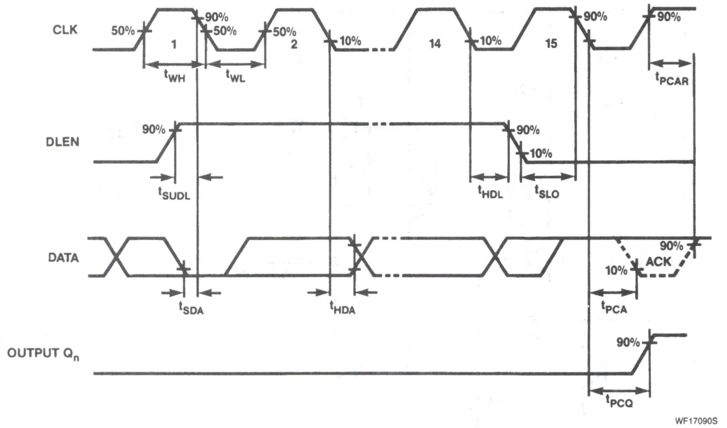
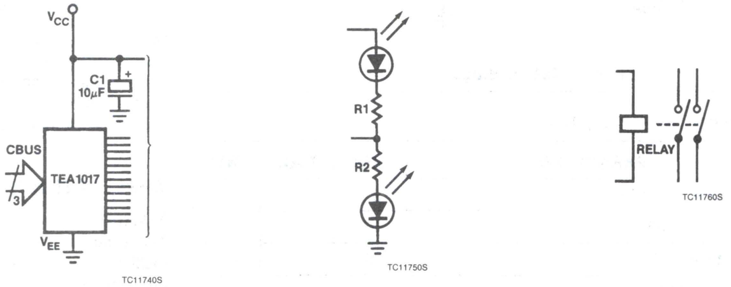

CLK
50%
1
90%
50%
50%
2
10%
14
10%
15
90%
90%
t_{WH}
t_{WL}
t_{PCAR}
DLEN
90%
90%
10%
t_{SUDL}
t_{HDL}
t_{SLO}
DATA
90%
ACK
10%
t_{SDA}
t_{HDA}
t_{PCA}
OUTPUT Q_n
90%
t_{PCQ}
WF17090S

Figure 5. CBUS Timing. For the TEA1017, a 14-Bit Data Word is Used; the First Bit Must be a Zero


V_{CC}
C1
10µF
+
CBUS
TEA1017
3
V_{EE}
TC11740S
R1
R2
TC11750S
RELAY
TC11760S

a. Status Indicator. Only One Output Stage is Shown

b. Driving a Relay

Figure 6

rotating the motor shown in Figure 7 in four steps.

Several stepping motors can be driven independently by one TEA1017. The speed of each motor is calculated in the microcontroller's main program and the bit patterns are joined in a subroutine with the clock rate determined by the motor with the highest stepping rate.

In chart recorders and X/Y plotters, one TEA1017 is usually sufficient for all functions (X/Y movement, pen up, pen down, etc.). Furthermore, the CBUS reduces the number of wires and interconnections needed.

Table 3. Phase Energization for a Four-Phase Unipolar Stepping Motor

CLOCK	OUTPUT			
	Q1	Q2	Q3	Q4
0	L	H	L	H
1	H	L	L	H
2	H	L	H	L
3	L	H	H	L

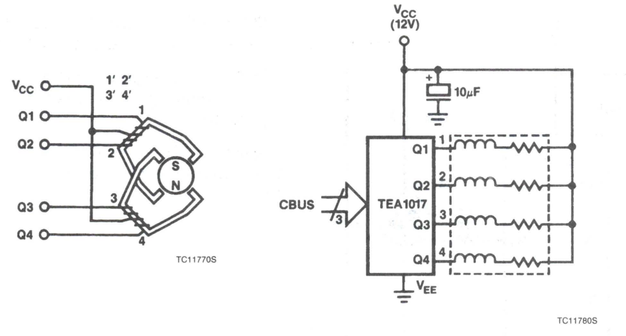
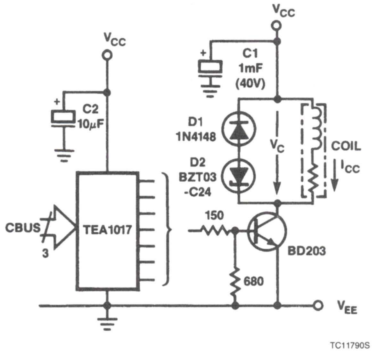
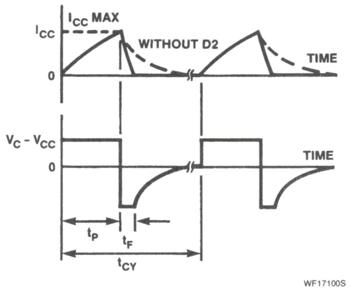


Figure 7. Driving a 4-Phase Unipolar Stepper Motor



NOTE:
The circuitry for one needle is shown

a. Driving Matrix Printer Head



NOTE:
t_P is the time a voltage is applied to the coil; t_f is the time in which the stored energy of the magnetic field is reduced to zero; t_{CY} is the pulse period.

b. Voltages and Currents for a Matrix Printer Head
Figure 8

Driving a Matrix Printer Head

Figure 8a shows the circuit for driving one needle of a 7- or 9-needle matrix printer head. Capacitor C_1 supplies the peak current for the printer head coil whose energization is controlled by a power transistor BD203 driven by a TEA1017. Diodes D1 and D2 limit the induced EMF. In addition, D2 improves the turn-off by rapidly reducing the magnetic energy stored in the coil. Furthermore, part of the heat generated during this energy reduction is dissipated in D2 instead of in the head.

The output of the TEA1017 is a pulse stream set by the characters to be printed. Supply voltage V_{CC} determines the rate of rise of current in the coil and the pulse width sets the maximum current, see Figure 8b.

One possibility is one TEA1017 driving a 7-needle head (via power transistors) and the carriage return, carriage forward, paper feed and line feed stepping motors.

Driving Triacs

Figure 9 shows a circuit for driving a BT138 triac with a TEA1017. In this circuit, the triac is triggered with negative gate current which reduces the drive required.

As shown, the triac can be used as a switch or as a phase controller. When used as a phase controller, the microcontroller is synchronized to the zero crossings of the mains. A zero cross-over detector is incorporated in our MAB8400 family of microcontrollers.

MAINS ISOLATION

The microcontroller for the TEA1017 can be isolated from mains-connected loads either:

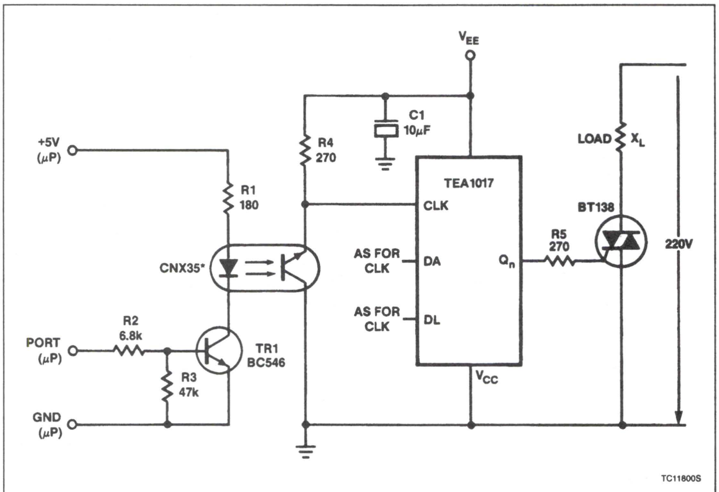
— at the outputs of the TEA1017 or

— at the CBUS inputs of the TEA1017.

When there are more than two mains-connected loads, it is best to isolate the three CBUS lines, for example, with optocouplers such as CNX35s (see Figure 9). R2 limits the load current of the output port to 1mA. TR1 drives the LED of the optocoupler. R4 determines the dynamic behavior of the circuit. With a driver transistor as shown, the TEA1017 can be driven at maximum clock frequency. TR1 can be omitted if a lower clock rate can be tolerated, but an optocoupler with a higher coupling efficiency (e.g., CNX36) should be used.

13-Bit Serial-to-Parallel Converter: TEA1017

AN103



VEE
C1
10µF
R4
270
+5V
(µP)
R1
180
TEA1017
CLK
LOAD
XL
BT138
R5
270
CNX35*
AS FOR CLK
DA
Qn
220V
AS FOR CLK
DL
R2
6.8k
PORT
(µP)
TR1
BC546
R3
47k
VCC
GND
(µP)
TC11800S

Figure 9. Driving a Triac

REFERENCES

1. 'I^{2}C Bus Specification.' Philips publication, 1983, ordering code 9398 615 00011.
2. 'Software Examples.' Philips publication, 1983, ordering code 9398 615 70011, pp.24-33.

Originally published in *Technical Publication 203,* ELCOMA, the Netherlands, 17 February 1986

Section 7
Timers

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Signetics

ICM7555

General Purpose CMOS Timer

Product Specification

Linear Products

DESCRIPTION

The ICM7555 is a CMOS timer providing significantly improved performance over the standard NE/SE555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$, and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher-frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

The ICM7555 is a stable controller capable of producing accurate time delays or frequencies.

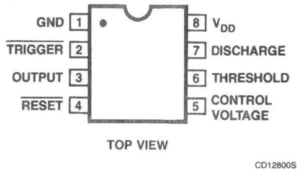
In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the bipolar 555 device, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuit is triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

FEATURES

- **Exact equivalent in most applications for NE/SE555**
- **Low supply current — 80μA (typ)**
- **Extremely low trigger, threshold, and reset currents — 20pA (typ)**
- **High-speed operation — 500kHz guaranteed**
- **Wide operating supply voltage range guaranteed 2 to 18V**
- **Normal reset function — no crowbarring of supply during output transition**
- **Can be used with higher-impedance timing elements than the bipolar 555 for longer time constants**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Typical temperature stability of 0.005%/°C at 25°C**
- **Outputs have very low offsets, HI and LO**

PIN CONFIGURATION

D, FE, and N Packages



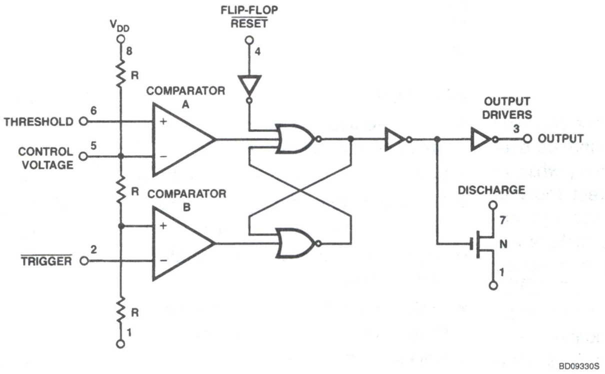
APPLICATIONS

- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Missing pulse detector**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	ICM7555CN
8-Pin Plastic SO	0 to +70°C	ICM7555CD
8-Pin Ceramic DIP	0 to +70°C	ICM7555CFE
8-Pin Plastic DIP	-40°C to +85°C	ICM7555IN
8-Pin Plastic SO	-40°C to +85°C	ICM7555ID
8-Pin Ceramic DIP	-40°C to +85°C	ICM7555IFE
8-Pin Plastic DIP	-55°C to +125°C	ICM7555MN
8-Pin Ceramic DIP	-55°C to +125°C	ICM7555MFE

EQUIVALENT BLOCK DIAGRAM



NOTE:
Unused inputs should be connected to appropriate voltage from Truth Table.

TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	$\overline{\text{RESET}}$[1]	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
$> 2/3(V+)$	$> 1/3(V+)$	HIGH	LOW	ON
$V_{TH} < 2/3$	$V_{TR} > 1/3$	HIGH	STABLE	STABLE
DON'T CARE	$< 1/3(V+)$	HIGH	HIGH	OFF

NOTE:
1. $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	+18	V
V_{TRIG}[1] V_{CV} V_{TH} V_{RST}	$\overline{\text{Trigger}}$ input voltage Control voltage Threshold input voltage $\overline{\text{RESET}}$ input voltage	> -0.3 to $< V_{DD} + 0.3$	V
I_{OUT}	Output current	100	mA
	Maximum power dissipation $T_A = 25°C$ (still-air)[2, 3] F package N package D package	 780 1160 780	 mW mW mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (Soldering 60s)	300	°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than $V_{DD} + 0.3V$ or less than GND − 0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555 must be turned on first.
2. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
3. See "Power Dissipation Considerations" section.

General Purpose CMOS Timer ICM7555

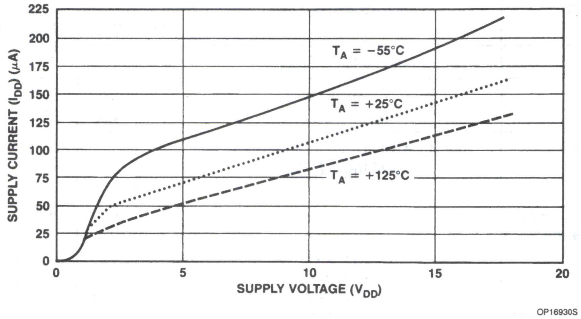
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ICM7555M			ICM7555I/C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply voltage	$T_{MIN} \leqslant T_A \leqslant T_{MAX}$	3		16	2		18	V
I_{DD}	Supply current[1]	$V_{DD} = V_{MIN}$		50	200		50	120	μA
		$V_{DD} = V_{MAX}$		180	300		180	300	μA
	Astable mode timing[2]	R_A, R_B = 1k to 100k, C = 0.1μF $5V \leqslant V_{DD} \leqslant 15V$							
	Initial accuracy			1.0	5.0		1.0	5.0	%
	Drift with supply voltage			0.1	3.0		0.1	3.0	%/V
	Drift with temperature[3]								
		$V_{DD} = 5V$		50			50		ppm/°C
		$V_{DD} = 10V$		75			75		ppm/°C
		$V_{DD} = 15V$		100			100		ppm/°C
V_{TH}	Threshold voltage	$V_{DD} = 5V$	0.63	0.65	0.67	0.63	0.65	0.67	× V_{DD}
V_{TRIG}	Trigger voltage	$V_{DD} = 5V$	0.29	0.31	0.34	0.29	0.31	0.34	× V_{DD}
I_{TRIG}	Trigger current	$V_{DD} = V_{TRIG} = V_{MAX}$		50			50		pA
		$V_{DD} = V_{TRIG} = 5V$		10			10		pA
		$V_{DD} = V_{TRIG} = V_{MIN}$		1			1		pA
I_{TH}	Threshold current	$V_{DD} = V_{TH} = V_{MAX}$		50			50		pA
		$V_{DD} = V_{TH} = 5V$		10			10		pA
		$V_{DD} = V_{TH} = V_{MIN}$		1			1		pA
I_{RST}	Reset current	$V_{DD} = V_{RST} = V_{MAX}$		100			100		pA
		$V_{DD} = V_{RST} = 5V$		20			20		pA
		$V_{DD} = V_{RST} = V_{MIN}$		2			2		pA
V_{RST}	Reset voltage	$V_{DD} = V_{MIN}$ and V_{MAX}	0.4	0.7	1.0	0.4	0.7	1.0	V
V_{CV}	Control voltage	$V_{CC} = 5V$	0.62	0.65	0.67	0.62	0.65	0.67	V
V_{OL}	Output voltage (low)	$V_{DD} = V_{MAX}$, $I_{SINK} = 3.2mA$		0.1	0.4		0.1	0.4	V
		$V_{DD} = 5V$, $I_{SINK} = 3.2mA$		0.2	0.4		0.2	0.4	V
V_{OH}	Output voltage (high)	$V_{DD} = V_{MAX}$, $I_{SOURCE} = 1.0mA$	15.25	15.7		17.25	17.8		V
		$V_{DD} = 5V$, $I_{SOURCE} = 1.0mA$	4.0	4.5		4.0	4.6		V
V_{DIS}	Discharge output voltage	$V_{DD} = 5V$, $I_{DIS} = 10.0mA$		0.2	0.4		0.2	0.4	V
t_R	Rise time of output[3]	$R_L = 10M\Omega$, $C_L = 10pF$, $V_{DD} = 5V$		45	75		45	75	ns
t_F	Fall time of output[3]	$R_L = 10M\Omega$, $C_L = 10pF$, $V_{DD} = 5V$		20	75		20	75	ns
f_{MAX}	Maximum oscillator frequency (astable mode)		500			500			kHz

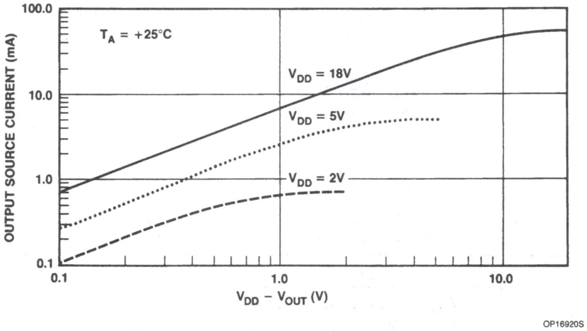
NOTES:

1. The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD, and $\overline{\text{RESET}}$ voltages.
2. Astable timing is calculated using the following equation: $f = \frac{1.38}{(R_A + 2R_B)C}$. The components are defined in Figure 2.
3. Parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

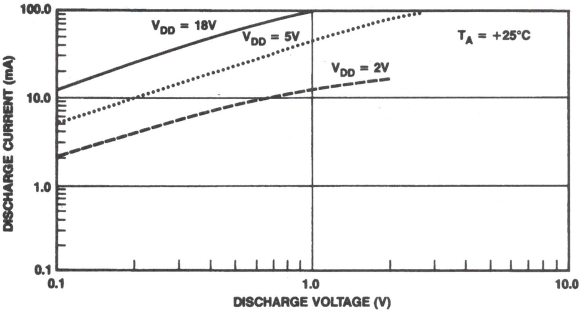


Supply Current vs. Supply Voltage



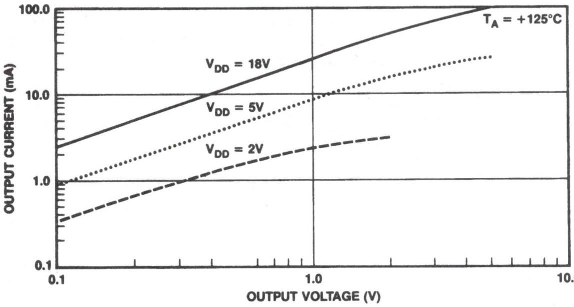
High Output Voltage Drop Vs Output Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



OP19470S

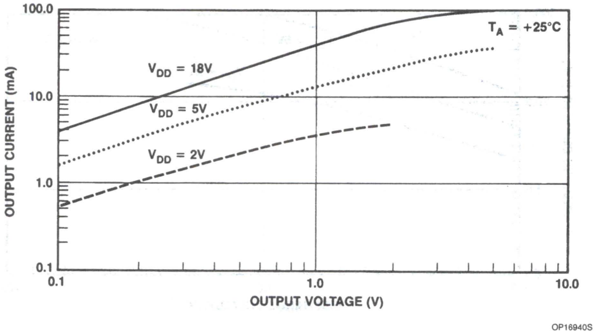
Discharge Low Output Voltage vs Discharge Sink Current



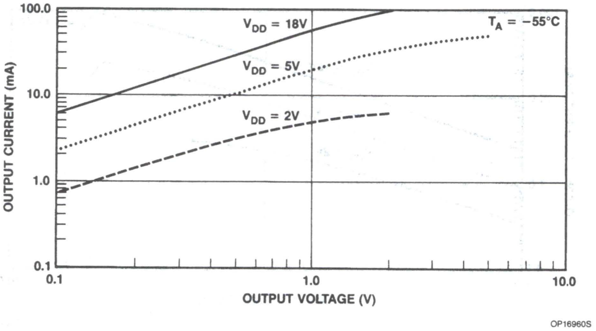
OP16950S

Low Output Voltage vs Output Sink Current

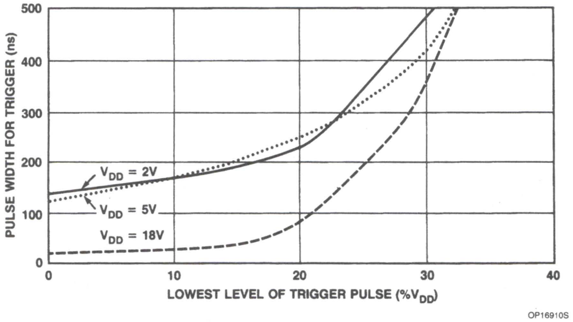
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Low Output Voltage vs Output Sink Current

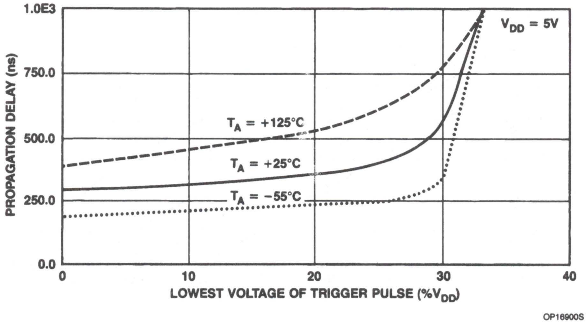


Low Output Voltage vs Output Sink Current

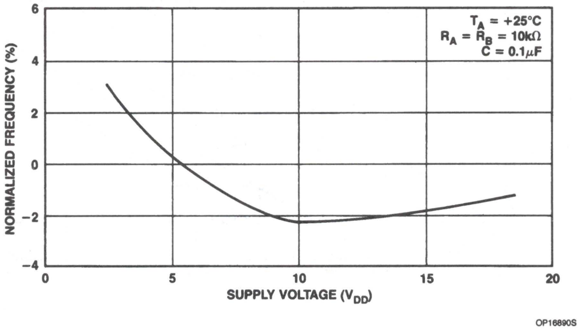


Minimum Pulse Width for Triggering

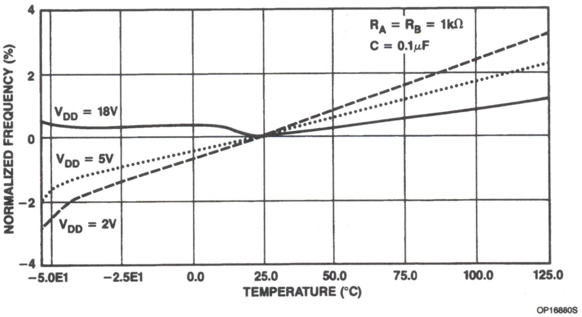
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Propagation Delay vs Voltage Level of Trigger Pulse

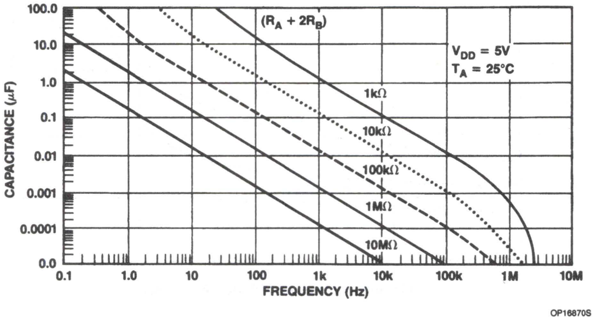


Normalized Frequency Stability as a Function of Supply Voltage Astable Mode)

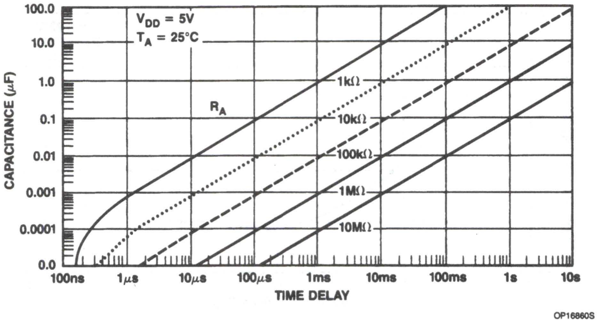


Normalized Frequency Stability as a Function of Temperature (Astable Mode)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Free-Running Frequency as a Function of R_A, R_B, and C



Monostable Time Delay vs R_A and C

APPLICATION NOTES

General

The ICM7555 device is, in most instances, a direct replacement for the NE/SE555 device. However, it is possible to effect economies in the external component count using the ICM7555. Because the bipolar 555 device produces large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555 device produces no such transients. See Figure 1.

The ICM7555 produces supply current spikes of only 2 – 3mA instead of 300 – 400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, 2 capacitors can be saved using an ICM7555.

Power Supply Considerations

Although the supply current consumed by the ICM7555 device is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 2 and 3.

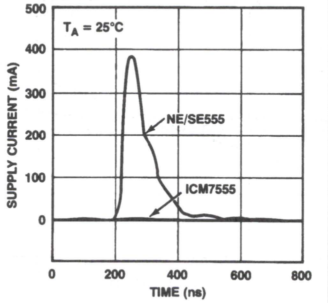


Figure 1. Supply Current Transient Compared With a Standard Bipolar 555 During an Output Transition

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the ICM7555 will drive at least 2 standard TTL loads.

Astable Operation

If the circuit is connected as shown in Figure 2, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus, the duty cycle (D) may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{DD} and 2/3 V_{DD}. Since the charge rate and the threshold levels are directly proportional to the supply voltage, the frequency of oscillation is independent of the supply voltage.

$$F = \frac{1.38}{(R_A + 2R_B}C \qquad D = \frac{R_A + R_B}{R_A + 2R_B}$$

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Initially, the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative TRIGGER pulse to Pin 2, the internal flip-flop is set which releases the short circuit across the external capacitor and drives the OUTPUT High. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. TRIGGER must return to a high state before the OUTPUT can return to a low state.

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode, or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

RESET

The RESET terminal is designed to have essentially the same trip voltage as the standard bipolar 555, i.e., 0.6 to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the RESET function is, however, much improved over the standard bipolar 555 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

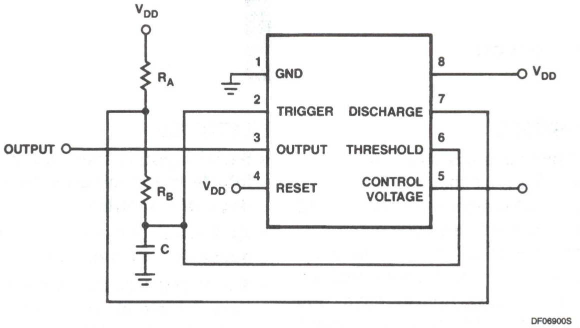

V_{DD}
R_A
R_B
C
OUTPUT
V_{DD}
1
2
3
4
GND
TRIGGER
OUTPUT
RESET
8
7
6
5
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
V_{DD}
DF06900S

Figure 2. Astable Operation

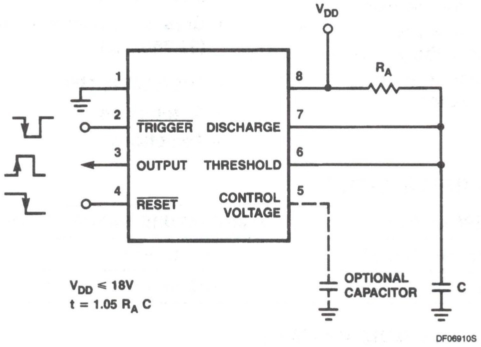

V_{DD}
R_A
1
2
3
4
TRIGGER
OUTPUT
RESET
8
7
6
5
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
OPTIONAL CAPACITOR
C
$V_{DD} \leq 18V$
$t = 1.05\ R_A\ C$
DF06910S

Figure 3. Monostable Operation

Signetics

PCF8573

Clock/Calendar With Serial I/O

Product Specification

Linear Products

DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real-time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two-lin bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2V nickel cadmium battery. The time base is generated from a 32.768kHz crystal-controlled oscillator.

FEATURES

- **Serial input/output bus (I^2C) interface for minutes, hours, days and months**
- **Additional pulse outputs for seconds and minutes**
- **Alarm register for presetting a time for alarm or remote switching functions**
- **Battery back-up for clock function during supply interruption**
- **Crystal oscillator control (32.768kHz)**

APPLICATIONS

- **Automotive**
- **Telephony**

ORDERING INFORMATION

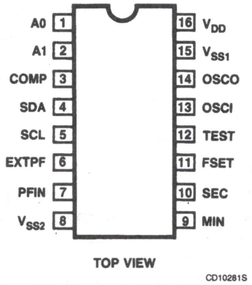
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to +85°C	PCF8573PN
16-Pin Plastic SOL (SOT-162A)	−40°C to +85°C	PCF8573T

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (clock)	−0.3 to 8	V
V_{SS2}	Supply voltage range (I^2C interface)	−0.3 to 8	V
I_{IN}	Input current	10	mA
I_{OUT}	Output current	10	mA
P_D	Maximum power dissipation per package	200	mW
T_A	Operating ambient temperature range	−40 to 85	°C
T_{STG}	Storage temperature range	−65 to 150	°C

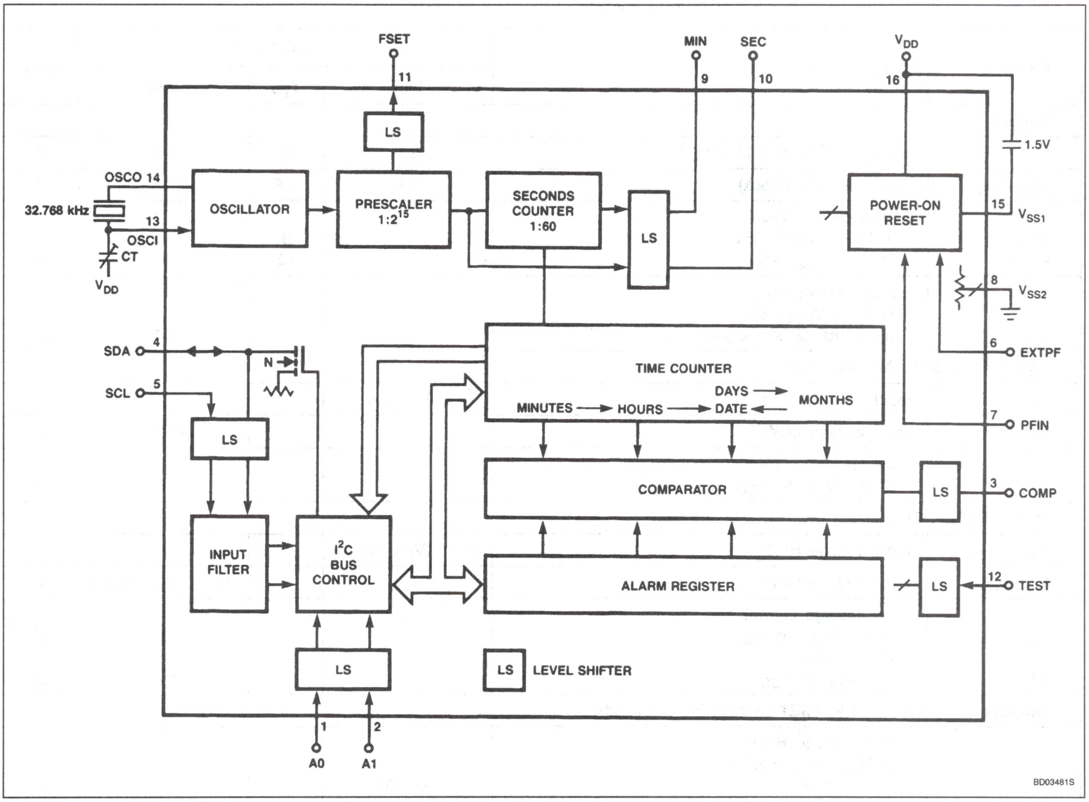
PIN CONFIGURATION

N, D Packages



PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address input
2	A1	Address input
3	COMP	Comparator output
4	SDA	Serial data line } I^2C bus
5	SCL	Serial clock line
6	EXTPF	Enable power fail flag input
7	PFIN	Power fail flag input
8	V_{SS2}	Negative supply 2 (I^2C interface)
9	MIN	One pulse per minute output
10	SEC	One pulse per second output
11	FSET	Oscillator tuning output
12	TEST	Test input; must be connected to V_{SS2} when not in use
13	OSCI	Oscillator input
14	OSCO	Oscillator input/output
15	V_{SS1}	Negative supply 1 (clock)
16	V_{DD}	Common positive supply

BLOCK DIAGRAM


FSET
11
MIN
9
SEC
10
VDD
16
1.5V
LS
OSCO 14
32.768 kHz
13
OSCI
CT
VDD
OSCILLATOR
PRESCALER 1:2^15
SECONDS COUNTER 1:60
LS
POWER-ON RESET
15
VSS1
8
VSS2
6
EXTPF
SDA
4
SCL
5
N
TIME COUNTER
DAYS
MONTHS
MINUTES
HOURS
DATE
7
PFIN
LS
COMPARATOR
LS
3
COMP
INPUT FILTER
I²C BUS CONTROL
ALARM REGISTER
LS
12
TEST
LS
LS
LEVEL SHIFTER
1
2
A0
A1
BD03481S

Clock/Calendar With Serial I/O PCF8573

DC ELECTRICAL CHARACTERISTICS V_{SS2} = 0V; T_A = −40 to + 85°C, unless otherwise specified. Typical values at T_A = + 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
$V_{DD} - V_{SS2}$	Supply voltage (I²C interface)	2.5	5	6.0	V
$V_{DD} - V_{SS1}$	Supply voltage (clock)	1.1	1.5	$(V_{DD} - V_{SS2})$	V
	Supply current V_{SS1}				
$-I_{SS1}$	at $V_{DD} - V_{SS1} = 1.5V$		3	10	µA
$-I_{SS1}$	at $V_{DD} - V_{SS1} = 5V$		12	50	µA
$-I_{SS2}$	Supply current V_{SS2} at $V_{DD} - V_{SS2} = 5V$ ($I_O = 0mA$ on all outputs)			50	µA
Inputs SCL, SDA, A0, A1, TEST					
V_{IH}	Input voltage HIGH	$0.7 \times V_{DD}$			V
V_{IL}	Input voltage LOW			$0.3 \times V_{DD}$	V
$\pm I_I$	Input leakage current at $V_I = V_{SS2}$ to V_{DD}			1	µA
Inputs EXTPF, PFIN					
$V_{IH} - V_{SS1}$	Input voltage HIGH	$0.7 \times (V_{DD} - V_{SS1})$			V
$V_{IL} - V_{SS1}$	Input voltage LOW	0		$0.3 \times (V_{DD} - V_{SS1})$	V
$\pm I_I$	Input leakage current at $V_I = V_{SS1}$ to V_{DD}			1	µA
$\pm I_I$	at $T_A = 25°C$; $V_I = V_{SS1}$ to V_{DD}			0.1	µA
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
V_{OH}	Output voltage HIGH at $V_{DD} - V_{SS2} = 2.5V$; $-I_O = 0.1mA$	$V_{DD} - 0.4$			V
V_{OH}	at $V_{DD} - V_{SS2} = 4$ to $6V$; $-I_O = 0.5mA$	$V_{DD} - 0.4$			V
V_{OL}	Output voltage LOW at $V_{DD} - V_{SS2} = 2.5V$; $I_O = 0.3mA$			0.4	V
V_{OL}	at $V_{DD} - V_{SS2} = 4$ to $6V$; $I_O = 1.6mA$			0.4	V
Output SDA (N-Channel open drain)					
V_{OL}	Output 'ON': $I_O = 3mA$ at $V_{DD} - V_{SS2} = 2.5$ to $6V$			0.4	V
I_O	Output 'OFF' (leakage current) at $V_{DD} - V_{SS2} = 6V$; $V_O = 6V$			1	µA
Internal Threshold Voltage					
V_{TH1}	Power failure detection	1	1.2	1.4	V
V_{TH2}	Power 'ON' reset at $V_{SCL} = V_{SDA} = V_{DD}$	1.5	2.0	2.5	V

Clock/Calendar With Serial I/O

PCF8573

AC ELECTRICAL CHARACTERISTICS V_{SS2} = 0V; T_A = −40 to +85°C, unless otherwise specified. Typical values at T_A = +25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Rise and Fall Times of Input Signals					
t_R, t_F	Input EXTPF			1	μs
t_R, t_F	Input PFIN			∞	μs
	Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels				
t_R	rise time			1	μs
t_F	fall time			0.3	μs
Frequency at SCL					
t_{LOW}	at $V_{DD} - V_{SS2}$ = 4 to 6V Pulse width LOW (see Figures 7 and 9	4.7			μs
t_{HIGH}	Pulse width HIGH (see Figures 7 and 9	4			μs
t_I	Noise suppression time constant at SCL and SDA input	0.25	1	2.5	μs
c_{IN}	Input capacitance (SCL, SDA)			7	pF
Oscillator					
C_{OUT}	Integrated oscillator capacitance		40		pF
R_F	Oscillator feedback resistance		3		MΩ
f/f_{OSC}	Oscillator stability for: $\triangle(V_{DD} - V_{SS1})$ = 100mV at $V_{DD} - V_{SS1}$ = 1.55V; T_A = 25°C		2×10^{-6}		
	Quartz crystal parameters				
	Frequency = 32.768 kHz				
R_S	Series resistance			40	kΩ
C_L	Parallel capacitance		9		pF
C_T	Trimmer capacitance	5		25	pF

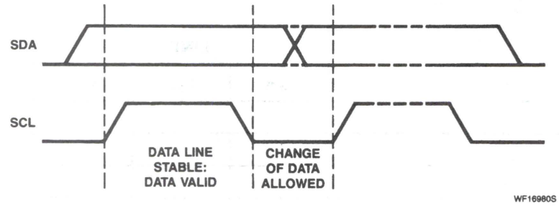


Figure 1. Bit Transfer

Table 1. Cycle Length of the Time Counter

UNIT	NUMBER OF BITS	COUNTING CYCLE	CARRY FOR FOLLOWING UNIT	CONTENT OF MONTH COUNTER
Minutes	7	00 to 59	59 → 00	
Hours	6	00 to 23	23 → 00	
Days	6	01 to 28	28 → 01 or 29 → 01	2 (see note)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
Months	5	01 to 12	12 → 01	

NOTE: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the time base for the prescaler. The frequency is determined by a single 32.768kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and Time Counter

The prescaler provides a 128Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC and MIN, respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1:1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Alarm Register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Table 2. Power Fail Selection

EXTPF	PFIN	FUNCTION
0	0	Power fail is sensed internally
0	1	Test mode
1	0	Power fail is sensed externally
1	1	No power fail sensed

NOTE:
0: connected to V_{SS1} (LOW)
1: connected to V_{DD} (HIGH)

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal, the flag COMP will be set 4ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set, and then it will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

Power On/Power Fail Detection

If the voltage $V_{DD} - V_{SS1}$ falls below a certain value, the operation of the clock becomes undefined. Thus, a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTIVE ADDRESS has been received. The flag POWF can be set by an internally-generated power fail level-discriminator signal for application with ($V_{DD} - V_{SS1}$) greater than V_{TH1}, or by an externally-generated power fail signal for application with ($V_{DD} - V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally-or externally-controlled POWF can be selected by input EXTPF as shown in Table 2.

The external power fail control operates by absence of the $V_{DD} - V_{SS2}$ supply. Therefore, the input levels applied to PFIN and EXTPF must be within the range of $V_{DD} - V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power-on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD} - V_{SS2}$ is less than V_{TH2}.

Clock/Calendar With Serial I/O PCF8573

Interface Level Shifters

The level shifters adjust the 5V operating voltage ($V_{DD} - V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD} - V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD} - V_{SS2}$ supply voltage. If the voltage $V_{DD} - V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD} - V_{SS2}$ and the $V_{DD} - V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD} - V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer (see Figure 1)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and Stop Conditions (see Figure 2)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System Configuration (see Figure 3)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge (see Figure 4)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse. So that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition (see Figures 11 and 12).

Timing Specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-Speed Mode — Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 5.

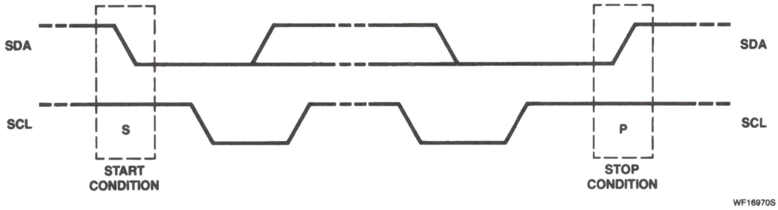


Figure 2. Definition of Start and Stop Conditions

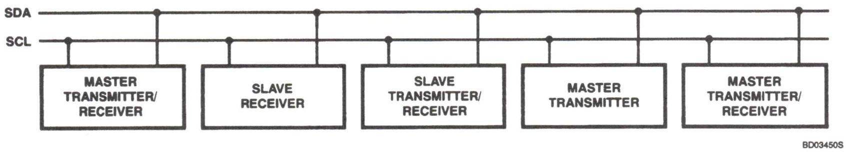

SDA
SCL
MASTER TRANSMITTER/ RECEIVER
SLAVE RECEIVER
SLAVE TRANSMITTER/ RECEIVER
MASTER TRANSMITTER
MASTER TRANSMITTER/ RECEIVER
BD03450S

Figure 3. System Configuration

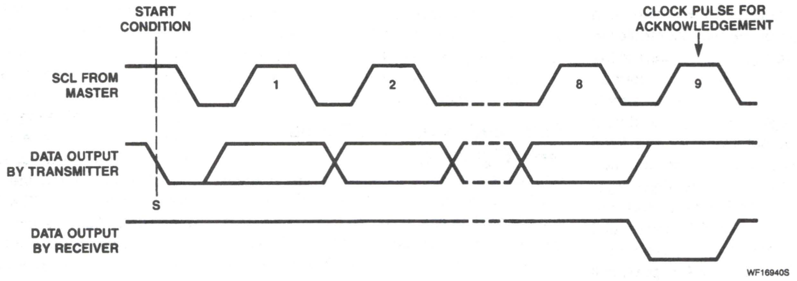
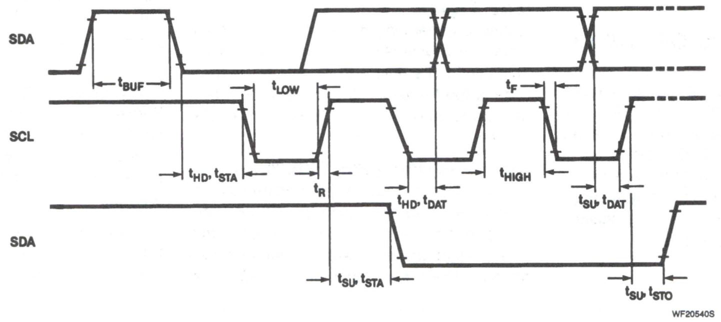

START CONDITION
CLOCK PULSE FOR ACKNOWLEDGEMENT
SCL FROM MASTER
1
2
8
9
DATA OUTPUT BY TRANSMITTER
S
DATA OUTPUT BY RECEIVER
WF16940S

Figure 4. Acknowledgement on the I^2C Bus


SDA
t_{BUF}
t_{LOW}
t_F
SCL
t_{HD}, t_{STA}
t_R
t_{HD}, t_{DAT}
t_{HIGH}
t_{SU}, t_{DAT}
SDA
t_{SU}, t_{STA}
t_{SU}, t_{STO}
WF20540S

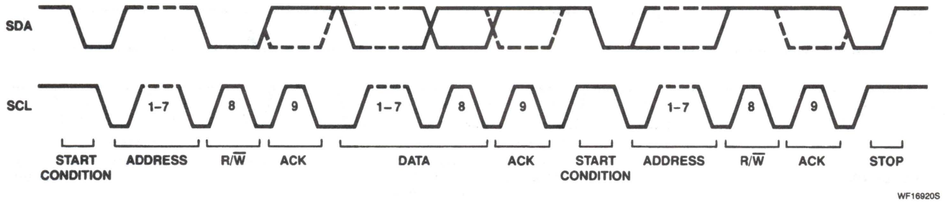
Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
t_{HD}, t_{STA}	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	$4.7\mu s$	Clock LOW period
$t_{HIGHmin}$	$4\mu s$	Clock HIGH period
t_{SU}, t_{STA}	$t \geqslant t_{LOWmin}$	Start condition setup time, only valid for repeated start code
t_{HD}, t_{DAT}	$t \geqslant 0\mu s$	Data hold time
t_{SU}, t_{DAT}	$t \geqslant 250ns$	Data setup time
t_R	$t \leqslant 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300ns$	Fall time of both the SDA and SCL line
t_{SU}, t_{STO}	$t \geqslant t_{LOWmin}$	Stop condition setup time

NOTE:

1. All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

Figure 5. Timing of the High-Speed Mode

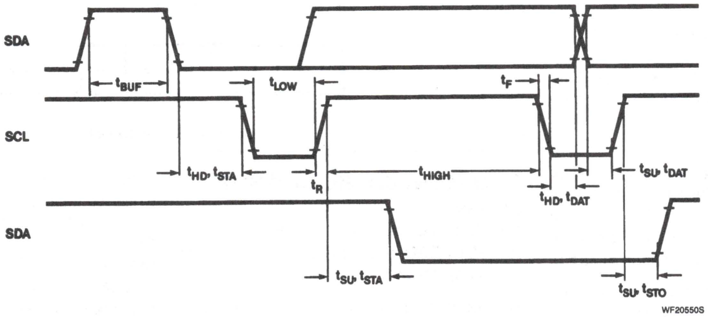

SDA
SCL
1–7
8
9
1–7
8
9
1–7
8
9
START CONDITION
ADDRESS
R/$\overline{W}$
ACK
DATA
ACK
START CONDITION
ADDRESS
R/$\overline{W}$
ACK
STOP
WF16920S

Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Figure 6. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode — Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105μs and a minimum HIGH period of 365μs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 7.


SDA
SCL
SDA
t_{BUF}
t_{LOW}
t_F
t_{HD}, t_{STA}
t_R
t_{HIGH}
t_{HD}, t_{DAT}
t_{SU}, t_{DAT}
t_{SU}, t_{STA}
t_{SU}, t_{STO}
WF20550S

Where:

t_{BUF}	$t \geqslant 105\mu s$ (t_{LOWmin})
t_{HD}, t_{STA}	$t \geqslant 365\mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\mu s \pm 25\mu s$
t_{HIGH}	$390\mu s \pm 25\mu s$
t_{SU}, t_{STA}	$130\mu s \pm 25\mu s$*
t_{HD}, t_{DAT}	$t \geqslant 0\mu s$
t_{SU}, t_{DAT}	$t \geqslant 250ns$
t_R	$t \leqslant 1\mu s$
t_F	$t \leqslant 300ns$
t_{SU}, t_{STO}	$130\mu s \pm 25\mu s$

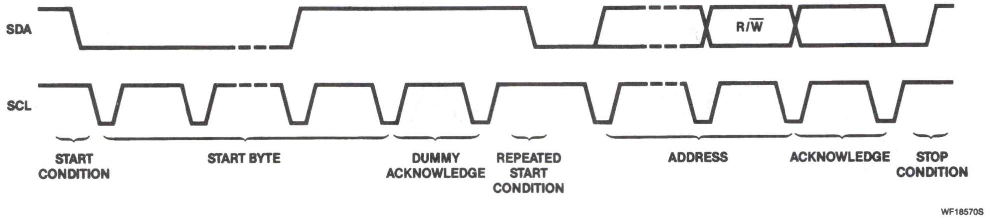
*Only valid for repeated start code.

NOTE:

1. All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}; for definitions see high-speed mode.

Figure 7. Timing of the Low-Speed Mode

Clock/Calendar With Serial I/O PCF8573


SDA
SCL
R/$\overline{W}$
START CONDITION
START BYTE
DUMMY ACKNOWLEDGE
REPEATED START CONDITION
ADDRESS
ACKNOWLEDGE
STOP CONDITION
WF18570S

Where:

Clock t_{LOWmin}	130µs ± 25µs
$t_{HIGHmin}$	390µs ± 25µs
Mark-to-space ratio	1:3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

NOTE:
1. The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: *ICs for digital systems in radio, audio and video equipment.*

Figure 8. Complete Data Transfer in the Low-Speed Mode

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave Address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore, the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Figure 9.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

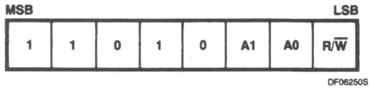

MSB
LSB
1
1
0
1
0
A1
A0
R/$\overline{W}$
DF06250S

Figure 9. Slave Address

Clock/Calendar READ/WRITE Cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Figures 10 and 11.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

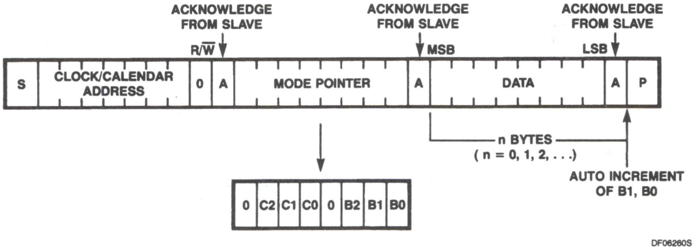

ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM SLAVE
R/$\overline{W}$
MSB
LSB
S
CLOCK/CALENDAR ADDRESS
0
A
MODE POINTER
A
DATA
A
P
n BYTES
(n = 0, 1, 2, . . .)
AUTO INCREMENT OF B1, B0
0
C2
C1
C0
0
B2
B1
B0
DF06260S

Figure 10. Master Transmitter Transmits to Clock/Calendar Slave Receiver

Table 3. CONTROL-nibble

	C2	C1	C0	FUNCTION
0	0	0	0	Execute address
0	0	0	1	Read control/status flags
0	0	1	0	Reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	Time adjust, with carry for minute counter[1]
0	1	0	0	Reset NODA flag
0	1	0	1	Set NODA flag
0	1	1	0	Reset COMP flag

NOTE:

1. If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 sec. From the count 30 there is a carry which adjusts the time by max. +30 sec.

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register, respectively.

Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

Table 4. ADDRESS-nibble

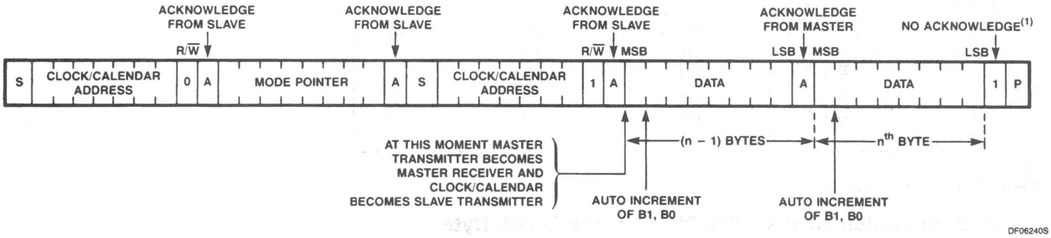
	B2	B1	B0	ADDRESSED TO:
0	0	0	0	Time counter hours
0	0	0	1	Time counter minutes
0	0	1	0	Time counter days
0	0	1	1	Time counter months
0	1	0	0	Alarm register hours
0	1	0	1	Alarm register minutes
0	1	1	0	Alarm register days
0	1	1	1	Alarm register months

Table 5. Placement of BCD Digits in the DATA Byte

MSB			DATA				LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
X	X	D	D	D	D	D	D	Hours
X	D	D	D	D	D	D	D	Minutes
X	X	D	D	D	D	D	D	Days
X	X	X	D	D	D	D	D	Months

NOTE:

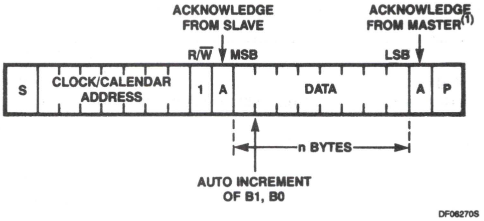
1. Where "X" is the don't care bit and "D" is the data bit.


ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM MASTER
NO ACKNOWLEDGE(1)
R/W
R/W
MSB
LSB
MSB
LSB
S
CLOCK/CALENDAR ADDRESS
0
A
MODE POINTER
A
S
CLOCK/CALENDAR ADDRESS
1
A
DATA
A
DATA
1
P
AT THIS MOMENT MASTER TRANSMITTER BECOMES MASTER RECEIVER AND CLOCK/CALENDAR BECOMES SLAVE TRANSMITTER
(n − 1) BYTES
nth BYTE
AUTO INCREMENT OF B1, B0
AUTO INCREMENT OF B1, B0
DF06240S

NOTE:

The master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave.

Figure 11. Master Transmitter Reads Clock/Calendar After Setting Mode Pointer


ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM MASTER(1)
R/$\overline{W}$
MSB
LSB
S
CLOCK/CALENDAR ADDRESS
1
A
DATA
A
P
n BYTES
AUTO INCREMENT OF B1, B0
DF06270S

NOTE:
The master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave.

Figure 12. Master Reads Clock/Calendar Immediately After First Byte

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER conditon occurs.

Table 6. Slave Receiver Acknowledgement

MODE POINTER								ACKNOWLEDGE ON BYTE		
								Address	Mode pointer	Data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

NOTE:
1. Where "X" is the don't care bit.

Table 7. Organization of the BCD Digits in the DATA Byte

MSB		DATA				LSB		ADDRESSED TO:
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	
0	0	D	D	D	D	D	D	Hours
0	D	D	D	D	D	D	D	Minutes
0	0	D	D	D	D	D	D	Days
0	0	0	D	D	D	D	D	Months
0	0	0	*	**	NODA	COMP	POWF	Control/status flags

NOTES:
1. Where: "D" is the data bit, * = minutes, ** = seconds.

APPLICATION INFORMATION

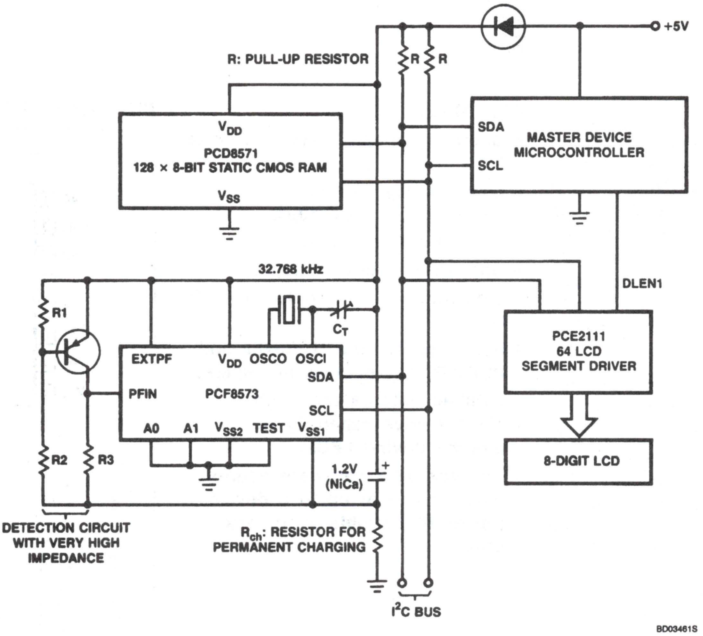

+5V
R: PULL-UP RESISTOR
R
R
V_{DD}
PCD8571
128 × 8-BIT STATIC CMOS RAM
V_{SS}
SDA
SCL
MASTER DEVICE MICROCONTROLLER
DLEN1
32.768 kHz
C_T
R1
EXTPF
V_{DD} OSCO OSCI
SDA
PFIN
PCF8573
SCL
A0 A1 V_{SS2} TEST V_{SS1}
PCE2111
64 LCD
SEGMENT DRIVER
8-DIGIT LCD
R2
R3
1.2V (NiCa)
DETECTION CIRCUIT WITH VERY HIGH IMPEDANCE
R_{ch}: RESISTOR FOR PERMANENT CHARGING
I^2C BUS
BD03461S

Figure 13. Application Example of the PCF8573 Clock/Calendar

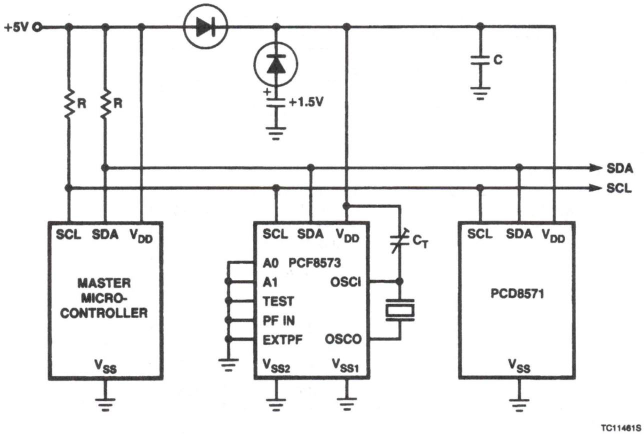

+5V
R
R
+1.5V
C
SDA
SCL
SCL SDA V_{DD}
MASTER MICRO-CONTROLLER
V_{SS}
SCL SDA V_{DD}
A0 PCF8573
A1 OSCI
TEST
PF IN
EXTPF OSCO
V_{SS2} V_{SS1}
C_T
SCL SDA V_{DD}
PCD8571
V_{SS}
TC11461S

Figure 14. Application Example of the PCF8573 With Common V_{SS1} and V_{SS2} Supply

Signetics

PCF8574
8-Bit Remote I/O Expander

Product Specification

Linear Products

DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I^2C). It can also interface microcomputers without a serial interface to the I^2C bus (as a slave function only). The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.

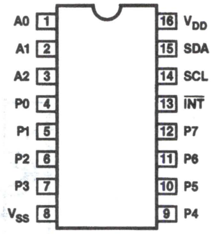
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C bus. This means that the PCF8574 can remain a simple slave device.

FEATURES

- **Operating supply voltage: 2.5V to 6V**
- **Low standby current consumption: max. 10μA**
- **Bidirectional expander**
- **Open-drain interrupt output**
- **8-bit remote I/O port for the I^2C bus**
- **Peripheral for the MAB8400 and PCF8500 microcomputer families**
- **Latched outputs with high current drive capability for directly driving LEDs**
- **Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD07880S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address inputs
2	A1	
3	A2	
4	P0	8-bit quasi-bidirectional I/O ports
5	P1	
6	P2	
7	P3	
8	V_{SS}	
9	P4	8-bit quasi-bidirectional I/O ports
10	P5	
11	P6	
12	P7	
13	$\overline{INT}$	Interrupt output
14	SCL	Serial clock line
15	SDA	Serial data line
16	V_{DD}	Positive supply

ORDERING INFORMATION

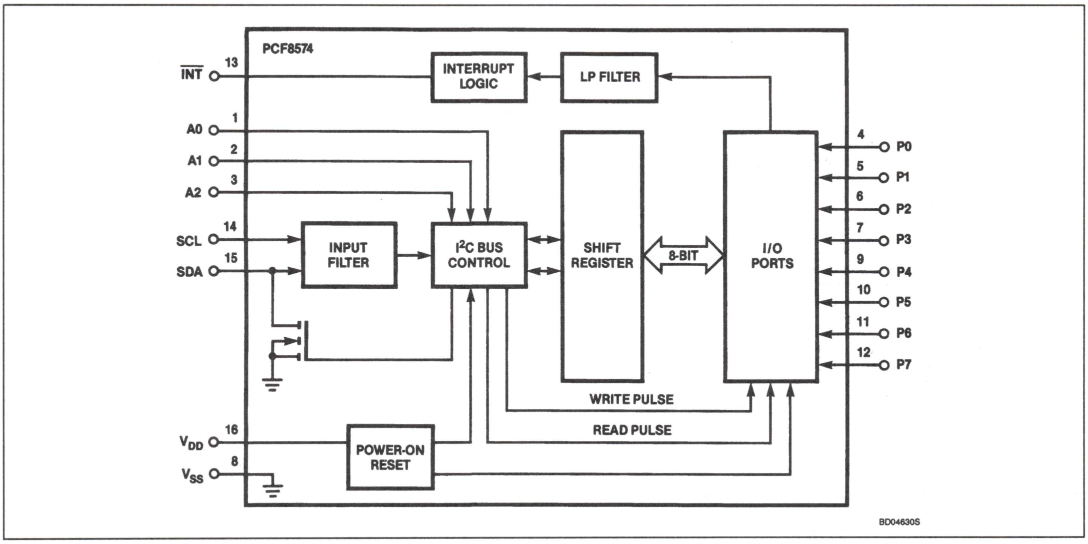
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to +85°C	PCF8574PN
16-Pin Plastic SO package (SO16L; SOT-162A)	−40°C to +85°C	PCF8574TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to +7	V
V_I	Input voltage range (any pin)	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
$\pm I_I$	DC current into any input	20	mA
$\pm I_O$	DC current into any output	25	mA
$\pm I_{DD}$; I_{SS}	V_{DD} or V_{SS} current	100	mA
P_{TOT}	Total power dissipation	400	mW
P_O	Power dissipation per output	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

8-Bit Remote I/O Expander PCF8574

BLOCK DIAGRAM


PCF8574
INT
13
A0
1
A1
2
A2
3
SCL
14
SDA
15
VDD
16
VSS
8
INTERRUPT LOGIC
LP FILTER
INPUT FILTER
I²C BUS CONTROL
SHIFT REGISTER
8-BIT
I/O PORTS
POWER-ON RESET
WRITE PULSE
READ PULSE
4 P0
5 P1
6 P2
7 P3
9 P4
10 P5
11 P6
12 P7
BD04630S

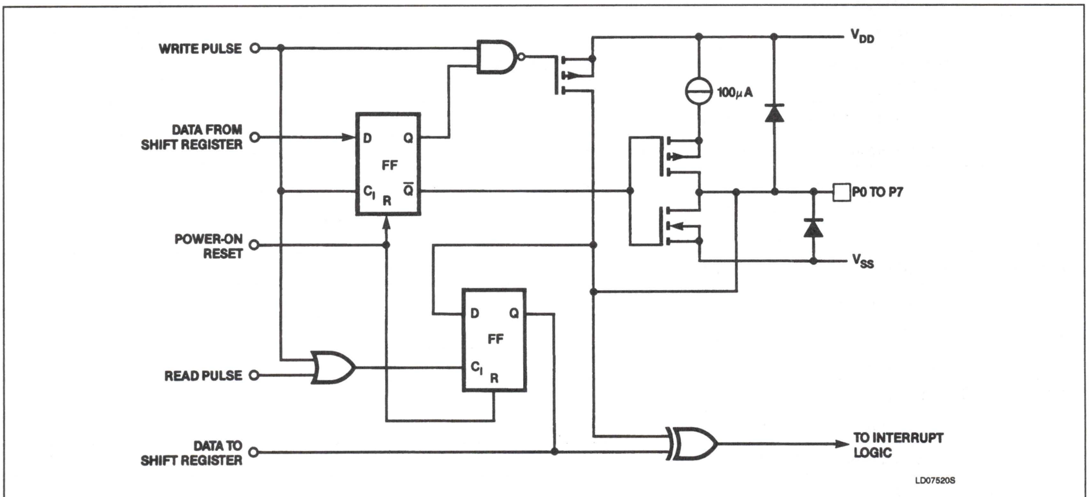

WRITE PULSE
DATA FROM SHIFT REGISTER
POWER-ON RESET
READ PULSE
DATA TO SHIFT REGISTER
D
Q
FF
CI
R
Q̄
D
Q
FF
CI
R
VDD
100μA
P0 TO P7
VSS
TO INTERRUPT LOGIC
LD07520S

Figure 1. Simplified Schematic Diagram of Each Port

DC ELECTRICAL CHARACTERISTICS $V_{DD} = 2.5$ to 6V; $V_{SS} = 0V$; $T_A = -40°C$ to $+85°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 16)					
V_{DD}	Supply voltage	2.5		6	V
 I_{DD} I_{DDO}	Supply current at $V_{DD} = 6V$; no load, inputs at V_{DD}, V_{SS} operating standby			 100 10	 µA µA
V_{REF}	Power-on reset voltage level[1]		1.3	2.4	V
Input SCL; input/output SDA (Pins 14; 15)					
V_{IL}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		$V_{DD} + 0.5$	V
I_{OL}	Output current LOW at $V_{OL} = 0.4V$	3			mA
$\|I_{LI}\|$	Input/output leakage current			100	nA
f_{SCL}	Clock frequency (See Figure 6)			100	kHz
t_S	Tolerable spike width at SCL and SDA input			100	ns
C_I	Input capacitance (SCL, SDA) at $V_I = V_{SS}$			7	pF
I/O ports (Pins 4 to 7; 9 to 12)					
V_{IL}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		$V_{DD} + 0.5V$	V
$\pm I_{IHL}$	Maximum allowed input current through protection diode at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$			400	µA
I_{OL}	Output current LOW at $V_{OL} = 1V$; $V_{DD} = 2.5V$	5			mA
$-I_{OH}$	Output current HIGH at $V_{OH} = V_{SS}$ (current source only)	30	100	300	µA
$-I_{OH}t$	Transient pull-up current HIGH during acknowledge (see Figure 14) at $V_{OH} = V_{SS}$		0.5		mA
$C_{I/O}$	Input/output capacitance			10	pF
Port timing; $C_L \leqslant 100pF$ (see Figures 10 and 11)					
t_{PV}	Output data valid			4	µs
t_{PS}	Input data setup	0			µs
t_{PH}	Input data hold	4			µs
Interrupt $\overline{INT}$ (Pin 13)					
I_{OL}	Output current LOW at $V_{OL} = 0.4V$	1.6			mA
$\|I_{OH}\|$	Output current HIGH at $V_{OH} = V_{DD}$			100	nA
$\overline{INT}$ timing; $C_L \leqslant 100pF$ (see Figure 11)					
t_{IV} t_{IR}	Input data valid Reset delay			4 4	µs µs
Select inputs A0, A1, A2 (Pins 1 to 3)					
V_{IH}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		$V_{DD} + 0.5V$	V
$\|I_{L}\|$	Input leakage current at $V_I = V_{DD}$ or V_{SS}			100	nA

NOTE:

1. The power-on reset circuit resets the I^2C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

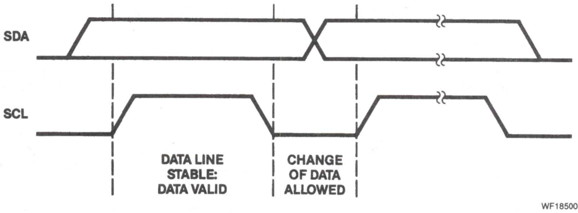

SDA
SCL
DATA LINE STABLE: DATA VALID
CHANGE OF DATA ALLOWED
WF18500S

Figure 2. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

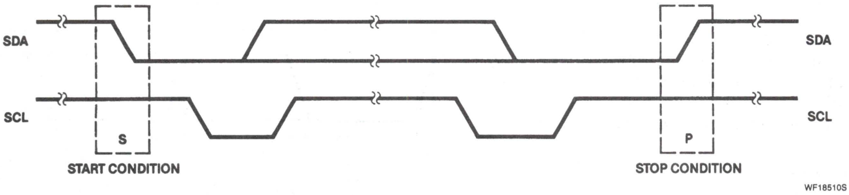

SDA
SCL
S
START CONDITION
SDA
SCL
P
STOP CONDITION
WF18510S

Figure 3. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

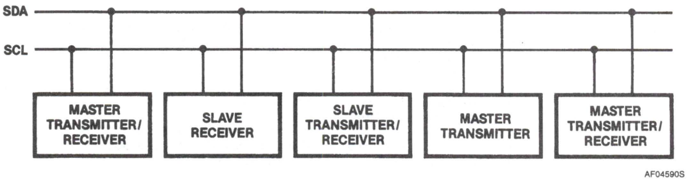

SDA
SCL
MASTER TRANSMITTER/ RECEIVER
SLAVE RECEIVER
SLAVE TRANSMITTER/ RECEIVER
MASTER TRANSMITTER
MASTER TRANSMITTER/ RECEIVER
AF04590S

Figure 4. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge. Related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

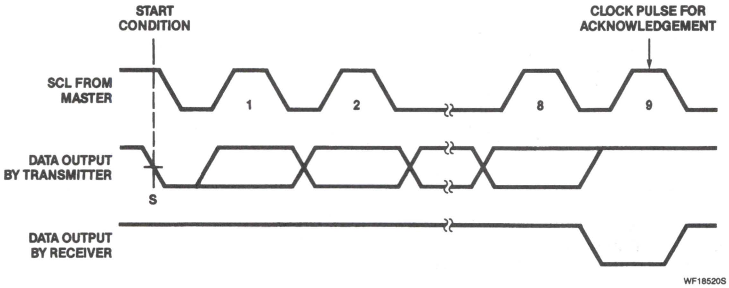


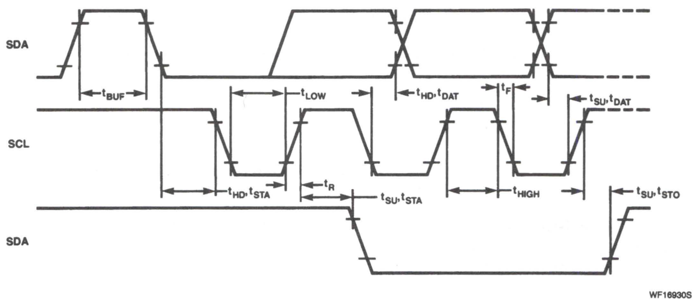
Figure 5. Acknowledgement on the I²C Bus

Timing Specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-Speed Mode

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 6.



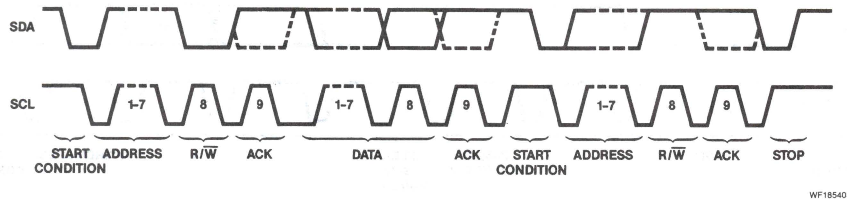
Where:

t_{BUF}	$t \geqslant t_{LOW\ min}$	The minimum time the bus must be free before a new transmission can start
$t_{HD};\ t_{STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
$t_{SU};\ t_{STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time; only valid for repeated start code
$t_{HD};\ t_{DAT}$	$t \geqslant 0\mu s$	Data hold time
$t_{SU};\ t_{DAT}$	$t \geqslant 250ns$	Data setup time
t_R	$t \leqslant 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300ns$	Fall time of both the SDA and SCL line
$t_{SU};\ t_{STO}$	$t \geqslant t_{LOWmin}$	Stop condition setup time

NOTE:
All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 6. Timing of the High-Speed Mode

8-Bit Remote I/O Expander PCF8574


SDA
SCL
1-7
8
9
1-7
8
9
1-7
8
9
START CONDITION
ADDRESS
R/$\overline{W}$
ACK
DATA
ACK
START CONDITION
ADDRESS
R/$\overline{W}$
ACK
STOP
WF18540S

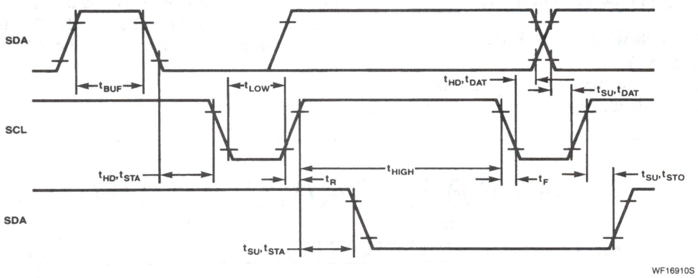
Where:

Clock t_{LOWmin}	4.7µs
$t_{HIGHmin}$	4µs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Maximum number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Figure 7. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode

Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105µs and a minimum HIGH period of 365µs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 8.


SDA
SCL
SDA
t_{BUF}
t_{LOW}
t_{HD}, t_{DAT}
t_{SU}, t_{DAT}
t_{HD}, t_{STA}
t_R
t_{HIGH}
t_F
t_{SU}, t_{STO}
t_{SU}, t_{STA}
WF16910S

Where:

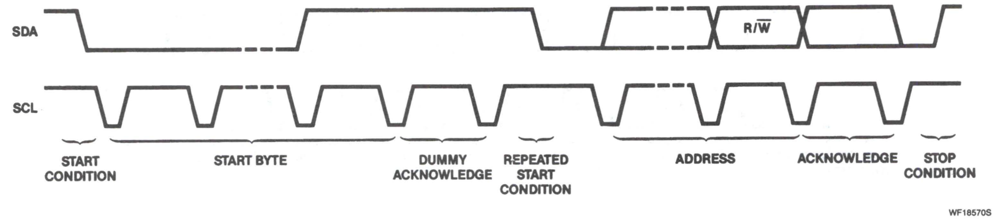
t_{BUF}	$t \geq 105µs$ (t_{LOWmin})
t_{HD}; t_{STA}	$t \geq 365µs$ ($t_{HIGHmin}$)
t_{LOW}	130µs ± 25µs
t_{HIGH}	390µs ± 25µs
t_{SU}; t_{STA}	130µs ± 25µs*
t_{HD}; t_{DAT}	$t \geq 0µs$
t_{SU}; t_{DAT}	$t \geq 250ns$
t_R	$t \leq 1µs$
t_F	$t \leq 300ns$
t_{SU}; t_{STO}	130µs ± 25µs

NOTES:

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

* Only valid for repeated start code.

Figure 8. Timing of the Low-Speed Mode


SDA
SCL
R/$\overline{W}$
START CONDITION
START BYTE
DUMMY ACKNOWLEDGE
REPEATED START CONDITION
ADDRESS
ACKNOWLEDGE
STOP CONDITION
WF18570S

Where:

Clock t_{LOWmin}	130µs ± 25µs
$t_{HIGHmin}$	390µs ± 25µs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Figure 9. Complete Data Transfer in the Low-Speed Mode

FUNCTIONAL DESCRIPTION

Addressing (See Figures 10 and 11)

Each bit of the PCF8574 I/O port can be independently used as an input or an output.

Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

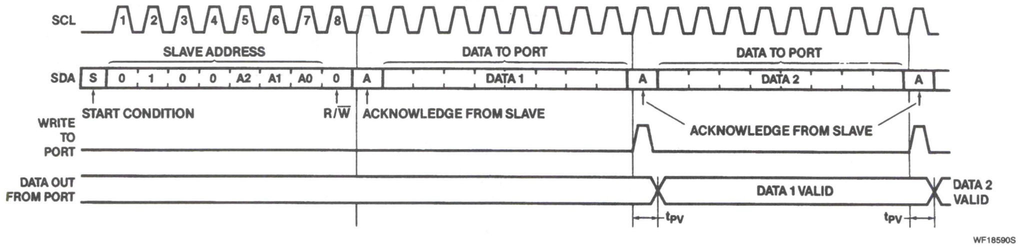
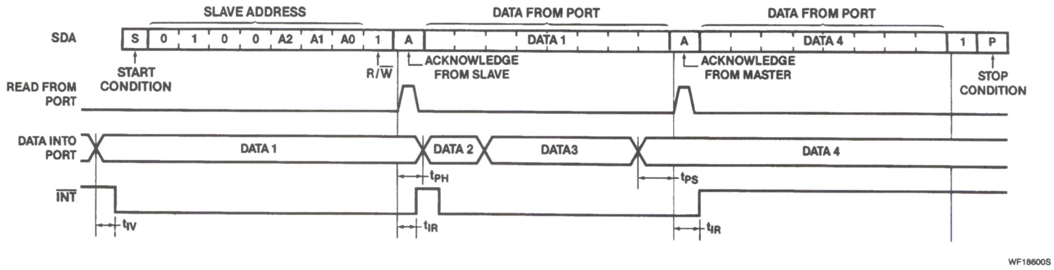

SCL
1 2 3 4 5 6 7 8
SLAVE ADDRESS
DATA TO PORT
DATA TO PORT
SDA
S 0 1 0 0 A2 A1 A0 0 A
DATA 1
A
DATA 2
A
START CONDITION
R/$\overline{W}$
ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM SLAVE
WRITE TO PORT
DATA OUT FROM PORT
DATA 1 VALID
DATA 2 VALID
t_{PV}
t_{PV}
WF18590S

Figure 10. WRITE Mode (Output Port)


SLAVE ADDRESS
DATA FROM PORT
DATA FROM PORT
SDA
S 0 1 0 0 A2 A1 A0 1 A
DATA 1
A
DATA 4
1 P
START CONDITION
R/$\overline{W}$
ACKNOWLEDGE FROM SLAVE
ACKNOWLEDGE FROM MASTER
STOP CONDITION
READ FROM PORT
DATA INTO PORT
DATA 1
DATA 2
DATA3
DATA 4
t_{PH}
t_{PS}
$\overline{INT}$
t_{IV}
t_{IR}
t_{IR}
WF18600S

NOTE:
A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Figure 11. READ Mode (Input Port)

Interrupt (See Figures 12 and 13)

The PCF8574 provides an open-drain output ($\overline{\text{INT}}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{IV} the signal $\overline{\text{INT}}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt. Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{\text{INT}}$.

Reading from or writing to another device does not affect the interrupt circuit.

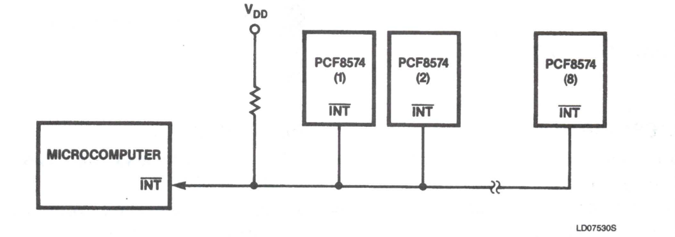

V_DD
PCF8574 (1)
PCF8574 (2)
PCF8574 (8)
INT
INT
INT
MICROCOMPUTER
INT
LD07530S

Figure 12. Application of Multiple PCF8574s With Interrupt

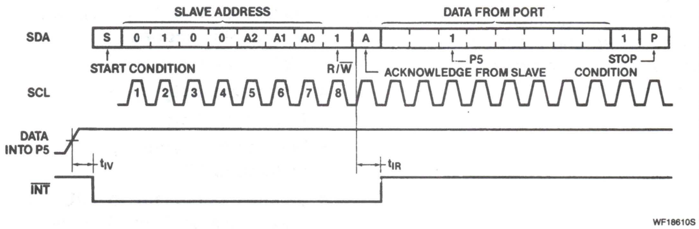

SLAVE ADDRESS
DATA FROM PORT
SDA
S
0
1
0
0
A2
A1
A0
1
A
1
1
P
START CONDITION
R/W
ACKNOWLEDGE FROM SLAVE
P5
STOP CONDITION
SCL
1
2
3
4
5
6
7
8
DATA INTO P5
t_IV
t_IR
INT
WF18610S

Figure 13. Interrupt Generated by a Change of Input to Port P5

Quasi-Bidirectional I/O Ports (See Figure 14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW-to-HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

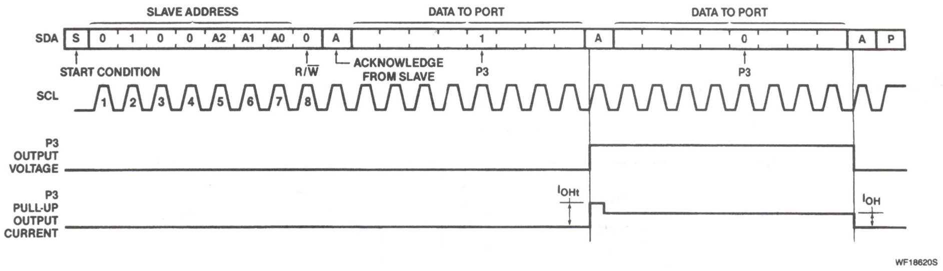

SLAVE ADDRESS
DATA TO PORT
DATA TO PORT
SDA
S
0
1
0
0
A2
A1
A0
0
A
1
A
0
A
P
START CONDITION
R/W
ACKNOWLEDGE FROM SLAVE
P3
P3
SCL
1
2
3
4
5
6
7
8
P3 OUTPUT VOLTAGE
P3 PULL-UP OUTPUT CURRENT
I_OHt
I_OH
WF18620S

Figure 14. Transient Pull-Up Current I_{OHt} While P3 Changes From LOW-to-HIGH and Back to LOW

Signetics

NE/SA/SE556/NE/SA/SE556-1/SE556-1C
Dual Timer

Product Specification

Linear Products

DESCRIPTION

Both the 556 and 556-1 Dual Monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. The 556 and 556-1 are a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other, sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

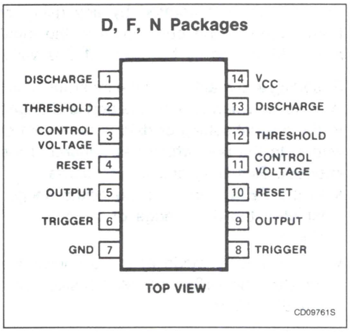
FEATURES

- Turn-off time less than 2μs (556-1, 1C)
- Maximum operating frequency > 500kHz (556-1, 1C)
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005%/°C
- SE556-1 compliant to MIL-STD or JAN available from Signetics' Military Division

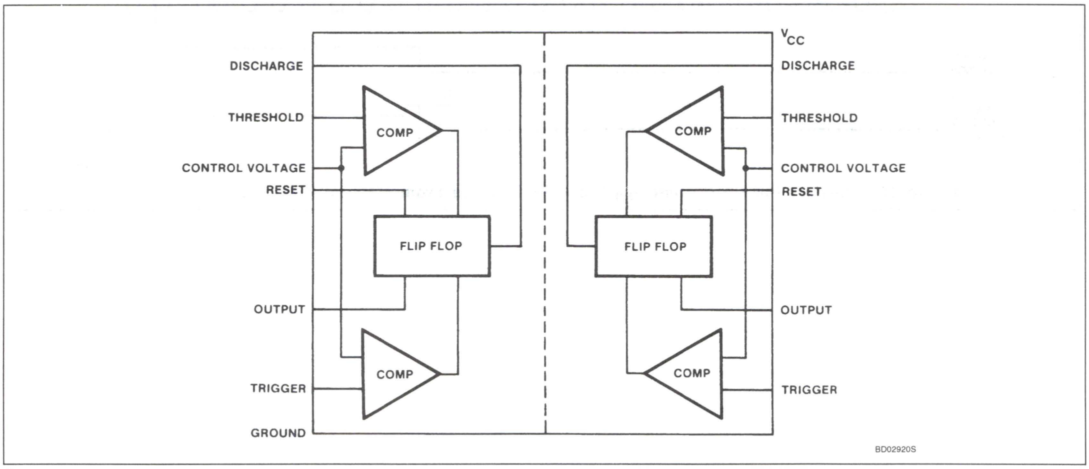
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch-Tone® encoder

PIN CONFIGURATION

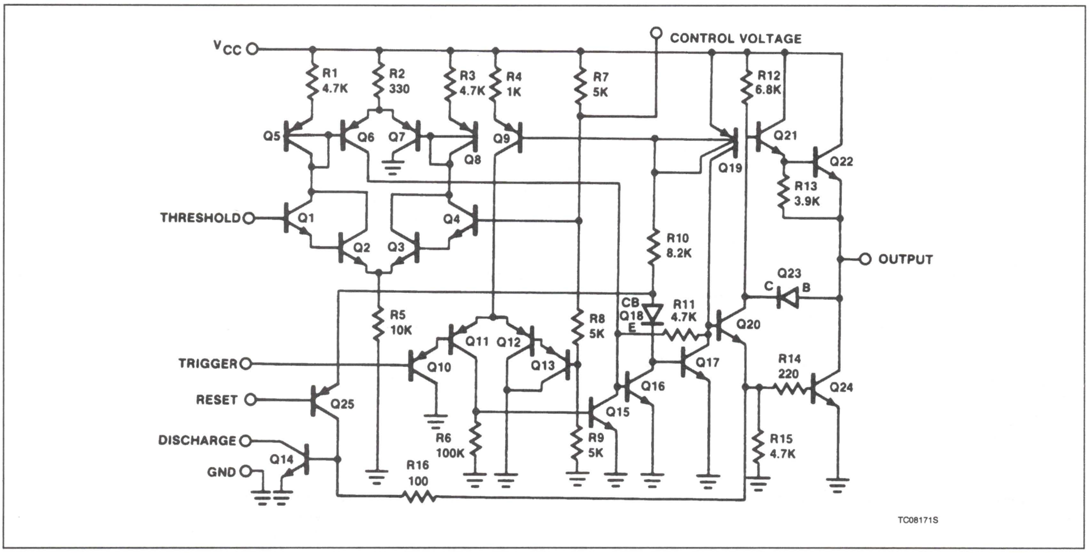

D, F, N Packages
DISCHARGE 1
THRESHOLD 2
CONTROL VOLTAGE 3
RESET 4
OUTPUT 5
TRIGGER 6
GND 7
14 V_{CC}
13 DISCHARGE
12 THRESHOLD
11 CONTROL VOLTAGE
10 RESET
9 OUTPUT
8 TRIGGER
TOP VIEW
CD09761S

BLOCK DIAGRAM


DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
GROUND
COMP
FLIP FLOP
COMP
V_{CC}
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
COMP
FLIP FLOP
COMP
BD02920S

®Touch-Tone is a registered trademark of AT&T

EQUIVALENT SCHEMATIC (Shown for one circuit only)


VCC
CONTROL VOLTAGE
R1 4.7K
R2 330
R3 4.7K
R4 1K
R7 5K
R12 6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R13 3.9K
THRESHOLD
Q1
Q2
Q3
Q4
R10 8.2K
OUTPUT
Q23
C
B
R5 10K
CB
Q18
E
R11 4.7K
R8 5K
Q20
Q11
Q12
TRIGGER
Q10
Q13
Q17
R14 220
Q24
RESET
Q25
Q16
Q15
DISCHARGE
Q14
R6 100K
R9 5K
R15 4.7K
GND
R16 100
TC08171S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE556D
14-Pin Cerdip	0 to +70°C	NE556F
14-Pin Plastic DIP	0 to +70°C	NE556N
14-Pin Cerdip	0 to +70°C	NE556-1F
14-Pin Plastic DIP	0 to +70°C	NE556-1N
14-Pin Plastic DIP	−40°C to +85°C	SA556N
14-Pin Cerdip	−40°C to +85°C	SA556-1F
14-Pin Plastic DIP	−40°C to +85°C	SA556-1N
14-Pin Cerdip	−55°C to +125°C	SE556F
14-Pin Plastic DIP	−55°C to +125°C	SE556N
14-Pin Plastic DIP	−55°C to +125°C	SE556CN
14-Pin Cerdip	−55°C to +125°C	SE556-1F
14-Pin Plastic DIP	−55°C to +125°C	SE556-1N
14-Pin Cerdip	−55°C to +125°C	SE556-1CF
14-Pin Plastic DIP	−55°C to +125°C	SE556-1CN

Dual Timer

NE/SA/SE556/NE/SA/SE556-1/SE556-1C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage NE/SA556, 556-1, SE556C, SE556-1C SE556-1, SE556	 +16 +18	 V V
P_D	Maximum allowable power dissipation[1]	800	mW
T_A	Operating temperature range NE556-1, NE556 SA556-1, SA556 SE556-1, SE556-1C, SE556, SE556C	 0 to +70 -40 to +85 -55 to +125	 °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTE:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the N and F packages. At ambient temperatures above 25°C, where this limit would be exceeded, the Maximum Allowable Power Dissipation must be derated by the following:
   D package 115 °C/W
   N package 80 °C/W
   F package 100 °C/W

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	$V_{CC} = 5V$, $R_L = \infty$		6	10		6	12	mA
		$V_{CC} = 15V$, $R_L = \infty$		20	24		20	30	mA
	Timing error (monostable)	$R_A = 2k\Omega$ to $100k\Omega$							
	Initial accuracy[2]	$C = 0.1\mu F$		0.5			0.75	3.0	%
	Drift with temperature	$T = 1.1$ RC		30	100		50	150	ppm/°C
	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, $R_B = 1k\Omega$ to $100k\Omega$							
	Initial accuracy[2]	$C = 0.\mu F$		4	6		5	13	%
	Drift with temperature	$V_{CC} = 15V$		400	500		400	500	ppm/°C
	Drift with supply voltage			0.15	0.6		0.3	1	%/V
	Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
		$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
	Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
		$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
	Threshold current[3]			30	250		30	250	nA
	Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
		$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
	Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	µA
	Reset voltage[5]		0.3	0.7	1.0	0.3	0.7	1.0	V
	Reset current			0.1	0.4		0.1	0.6	mA
	Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	$V_{CC} = 15V$							
		$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
		$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
	SE556	$I_{SINK} = 100mA$		2.0	2.25				V
	SE556-1			0.8	1.2				V
	NE/SA556/SE556C						2.0	3.2	V
	NE556-1/SE556-1C						2.0	2.5	V

Dual Timer NE/SA/SE556/NE/SA/SE556-1/SE556-1C

ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
		$I_{SINK} = 200mA$		2.5			2.5		V
		$V_{CC} = 5V$							
		$I_{SINK} = 8mA$		0.1	0.2		0.25	0.3	V
		$I_{SINK} = 5mA$		0.05	0.15		0.15	0.25	V
V_{OH}	Output voltage (high)	$V_{CC} = 15V$							
		$I_{SOURCE} = 200mA$		12.5			12.5		V
		$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
		$V_{CC} = 5V$							
		$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[6] NE556-1/SE556-1/SE556-1C	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA
	Matching characteristics[4]								
	Initial accuracy[2]			0.5	1.0		1.0	2.0	%
	Drift with temperature			10			± 10		ppm/°C
	Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

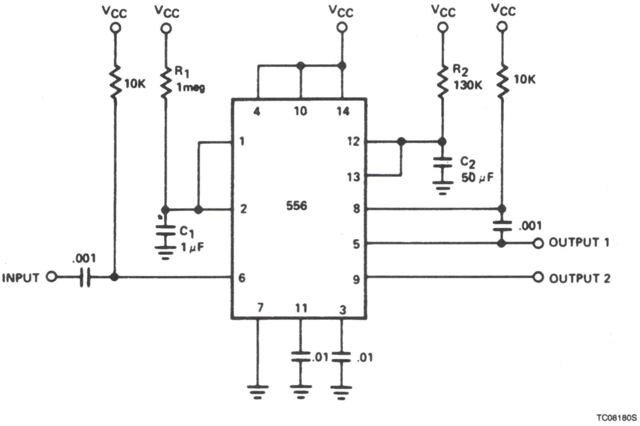
NOTES:

1. Supply current when output is high is typically 1.0mA less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine maximum value of $R_A + R_B$. For 15V operation, the max total R = 10MΩ, and for 5V operation, the maximum total R = 3.4MΩ.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.
6. Time measured from a positive-going input pulse from 0 to 0.4 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL APPLICATIONS

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001μF coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.



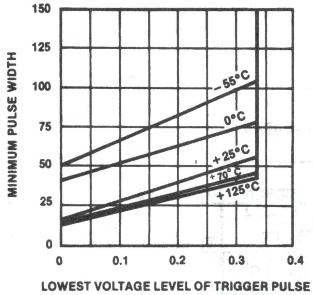
V_{CC}
10K
R1 1meg
4
10
14
R2 130K
10K
1
12
13
C2 50 µF
2
556
8
C1 1µF
.001
5
OUTPUT 1
.001
INPUT
6
9
OUTPUT 2
7
11
3
.01
.01
TC08180S

NOTE:
All resistor values are in Ω.

Sequential Timer

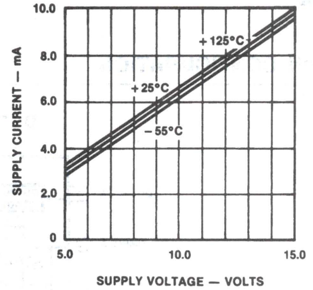
TYPICAL PERFORMANCE CHARACTERISTICS

Minimum Pulse Width Required for Triggering



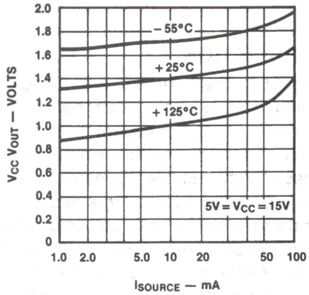
OP04190S

Supply Current vs Supply Voltage



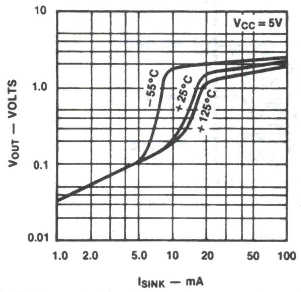
OP04200S

High Output Voltage Drop vs Output Source Current



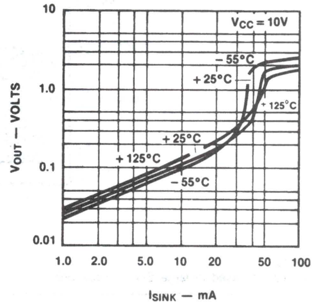
OP04210S

Low Output Voltage vs Output Sink Current



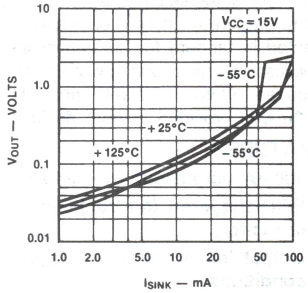
OP04220S

Low Output Voltage vs Output Sink Current



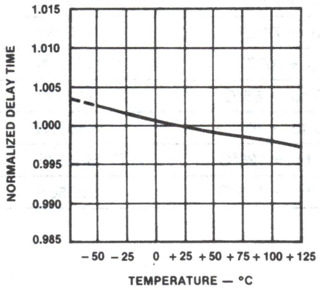
OP04230S

Low Output Voltage vs Output Sink Current



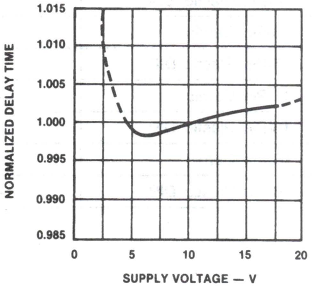
OP04240S

Delay Time vs Temperature



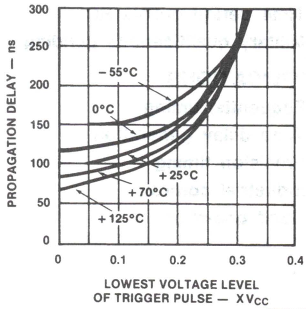
OP04250S

Delay Time vs Supply Voltage



OP04260S

Propagation Delay vs Voltage Level of Trigger Pulse



OP04270S

Signetics

NE/SA/SE558
Quad Timer

Product Specification

Linear Products

DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays; from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timer sections in the 558 are edge-triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

FEATURES

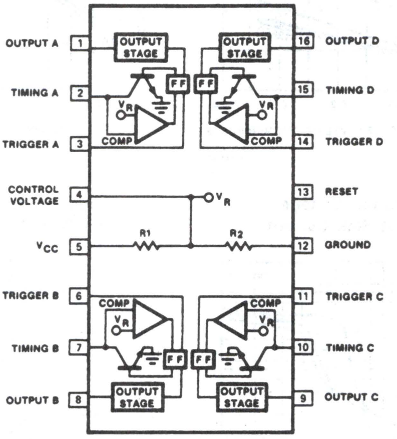
- **100mA output current per section**
- **Edge-triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 18V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**
- **Military qualifications pending**

APPLICATIONS

- **Sequential timing**
- **Time delay generation**
- **Precision timing**
- **Industrial controls**
- **Quad one-shot**

PIN CONFIGURATION

D[1] F, N Packages


OUTPUT A 1
TIMING A 2
TRIGGER A 3
CONTROL VOLTAGE 4
V_{CC} 5
TRIGGER B 6
TIMING B 7
OUTPUT B 8
OUTPUT C 9
TIMING C 10
TRIGGER C 11
GROUND 12
RESET 13
TRIGGER D 14
TIMING D 15
OUTPUT D 16
OUTPUT STAGE
FF
COMP
V_R
R1
R2

TOP VIEW

CD11140S

NOTE:
1. SOL released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE558D
16-Pin Cerdip	0 to +70°C	NE558F
16-Pin Plastic DIP	0 to +70°C	NE558N
16-Pin Cerdip	−40°C to +85°C	SA558F
16-Pin Plastic DIP	−40°C to +85°C	SA558N
16-Pin Cerdip	−55°C to +125°C	SE558F
16-Pin Plastic DIP	−55°C to +125°C	SE558N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage NE/SA558 SE558	 +16 +18	 V V
P_D	Maximum power dissipation $T_A = 25°C$ ambient (still-air)[1] F package N package D package	 1190 1450 1090	 mW mW mW
T_A	Operating ambient temperature range NE558 SA558 SE558	 0 to +70 -40 to +85 -55 to +125	 °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

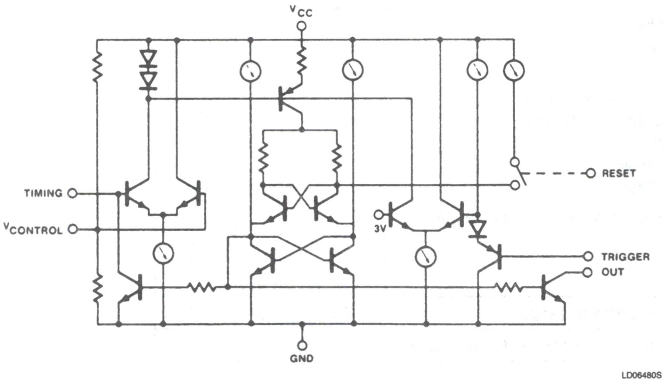
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE558			NE/SA558			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current	V_{CC} = Reset = 15V		16	32		16	36	mA
	Timing accuracy (t = RC)	R = 2kΩ to 100kΩ, C = 1μF							
	Initial accuracy			±1.0	3		±2	5	%
	Drift with temperature			30	100		30	150	ppm/°C
	Drift with supply voltage			0.1	0.9		0.1	0.9	%/V
	Trigger voltage[1]	V_{CC} = 15V	0.8		2.4	0.8		2.4	V
	Trigger current	Trigger = 0V		5	30		5	100	μA
	Reset voltage[2]		0.8		2.4	0.8		2.4	V
	Reset current	Reset		50	300		50	500	μA
	Threshold voltage			0.63			0.63		× V_{CC}
	Threshold leakage			15			15		nA
V_{OUT}	Output voltage[3]	I_L = 10mA I_L = 100mA		0.1 0.7	0.2 1.5		0.1 1.0	0.4 2.0	V V
	Output leakage			10	500		10	500	nA
t_{PD}	Propagation delay			1.0			1.0		μs
t_R	Rise time of output	I_L = 100mA		100			100		ns
t_F	Fall time of output	I_L = 100mA		100			100		ns

NOTES:

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset, the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8V, outputs set low and trigger inhibited. For reset above 2.4V, trigger enabled.
3. The 558 output structure is open-collector which requires a pull-up resistor to V_{CC} to sink current. The output is normally low sinking current.

558 EQUIVALENT CIRCUIT


VCC
RESET
TIMING
VCONTROL
3V
TRIGGER
OUT
GND
LD06480S

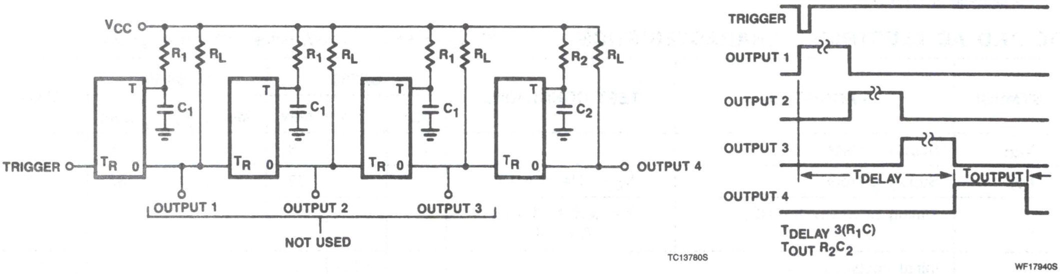
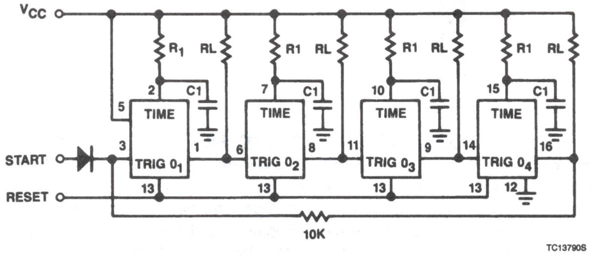
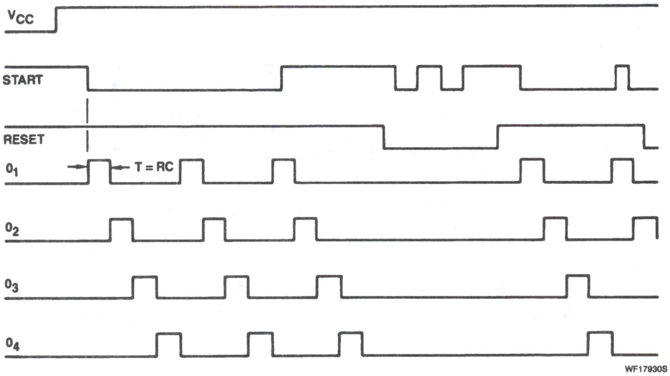

VCC
R1
RL
R1
RL
R1
RL
R2
RL
T
C1
C1
C1
C2
TRIGGER
TR
0
OUTPUT 4
OUTPUT 1
OUTPUT 2
OUTPUT 3
NOT USED
TC13780S
TRIGGER
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
TDELAY
TOUTPUT
TDELAY 3(R1C)
TOUT R2C2
WF17940S

Figure 1. Long-Time Delay


VCC
R1
RL
R1
RL
R1
RL
R1
RL
C1
C1
C1
C1
2
7
10
15
5
TIME
TIME
TIME
TIME
START
3
TRIG 0$_1$
1
6
TRIG 0$_2$
8
11
TRIG 0$_3$
9
14
TRIG 0$_4$
16
RESET
13
13
13
13
12
10K
TC13790S

a. Ring Counter



b. Expected Waveforms

Figure 2

AN171
NE558 Applications

Application Note

INTRODUCTION

The 558 is a monolithic Quad Timer designed to be used in the timing range from a few microseconds to a few hours. Four entirely independent timing functions can be achieved using a timing resistor and capacitor for each section. Two sections of the quad may be interconnected for astable operation. All four sections may be used together, in tandem, for sequential timing applications up to several hours. No coupling capacitors are required when connecting the output of one timer section to the input of the next.

FEATURES

- **100mA output current per section**
- **Edge-triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 16V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**

CIRCUIT OPERATIONS

In the one-shot mode of operation, it is necessary to supply a minimum of two external components (the resistor and capacitor) for timing. The time period is equal to the product of R and C. An output load must be present to complete the circuit due to the output structure of the 558.

For astable operation, it is desirable to cross-couple two devices from the 558 Quad. The outputs are direct-coupled to the opposite trigger input. The duty cycle can be set by the ratio of R_1C_1 to R_2C_2, from close to zero to almost 100%. An astable circuit using one timer is shown in Figure 5b.

OUTPUT STRUCTURE 558

The 558 structure is open-collector which requires a pull-up resistor to V_{CC} and is capable of sinking 100mA per unit, but not to exceed the power dissipation and junction temperature rating of the die and package. The output is normally low and is switched high when triggered.

RESET

A reset function has been made available to reset all sections simultaneously to an output low state. During reset the trigger is disabled. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

The reset voltage must be brought below 0.8V to insure reset.

THE CONTROL VOLTAGE

The control voltage is also made available on the 558 timer. This allows the threshold voltage to be modulated, therefore controlling the output pulse width and duty cycle with an external control voltage. The range of this control voltage is from about 0.5V to V_{CC} minus 1V. This will give a cycle time variation of about 50:1. In a sequential timer with voltage-controlled cycle time, the timing periods remain proportional over the adjustment range.

TEST BOARD FOR 558

The circuit layout can be used to test and characterize the 558 timer. S_2 is used to connect the loads to either V_{CC} or ground. The main precaution, in layout of the 558 circuit, is the path of the discharge current from the timing capacitor to ground (Pin 12). The path must be direct to Pin 12 and not on the ground bus. This is to prevent voltage spikes on the ground bus return due to current switching transient. It is also wise to use good power supply bypassing when large currents are being switched.

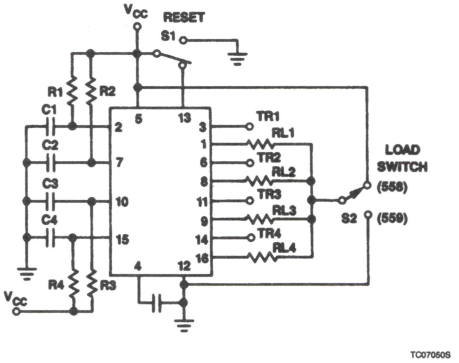
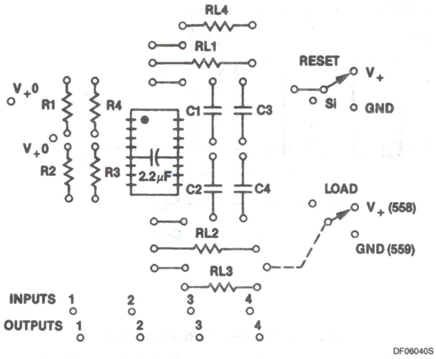
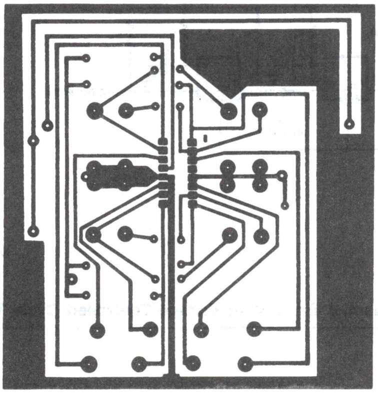


Figure 1. 558 Test Circuit


RL4
RL1
RESET
V+
Si
GND
V+
R1
R4
C1
C3
V+
R2
R3
2.2μF
C2
C4
LOAD
V+ (558)
RL2
GND (559)
RL3
INPUTS 1 2 3 4
OUTPUTS 1 2 3 4
DF06040S

a. Test Board Layout

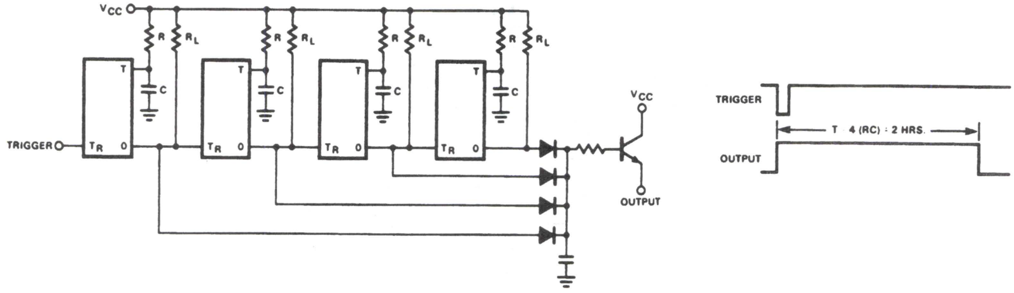


b. Foil Side

Figure 2

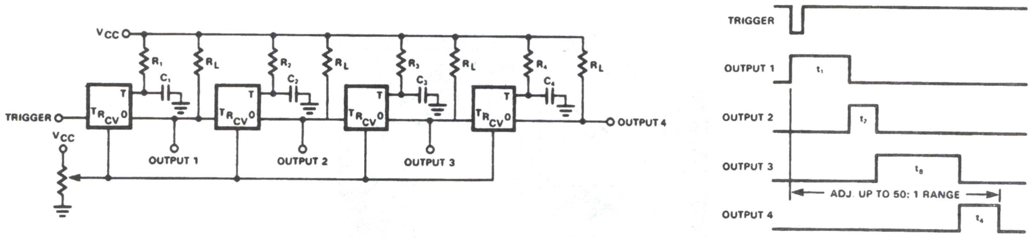
NE558 Applications

AN171


VCC
R
RL
T
C
TRIGGER
TR
O
VCC
OUTPUT
TRIGGER
T = 4 (RC) = 2 HRS.
OUTPUT

TC07060S

Figure 3. 558 Two-Hour Timer

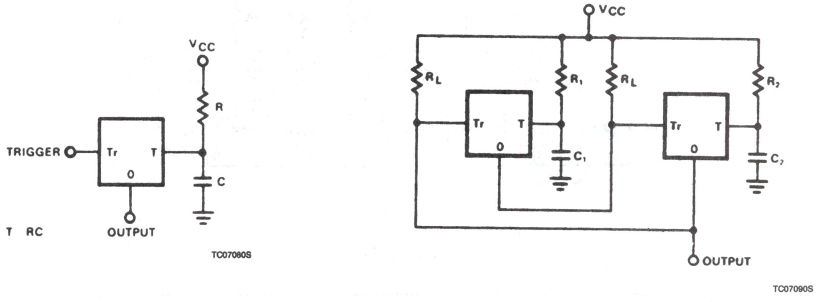

VCC
R1
RL
R2
R3
R4
C1
C2
C3
C4
T
TR
CV
O
TRIGGER
VCC
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
TRIGGER
OUTPUT 1
t1
OUTPUT 2
t2
OUTPUT 3
t3
ADJ. UP TO 50: 1 RANGE
OUTPUT 4
t4

TC07071S

NOTE:
t_1,t_2,t_3,t_4 remain proportional over entire adj. range.

Figure 4. 558 Sequential Timer With Voltage-Controlled Cycle Time (50:1 Range)

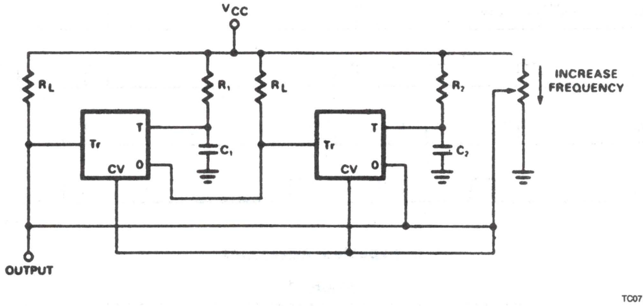
NE558 Applications


VCC
R
TRIGGER
Tr
T
0
C
OUTPUT
T RC
TC07080S
VCC
RL
R1
RL
R2
Tr
T
0
C1
Tr
T
0
C2
OUTPUT
TC07090S

NOTE:
T = RC

a. Monostable Operation (One-Shot)

b. 558 Astable Operation (Oscillator)


VCC
RL
R1
RL
R2
INCREASE FREQUENCY
Tr
T
CV
0
C1
Tr
T
CV
0
C2
OUTPUT
TC07100S

c. 558 Variable Frequency Oscillator With Fixed Duty Cycle

Figure 5

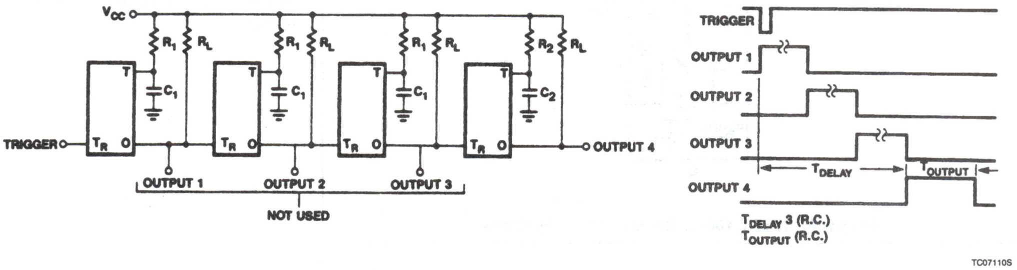
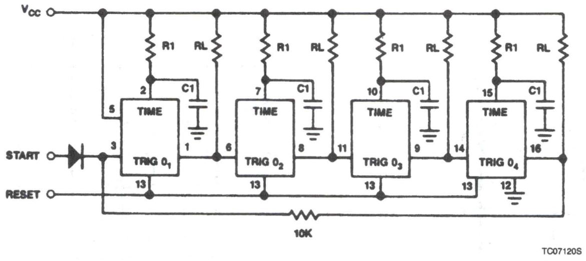
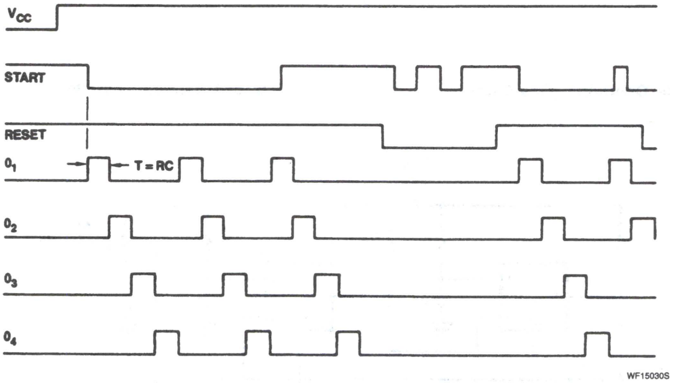

VCC
R1
RL
R1
RL
R1
RL
R2
RL
T
C1
T
C1
T
C1
T
C2
TRIGGER
TR
O
OUTPUT 4
OUTPUT 1
OUTPUT 2
OUTPUT 3
NOT USED
TRIGGER
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
TDELAY
TOUTPUT
TDELAY 3 (R.C.)
TOUTPUT (R.C.)
TC07110S

Figure 6. 558 Long Time Delay


VCC
R1
RL
C1
TIME
TRIG O1
TRIG O2
TRIG O3
TRIG O4
START
RESET
2
5
3
1
6
7
8
11
10
9
14
15
16
13
12
10K
TC07120S

a. 558 Ring Counter



b. Expected Waveforms

Figure 7

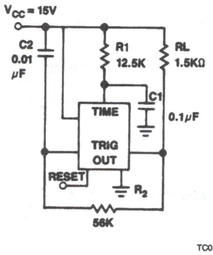

VCC = 15V
C2
0.01 μF
R1
12.5K
RL
1.5KΩ
C1
0.1μF
TIME
TRIG
OUT
RESET
R2
56K
TC07132S

Figure 8. NE558 400Hz Square Wave Oscillator

A single section of the quad time may be used as a non-precision oscillator. The values given are for oscillation at about 400Hz. $T_1 \approx R_1C_1$ and $T_2 \approx 2.25\ R_2C_2$ for V_{CC} of 15V. The frequency of oscillation is subject to the changes in V_{CC}.

Signetics

NE/SE555/SE555C
Timer

Product Specification

Linear Products

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

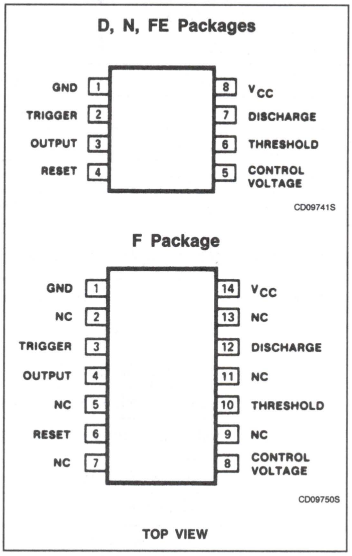
FEATURES

- **Turn-off time less than 2μs**
- **Max. operating frequency greater than 500kHz**
- **Timing from microseconds to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**

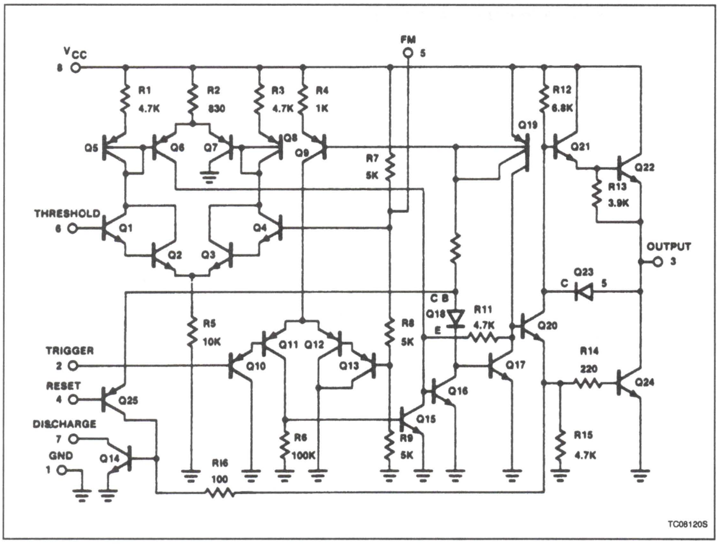
APPLICATIONS

- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Missing pulse detector**

PIN CONFIGURATIONS


D, N, FE Packages
GND 1
TRIGGER 2
OUTPUT 3
RESET 4
8 V_{CC}
7 DISCHARGE
6 THRESHOLD
5 CONTROL VOLTAGE
CD09741S
F Package
GND 1
NC 2
TRIGGER 3
OUTPUT 4
NC 5
RESET 6
NC 7
14 V_{CC}
13 NC
12 DISCHARGE
11 NC
10 THRESHOLD
9 NC
8 CONTROL VOLTAGE
CD09750S
TOP VIEW

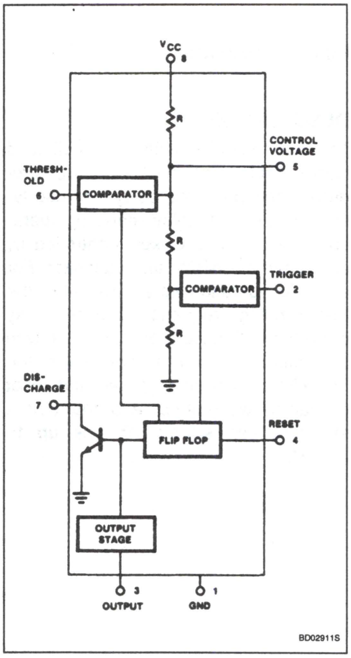
EQUIVALENT SCHEMATIC


V_{CC} 8
FM 5
R1 4.7K
R2 830
R3 4.7K
R4 1K
R12 6.8K
Q19
Q21
Q22
R13 3.9K
Q5
Q6
Q7
Q8
Q9
R7 5K
THRESHOLD 6
Q1
Q4
Q2
Q3
OUTPUT 3
Q23
C
B
Q18
E
R11 4.7K
Q20
R5 10K
Q11 Q12
R8 5K
TRIGGER 2
Q10
Q13
Q17
R14 220
Q24
RESET 4
Q25
Q16
DISCHARGE 7
Q15
R6 100K
R9 5K
R15 4.7K
GND 1
Q14
R16 100
TC08120S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Hermetic Cerdip	0 to +70°C	NE555FE
8-Pin Plastic SO	0 to +70°C	NE555D
8-Pin Plastic DIP	0 to +70°C	NE555N
8-Pin Hermetic Cerdip	−55°C to +125°C	SE555CFE
8-Pin Plastic DIP	−55°C to +125°C	SE555CN
14-Pin Plastic DIP	−55°C to +125°C	SE555N
8-Pin Hermetic Cerdip	−55°C to +125°C	SE555FE
14-Pin Ceramic DIP	0 to +70°C	NE555F
14-Pin Ceramic DIP	−55°C to +125°C	SE555F
14-Pin Ceramic DIP	−55°C to +125°C	SE555CF

BLOCK DIAGRAM


VCC
8
R
CONTROL VOLTAGE
5
THRESHOLD
6
COMPARATOR
R
TRIGGER
2
COMPARATOR
R
DISCHARGE
7
RESET
4
FLIP FLOP
OUTPUT STAGE
3
OUTPUT
1
GND
BD02911S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE555 NE555, SE555C	 +18 +16	 V V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range NE555 SE555, SE555C	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTE:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:

   D package 160 °C/W
   FE package 150 °C/W
   N package 100 °C/W
   F package 105 °C/W

DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to +15 unless otherwise specified.

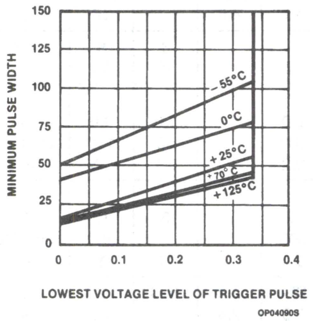
SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	$V_{CC} = 5V$, $R_L = \infty$		3	5		3	6	mA
		$V_{CC} = 15V$, $R_L = \infty$		10	12		10	15	mA
	Timing error (monostable)	$R_A = 2k\Omega$ to $100k\Omega$							
t_M	Initial accuracy[2]	$C = 0.1\mu F$		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, $R_B = 1k\Omega$ to $100k\Omega$							
t_A	Initial accuracy[2]	$C = 0.1\mu F$		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	$V_{CC} = 15V$			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
		$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
		$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
		$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]		0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current			0.1	0.4		0.1	0.4	mA
	Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	$V_{CC} = 15V$							
		$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
		$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
		$I_{SINK} = 100mA$		2.0	2.2		2.0	2.5	V
		$I_{SINK} = 200mA$		2.5			2.5		V
		$V_{CC} = 5V$							
		$I_{SINK} = 8mA$		0.1	0.25		0.3	0.4	V
		$I_{SINK} = 5mA$		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	$V_{CC} = 15V$							
		$I_{SOURCE} = 200mA$		12.5			12.5		V
		$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
		$V_{CC} = 5V$							
		$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	$V_{RESET} = V_{CC}$		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	ns

NOTES:

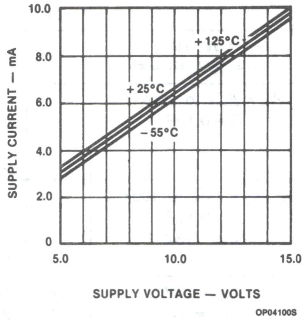
1. Supply current when output high typically 1mA less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine the max value of $R_A + R_B$, for 15V operation, the max total R = 10MΩ, and for 5V operation, the max. total R = 3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8 × V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

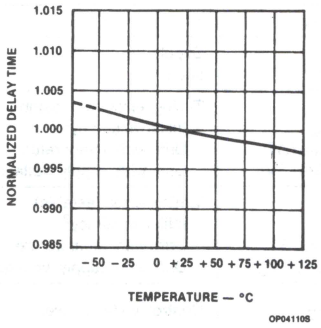
Minimum Pulse Width Required for Triggering



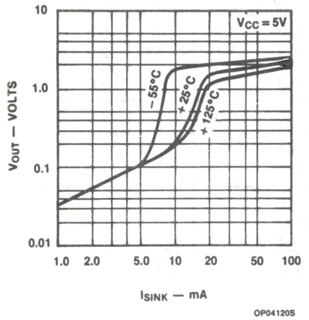
Supply Current vs Supply Voltage



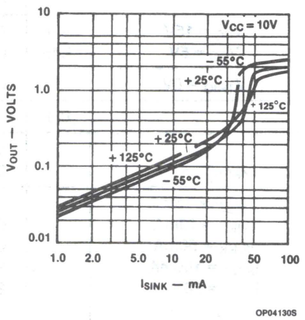
Delay Time vs Temperature



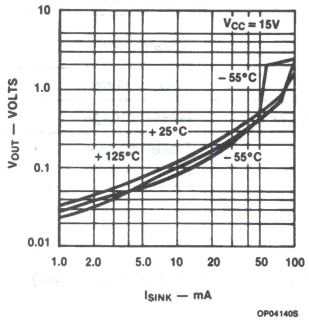
Low Output Voltage vs Output Sink Current



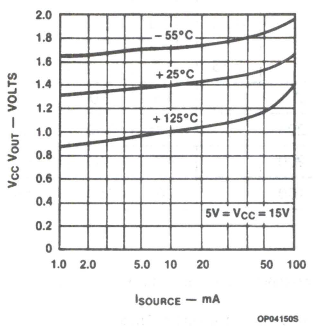
Low Output Voltage vs Output Sink Current



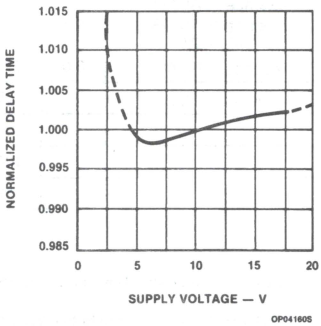
Low Output Voltage vs Output Sink Current



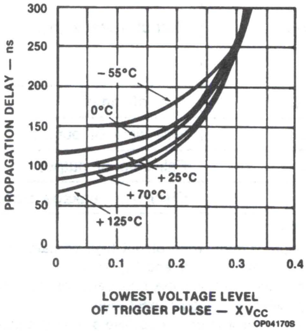
High Output Voltage Drop vs Output Source Current



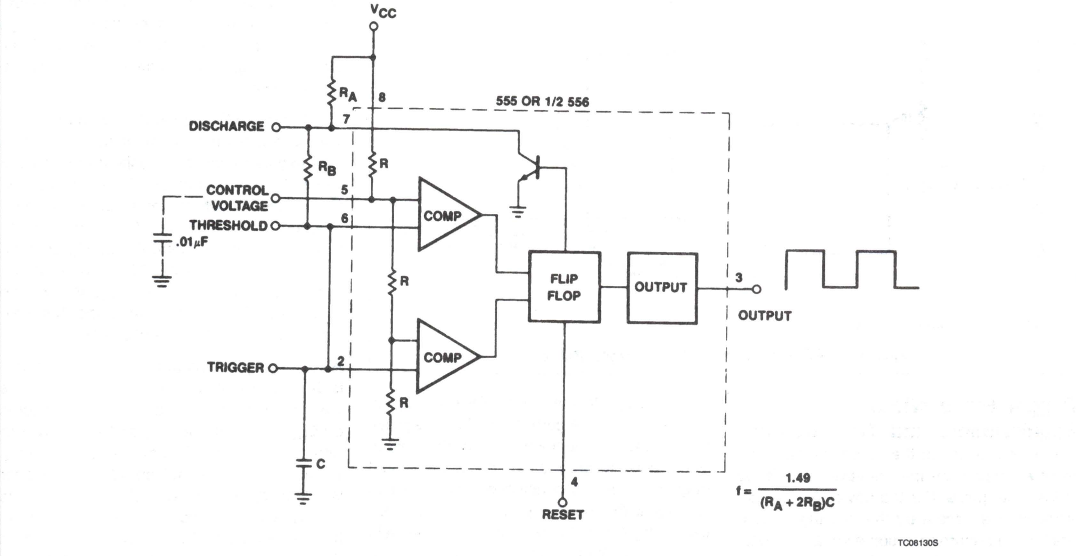
Delay Time vs Supply Voltage



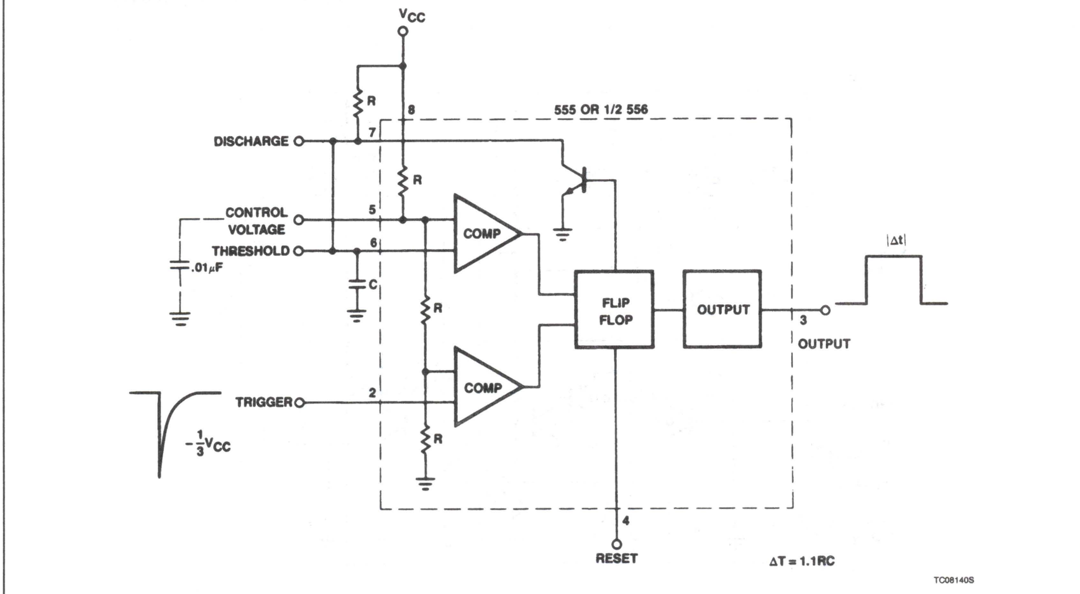
Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS

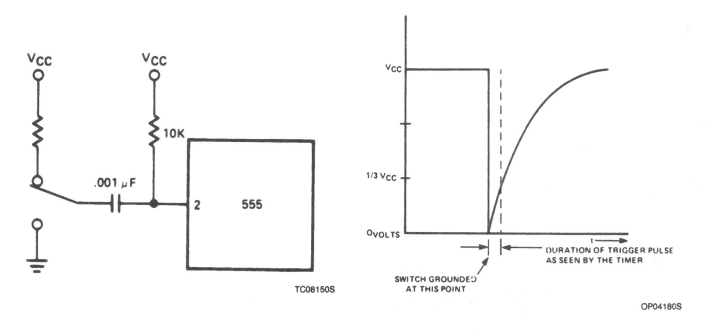

VCC
RA
8
555 OR 1/2 556
DISCHARGE
7
RB
R
CONTROL VOLTAGE
5
THRESHOLD
6
.01μF
COMP
FLIP FLOP
OUTPUT
3
OUTPUT
R
COMP
TRIGGER
2
R
C
4
RESET
f = 1.49 / (RA + 2RB)C
TC08130S

Astable Operation


VCC
R
8
555 OR 1/2 556
DISCHARGE
7
R
CONTROL VOLTAGE
5
THRESHOLD
6
.01μF
C
COMP
FLIP FLOP
OUTPUT
3
OUTPUT
|Δt|
R
COMP
TRIGGER
2
-1/3VCC
R
4
RESET
ΔT = 1.1RC
TC08140S

Monostable Operation

TYPICAL APPLICATIONS


VCC
VCC
10K
.001 µF
2
555
TC08150S
VCC
1/3 VCC
0VOLTS
t
DURATION OF TRIGGER PULSE AS SEEN BY THE TIMER
SWITCH GROUNDED AT THIS POINT
OP04180S

NOTE: All resistor values are in Ω.

Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

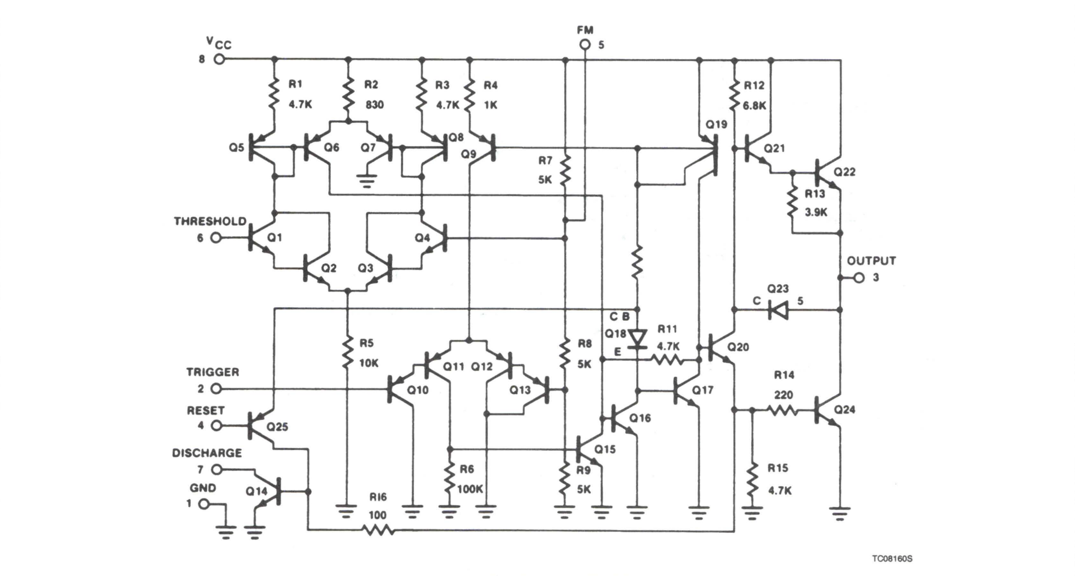

VCC
8
FM
5
R1 4.7K
R2 830
R3 4.7K
R4 1K
R12 6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R7 5K
R13 3.9K
THRESHOLD 6
Q1
Q4
Q2
Q3
OUTPUT 3
Q23
C
5
C B
Q18
E
R11 4.7K
Q20
R5 10K
R8 5K
TRIGGER 2
Q11
Q12
Q10
Q13
Q17
R14 220
Q24
RESET 4
Q25
Q16
DISCHARGE 7
Q15
R6 100K
R9 5K
R15 4.7K
GND 1
Q14
R16 100
TC08160S

Figure 2. Schematic 555 or 1/2 556 Dual Timer

Signetics

Linear Products

AN170
NE555 and NE556 Applications

Application Note

INTRODUCTION

In mid 1972, Signetics introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the IC operational amplifier.

The simplicity of the timer, in conjunction with its ability to produce long time delays in a variety of applications, has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 1.

The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at ⅔ of supply voltage level and the trigger comparator is referenced at ⅓ of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below ⅓ of the supply, the comparator changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network. When the capacitor voltage exceeds ⅔ of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", thereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.

The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of 1% with a 50ppm/°C timing drift with temperature. To operate the timer as a one-shot, only two external components are necessary; resistance & capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to 500kHz can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage control of timing and oscillation functions is also available.

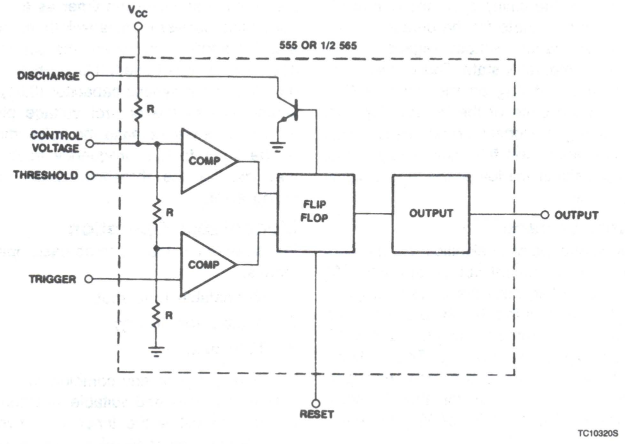


Figure 1. 555/556 Timer Functional Block Diagram

Timer Circuitry

The timer is comprised of five distinct circuits: two voltage comparators; a resistive voltage divider reference; a bistable flip-flop; a discharge transistor; and an output stage that is the "totem-pole" design for sink or source capability. $Q_{10}-Q_{13}$ comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger, Q_{10} and Q_{11} turn on when the voltage at Pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R_7, R_8 and R_9. All three resistors are of equal value (5kΩ). At 15V supply, the triggering level would be 5V. When Q_{10} and Q_{11} turn on, they provide a base drive for Q_{15}, turning it on. Q_{16} and Q_{17} form a bistable flip-flop. When Q_{15} is saturated, Q_{16} is 'off' and Q_{17} is saturated. Q_{16} and Q_{17} will remain in these states even if the trigger is removed and Q_{15} is turned 'off'. While Q_{17} is saturated, Q_{20} and Q_{14} are turned off.

The output structure of the timer is a "totem-pole" design, with Q_{22} and Q_{24} being large geometry transistors capable of providing 200mA with a 15V supply. While Q_{20} is 'off', base drive is provided for Q_{22} by Q_{21}, thus providing a high output.

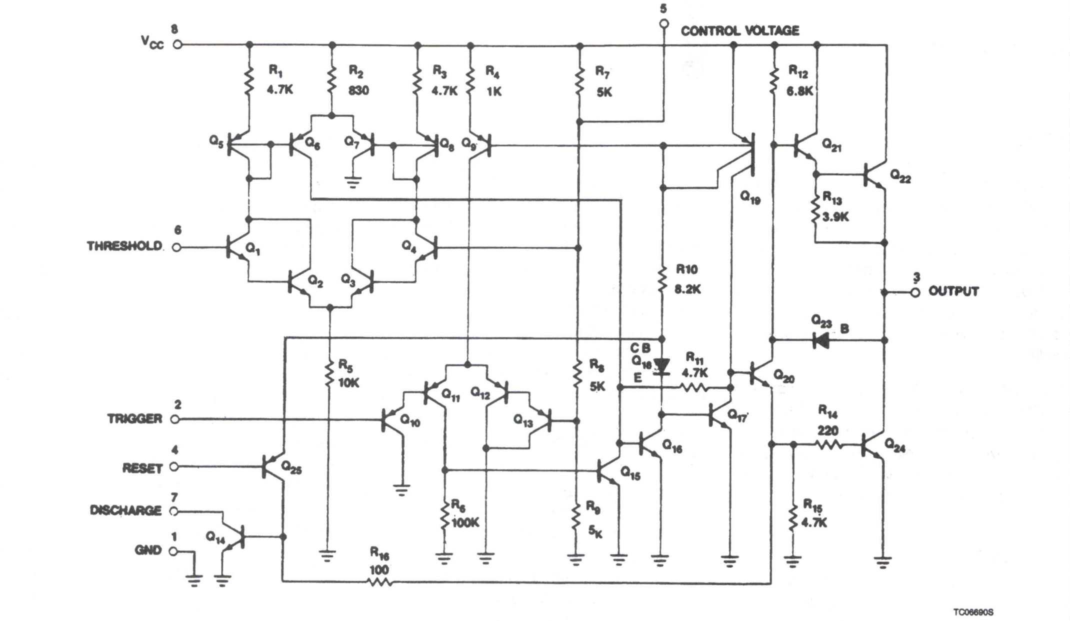
For the duration that the output is in a high state, the discharge transistor is 'off'. Since the collector of Q_{14} is typically connected to the external timing capacitor, C, while Q_{14} is off, the timing capacitor now can charge through the timing resistor, R_A.

The capacitor voltage is monitored by the threshold comparator (Q_1-Q_4) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from Q_3 and Q_4 thru Q_1 and Q_2. Amplification of the current change is provided by Q_5 and Q_6. Q_5-Q_6 and Q_7-Q_8 comprise a diode-biased amplifier. The amplified current change from Q_6 now provides a base drive for Q_{16} which is part of the bistable flip-flop, to change states. In doing so, the output is driven "low", and Q_{14}, the discharge transistor, is turned "on", shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is essential that one understands

NE555 and NE556 Applications

AN170



NOTE:
All resistor values are in ohms.

Figure 2. Schematic of 555 or ½ 556 Dual Timer

all the variations possible in order to utilize this device to its fullest extent.

Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop is set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, Q_{25}, is off with its base held high. When the base of Q_{25} is grounded, it turns on, providing base drive to Q_{14}, turning it on. This discharges the timing capacitor, resets the flip-flop at Q_{17}, and drives the output low. The reset overrides all other functions within the timer.

Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative-going edge of the input pulse. For the device to time-out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the timeout period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger (see Figure 3), a short negative-going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, $Q_{10} - Q_{13}$, and the threshold comparator, $Q_1 - Q_4$, are referenced to an internal resistor divider network, R_7, R_8, R_9. This network establishes the nominal two thirds of supply voltage (V_{CC}) trip point for the threshold comparator and one third of V_{CC} for the trigger comparator. The two thirds point at the junction of R_7, R_8 and the base of Q_4 is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage-controlled oscillator, pulse-width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor (0.01µF) be placed across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one-shot)
2. Astable (oscillatory)
3. Time delay

By utilizing one or any combination of basic operating modes and suitable variations, it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.

NE555 and NE556 Applications AN170

One of the simplest and most widely used operating modes of the timer is the monostable (one-shot). This configuration requires only two external components for operation (see Figure 4). The sequence of events starts when a voltage below one third V_{CC} is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative-going pulse. On the negative-going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, C, starts charging through the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant T = RC. Ignoring capacitor leakage, the capacitor will reach the two thirds V_{CC} level in 1.1 time constants or

$$T = 1.1\,RC \qquad (1)$$

Where T is in seconds, R is in ohms, and C is in Farads. This voltage level trips the threshold comparator, which in turn drives the output low and turns on the discharge transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

Astable Operation

In the astable (free-run) mode, only one additional component, R_B, is necessary. The trigger is now tied to the threshold pin. At power-up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path through R_A and R_B. When the capacitor reaches the threshold level of ⅔ V_{CC}, the output drops low and the discharge transistor turns on.

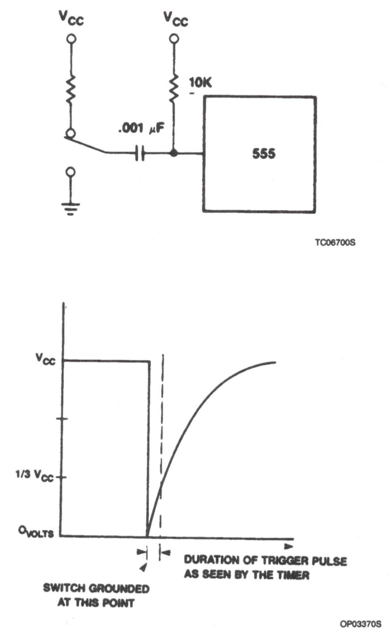

VCC
VCC
10K
.001 μF
555
TC06700S
VCC
1/3 VCC
0VOLTS
DURATION OF TRIGGER PULSE
AS SEEN BY THE TIMER
SWITCH GROUNDED
AT THIS POINT
OP03370S

Figure 3. AC Coupling of the Trigger Pulse

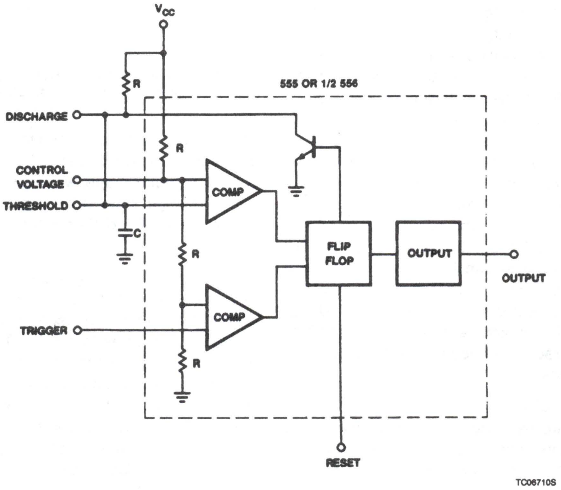

VCC
R
555 OR 1/2 556
DISCHARGE
R
CONTROL
VOLTAGE
THRESHOLD
COMP
C
R
FLIP
FLOP
OUTPUT
OUTPUT
COMP
TRIGGER
R
RESET
TC06710S

Figure 4. Monostable Operation

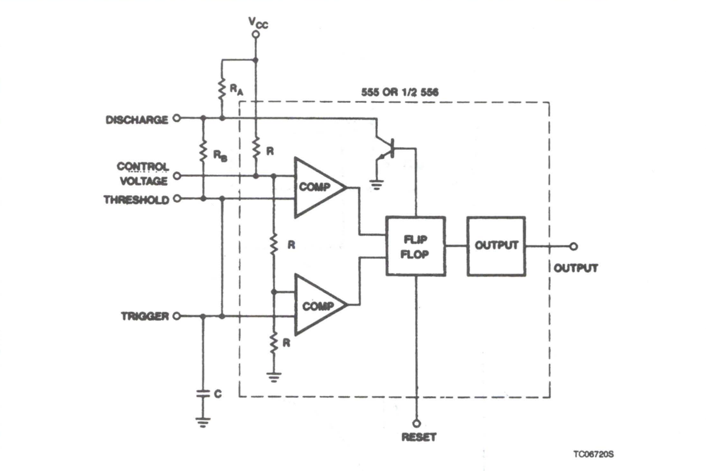


Figure 5. Astable Operation

The timing capacitor now discharges through R_B. When the capacitor voltage drops to ⅓ V_{CC}, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$f = \frac{1.49}{(R_A + 2R_B)\,C} \qquad (2)$$

Selecting the ratios of R_A and R_B varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if $R_A = 0$, the charge time cannot be made smaller than the discharge time because the charge path is $R_A + R_B$ while the discharge path is R_B alone. In this case it becomes necessary to insert a diode in parallel with R_B, cathode toward the timing capacitor. Another diode is desirable, but not mandatory (this one in series with R_B), cathode away from the timing capacitor. Now the charge path becomes R_A, through the parallel diode into C. Discharge is through the series diode and R_B to the discharge transistor. This scheme will afford a duty cycle range from less than 5% to greater than 95%. It should be noted that for reliable operation a minimum value of 3kΩ for R_B is recommended to assure that oscillation begins.

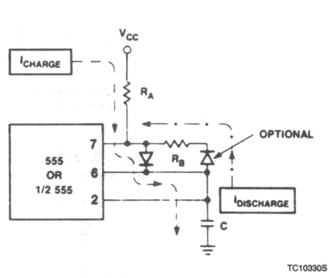


Figure 6. Method of Achieving Duty Cycles Less Than 50%

Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied, immediately changed to the high state, timed out, and returned to its pre-trigger low state. In the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.

The threshold and trigger are tied together, monitoring the capacitor voltage. The discharge function is not used. The operation sequence begins as transistor (T_1) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off, the capacitor commences its charge cycle. When the capacitor reaches the threshold level, only then does the output change from its normally high state to the low state. The output will remain low until T_1 is again turned on.

GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5V to 15V_{DC} with 16V_{DC} being the absolute maximum rating. Most of the devices, however, will operate at voltage levels as low as 3V_{DC}. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply voltage may be provided by any number of sources, however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts, causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem-pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the V_{CC} and ground, directly across the device, is necessary and ideal. The size of a capacitor will depend on the specific application. Values of capacitance from 0.01µF to 10µF are not uncommon, but note that the bypass capacitor would be as close to the device as physically possible.

Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.

Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e., deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by 0.01% to 10% and 20%. Capacitors may have a 5% to 10% deviation from rated capacity. Therefore, in a system where

NE555 and NE556 Applications

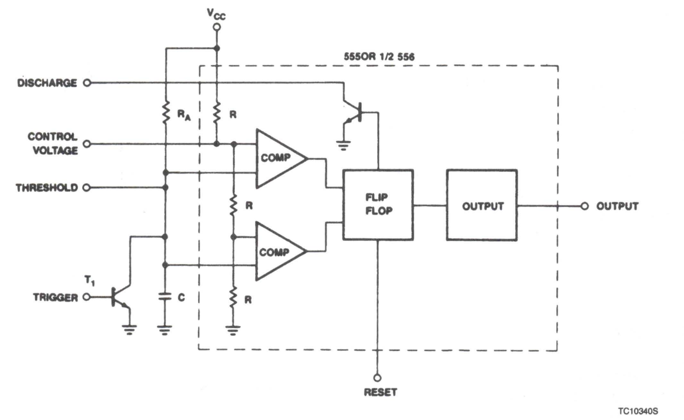


Figure 7. Time Delay Operation

timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance, will allow for best adjustability and performance.

The timing capacitor should be a high quality, stable component with very low leakage characteristics. *Under no circumstances should ceramic disc capacitors be used in the timing network!* Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantalum, or similar types.

The timer typically exhibits a small negative temperature coefficient (50ppm/°C). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is $0.25\mu A$. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$V_{potential} = V_{CC} - V_{capacitor}$$

$$V_{potential} = V_{CC} - \tfrac{2}{3}\,V_{CC} = \tfrac{1}{3}V_{CC}$$

Maximum resistance is then defined as

$$R_{MAX} = \frac{V_{CC} - V_{cap}}{I_{thresh}} \qquad (3)$$

Example: $V_{CC} = 15V$

$$R_{MAX} = \frac{15 - 10}{0.25(10^{-6})} = 20M\Omega$$

$V_{CC} = 5V$

$$R_{MAX} = \frac{5 - 3.33}{0.25(10^{-6})} \quad 6.6M\Omega$$

NOTE:

If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, Q_{14}, is current-limited at 35mA to 55mA internally. Thus, at the current limiting values, Q_{14} establishes high saturation voltages. When examining the currents at Q_{14}, remember that the transistor, when turned on, will be carrying two current loads. The first being the constant current through timing resistor, R_A. The second will be the varying discharge current from the timing capacitor. To provide best operation, the current contributed by the R_A path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5kΩ value be the minimum feasible value for R_A. This does not mean lower values cannot be used successfully in certain applications, yet there are extreme cases that should be avoided if at all possible.

Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized, though. (It should be a cardinal rule that applies to the usage of all ICs.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor may be necessary.

The most important characteristic of the capacitor should be as low a leakage as possible. Obviously, any leakage will subtract from the charge count, causing the calculated time to be longer than anticipated.

Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R_7, or R_8. The combination of R_7, R_8 and R_9 comprises the resistive voltage divider network that establishes the nominal ⅓ V_{CC} trigger comparator level (junction R_8, R_9) and the ⅔ V_{CC} level for the threshold comparator (junction R_7, R_8).

For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications, becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold comparator "set" level above or below the ⅔ V_{CC} nominal, thereby varying the timing. In the monostable mode, the control voltage may be varied from 45% to 90% of V_{CC}. The 45 – 90% figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free-run) mode, the control voltage limitations are from 1.7V to V_{CC}. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level, it also raise the trigger comparator level by one-half that amount due to R_8 and R_9 of Figure 2. As a voltage-controlled oscillator, one can expect ±25% around center frequency (f_O) to be virtually linear with a normal RC timing circuit. For wider linear variations around f_O it may be desirable to replace the charging resistor with a constant-current source. In this manner, the exponential charging characteristics of the classical configuration will be altered to linear charge time.

Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable, it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e., device off during power-up). It can also be used in conjunction with the trigger pin to establish a positive edge-triggered circuit as opposed to the normal negative edge-trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4V and 1.0V (min/max). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1V. At that point the trigger is in the "turn on" region, below ⅓ V_{CC}. This will cause the device to trigger immediately, effectively triggering on the positive-going edge if a pulse is applied to Pins 4 and 2 simultaneously.

FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncrasies that may exhibit themselves from time to time in various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the *first time constant* is approximately *twice as long as the rest.* Why?
   Answer: In the oscillator mode the capacitor voltage fluctuates between ½ and ⅔ of the supply voltage. When reset is pulled down, the capacitor discharges completely. Thus for the first cycle it must charge from ground to ⅔ V_{CC}, which takes twice as long.
2. What is *maximum frequency of oscillations?*
   Answer: Most devices will oscillate about 1MHz. However, in the interest of temperature stability, one should operate only up to about 500kHz.
3. What is *temperature drift* for *oscillator mode?*
   Answer: Temperature drift of oscillator mode is 3 times that of one-shot mode due to the addition of a second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.
4. Oscillator exhibits spurious *oscillations on crossover points.* Why?
   Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.
5. Trying to drive a *relay* but 555 *hangs up.* How come?
   Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving Pin 3 below a negative 0.6V. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode, thus preventing Pin 3 from ever seeing a negative voltage.
6. Double triggering of the TTL loads sometimes occurs. Why?
   Answer: Due to the high current capability and fast rise and fall times of the output, a totem-pole structure different from the TTL classical structure was used. Near TTL threshold this output exhibits a crossover distortion which may double trigger logic. A 1000pF capacitor from the output to ground will eliminate any false triggering.
7. What is the longest time I can get out of the timer?
   Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point, dependent on required accuracy. Normally 20 to 30 min. is the longest feasible time.

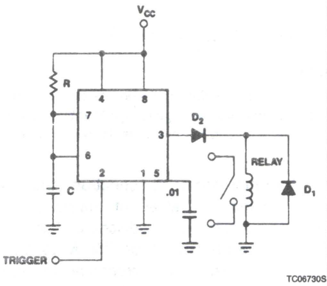


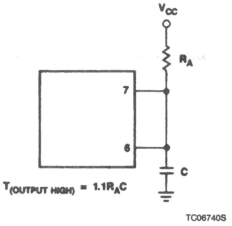
Figure 8. Driving High Q Inductive Loads

DESIGN FORMULAS

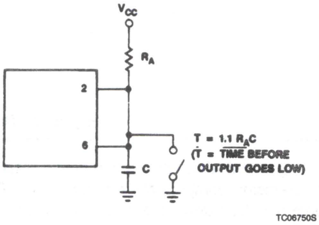
Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.

APPLICATIONS

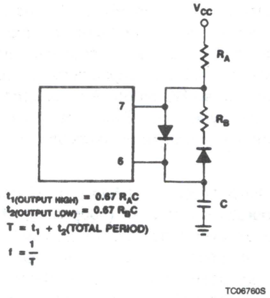
The timer, since introduction, has spurred the imagination of thousands. Thus, the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.



a. Monostable Timing

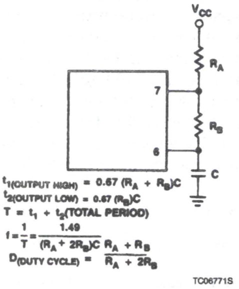


b. True Time Delay



V_{CC}
R_A
7
R_B
6
C
$t_{1(OUTPUT\ HIGH)} = 0.67\ R_AC$
$t_{2(OUTPUT\ LOW)} = 0.67\ R_BC$
$T = t_1 + t_2$(TOTAL PERIOD)
$f = \frac{1}{T}$
TC06760S

c. Modified Duty Cycle (Astable)



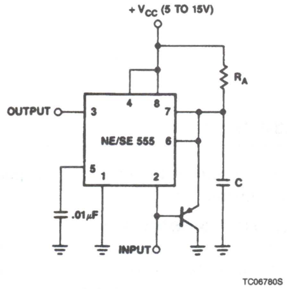
V_{CC}
R_A
7
R_B
6
C
$t_{1(OUTPUT\ HIGH)} = 0.67\ (R_A + R_B)C$
$t_{2(OUTPUT\ LOW)} = 0.67\ (R_B)C$
$T = t_1 + t_2$(TOTAL PERIOD)
$f = \frac{1}{T} = \frac{1.49}{(R_A + 2R_B)C}$
$D_{(DUTY\ CYCLE)} = \frac{R_A + R_B}{R_A + 2R_B}$
TC06771S

d. Astable Timing

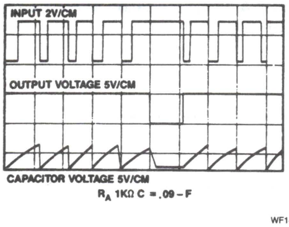
Figure 9

Missing Pulse Detector

Using the circuit of Figure 10a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 10b shows the actual waveforms seen in this mode of operation.


+V$_{CC}$ (5 TO 15V)
R$_A$
OUTPUT
3
4
8
7
NE/SE 555
6
5
1
2
C
.01μF
INPUT
TC06780S

a. Schematic Diagram



b. Expected Waveforms

Figure 10

Frequency Divider

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle.

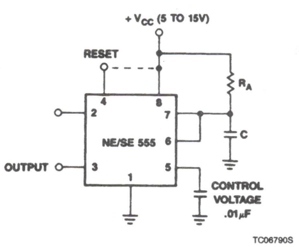

+V$_{CC}$ (5 TO 15V)
RESET
R$_A$
4
8
2
7
NE/SE 555
6
C
OUTPUT
3
5
1
CONTROL VOLTAGE
.01μF
TC06790S

Figure 11a. Schematic Diagram

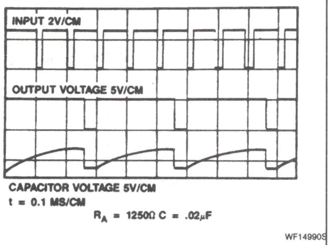
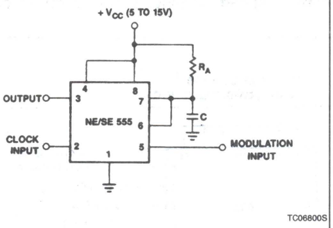


Figure 11b. Expected Waveforms

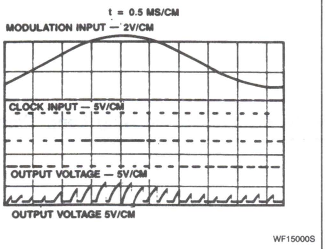
Figure 11b shows the waveforms of the timer in Figure 11a when used as a divide-by-three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 12a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (Pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 12b shows the actual waveform generated with this circuit.


+V$_{CC}$ (5 TO 15V)
R$_A$
OUTPUT
3
4
8
7
NE/SE 555
6
C
CLOCK INPUT
2
5
1
MODULATION INPUT
TC06800S

a. Device Schematic

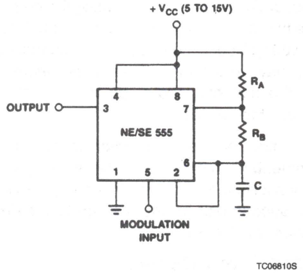


b. Expected Waveforms

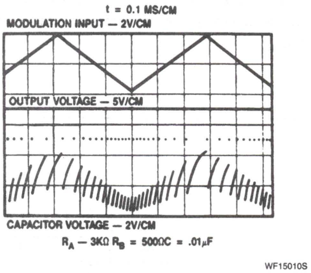
Figure 12

Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 13a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage, and hence the time delay, is varied. Figure 13b shows the waveform generated for triangle-wave modulation signal.

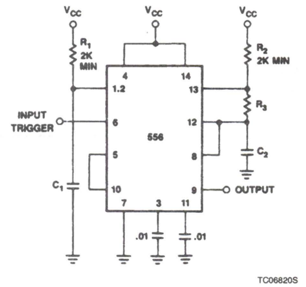

+V$_{CC}$ (5 TO 15V)
R$_A$
OUTPUT
3
4
8
7
NE/SE 555
R$_B$
6
1
5
2
C
MODULATION INPUT
TC06810S

a. Schematic Diagram



b. Expected Waveform

Figure 13


V$_{CC}$
V$_{CC}$
V$_{CC}$
R$_1$ 2K MIN
R$_2$ 2K MIN
4
14
1.2
13
R$_3$
INPUT TRIGGER
6
12
556
5
8
C$_2$
C$_1$
10
9
OUTPUT
7
3
11
.01
.01
TC06820S

NOTE:
All resistor values are in ohms.

Figure 14. Tone Burst Generator

Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one-shot and the second half as an oscillator (Figure 14).

The pulse established by the one-shot turns on the oscillator, allowing a burst to be generated.

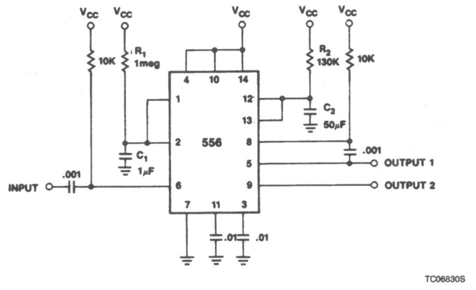
Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001μF coupling capacitor, sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay (Figure 15).

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed-out (determined by 1.1 R_1C_1) the second half begins. Its duration is determined by 1.1 R_2C_2.

Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays, expensive capacitors with extremely low leakage are required. The practicality of the components involved limits the time between pulses to around twenty minutes.


VCC
VCC
VCC
VCC
VCC
10K
R1 1meg
R2 130K
10K
C2 50µF
C1 1µF
556
4
10
14
1
12
13
2
8
5
6
9
7
11
3
.001
.001
.01
.01
INPUT
OUTPUT 1
OUTPUT 2
TC06830S

NOTE:
All resistor values are in ohms.

Figure 15. Sequential Timer

To achieve longer time periods, both halves may be connected in tandem with a "divide-by" network in between.

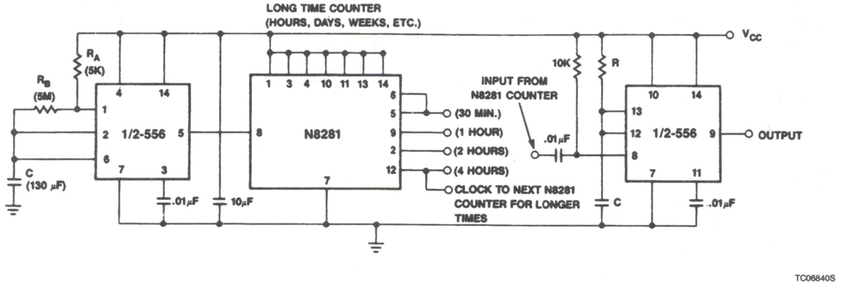
The first timer section operates in an oscillatory mode with a period of $1/f_O$. This signal is then applied to a "divide-by-N" network to give an output with the period of N/f_O. This can then be used to trigger the second half of the 556. The total time is now a function of N and f_O (Figure 16).

Speed Warning Device (1)

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 17a).

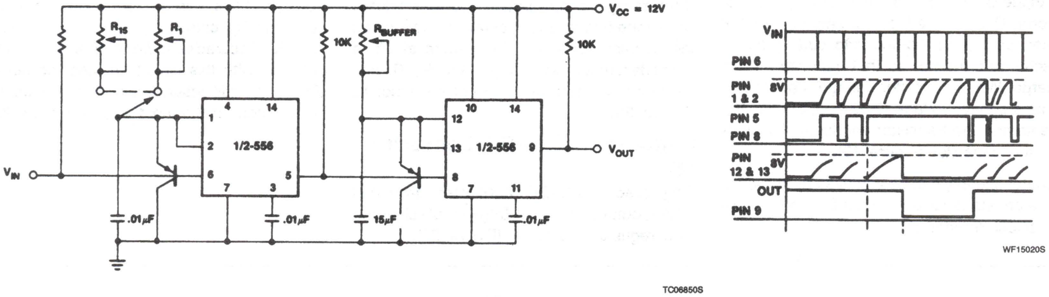
Car Tachometer (1)

The timer receives pulses from the distributor points. Meter M receives a calibrated current thru R_6 when the timer output is high. After time-out, the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 18).


LONG TIME COUNTER
(HOURS, DAYS, WEEKS, ETC.)
VCC
RA (5K)
RB (5M)
C (130 µF)
1/2-556
4
14
1
2
5
6
7
3
.01µF
10µF
N8281
1 3 4 10 11 13 14
8
6
5
9
2
12
7
(30 MIN.)
(1 HOUR)
(2 HOURS)
(4 HOURS)
CLOCK TO NEXT N8281 COUNTER FOR LONGER TIMES
INPUT FROM N8281 COUNTER
10K
R
.01µF
C
1/2-556
10
14
13
12
9
8
7
11
OUTPUT
.01µF
TC06840S

NOTE:
All resistor values are in ohms.

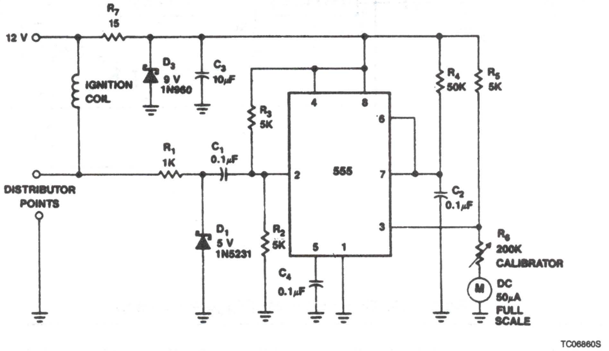
Figure 16. Method of Achieving Long Time Delays


V_{CC} = 12V
R_{15}
R_1
10K
R_{BUFFER}
10K
4
14
1
2
1/2-556
6
7
3
5
10
14
12
13
1/2-556
9
8
7
11
V_{IN}
V_{OUT}
.01µF
.01µF
15µF
.01µF
TC06850S
V_{IN}
PIN 6
PIN 1 & 2
8V
PIN 5
PIN 8
PIN 12 & 13
8V
OUT
PIN 9
WF15020S

a. Schematic of Speed Warning Device

b. Operating Waveforms Speed Warning Device

Figure 17


R_7
15
12 V
D_3
9 V
1N960
C_3
10µF
IGNITION COIL
R_3
5K
4
8
6
555
2
7
3
5
1
R_1
1K
C_1
0.1µF
DISTRIBUTOR POINTS
D_1
5 V
1N5231
R_2
5K
C_4
0.1µF
R_4
50K
R_5
5K
C_2
0.1µF
R_6
200K
CALIBRATOR
M
DC
50µA
FULL SCALE
TC06860S

NOTE:
All resistor values are in ohms.

Figure 18. Tachometer

Oscilloscope-Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage ($0.33V_{CC}$), the flip-flop resets and the transistor conducts, discharging the capacitor (Figure 19).

Greater linearity can be achieved by substituting a constant-current source for the frequency adjust resistor (R).

Square Wave Tone Burst Generator (4)

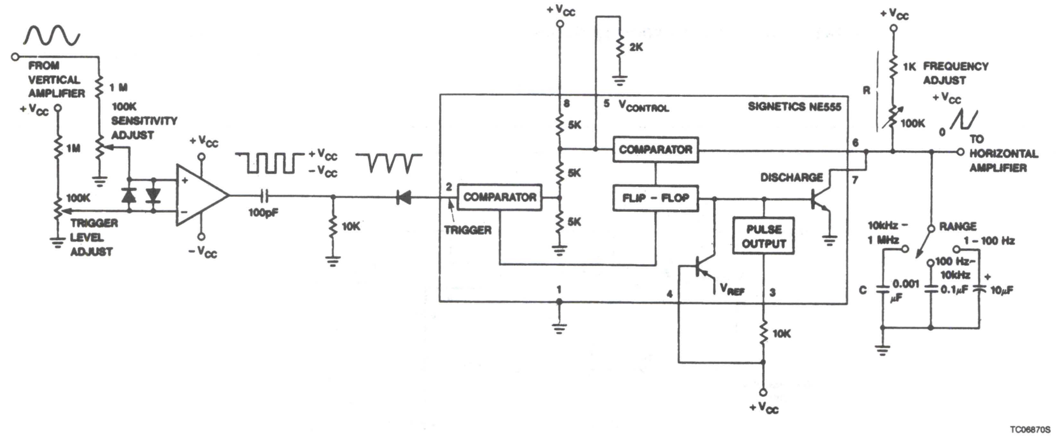
Depressing the pushbutton provides square wave tone bursts whose duration depends on the duration for which the voltage at Pin 4 exceeds a threshold. Components R_1, R_2 and C_1 cause the astable action of the timer IC (Figure 20).

Regulated DC-to-DC Converter (2)

Regulated DC-to-DC converter produces $15V_{DC}$ outputs from a $+5V_{DC}$ input. Line and load regulation is 0.1% (Figure 21).

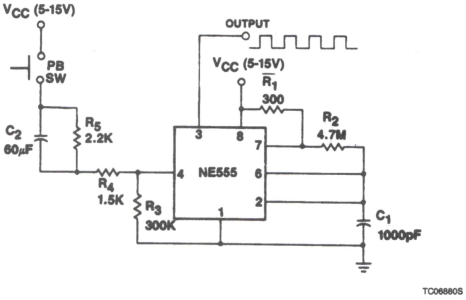
Voltage-to-Pulse Duration Converter (1)

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a), and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 22).


FROM VERTICAL AMPLIFIER
1 M
+Vcc
1M
100K SENSITIVITY ADJUST
100K
TRIGGER LEVEL ADJUST
+Vcc
-Vcc
+Vcc
-Vcc
100pF
10K
2
TRIGGER
COMPARATOR
+Vcc
2K
8
5 VCONTROL
5K
5K
5K
COMPARATOR
FLIP - FLOP
SIGNETICS NE555
DISCHARGE
PULSE OUTPUT
VREF
1
4
3
6
7
10K
+Vcc
+Vcc
1K FREQUENCY ADJUST
R
100K
+Vcc
0
TO HORIZONTAL AMPLIFIER
RANGE
10kHz - 1 MHz
1 - 100 Hz
100 Hz-10kHz
C
0.001 μF
0.1μF
10μF
TC06870S

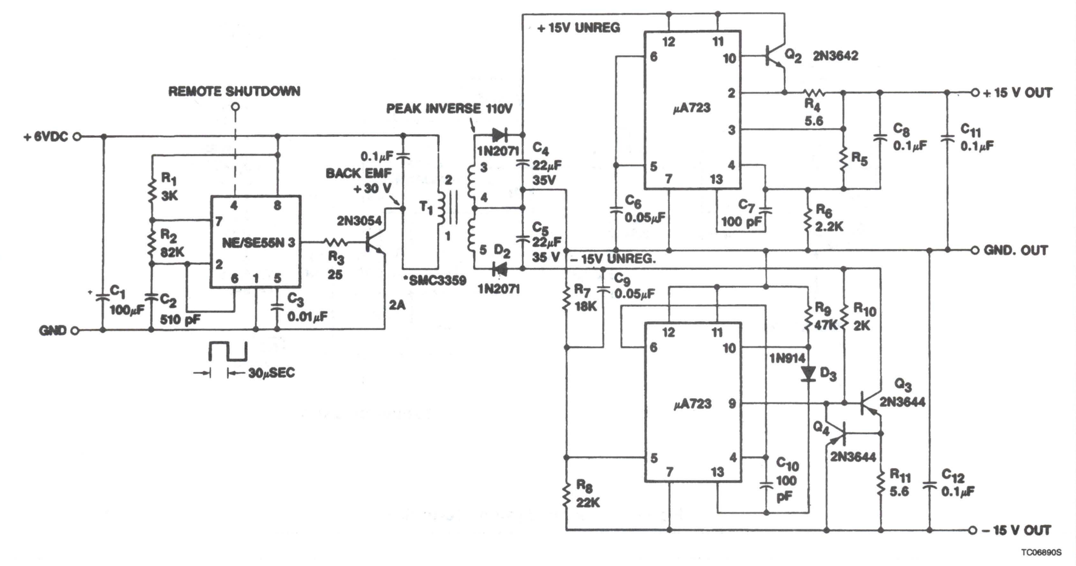
NOTE:
All resistor values are in ohms.

Figure 19. Schematic of Triggered Sweep


VCC (5-15V)
PB SW
C2 60μF
R5 2.2K
R4 1.5K
R3 300K
OUTPUT
VCC (5-15V)
R1 300
R2 4.7M
3
8
7
4
NE555
6
2
1
C1 1000pF
TC06880S

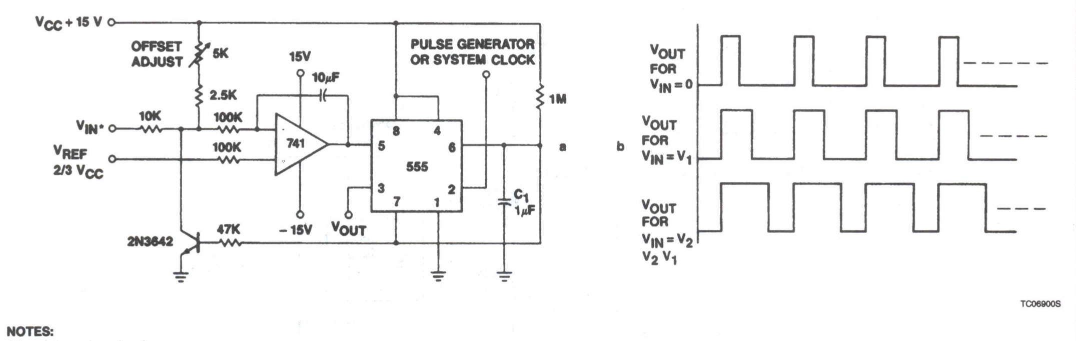
NOTE:
All resistor values are in ohms.

Figure 20. Square Wave Tone Burst Generator


+15V UNREG
REMOTE SHUTDOWN
PEAK INVERSE 110V
+6VDC
R1 3K
R2 82K
NE/SE555N
4 8 7 3 2 6 1 5
0.1μF
BACK EMF +30 V
2N3054
R3 25
T1
*SMC3359
2A
1N2071
C4 22μF 35V
C5 22μF 35 V
D2
1N2071
C1 100μF
C2 510 pF
C3 0.01μF
GND
30μSEC
μA723
12 11 6 10 2 3 5 4 7 13
Q2 2N3642
R4 5.6
R5
C8 0.1μF
C11 0.1μF
+15 V OUT
C6 0.05μF
C7 100 pF
R6 2.2K
GND. OUT
−15V UNREG.
C9 0.05μF
R7 18K
R9 47K
R10 2K
1N914
D3
μA723
9
Q3 2N3644
Q4 2N3644
C10 100 pF
R8 22K
R11 5.6
C12 0.1μF
−15 V OUT
TC06890S

NOTES:
All resistor values are in ohms.
*Shafer Magnetics
Covina, Calif,
(213) 331-3115

Figure 21. Regulated DC-to-DC Converter


VCC +15 V
OFFSET ADJUST
5K
2.5K
10K
VIN*
100K
100K
VREF 2/3 VCC
15V
10μF
741
−15V
VOUT
2N3642
47K
PULSE GENERATOR OR SYSTEM CLOCK
8 4 5 6 3 7 1 2
555
1M
C1 1μF
a
b
VOUT FOR VIN = 0
VOUT FOR VIN = V1
VOUT FOR VIN = V2
V2 V1
TC06900S

NOTES:
All resistor values in ohms
*V_{IN} is limited to 2 diode drops within ground or below V_{CC}

Figure 22. Voltage-to-Pulse Duration Converter

Servo System Controller (1)

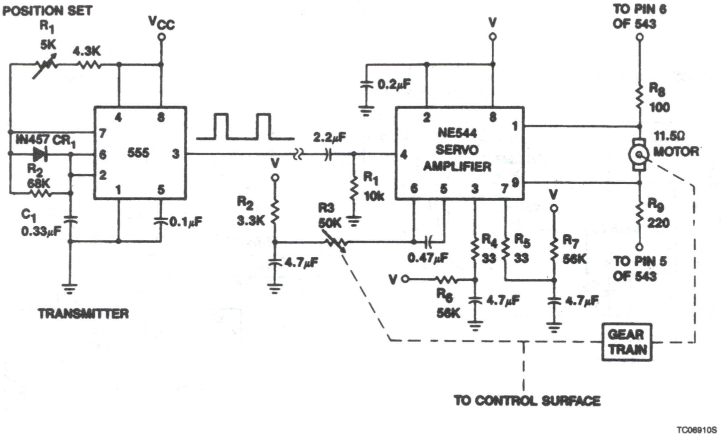
To control a servo motor remotely, the 555 needs only six extra components (Figure 23).

Stimulus Isolator (5)

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200V at 200μA (Figure 24).

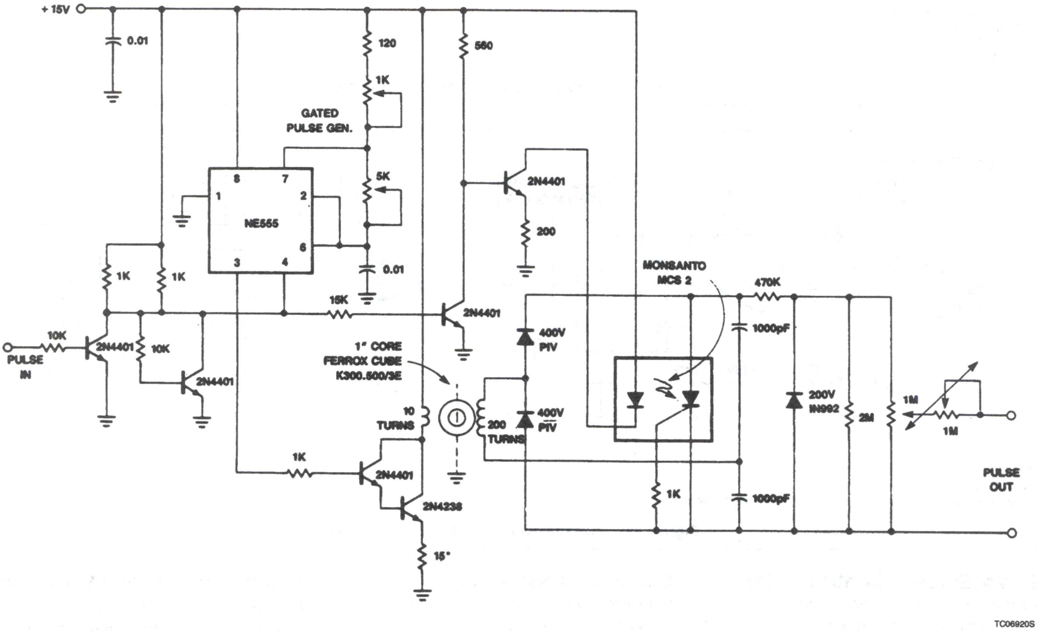
Voltage-to-Frequency Converter (0.2% Accuracy) (6)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to −10V range. Its mirror image (b) provides the same linearity over the 0 to +10V range, but is not DTL/TTL compatible (Figure 25).


POSITION SET
R1
5K
4.3K
VCC
IN457 CR1
R2
68K
C1
0.33μF
555
4
8
7
6
2
1
5
3
0.1μF
TRANSMITTER
2.2μF
V
R2
3.3K
4.7μF
R1
10k
R3
50K
0.2μF
NE544
SERVO
AMPLIFIER
0.47μF
R4
33
R5
33
R6
56K
R7
56K
4.7μF
4.7μF
TO PIN 6
OF 543
R8
100
11.5Ω
MOTOR
R9
220
TO PIN 5
OF 543
GEAR
TRAIN
TO CONTROL SURFACE
TC06910S

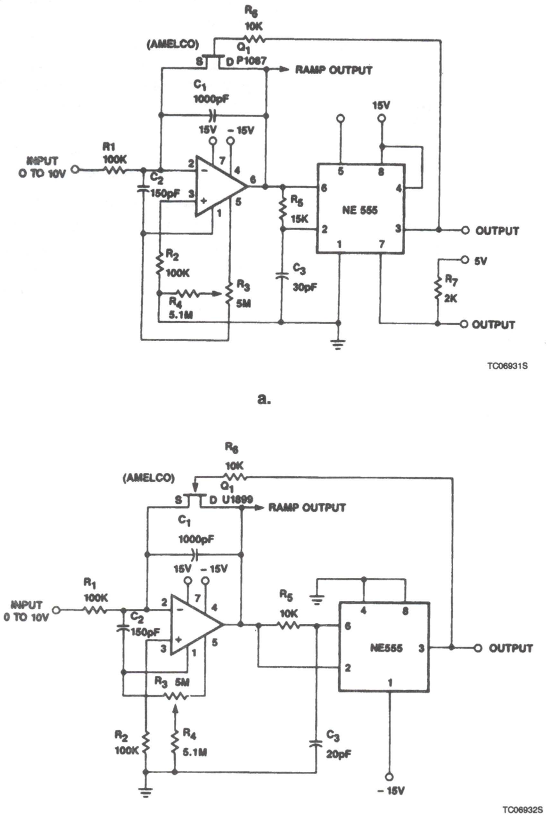
NOTE:
All resistor values in ohms.

Figure 23. Servo System Controller


+15V
0.01
120
1K
GATED
PULSE GEN.
5K
NE555
8
7
1
2
6
3
4
0.01
560
2N4401
200
1K
1K
10K
PULSE
IN
2N4401
10K
2N4401
15K
2N4401
1" CORE
FERROX CUBE
K300.500/3E
10
TURNS
200
TURNS
1K
2N4401
2N4236
15*
400V
PIV
400V
PIV
MONSANTO
MCS 2
470K
1000pF
1K
1000pF
200V
IN992
2M
1M
1M
PULSE
OUT
TC06920S

NOTES:
All resistor values in ohms
*Power rating depends on duty cycle from 1/2W for 20-25% duty cycle to 15-20W for 75-90% duty cycle

Figure 24. Stimulus Isolator

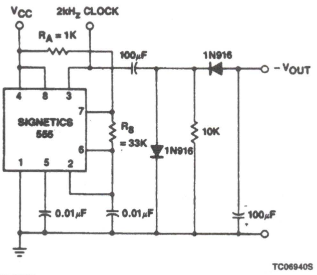

R6
10K
(AMELCO)
Q1
S D P1087
RAMP OUTPUT
C1
1000pF
15V -15V
15V
R1
100K
INPUT
0 TO 10V
C2
150pF
R5
15K
NE 555
OUTPUT
5V
R2
100K
R3
5M
R4
5.1M
C3
30pF
R7
2K
OUTPUT
TC06931S
R6
10K
(AMELCO)
Q1
S D U1899
RAMP OUTPUT
C1
1000pF
15V -15V
R1
100K
INPUT
0 TO 10V
C2
150pF
R5
10K
NE555
OUTPUT
R3 5M
R2
100K
R4
5.1M
C3
20pF
-15V
TC06932S

a.

b.

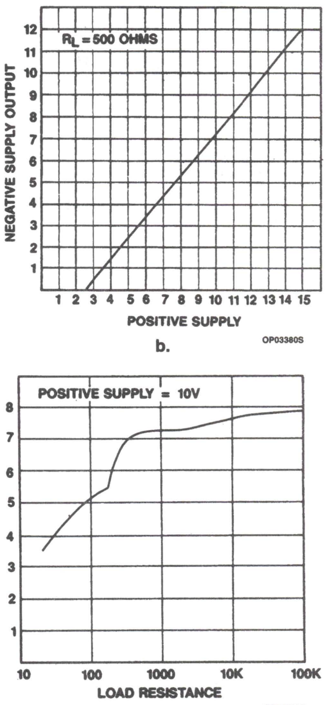
NOTE:
All resistor values in ohms

Figure 25


VCC
2kHz CLOCK
RA = 1K
100μF
1N916
-VOUT
SIGNETICS
555
RB
= 33K
1N916
10K
0.01μF
0.01μF
100μF
TC06940S

NOTE:
All resistor values are in ohms

a. Positive-to-Negative Converter



b.

c.

Figure 26

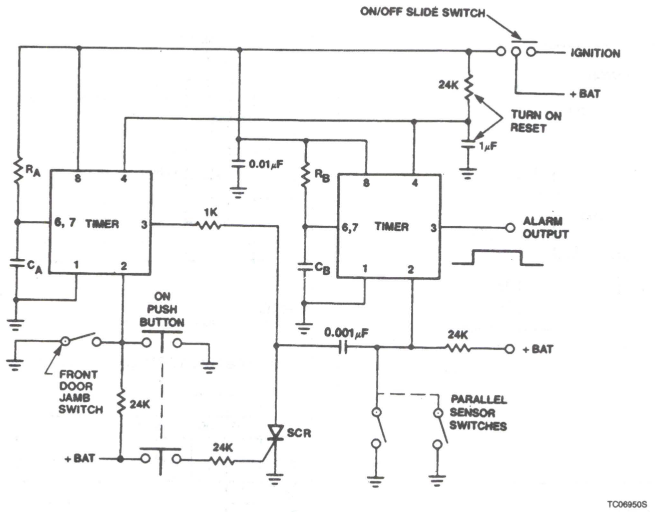
Positive-to-Negative Converter (7)

Transformerless DC – DC converter derives a negative supply voltage from a positive. As a bonus, the circuit also generates a clock signal.

The negative output voltage tracks the DC input voltage linearity (a), but its magnitude is about 3V lower. Application of a 500Ω load, (b), causes 10% change from the no-load value (Figure 26).

Auto Burglar Alarm (8)

Timer A produces a safeguard delay, allowing driver to disarm alarm and eliminating a vulnerable outside control switch. The SCR prevents timer A from triggering timer B, unless timer B is triggered by strategically-located sensor switches (Figure 27).


ON/OFF SLIDE SWITCH
IGNITION
+BAT
24K
TURN ON
RESET
1µF
R_A
8
4
6, 7 TIMER
3
C_A
1
2
0.01µF
R_B
1K
8
4
6,7 TIMER
3
ALARM
OUTPUT
C_B
1
2
ON
PUSH
BUTTON
FRONT
DOOR
JAMB
SWITCH
24K
0.001µF
24K
+BAT
PARALLEL
SENSOR
SWITCHES
SCR
24K
+BAT
TC06950S

NOTES:
Timer Signetics NE555
All resistor values in ohms

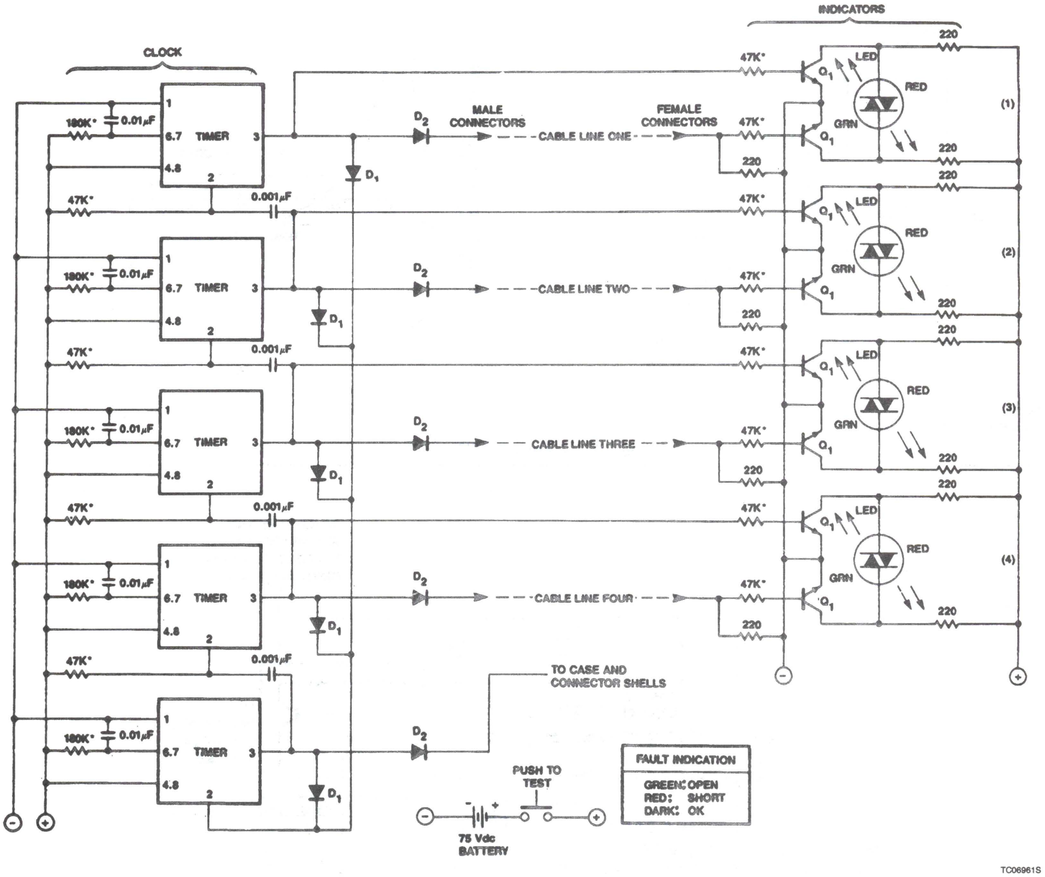
Figure 27. Auto Burglar Alarm

Cable Tester (9)

Compact tester checks cables for open-circuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse-generated by the timer IC appears at both ends of the line. A clock pulse just at the clock end of the line lights a green light-emitting diode, and a clock pulse only at the other end lights a red LED (Figure 28).

Low Cost Line Receiver (10)

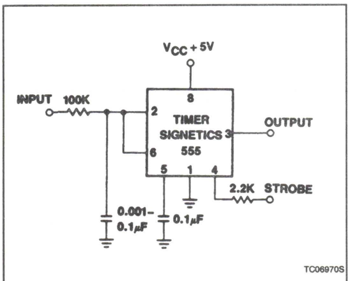
The timer makes an excellent line receiver for control applications involving relatively slow electromechanical devices. It can work without special drivers over single unshielded lines (Figure 29).


CLOCK
INDICATORS
180K*
0.01μF
1
6.7
TIMER
3
4.8
2
47K*
0.001μF
D2
D1
MALE CONNECTORS
FEMALE CONNECTORS
CABLE LINE ONE
CABLE LINE TWO
CABLE LINE THREE
CABLE LINE FOUR
47K*
220
Q1
LED
RED
GRN
(1)
(2)
(3)
(4)
TO CASE AND CONNECTOR SHELLS
PUSH TO TEST
75 Vdc BATTERY
FAULT INDICATION
GREEN: OPEN
RED: SHORT
DARK: OK
TC06961S

NOTES:
D_1 Silicon Signal Diode
D_2 1-A Silicon Diode
Q_1 200mW NPN Silicon, 2N2926 or ½ 2N2903

Timer Signetics NE555V
LED Monsanto MV5491
*½W Resistors

Figure 28. Cable Tester


VCC +5V
INPUT 100K
8
2
TIMER
SIGNETICS
555
3
OUTPUT
6
5
1
4
2.2K STROBE
0.001–
0.1μF
0.1μF
TC06970S

NOTE:
All resistor values are in ohms.

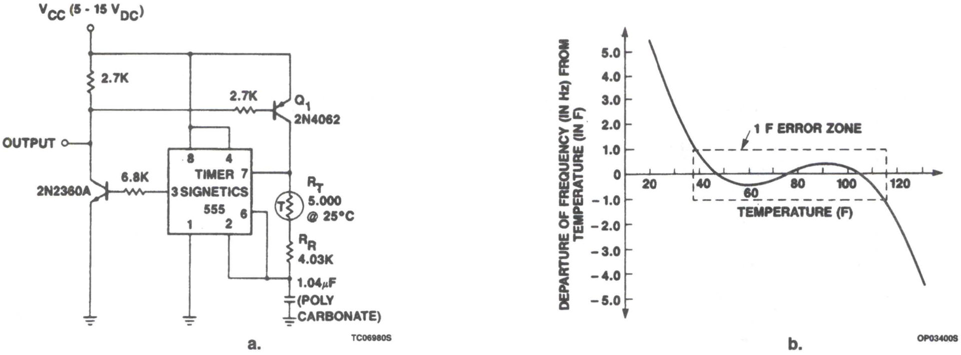
Figure 29. Low Cost Line Receiver

Temperature Control (11)

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within ± 1Hz over a 78°F temperature range (Figure 30).

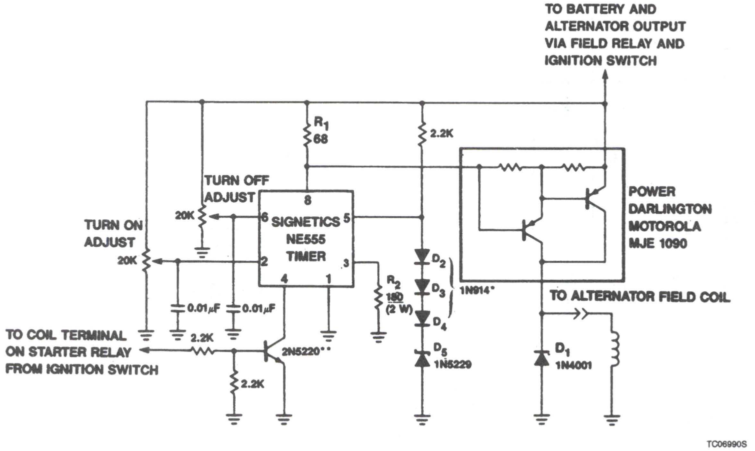
Automobile Voltage Regulator (12)

A monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (Pin 3) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4V in this case), the timer turns on and the Darlington pair conducts (Figure 31).


VCC (5 - 15 VDC)
2.7K
2.7K
Q1
2N4062
OUTPUT
6.8K
2N2360A
8
4
TIMER 7
3 SIGNETICS
555
6
1
2
RT
5.000
@ 25°C
RR
4.03K
1.04μF
(POLY
CARBONATE)
a.
TC06980S
DEPARTURE OF FREQUENCY (IN Hz) FROM TEMPERATURE (IN F)
5.0
4.0
3.0
2.0
1.0
0
-1.0
-2.0
-3.0
-4.0
-5.0
1 F ERROR ZONE
20
40
60
80
100
120
TEMPERATURE (F)
b.
OP03400S

NOTE:
All resistor values are in ohms.

Figure 30. Temperature Control


TO BATTERY AND
ALTERNATOR OUTPUT
VIA FIELD RELAY AND
IGNITION SWITCH
R1
68
2.2K
TURN OFF
ADJUST
20K
8
6 SIGNETICS 5
NE555
TIMER
2
3
4
1
TURN ON
ADJUST
20K
0.01μF
0.01μF
POWER
DARLINGTON
MOTOROLA
MJE 1090
D2
D3
D4
1N914*
R2
180
(2 W)
D5
1N5229
TO ALTERNATOR FIELD COIL
D1
1N4001
TO COIL TERMINAL
ON STARTER RELAY
FROM IGNITION SWITCH
2.2K
2N5220**
2.2K
TC06990S

NOTES:
* Can be any general purpose Silicon diode or 1N4157 device.
**Can be any general purpose Silicon transistor.
All resistor values are in ohms.

Figure 31. Automobile Voltage Regulator

Switching Regulator (13)

The basic regulator of Figure 32 is shown here with its associated timing and pulse-generating circuitry. The block diagram illustrates how the overall regulator works. The multivibrator determines switching frequency, and the error amplifier adjusts the pulse width of the modulator to maintain output voltage at the desired level. The output resistor divider provides the sensing voltage (Figure 35).

DC-to-DC Converter (14)

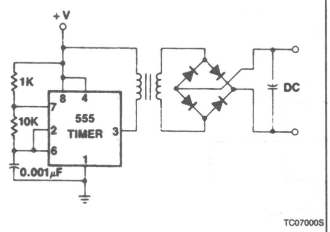

+V
1K
10K
0.001μF
8 4
7
2
6
555
TIMER
3
1
DC
TC07000S

Figure 32. DC-to-DC Converter

Ramp Generator (14)

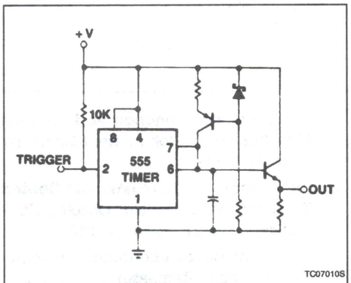

+V
10K
TRIGGER
8 4
7
2
6
555
TIMER
1
OUT
TC07010S

Figure 33. Ramp Generator

Audio Oscillator (14)

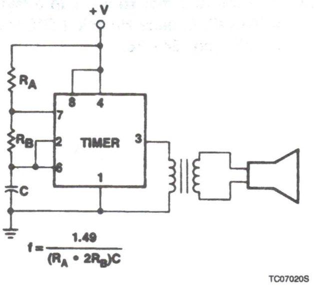
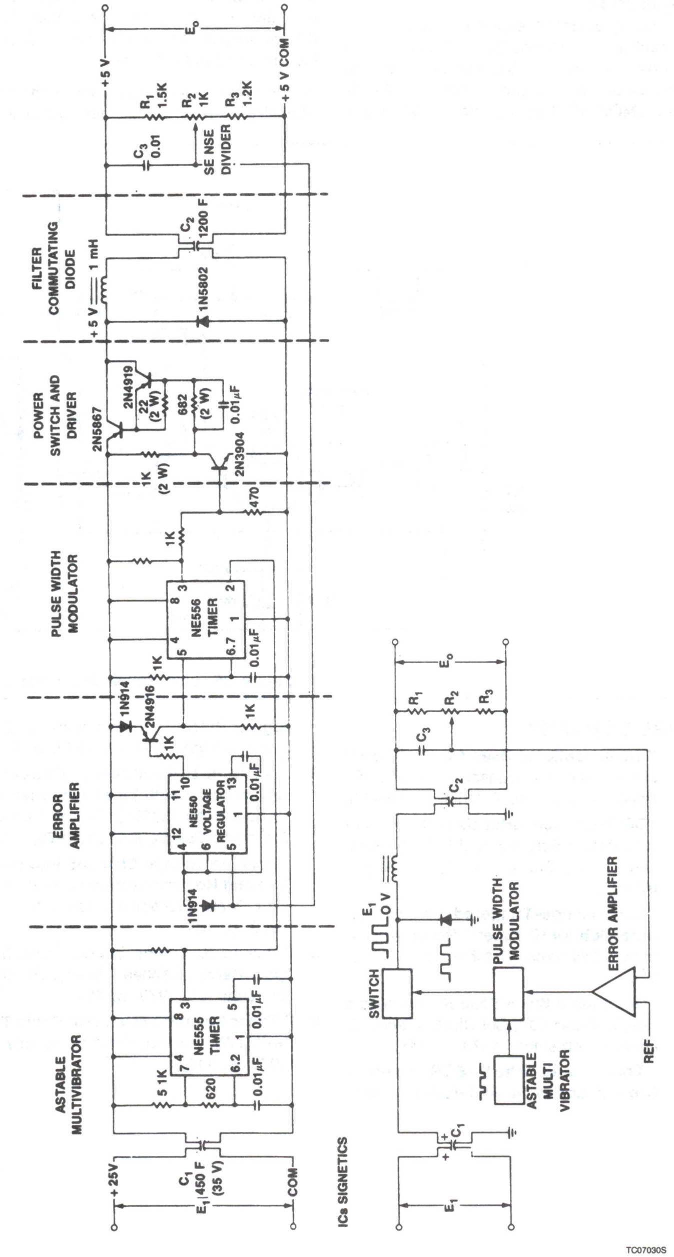

+V
R_A
R_B
C
8 4
7
2
6
TIMER
3
1
f = 1.49 / (R_A • 2R_B)C
TC07020S

Figure 34. Audio Oscillator


E_o
+5 V
+5 V COM
R_1 1.5K
R_2 1K
R_3 1.2K
C_3 0.01
SENSE DIVIDER
C_2 1200 F
FILTER COMMUTATING DIODE
+5 V
1 mH
1N5802
POWER SWITCH AND DRIVER
2N5867
2N4919
22 (2 W)
682 (2 W)
0.01μF
1K (2 W)
2N3904
470
PULSE WIDTH MODULATOR
1K
NE556 TIMER
8 3 2
4 5
1
6.7
0.01μF
1K
1N914
2N4916
1K
1K
ERROR AMPLIFIER
NE550 VOLTAGE REGULATOR
11 10
12
4
6
5
13
1
0.01μF
1N914
ASTABLE MULTIVIBRATOR
NE555 TIMER
8 3
4
7
5
1
6.2
0.01μF
0.01μF
5 1K
620
+25V
C_1 450 F (35 V)
COM
E_1
ICs SIGNETICS
E_o
R_1
R_2
R_3
C_3
C_2
E_1
0 V
SWITCH
PULSE WIDTH MODULATOR
ERROR AMPLIFIER
REF
ASTABLE MULTI VIBRATOR
C_1
E_1
TC07030S

NOTE:
All resistor values are in ohms.

Figure 35. Switching Regulator

NE555 and NE556 Applications

AN170

Low Power Monostable Operation

In battery-operated equipment where load current is a significant factor, Figure 36 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series and 74L00 series. During the monostable time, the current drawn is 4.5mA for T = 1.1RC. The rest of the time the current drawn is less than 50μA. (Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.)

In other low power operations of the timer where V_{CC} is removed until timing is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into Pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

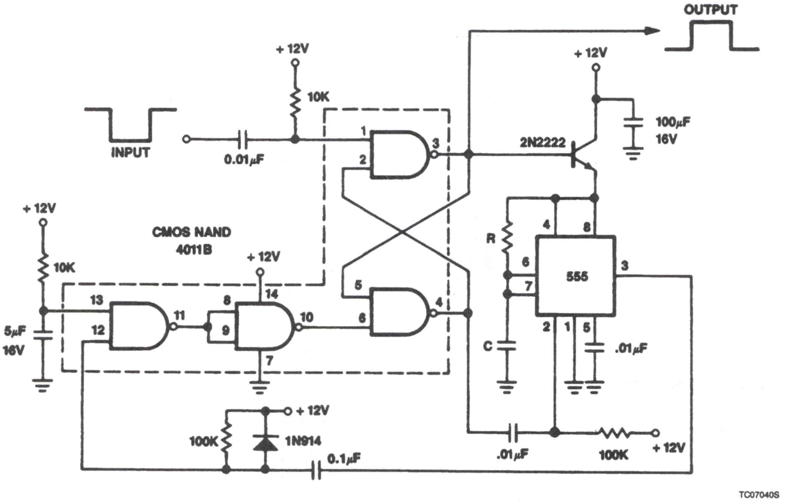


Figure 36. Low Power Monostable

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13. **"Switching Regulators, the Efficient Way to Power"**, Robert Olla, *Electronics*, August 16, 1973, pp. 94 – 95.
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Signetics

Linear Products

Section 8
Power Conversion and Control

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Symbols and Definitions for Voltage Regulators

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Current Limiting

The ability of the amplified segment to limit the output current of the device when safe operating limits are exceeded. Measured in amperes (pre-determined).

Duty Cycle (δ)

The time the output is turned on. Usually expressed as a percent of the period.

Efficiency

Regarding a regulator, the ratio of the total power input to the usable power output. Expressed as a percentage. (For example, if a regulator has a 50W input and a 40W output, its efficiency is 80%).

EMI/RFI

Electromagnetic Interference/Radio Frequency Interference regarding regulators, magnetic field disturbance and radio frequency interference signals generated especially by SMPS devices. Measurement is generally unspecified.

Line Regulation

Sometimes referred to as "static regulation". This term refers to the changes in the output as the input is varied slowly from its rated minimum value to its rated maximum value (from 105 VAC_{RMS} to 125 VAC_{RMS}). Measured in mV/V.

Load Regulation

Sometimes referred to as "dynamic regulation". This term refers to the changes in the output when load conditions are suddenly changed (from no load to full load). Measured in mV/V.

Package Type Designation

See full package designations in Appendix.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Power Dissipation

The ability of the regulator to tolerate excessively high levels of input power while maintaining its operation within the safe operating area of its active devices. Measured in watts.

Safe Operating Area Restriction (SOAR)

Limits the output current of the amplifier to maintain safe (no thermal runaway) operating conditions. (Accomplished through internal sensor amplifiers.)

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{SOLD}

Soldering temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10sec).

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

Thermal Regulation

Referred to as changes due to ambient variations of thermal drift. Also referred to as temperature coefficient, measured in ppm/°C or mV/°C.

Thermal Shutdown

The ability of the regulator to shut itself down when the maximum die temperature is exceeded. Measured in degrees Celsius.

Transient Response

The ability of the regulator to respond to rapid changes in line variations, load variations, or intermittent transient input conditions. (Transient Response is often referred to as "recovery time"). Measured in milliseconds.

Truth Tables

0 = logic level LOW

1 = logic level HIGH

X = don't care condition; has no effect under circuit conditions listed.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Voltage Limiting

The ability of the regulator to "shut down" in the event that the internal reference sources fail to function properly. Measured in volts.

Signetics

Linear Products

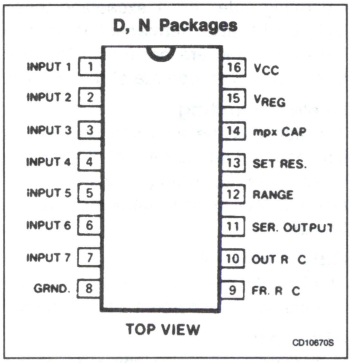
NE5044
Programmable Seven-Channel RC Encoder

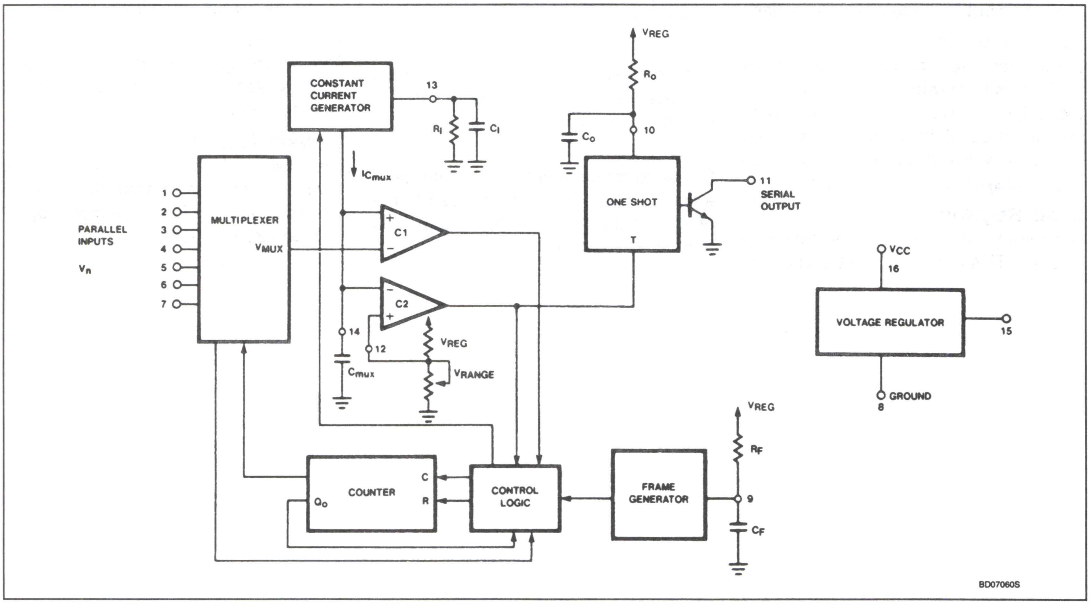
Product Specification

DESCRIPTION
The NE5044 is a programmable parallel input, serial output pulse width encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulse width modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An on-board 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

FEATURES
- **3 to 7 channels, externally selectable**
- **Constant-current dual linear ramp for linearity better than 0.3%**
- **Internal voltage regulator for low drift**
- **Wide supply range 4.5 – 12V**
- **Fixed or variable frame rate set by external RC**
- **External control for channel gain or range**
- **Versatile applications: exponential rates, mixing, dual rate, reversing, etc.**
- **Compatible with all transmission mediums**

APPLICATIONS
- **Radio-controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote-controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/ controls**
- **Remote analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION

D, N Packages
INPUT 1 1
INPUT 2 2
INPUT 3 3
INPUT 4 4
INPUT 5 5
INPUT 6 6
INPUT 7 7
GRND. 8
16 VCC
15 VREG
14 mpx CAP
13 SET RES.
12 RANGE
11 SER. OUTPUT
10 OUT R C
9 FR. R C
TOP VIEW
CD10670S

BLOCK DIAGRAM

CONSTANT CURRENT GENERATOR
13
R_I
C_I
I_Cmux
MULTIPLEXER
V_MUX
PARALLEL INPUTS
V_n
1
2
3
4
5
6
7
C1
C2
14
12
C_mux
V_REG
V_RANGE
V_REG
R_O
C_O
10
ONE SHOT
T
11
SERIAL OUTPUT
VCC
16
VOLTAGE REGULATOR
15
GROUND
8
V_REG
R_F
9
C_F
COUNTER
C
R
Q_0
CONTROL LOGIC
FRAME GENERATOR
BD07060S

Programmable Seven-Channel RC Encoder NE5044

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO Package	0 to +70°C	NE5044D
16-Pin Plastic DIP	0 to +70°C	NE5044N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	13	V
I_{OUT}	Regulator output current	−25	mA
	Serial output peak current	30	mA
	Constant-current generator	−1	mA
	Parallel inputs, range input	0-V_{REG}	V
	One-shot input, frame generator input	0-V_{REG}	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. $T_A = 25°C$ unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS Test Conditions $T_A = 25°C$, $V_{CC} = 10V$ using Test Circuit, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Power supply requirements						
V_{CC}	Power supply voltage range		4.5		12	V
I_{CC}	Power supply current	Excluding control pots and serial output currents		11	15	mA
Voltage regulator						
V_{REG}	Output voltage		4.5	5.0	5.5	V
I_{OUT}	Output current	$V_R \geqslant 4.5V$			−20	mA
	Line regulation	$7 \leqslant V_{CC} \leqslant 12$		0.005	0.02	V/V
Multiplexer						
I_{IN}	Input current	$V_n = 2.5V$		±30	±200	nA
V_{IN}	Input voltage range	$V_n - V_{Range} \geqslant 0.75V$	1.5		5	V
	Crosstalk			±1	±5	μs

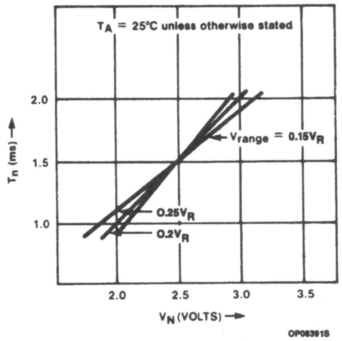
AC ELECTRICAL CHARACTERISTICS Test conditions $T_A = 25°C$, $V_{CC} = 10V$ using Test Circuit, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Output pulse						
t_n	Position	$R_I \bullet C_{MUX} = 1.25ms$ $V_n = 0.5V_{REG}$; $V_{RANGE} = 0.2V_{REG}$	1350	1500	1650	μs
	Position linearity error			5		μs
	Position tempco	$0°C \leqslant T_A \leqslant 70°C$		0.15		μs/°C
	Position PSR	$6V \leqslant V_{CC} \leqslant 12V$		0.5	1	μs/V
t_O	Width	$R_OC_O = 300\mu s$	240	285	330	μs
	Saturation voltage	$I_O = 25mA$		0.6	1	V
I_{11}	Leakage current			0.05	50	μA
R_I	Range input voltage	$R_I = 50k\Omega$ $R_I = 25k\Omega$	0.75 1.00			V V
	Frame time (fixed)	$R_FC_F = 30ms$	17	20	23	ms
	Inhibit threshold				0.4	V

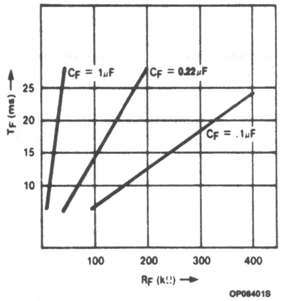
Programmable Seven-Channel RC Encoder | NE5044

TYPICAL PERFORMANCE CHARACTERISTICS

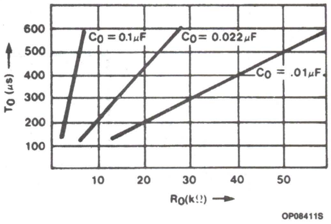
Output Pulse Width (T_n) vs Input Voltage (V_n)



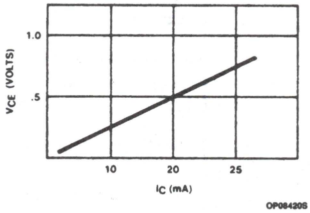
Frame Time (t_F) vs R_F



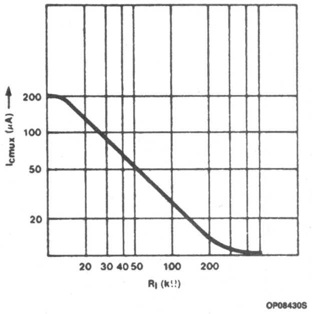
Output One-Shot Time (t_O) vs R_O



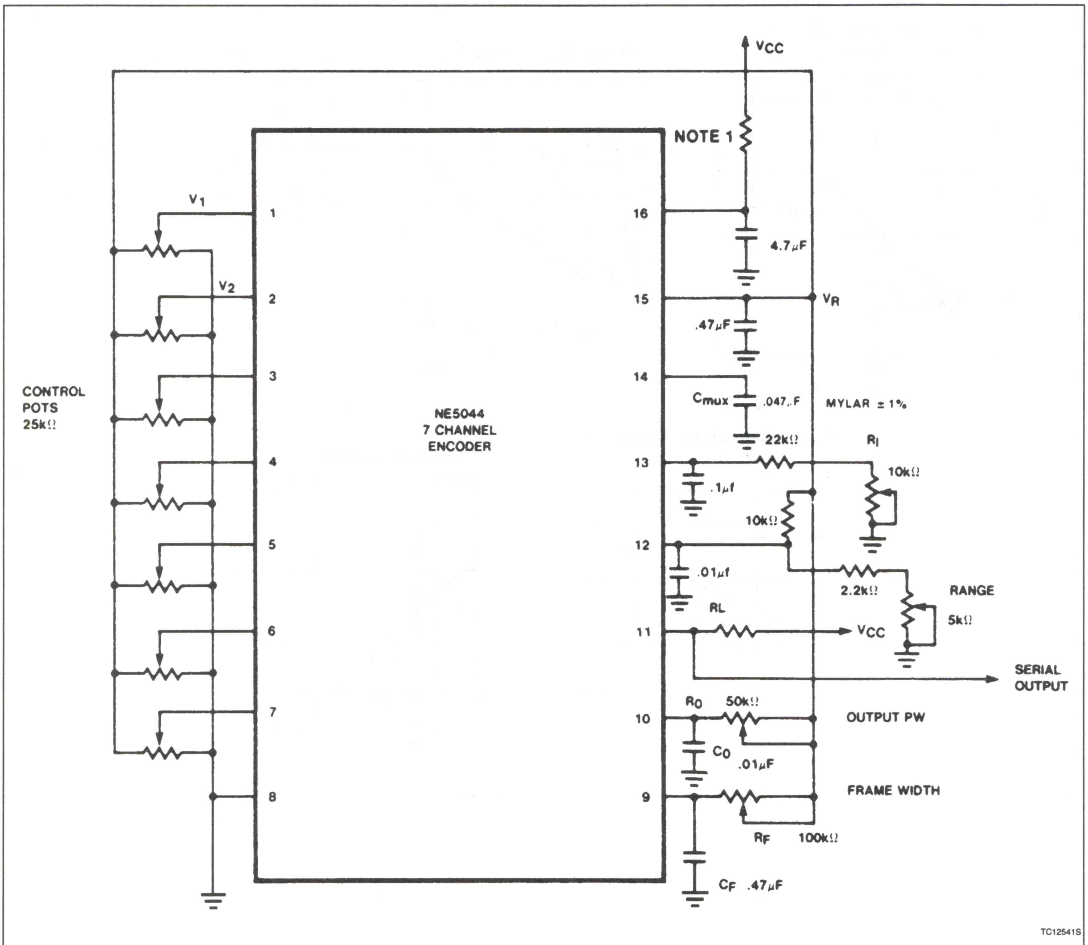
Output Saturation Voltage vs Output Current



Constant-Current vs R_I



TEST CIRCUIT


VCC
NOTE 1
V1
V2
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
CONTROL POTS 25kΩ
NE5044 7 CHANNEL ENCODER
4.7μF
.47μF
VR
Cmux
.047μF
MYLAR ± 1%
22kΩ
RI
10kΩ
.1μf
10kΩ
.01μf
2.2kΩ
RANGE
5kΩ
RL
VCC
SERIAL OUTPUT
RO
50kΩ
OUTPUT PW
CO
.01μF
FRAME WIDTH
RF
100kΩ
CF .47μF
TC12541S

NOTE:
At supply voltages exceeding 12V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended.

CIRCUIT OPERATION

The NE5044 is a programmable parallel input, serial output encoder containing all the active circuitry necessary to generate a precise pulse width modulated signal with 3 to 7 channels. The number of channels is externally programmable by grounding unused control inputs. A multiplexed dual linear ramp technique is used to provide excellent linearity, minimal crosstalk and low temperature drift. An on-board 5V regulator eliminates power supply sensitivities and has up to 20mA current capability for driving external loads. The encoder can be used in the fixed-frame mode or, with the addition of one external NPN transistor, as a variable-frame encoder.

The multiplexer functions as a strobed voltage-follower so that each input, when active, appears as a high-impedance input (> 1MΩ) and transfers the input voltage to the output. Only one of the seven inputs is active at any time and when a given input is inactive, it appears as an open circuit. The high-impedance multiplexer inputs eliminate loading on control inputs and simplify mixing circuits where several controls may be mixed onto one input.

Channel 4, 5, 6 and 7 inputs may also be used to select the desired number of output pulses by grounding one or more of these pins. That is, by grounding Pin 4 (Channel 4 input) only the first three inputs of the encoder will be used and a 3-channel encoder results. Grounding Pin 5 results in a 4-channel encoder, and so on. Thus, any number of channels between 3 and 7 may be selected. Internal voltage clamping prevents encoder malfunction if any input is shorted to supply, ground or open-circuited. The remaining channels will continue to be encoded except as noted above. This feature eliminates catastrophic failures due to control pot open- or short-circuits.

Programmable Seven-Channel RC Encoder NE5044

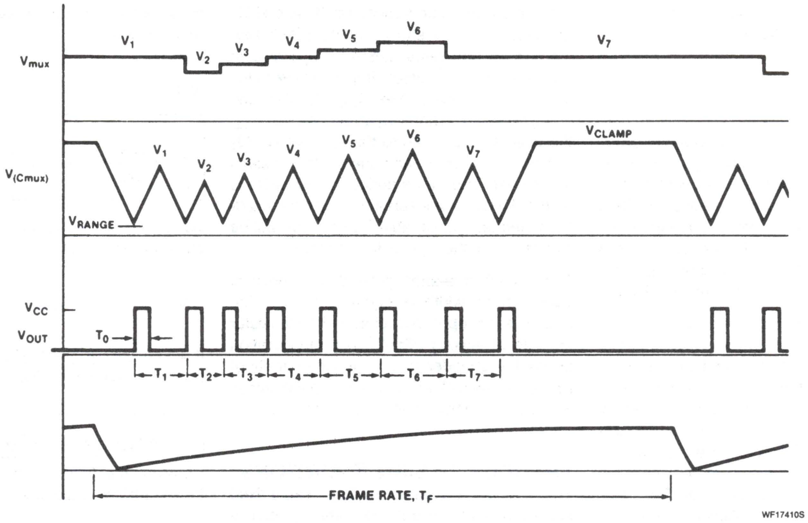

V_{mux}
V_1
V_2
V_3
V_4
V_5
V_6
V_7
$V_{(Cmux)}$
V_{CLAMP}
V_{RANGE}
V_{CC}
V_{OUT}
T_0
T_1
T_2
T_3
T_4
T_5
T_6
T_7
FRAME RATE, T_F
WF17410S

Figure 1. Encoder Timing Diagram — Fixed-Frame

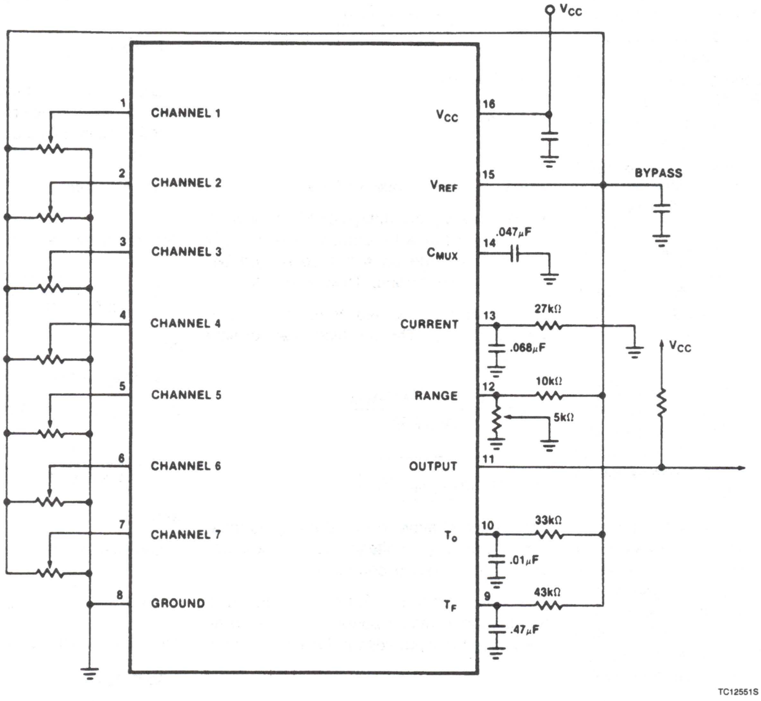

V_{CC}
1 CHANNEL 1
2 CHANNEL 2
3 CHANNEL 3
4 CHANNEL 4
5 CHANNEL 5
6 CHANNEL 6
7 CHANNEL 7
8 GROUND
16 V_{CC}
15 V_{REF}
BYPASS
14 C_{MUX}
.047μF
13 CURRENT
27kΩ
.068μF
V_{CC}
12 RANGE
10kΩ
5kΩ
11 OUTPUT
10 T_o
33kΩ
.01μF
9 T_F
43kΩ
.47μF
TC12551S

Figure 2

The constant-current generator is a bidirectional current source whose current is set by an external resistor R_I, where:

$$I_C = \pm \frac{V_R}{2R_I}$$

The current generator alternately charges and discharges the capacitor C_{MUX}. An internal feedback loop maintains a constant current and very high output impedance. This yields a typical linearity error of voltage input to pulse width output for the encoder of less than 0.1%. An external capacitor, C_I, is required to insure stability of the feedback loop.

Two high gain comparators, C1 and C2, compare the voltage across C_{MUX} with the multiplexer output voltage and the range input voltage. The input bias currents and offset voltages of these comparators are sufficiently low so as to not influence the overall accuracy of the encoder. The comparators feed the counter control logic which in turn controls the counter and current generator. The operation of this loop is as follows: When I_C is positive (sourced from the current generator into C_{MUX}) the capacitor linearly charges up until it reaches a voltage equal to the multiplexer output voltage; assume this to be the voltage at Pin 1, V1. At this time the output of C1 goes high, which reverses the direction of I_C (sinking into current generator from C_{MUX}). C_{MUX} now linearly discharges until it reaches the voltage set on Pin 12, V_{RANGE}. At this time the output of C2 goes high, which again reverses the polarity of I_C, clocks the counter, and triggers the output one-shot. C_{MUX} again charges up but now C1 goes high when C_{MUX} reaches V2, the voltage on Pin 2. The resulting voltage waveform on C_{MUX} is a triangle wave whose positive peaks correspond to the voltages on Pins 1 through 7 for the first through seventh peaks and whose negative peaks are constant and equal to V_{RANGE}. This waveform is shown in the first portion of Figure 1.

Independent control of I_C and V_{RANGE} allows the encoder to be tailored to virtually any combination of input voltage changes and output pulse width changes. The functional relationships between these variables will be defined in the next section.

The frame generator controls the encoder frame time. It can operate as an astable or monostable multivibrator whose period is 0.66 × R_FC_F. The encoder will generate a synchronizing pulse at the end of each frame. When C_{MUX} reaches the seventh positive peak it reverses and discharges to V_{RANGE}. The counter is clocked to the state where Q_O is high when $VC_{MUX} = V_{RANGE}$. C_{MUX} again charges up, but now the output of C1 is ignored, due to Q_O being high, and charges up to V_{CLAMP} and remains there. The encoder will remain in this state until a pulse from the frame generator is received. If R_F and C_F are connected as shown in the Block Diagram, then the frame generator operates in the astable mode, producing a narrow pulse output. This pulse allows C_{MUX} to start discharging again. When C_{MUX} reaches V_{RANGE}, the counter is clocked to the state where Q_1 is high (channel 1) and the entire process starts over. The frame period in this mode is 0.66 × R_FC_F and is referred to as the fixed-frame mode. The variable-frame mode will be discussed in the application section.

The output one-shot generates a positive pulse whose width is equal to R_OC_O. The output is an open-collector, NPN transistor capable of sinking 25mA. This configuration allows the encoder to drive a wide variety of RF stages as well as providing current pulses in 2-wire communications applications.

ENCODER DESIGN EQUATIONS

The triangular waveform on C_{MUX} has a fixed slope (constant current) and variable positive peak voltages. The time between the negative peaks of C_{MUX}, which is equal to the output period for that channel, is given by:

$$t_n = \frac{2\,(V_n - V_{RANGE})\,C_{MUX}}{I_C}$$

I_C is given by:

$$I_C = \frac{V_R}{2R_I},$$

where V_R = Reference Voltage.

Additionally, V_n, the voltage on Pin n, which is the control voltage for Channel n, is typically the wiper voltage on a pot connected between V_R and ground. Thus $V_n = X_nV_R$.

V_{RANGE} is also derived from V_R so that $V_{RANGE} = Y\ V_R$. The resulting channel time period is:

$$t_n = \frac{2\,(X_n - Y)\,V_R \cdot C_{MUX}}{(V_R/2R_I)}$$

$$\boxed{t_n = 4R_I\,C_{MUX}(X_n - Y)}$$

Thus, each channel pulse width, t_n, is independent of supply voltage and depends only on external passive components.

The conversion rate, CR, for each channel is the change in output period, Δt_n, divided by the change in input voltage for that channel, ΔV_n.

$$CR = \frac{\Delta t_n}{\Delta V_n} = \frac{\Delta t_n}{\Delta X_n} = 4\,R_I\,C_{MUX}$$

In most applications, the input variable X_n will have some neutral or center value about which it will vary, thus

$$X_n = X_o + x_n,$$

and

$$\boxed{CR = \frac{\Delta t_n}{\Delta X_n} = 4R_IC_{MUX}}$$

Where X_O is the neutral value for X and is assumed to be the same for all n. Now

$$t_n = 4R_IC_{MUX}\ (X_O - Y + X_n)$$

If we let $t_{NEUTRAL} = 4R_IC_{MUX}\ (X_O - Y)$ be the neutral value for t_n, then

$$\boxed{t_n = t_{NEUTRAL} + 4R_IC_{MUX}\ (X_n)}$$

Consider the following example to see how these design equations are used.

Assume:

$t_{NEUTRAL} = 1.5ms$

$X_O = 0.5$ — Control pot in center at

$t_n = t_{NEUTRAL}$

$\Delta x_n = \pm 0.1$ — Control pot resistance varies ± 10% (of total resistance) around neutral. This should include mechanical trim if used.

$\Delta t_n = \pm 0.5ms$

For this example, the conversion rate is

$$CR = \frac{\Delta t_n}{\Delta X_n} = \frac{0.5ms}{0.1} = 5ms,$$

so

$$4R_IC_{MUX} = 5ms.$$

If we let $C_{MUX} = 0.047\mu F$ then

$$R_I = \frac{5ms}{4 \times 0.047\mu F} = 26.5k\Omega = 27k\Omega$$

and

$$t_{NEUTRAL} = 1.5ms = 4R_IC_{MUX}(X_o - Y)$$

$$Y = 0.5 - \frac{1.5ms}{5ms} = 0.2.$$

The output pulse width is given by

$$t_O = R_OC_O$$

so if $t_O = 330\mu s$ and $C_O = 0.01\mu F$ then

$$R_O = \frac{330\mu s}{0.01\mu F} = 33k\Omega$$

The frame time constant, t_F, is given by

$$t_F = 0.66\ R_F C_F.$$

If $t_F = 20\text{ms}$ and $C_F = 0.47\mu F$

$$R_F = \frac{20\text{ms}}{0.66 \times 0.47\mu F} = 62\text{k}$$

Figure 2 shows the external connections for this example.

It should be noted that the temperature stability of all the encoded times depend on the temperature coefficients of the respective external R_C time constants. No internal temperature compensation is used on the chip. The typical temperature sensitivity of t_n using wirewound resistors and polycarbonate capacitors is less than 100ppm/°C in the −20°C to +70°C temperature range. For the above example, this corresponds to a change in t_n of ±7.5µs for a change in temperature of ±50°C.

AN131
Applications Using the NE5044 Encoder

Application Note

The encoder inputs have been designed to accept a wide variety of signal sources. This can range from simple systems using as an input the wiper of a control pot which is connected between V_R and ground, to complex systems incorporating mixing, exponential processing and/or control polarity reversing. In all cases, it must be remembered that the control inputs to the encoder look like voltage-followers, that is, they draw only very small currents (>200nA). The voltage range for these inputs is +1.5V to +5V; however, internal clamps limit the linear control to approximately +1.5V to +3.5V. These clamps prevent interaction between channels if one input is open-circuited or shorted to supply or ground.

An example was worked out previously which utilized mechanical fine trim of the inputs (where the control pot body is rotated a small amount). In some applications, it is desirable to implement this fine trim electrically with the use of an additional pot. Many methods exist to achieve this and two are shown below.

In Figure 1 the series resistors R_T and R_C are much larger than the control pots so as to minimize non-linearity errors, and the ratio of R_T to R_C controls the relative sensitivity of the control and trim pots. This scheme allows the control pot to be centered at neutral so polarity reversing can be achieved by reversing V_R and ground on the pots.

The second approach, shown in Figure 2, is a simpler method for achieving electrical trim.

$$T_n = 4R_IC_{MUX}\left(\frac{R_T + X_nR_C}{R_T + R_C} - Y\right)$$

$$CR = 4R_IC_{MUX}\left(\frac{1}{1 + R_T/R_C}\right)$$

Interfacing the 5044 encoder to the modulator of an RF transistor can be done in several ways, depending on the desired output power, frequency stability and oscillator leakage. The simplest method is to use the 5044 output to directly modulate the bias current of a crystal-controlled oscillator. Figure 3 shows an example of such a connection.

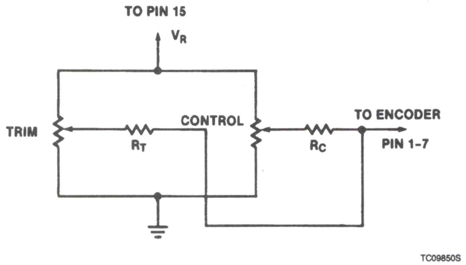


Figure 1

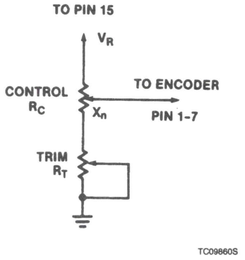


Figure 2

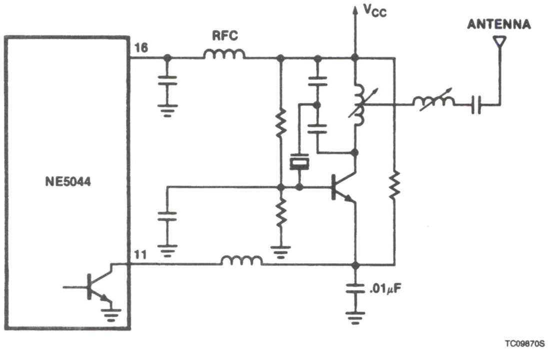


Figure 3. Modulated Oscillator Output Stage RF Transmitter

Applications Using the NE5044 Encoder

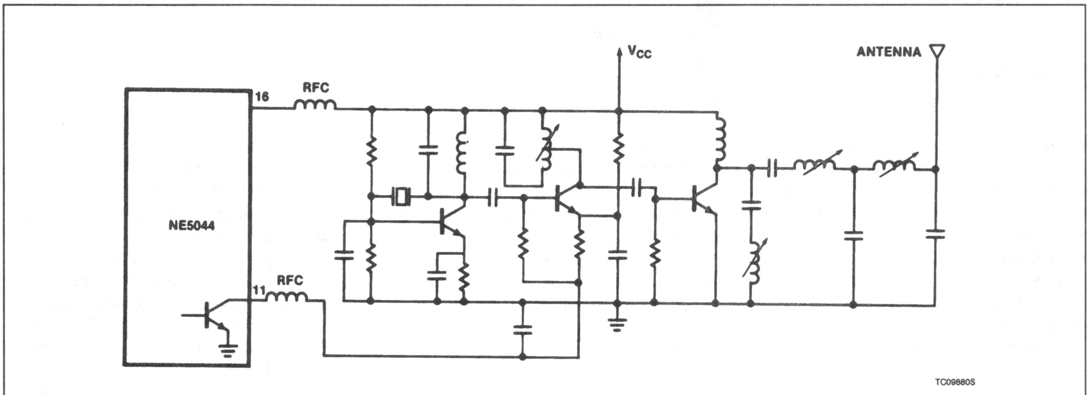


Figure 4. 5044 With High Performance RF Transmitter

In a high performance system, separate oscillator, modulator and RF output stages may be required. An example of such a circuit is shown in Figure 4. In some systems, it may be required to provide additional filtering between the encoder output (Pin 11) and the RF modulator to comply with FCC regulations.

In the previous section, a design example was given for a fixed-frame encoder (T_F constant). In some applications, it may be desirable to make the frame time variable, allowing the synchronization pulse, which follows the last channel, to remain constant. The variable-frame mode simplifies the synchronization pulse detector in the receiver since the pulse does not vary with the control inputs. However, the variable frame time may complicate the design of the pulse stretchers in the servos. The 5044 can be operated as a variable-frame encoder by discharging the capacitor C_F each time the output goes high. After the last output pulse, C_F is allowed to charge fully and the frame generator resets the encoder to channel 1. In this mode, the frame generator operates as a monostable multivibrator. Figure 5 shows the external connection. The sync pulse width (time between the falling edge of the last output pulse and the rising edge of the first pulse) is given by

$$t_S = 0.85\ R_FC_F + R_IC_{MUX}.$$

So if a sync of 6ms is desired and $C_F = 0.1\mu F$, then

$$R_F = \frac{0.85 \times 6ms - 0.047\mu F \times 27k\Omega}{0.1\mu F} \cong 39k\Omega.$$

Some applications may require an RF bypass on each of the multiplexer inputs, depending on PC board layout and the wiring between the control pots and the board. If such is the case, a 0.001μF capacitor is sufficient. Pin 12 may also require a bypass capacitor of 0.1μF.

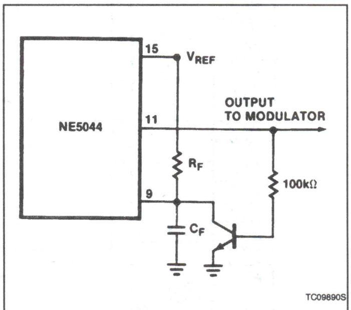


Figure 5. 5044 Variable-Frame Encoder

Signetics

AN1311

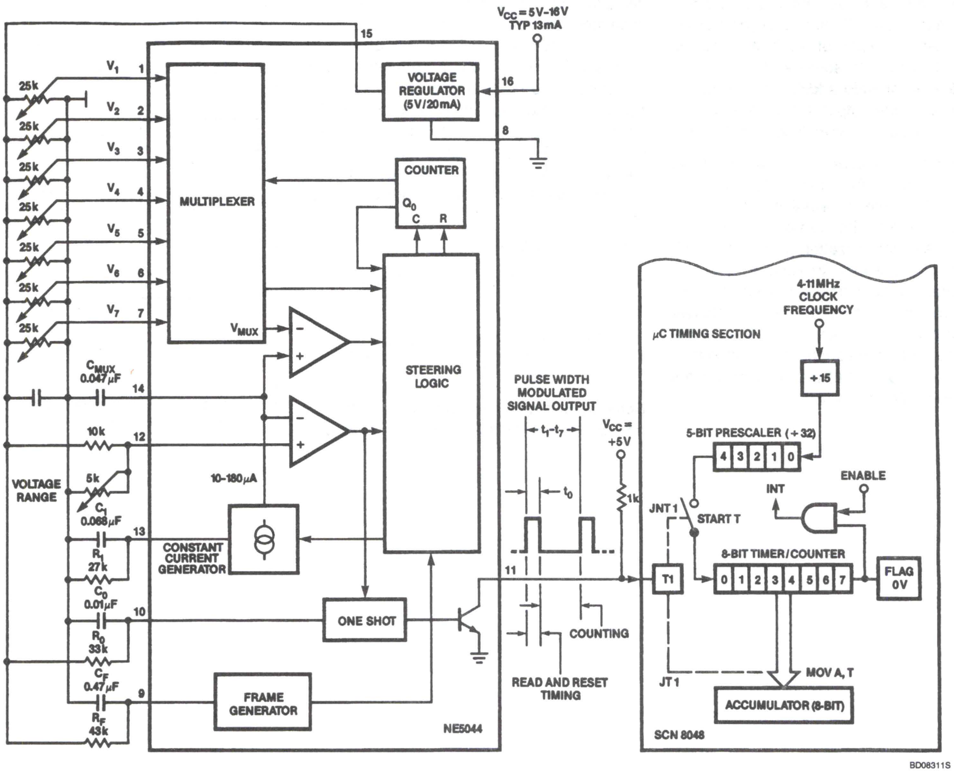
Low Cost A/D Conversion Using the NE5044

Application Note

Linear Products

Figure 1 shows an application for a multiplex A/D conversion using the pulse position encoder NE5044. In addition to its low cost per channel, the NE5044 has the following advantages:

- By grounding unused channel inputs between 3 and 7, high impedance analog inputs are available.
- Because of the serial output, only one microprocessor input is required.
- The 25mA output permits direct connection of optical couplers for optical isolation.
- The encoder in the 16-pin dual in-line package operates between 5 and 16V, but only uses 13mA.
- The non-linearity of the dual ramp conversion is between 0.1 and 0.3%.
- A voltage regulator with 20mA capability is on-chip.
- The seven analog inputs operate between approximately 1.5 and 3V with input current of 200nA.
- Open or short conditions, or connection to 5V are detected.
- The pulse which is to be measured is connected to the input T1 of the SCN8048. The instruction associated with this input, JUMP on NOT T1(JNT 1) and JUMP on T1 are used to start the 8-bit timer by using instruction start T. The instruction MOVE A, T transfers the result.



V_{CC} = 5V-16V TYP 13mA
15
16
8
VOLTAGE REGULATOR (5V/20mA)
25k
V_1 1
V_2 2
V_3 3
V_4 4
V_5 5
V_6 6
V_7 7
MULTIPLEXER
V_{MUX}
COUNTER
Q_0
C
R
STEERING LOGIC
C_{MUX} 0.047μF
14
10k
12
VOLTAGE RANGE
5k
C_1 0.068μF
13
R_1 27k
C_0 0.01μF
10
R_0 33k
C_F 0.47μF
9
R_F 43k
10-180μA
CONSTANT CURRENT GENERATOR
ONE SHOT
FRAME GENERATOR
NE5044
11
PULSE WIDTH MODULATED SIGNAL OUTPUT
t_1-t_7
t_0
COUNTING
READ AND RESET TIMING
V_{CC} = +5V
1k
μC TIMING SECTION
4-11MHz CLOCK FREQUENCY
÷15
5-BIT PRESCALER (÷32)
4 3 2 1 0
ENABLE
INT
JNT 1
START T
8-BIT TIMER/COUNTER
T1
0 1 2 3 4 5 6 7
FLAG 0V
JT 1
MOV A, T
ACCUMULATOR (8-BIT)
SCN 8048
BD08311S

Figure 1. The 7-Channel RC Encoder NE5044 has Various Advantages. The Serial Output of 7 Analog Values is Achieved by Pulse Position Modulation Within a Frame of Typically 20ms. The Pulse Widths Permit Processing Even With Slow Microcontrollers

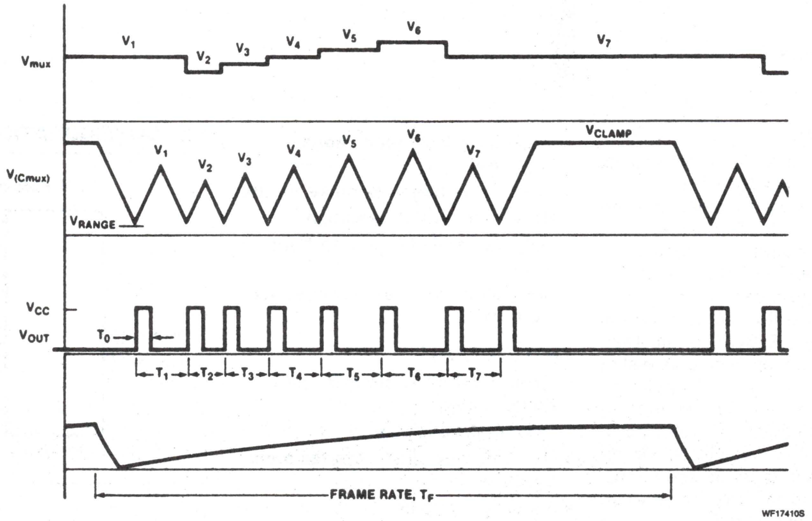

V_{mux}
V_1
V_2
V_3
V_4
V_5
V_6
V_7
$V_{(Cmux)}$
V_{CLAMP}
V_{RANGE}
V_{CC}
V_{OUT}
T_0
T_1
T_2
T_3
T_4
T_5
T_6
T_7
FRAME RATE, T_F
WF17410S

Figure 2. The NE5044 Timing Diagram

Originally published as "A/D — Umsetzer für Mikrocontroller," Klaus Petersen, Elektronik, April 19, 1985, Munich, Germany.

Signetics

NE5045
Seven-Channel RC Decoder

Product Specification

Linear Products

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $t_W = R_S C_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver, providing excellent isolation from the power supply as well as the decoder logic.

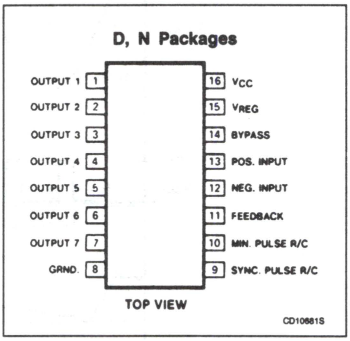
FEATURES

- **Decodes up to 7 channels**
- **High gain input amplifier**
- **Externally set sync. pause and minimum pulse**
- **Wide supply voltage range, 3.6V – 8V**
- **Positive or negative pulse inputs**
- **Noise and flutter rejection**
- **Outputs reset to zero without inputs**
- **Compatible with all transmission mediums**

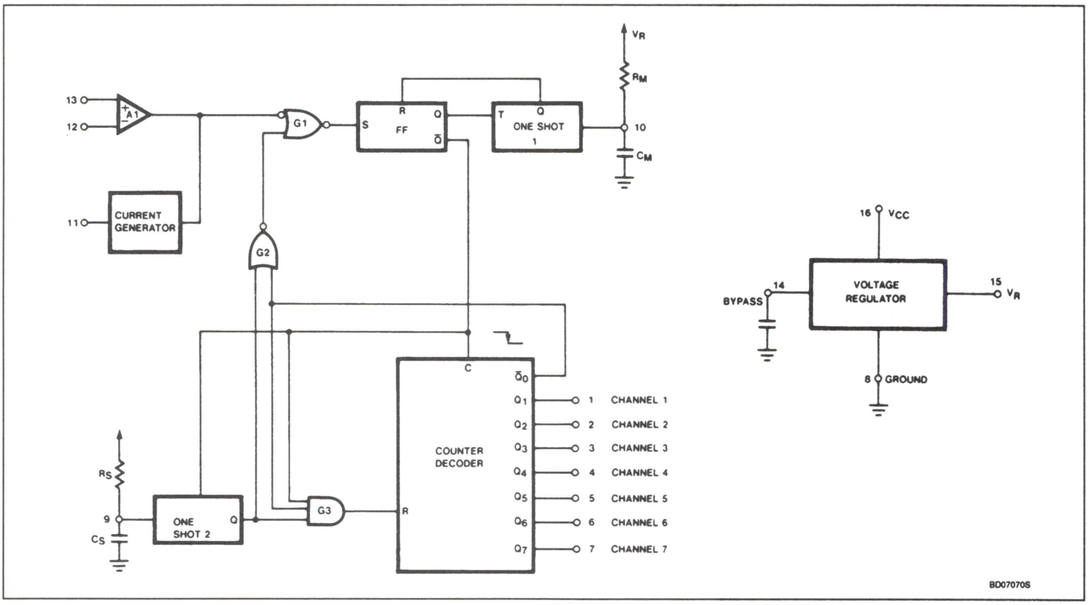
APPLICATIONS

- **Radio-controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote-controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/ controls**
- **Remote analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION


D, N Packages
OUTPUT 1 1
OUTPUT 2 2
OUTPUT 3 3
OUTPUT 4 4
OUTPUT 5 5
OUTPUT 6 6
OUTPUT 7 7
GRND. 8
16 VCC
15 VREG
14 BYPASS
13 POS. INPUT
12 NEG. INPUT
11 FEEDBACK
10 MIN. PULSE R/C
9 SYNC. PULSE R/C
TOP VIEW
CD10681S

BLOCK DIAGRAM


13
12
A1
11
CURRENT GENERATOR
G1
S
R
FF
Q
Q̄
T
Q
ONE SHOT 1
VR
RM
10
CM
G2
C
COUNTER DECODER
Q̄0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
1 CHANNEL 1
2 CHANNEL 2
3 CHANNEL 3
4 CHANNEL 4
5 CHANNEL 5
6 CHANNEL 6
7 CHANNEL 7
G3
R
RS
9
CS
ONE SHOT 2
Q
16 VCC
14
BYPASS
VOLTAGE REGULATOR
15 VR
8 GROUND
BD07070S

Seven-Channel RC Decoder NE5045

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5045D
16-Pin Plastic DIP	0 to +70°C	NE5045N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	10	V
I_{OUT}	Regulator output current	−25	mA
	Decoded output current	±5	mA
	Pause input voltage	0 to V_R	V
V_{IN}	Input amplifier voltage	0 to V_R	V
T_A	Operating temperature	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

NOTE:

1. $T_A = 25°C$ unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS

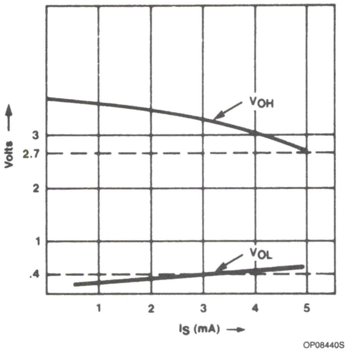
Standard conditions: $T_A = 25°C$, $V_{CC} = 5.0V$, unless otherwise stated, using Test Circuit.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Power supply requirements						
V_{CC}	Power supply voltage range	Test circuit	3.6		8.0	V
I_{CC}	Power supply current	Excluding input bias current		9.0	14.0	mA
Voltage regulator						
V_R	Output voltage		3.7	4.1	4.5	V
I_R	Output current	$V_R \geqslant 3.7V$			−15	mA
	Line regulation	$V_{CC} = 6V$ to $8V$		0.01	0.05	V/V
	Voltage drop	$V_{CC} = 4V$, $I_R = -10mA$			1.3	V
Input amplifier						
I_{BIAS}	Input bias current			10	100	nA
V_{IN}	Input voltage range		2.0		4.0	V
	Open-loop gain			60		dB
	Feedback current		100	200	400	μA
	Detection threshold	Test circuit, ΔV12 & 13		8	20	mV
t_S	Sync. pause time	$R_S C_S = 6.0ms$	5.1	6.0	6.9	ms
t_M	Minimum pulse time	$R_M C_M = 500\mu s$	405	475	545	μs
Outputs — all channels						
V_{OL}	Output voltage LOW	$I_{SINK} = 1mA$		0.25	0.5	V
V_{OH}	Output voltage HIGH	$I_{SOURCE} = 2mA$	2.7			V

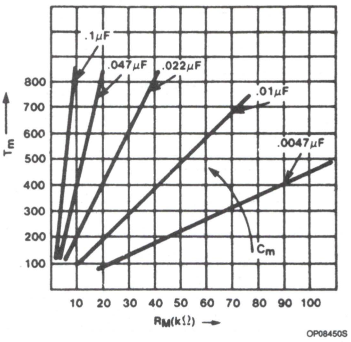
Seven-Channel RC Decoder NE5045

TYPICAL PERFORMANCE CHARACTERISTICS

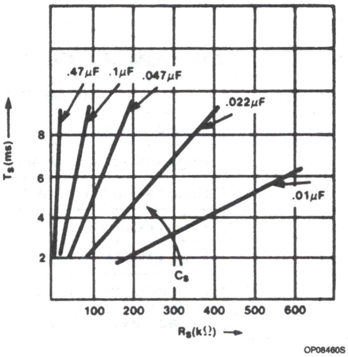
V_{OL} vs Sink Current and V_{OH} vs Source Current



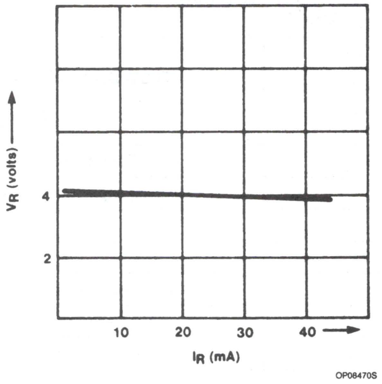
Minimum Pulse Time, t_M vs R_M, C_M



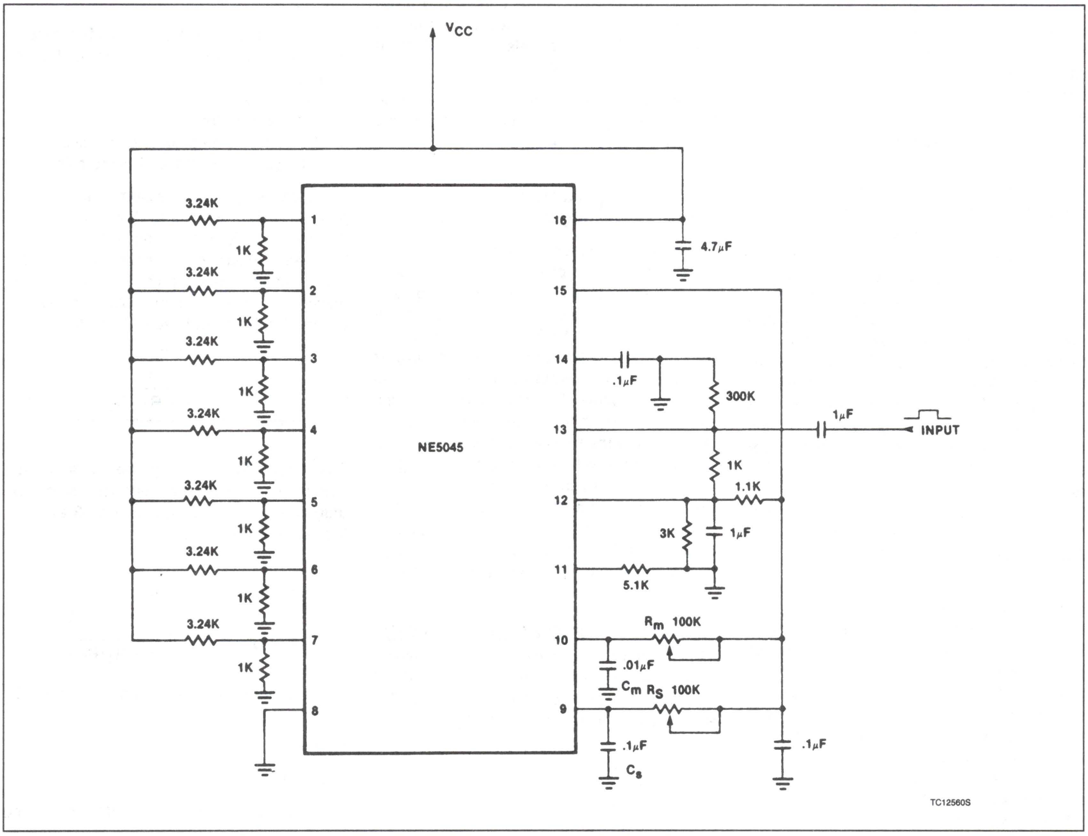
Sync Pause Time, t_S vs R_SC_S



Regulator Voltage vs Load Current



TEST CIRCUIT


VCC
NE5045
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
3.24K
3.24K
3.24K
3.24K
3.24K
3.24K
3.24K
1K
1K
1K
1K
1K
1K
1K
4.7μF
.1μF
300K
1μF
INPUT
1K
1.1K
3K
1μF
5.1K
Rm 100K
.01μF
Cm Rs 100K
.1μF
Cs
.1μF
TC12560S

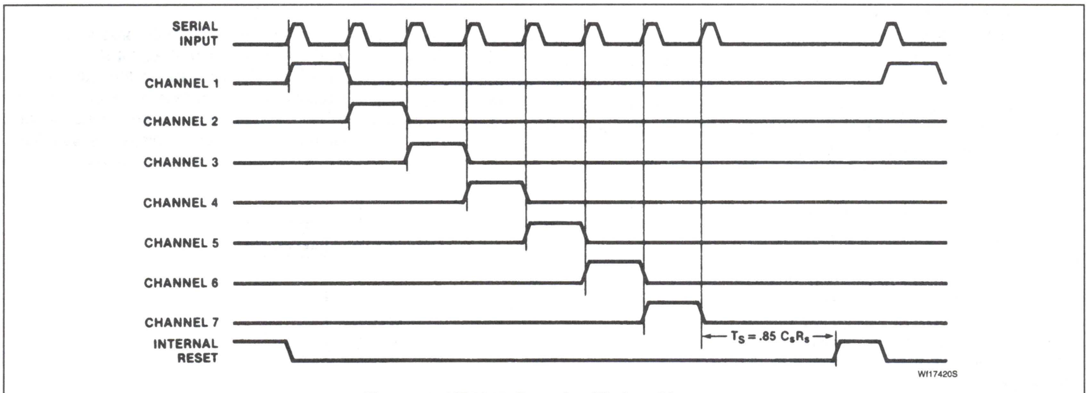

SERIAL INPUT
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
CHANNEL 5
CHANNEL 6
CHANNEL 7
INTERNAL RESET
Ts = .85 CsRs
WI17420S

Figure 1. NE5045 Decoder Timing Diagram

Seven-Channel RC Decoder NE5045

CIRCUIT OPERATION

The NE5045 is a serial input, parallel output decoder containing all the active circuitry necessary to separate up to 7 channels of information in a pulse width modulated system. An internal voltage regulator provides excellent power supply rejection for the decoder as well as a regulated output for a radio receiver, if used.

The high gain input amplifier, A1 ($A_V > 60dB$), allows either positive or negative pulses to be used and has input bias currents less than 10nA. Signals as low as $10mV_{P-P}$ can easily be demodulated. The feedback current generator can be used to provide positive feedback, thereby creating hysteresis in the input switching levels. Hysteresis prevents false triggering due to noise or IF amplifier distortion. If positive input pulses are used, the signal would be connected to the non-inverting input, Pin 13. In this case, the input threshold would be set by the voltage difference between Pin 12 and Pin 13, established externally with a resistive divider network. Design of the divider will be covered later. Negative input signals would be coupled to Pin 12, the inverting input.

The amplified signal from A1 is gated by G1 and in turn sets the flip-flop. Assume, for the time, that G2 is low. The combination of the flip-flop and One-Shot 1 produces a minimum pulse to clock the counter-decoder for each positive *edge* at Pin 13 which exceeds the voltage on Pin 12. The width of this pulse is: $t_M = R_M C_M$. With this arrangement, the system will not respond to any pulse after the first edge and before the end of t_M. In effect the input is turned off for a period equal to t_M following the leading edge of each input pulse. The noise immunity of the decoder is thus enhanced by the ratio of t_M to the period between input pulses. Obviously t_M must be less than the shortest period between input pulses.

The counter is clocked and One-Shot 2 is reset (capacitor C_S is discharged) each time the flip-flop is set. When the flip-flop is reset, C_S begins to charge up through R_S. The time constant $t_S = 0.85\ R_S C_S$ is normally much larger than the time between input pulses so that the output of One-Shot 2 remains low until the last pulse of a given frame is received. Figure 1 shows the timing diagram for the decoder. After the last pulse in a frame (system synchronized) $\overline{Q}_O$ will go low and G2 will go high. The input is now disabled by G1 until One-Shot 2 times out, at which time G2 will go low.

This connection serves two purposes:

(1) establishes synchronization in no more than one frame and

(2) prevents the counter-decoder from overflowing due to extra noise pulses in a given frame. Thus, any noise pulses in a frame will only affect those channels after that pulse and only in that frame.

If fewer than 7 channels of input are used then $\overline{Q}_O$ is high after the last pulse and the counter-decoder is reset when One-Shot 2 goes high.

Each channel has a totem-pole output stage capable of sourcing 2mA and sinking 1mA.

The voltage regulator operates in two modes, depending on the power supply voltage. If V_{CC} is greater than 5V, the voltage regulator acts as a series pass regulator with a nominal output voltage of 4.1V. When V_{CC} is less than 5V, the regulator acts as a dynamic decoupler where the bypass capacitor on Pin 14 filters out line transients. The internal pass transistor acts like an emitter-follower whose base is decoupled by the bypass capacitor. The value of capacitance will depend upon the degree of smoothing required and the amplitude of the line transients. If the regulator provides power for the radio receiver, this capacitor may have to be as large as 33μF. However, if this is not done, 1μF should be sufficient.

DECODER DESIGN EQUATIONS

The design of the decoder's external circuitry is quite simple. The minimum pulse One-Shot (#1) and the synchronization One-Shot (#2) each have time periods given by:

$$\boxed{t_M = R_M C_M}$$ and

$$\boxed{t_S = 0.85\ R_S C_S}$$

respectively. The constraints on these time periods are $t_M <$ the minimum input pulse width or time between leading edges of the input and $t_S >$ maximum input pulse width but $t_S <$ the sync pause (time between last pulse in frame and first pulse of the following frame).

The design of the input amplifier biasing network depends upon a number of factors, including:

1. Pulse polarity
2. Pulse amplitude
3. Variations in amplitude and noise
4. Detection threshold and hysteresis levels

For a very simple case, assume the input is a positive pulse train and the threshold of detection is desired to be 400mV without hysteresis. Figure 2 shows the input amplifier along with the associated biasing circuits. The resistors R_1 and R_2 set the voltage on Pin 12, which should be between 2V to 5V.

$$\boxed{V_{12} = V_R \frac{1}{1 + R_1/R_2}}$$

The threshold is set by the voltage drop across R_3, that is, the decoder will not be triggered until the voltage on Pin 13 exceeds the voltage on Pin 12.

$$V_{THRESHOLD} = V_{12} - V_{13}$$

$$V_{THRESHOLD} = V_{12} \left(\frac{1}{1 + R_4/R_3} \right)$$

If we assume $V_R = 4.1V$ and let $V_{12} = 3V$ then

$R_1 = 1.1k$

$R_2 = 3.0k$

The threshold is then set to 400mV by setting

$R_4/R_3 = 6.5$

R_4 should be sufficiently large so as to not load the input signal. If we let $R_3 = 51k$ then $R_4 = 330k$. Figure 3 shows the external connections for a complete decoder. Note that this circuit does not have provisions for noise filtering or rejection of amplitude variations.

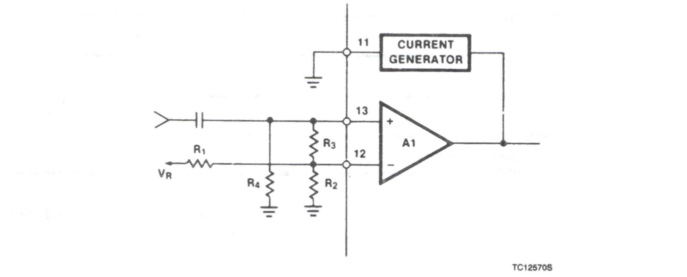


Figure 2. Input Amplifier Biasing NE5045

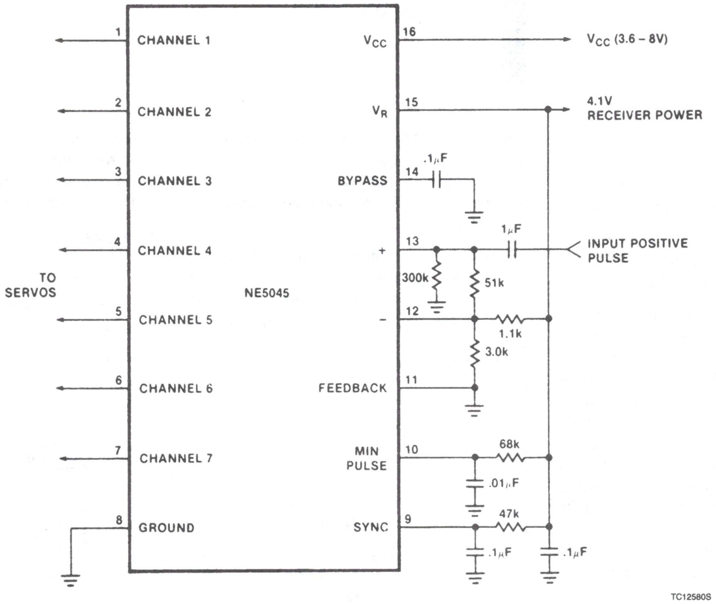

1
CHANNEL 1
2
CHANNEL 2
3
CHANNEL 3
4
CHANNEL 4
TO
SERVOS
5
CHANNEL 5
6
CHANNEL 6
7
CHANNEL 7
8
GROUND
NE5045
V_{CC}
16
V_{CC} (3.6 – 8V)
V_R
15
4.1V
RECEIVER POWER
BYPASS
14
.1μF
+
13
1μF
INPUT POSITIVE
PULSE
300k
51k
–
12
1.1k
3.0k
FEEDBACK
11
MIN
PULSE
10
68k
.01μF
SYNC
9
47k
.1μF
.1μF
TC12580S

Figure 3. NE5045 Decoder External Connections: $t_M = 0.68ms$; $t_S = 4ms$, $V_{THRESHOLD} = 400mV$

Signetics

Linear Products

AN132
Applications Using the NE5045 Decoder

Application Note

DECODER APPLICATIONS

In most applications, the decoder input will be derived from the decoder of a radio receiver and will have the following characteristics:

1. Contain thermal noise at low levels
2. Will vary in level depending on RF signal strength and may contain flutter

The thermal noise can be filtered with a simple RC circuit. This filter should have a cut-off frequency of about 3kHz which is approximately the bandwidth of the receiver IF amplifier. A lower cut-off frequency would limit the information rate and resolution of the system. Figure 1 shows the external connections for the decoder input amplifier in which the abovementioned conditions are handled. Diodes D_1 and D_2 charge the 1μF coupling capacitor to the peak input voltage minus the fixed voltage at Pin 12 and the diode drops. D_2 also clamps the input signal reaching A1. The 0.2μF capacitor forms a filter which allows the amplitude of the input to vary over a wide range and at high rates (as a result of RF flutter in the receiver) without false-triggering the decoder. When flutter occurs, the baseline of the positive input pulses varies as shown in Figure 2. The 0.2μF charges up to the average baseline voltage but the 10k resistor does not allow it to be charged by the information pulses. Thus, so long as the pulse peaks exceed the baseline voltage by greater than the drop across diode D_2, the system will be unaffected by baseline flutter no matter what its rate is.

Positive feedback has also been incorporated in the connection of Figure 1 to provide 100mV of hysteresis on the threshold. When the input (Pin 13) is low, the current generator is off and Pin 11 is near ground. However, when Pin 13 goes positive, the current generator turns on and approximately 150μA is sourced. This raises Pin 11 by 150μA × 4.7kΩ = 0.7V. The threshold is now given by

$$
\begin{aligned}
V_{THRESHOLD\ (ON)} &= V_{12} - V_{13} \\
&\simeq (V_{12} - V_{11}) \left(\frac{1}{1 + R_4/R_3} \right) \\
&\simeq (3 - 0.7) \left(\frac{1}{1 + 330k/51k} \right) \\
&= 0.3V
\end{aligned}
$$

So the threshold has been reduced by 100mV or the amplifier will not turn off until the input drops below 0.3V. A low pass filter is also used in the circuit of Figure 1. The 5.6kΩ and 0.01μF form a 2.8kHz low pass filter to improve the noise rejection characteristics of the detector.

A particular application of the NE5045 may not require all the components shown in Figure 1, however this circuit demonstrates all the features of the decoder which may be utilized.

Figure 3 shows a decoder connected for negative input pulses without hysteresis or flutter rejection. In this case, V_{13} is set to 3V and V_{12} is set to 3V + $V_{THRESHOLD}$.

If $V_{THRESHOLD} = 0.4V$

$$
R_4 = \frac{V_R - V_{12}}{V_{THRESHOLD}/51k} = \frac{4.1 - 3.4}{0.4/51k} = 89k\Omega \simeq 91k\Omega.
$$

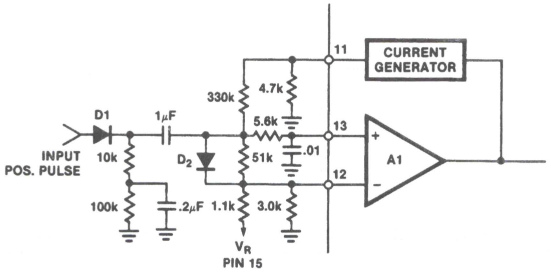


Figure 1. NE5045 Decoder Input Circuit With Flutter and Noise Filtering

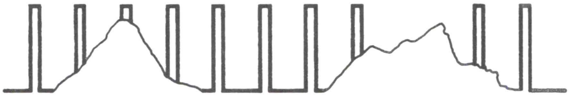


Figure 2. Input Signal With Fast Flutter

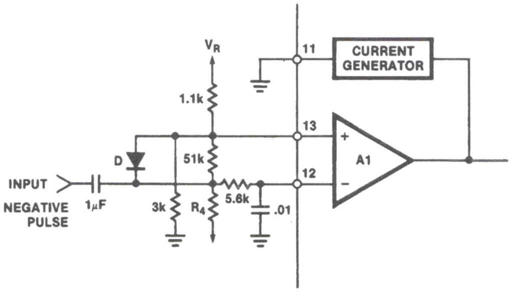


Figure 3. NE5045 Decoder With Negative Pulse Input

Signetics

Linear Products

AN1341
Control System for Home Computer and Robotics Applications

Application Note

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INTRODUCTION

With the rapid expansion of microprocessors and home computers into virtually all areas of modern life, there is an increasing need for methods of communication between computers and remote devices. Communication is usually accomplished by parallel digital data transfer and digital/analog conversion. This method is used in the case of most stationary computer peripheral devices. For movable peripheral equipment, or when communication has to cover larger distances, various forms of serial data concepts are used. The choice of a particular serial data bus system depends on cost/performance tradeoffs and possible requirements for coding and protocol standardization. In a digital system, a serial message unit typically consists of a byte of serial digital data plus additional bits for addressing, synchronization, and for other required system management functions.

In consumer applications, where low cost is an important factor, mixed digital and analog encoding methods can offer significant advantages over other serial encoding methods. The digital proportional system described here uses pulse-position modulation for serial data transfer. In contrast to pure digital encoding, where one message block (or frame) contains one byte of data, the digital proportional system packs several bytes of data into one frame. This is possible because the information is encoded in the form of pulse position.

This application note will first make a brief comparison of data transfer methods to show where the PPM transmission concept is advantageous. Then it will describe the control system that was implemented with recently developed integrated circuits. Next, it will explain the computer interface hardware and software, and, finally, it will use a robotics application as an example to point out the various features and the flexibility of the system.

Table 1. Comparison of Data Transfer Methods

TYPE	ENCODING	TYPICAL PERFORMANCE		APPLICATION
		Accuracy	Speed	
Digital bus	Parallel data	8-/16-bit	1Mbaud	Computer peripherals
Asynchronous or synchronous bus	Serial data	8-bit	300 – 1200 baud	Data communication Computer peripherals Robotics Serial ports (RS-232) Telephone modems
Computer network	Serial data	8-/16-bit	1Mbaud	Computer Communications
Digital proportional bus	Serial PPM	8-bit	3500baud	Consumer Home control Robotics

OVERVIEW OF THE CONTROL SYSTEM DATA BUSES

A comparison of various data transfer methods is shown in Table 1. The first three methods are purely digital and are mostly used for commercial data bus systems and for computer networks. The most common type of communication with a computer, besides the keyboard, is the standard parallel bus used to connect to peripheral equipment. It usually has 8 or 16 bits and typical megabaud transfer rates. For serial data transfer, asynchronous or synchronous data communication is used. Most common formats use 8 bits with modems operating at 300 to 1200baud. This is the standard method of serial communication used for peripherals, robotics, instrumentation ports, and telephone modems. The third method uses more sophisticated serial data computer networks. These networks, which are presently widely discussed in the industry, are high-performance buses with megabaud rates. They are intended for commercial computer communication, but not for low cost consumer applications.

The digital proportional bus uses pulse-position modulation for serial data transfer. It typically has 8-bit accuracy, with a speed of up to 3500baud. The serial bus is intended for low cost and medium-performance consumer applications such as home control, robotics, hobby, and educational uses. It is also used in consumer telemetry applications such as radio control. In contrast to the other buses in this table, the proportional bus uses mixed analog and digital encoding methods, which result in simple and compact hardware. The pulse positions are proportional to analog input voltages. The concept also lends itself to either amplitude or frequency modulation for remote control.

Other consumer-oriented serial buses belonging to this category are the D^2B and I^2C small area network serial buses developed by Philips[4]. These buses are digital encoding methods.

DIGITAL PROPORTIONAL ENCODING

A comparison between digital proportional and pure digital encoding methods is shown in Figure 1. Here one frame of digital data and digital proportional data are compared. The serial digital frame shown in the left part of the figure consists of one data byte plus additional bits for frame management. This format may vary when different standards are used. In contrast to this, a frame in a digital proportional system contains several bytes of data. This is because, with pulse-position coding, the data is represented by the time interval between pulses. In this case, a frame has 8 pulses and 7 bytes of data. In digitized form, each byte is 8-bit accurate. Notice that both systems have the amplitude noise immunity offered by digital encoding. One additional advantage of pulse-position coding is the fact that the analog voltage can be retrieved relatively easily anywhere in the system.

The pulse-position encoding process, which results in the pulse train shown in the figure, can be achieved using mixed digital and analog methods. Combined with a multiplex-

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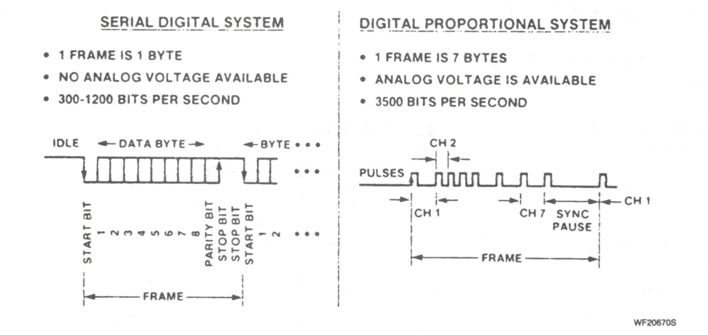

Figure 1. Comparison of Serial Digital Transmission and Digital Proportional Transmission

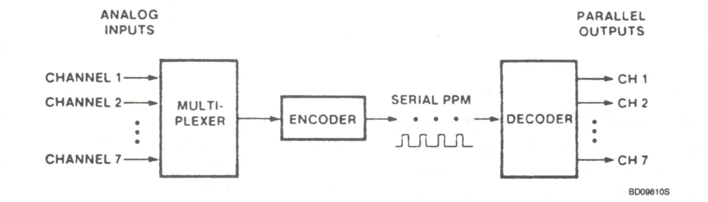

Figure 2. Standard Multiplexed Analog Proportional System

er, the standard serial data system is shown in Figure 2. Here seven parallel analog inputs are multiplexed and thus serialized. The pulse-position encoded pulses are transmitted to a decoder. The decoder converts the serial pulses into parallel pulse-width modulated outputs.

COMPUTER-CONTROLLED DIGITAL PROPORTIONAL CONTROL SYSTEM

If this bus is combined with a home computer or microprocessor, a complete serial data system is obtained as shown in Figure 3. First, digital information from the home computer is encoded in pulse position. The encoded information is transmitted over an RF link in this case. Other transmission methods such as wire, carrier current, fiber optics, or infrared can also be used. The signal is then detected, demultiplexed, and used for motion control functions, typically with a servomotor as shown. A return path for sense channel data, shown in the lower portion of the figure, uses the same encoding method but a different RF frequency. On the receiving end, pulse information is converted directly to the 8-bit digital form and fed back to the computer. The sensor data can then be processed to make control decisions. This means, with the system as shown here, all the elements of a computer remote-controlled system are present. The following section describes the building blocks required to implement this system.

IC BUILDING BLOCKS

Encoder

Encoder Circuit Operation

The digital-to-pulse encoder block diagram is shown in Figure 4. The encoder uses an 8-bit D/A converter and an analog-to-pulse-position converter. The encoder is a parallel input-serial output IC containing all the active circuitry necessary to generate a precise pulse-position modulated signal with seven channels. A multiplexed dual linear ramp technique is used to provide excellent linearity, minimal crosstalk, and low temperature drift. An on-chip 5V regulator, V_{REF}, eliminates power supply sensitivities and has up to 20mA current capability for driving external loads such as the RF transmitter. The encoder can be used in the fixed-frame mode, or, with the addition of one external NPN transistor, in the variable-frame mode.

The encoder inputs are either digital (i.e., inputs from the $D_0, D_1, \ldots, D_7$ computer I/O data lines), or multiplexed analog (i.e., inputs from the CH1, CH2, . . . , CH7 manual controls). The 8-bit parallel data from the computer I/O bus is converted into analog voltage, V_A, by the D/A converter. The manual inputs are usually joysticks. Each joystick presents an analog voltage to one of the multiplexer inputs. The analog multiplexer output voltage is V_A. Each channel has an input selector switch. The two input choices are either the computer mode (i.e., input from the D/A converter), or the manual mode (i.e., input from the analog multiplexed joysticks).

The multiplexer functions as a strobed voltage follower. Each multiplexer input, when active, is high impedance, and transfers the selected input voltage to the multiplexer output. The high-impedance multiplexer inputs eliminate the loading of the control inputs. This simplifies the mixing circuits where several control voltages may be mixed into one input.

The variable analog voltage, V_A, resulting either from the D/A conversion or from the analog multiplexer, is used to set the threshold of a comparator. V_A minimum = 2V corresponds to 0, i.e., all lines = 0 on the 8-bit data bus, and V_A maximum = 3V corresponds to $256 - 1 = 255$, i.e., all lines = 1 on the 8-bit data bus. The joystick range is also 2V to 3V.

Pulse-position timing is generated by alternately charging and discharging the C_{MUX} capacitor between two thresholds. The bottom threshold voltage is fixed at $V_{RANGE} = 1V$. The peak threshold voltage, V_A, defines each channel timing. The constant current generator, I_C, is a bidirectional current source whose current is set by an external resistor, R_I, where:

$$I_C = \pm \frac{V_{REF}}{2R_I}$$

An internal feedback loop maintains a constant current and very high output impedance. This yields a typical voltage-to-PPM encoder linearity error of less than 0.1%. An external capacitor, C_I, is required to ensure stability of the feedback loop. Independent control of I_C and V_{RANGE} allows the encoder to be tailored to virtually any combination of input voltage change and output pulse width change.

Two high-gain comparators, C1 and C2, compare the voltage across C_{MUX} with the multiplexer or the D/A output voltage, V_A, and with the range input voltage, V_{RANGE}. The input bias currents and offset voltages of these comparators are sufficiently low so as not to influence the overall accuracy of the encoder. The comparators feed the counter control logic, which counts the channels and controls the current source. The logic also controls two monostables that generate the frame timing and the output pulse timing. The logic operates as a loop: when I_C is positive (sourced from the current generator into

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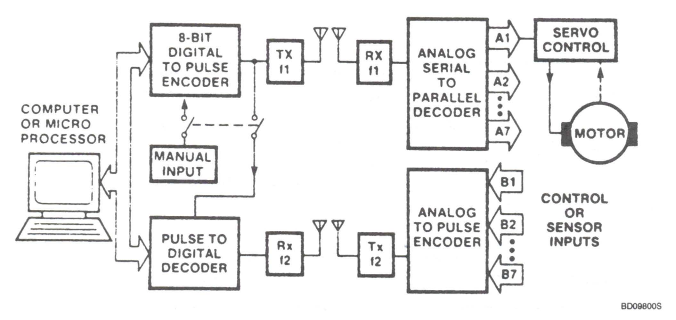
8-BIT DIGITAL TO PULSE ENCODER
TX I1
RX I1
ANALOG SERIAL TO PARALLEL DECODER
A1
A2
A7
SERVO CONTROL
MOTOR
COMPUTER OR MICRO PROCESSOR
MANUAL INPUT
PULSE TO DIGITAL DECODER
Rx I2
Tx I2
ANALOG TO PULSE ENCODER
B1
B2
B7
CONTROL OR SENSOR INPUTS
BD09800S

Figure 3. Block Diagram of the Analog/Digital Proportional Control System for Home Computer Applications

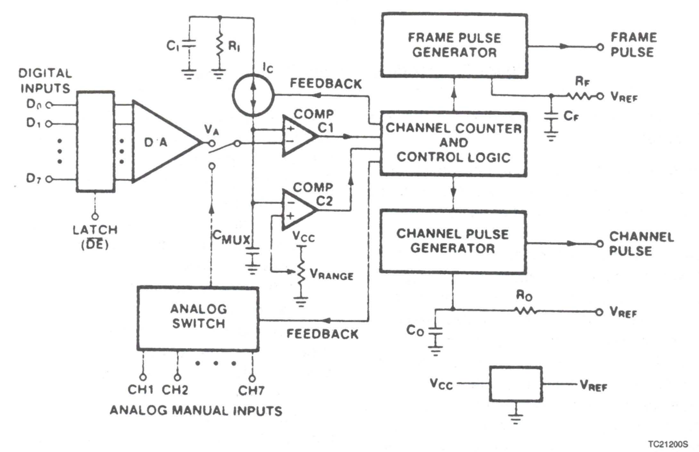
DIGITAL INPUTS
D0
D1
D7
LATCH (DE)
D/A
VA
CI
RI
IC
FEEDBACK
COMP C1
COMP C2
CMUX
VCC
VRANGE
ANALOG SWITCH
FEEDBACK
CH1 CH2 CH7
ANALOG MANUAL INPUTS
FRAME PULSE GENERATOR
FRAME PULSE
RF
VREF
CF
CHANNEL COUNTER AND CONTROL LOGIC
CHANNEL PULSE GENERATOR
CHANNEL PULSE
RO
VREF
CO
VCC
VREF
TC21200S

Figure 4. Block Diagram of the Analog/Digital-to-Pulse Position Encoder

C_{MUX}), the capacitor linearly charges up until it reaches a peak voltage, V_A. V_A is equal to the multiplexed output voltage for CH1, or the D/A output voltage for the first data byte. Assume this to be the voltage for channel 1, V_1. At this time the C1 comparator output goes High, which reverses the direction of I_C. I_C is then negative, sinking current into the generator from C_{MUX}. C_{MUX} then linearly discharges until it reaches the bottom threshold voltage set by V_{RANGE}. At that time the C2 comparator output goes High. This again reverses the polarity of I_C, clocks the counter, and triggers once the channel pulse generator. C_{MUX} again charges up, but then the C1 comparator output goes High when C_{MUX} reaches V_2, with the voltage on CH2. The resulting voltage waveform on C_{MUX} is a triangle wave whose positive peaks correspond to the V_A voltages on CH1 through CH7 (or to the 7 byte D/A input sequence), and whose negative peaks are constant and equal to V_{RANGE}. This waveform is shown in Figure 5.

Internal voltage clamping is used to prevent encoder malfunction if any input is shorted to supply, is grounded, or is open-circuited. This feature eliminates catastrophic failures due to opens or shorts in the control joystick potentiometers.

The frame pulse generator can operate as an astable or monostable multivibrator whose period is $0.66R_F\ C_F$. The encoder will generate a synchronizing pulse at the end of each frame. When V_{CMUX} reaches the seventh positive peak, it reverses and discharges to V_{RANGE}. When $V_{CMUX} = V_{RANGE}$, the counter is clocked to the state where C_{MUX} again charges up, but the output of the C1 comparator is ignored and C_{MUX} charges up to V_{CLAMP} and remains there, as shown in Figure 5. The encoder will remain in this state until a positive pulse from the frame generator is received. If R_F and C_F are connected as shown in Figure 4, the frame generator operates in the astable-multivibrator mode. It produces a narrow positive pulse output. This pulse allows C_{MUX} to start discharging again. When V_{CMUX} reaches V_{RANGE}, the counter is clocked to the state where the entire process starts over from channel 1. The frame period in this astable mode is referred to as the fixed-frame mode and as T_{FRAME} in Figure 5. The variable-frame mode, or the monostable-multivibrator mode, is discussed later.

The output of the channel pulse generator is a positive pulse width equal to $0.85R_O\ C_O$. The output stage is an open-collector NPN transistor capable of sinking 25mA. This configuration allows the encoder to drive a wide variety of RF stages and provides current pulses in 2-wire communication applications.

Encoder Design Equations

The triangular waveform on C_{MUX} has a fixed voltage slope (constant-current charging) and variable positive peak voltages. The time between the negative peaks of V_{CMUX}, equal to the output period for that channel, is given by:

$$t_N = \frac{2(V_N - V_{RANGE})C_{MUX}}{I_C}$$

V_N, the voltage on channel N, is either the wiper voltage on a joystick potentiometer connected between V_{REF} and ground, or the D/A output voltage, V_A. Thus $V_N = X_N\ V_{REF}$.

V_{RANGE} is also derived from V_{REF} so that $V_{RANGE} = Y\ V_{REF}$. The resulting channel time period is:

$$t_N = \frac{2(X_N - Y)V_{REF}C_{MUX}}{(V_{REF}/2R_I)}$$

$$t_N = 4R_I(X_N - Y)C_{MUX}$$

Thus, each channel pulse width, t_N, is independent of supply voltage and depends only on external passive components.

The conversion rate, CR, for each channel is the change in output period, dt_N, divided by the change in input voltage for that channel, dV_N.

$$\begin{aligned} CR &= dt_N/dV_N \\ &= (1/V_{REF})\ (dt_N/dX_N) \\ &= 4R_I\ C_{MUX}/V_{REF} \end{aligned}$$

In most applications, the input variable X_N will have a neutral, or center, value about which it will vary, thus:

$$X_N = X_O + X_N$$

and

$CR = (1/V_{REF})\ (dt_N/dx_N) = 4R_I\ C_{MUX}/V_{REF}$

where X_O is the neutral value for X and is assumed to be the same for all N. Now:

$$t_N = 4(X_O - Y + X_N)R_I\ C_{MUX}$$

If we let:

$$t_{NEUTRAL} = 4(X_O - Y)R_I\ C_{MUX}$$

be the neutral value for t_N, then:

$$t_N = t_{NEUTRAL} + 4X_N\ R_I\ C_{MUX}$$

It should be noted that the temperature stability of all the encoded times depends on the temperature coefficients of the respective external RC time constants. The typical temperature sensitivity of t_N using wire-wound resistors and polycarbonate capacitors is less than 100ppm/°C in the −20°C to +70°C temperature range. For the above example, this corresponds to a change in t_N of $\pm 7.5\mu s$ for a change in temperature of ±50°C.

Interfacing the encoder to the modulator of an RF transmitter can be done in several ways depending on the desired output power, frequency stability, and oscillator leakage. The simplest method is to use the PPM output to modulate directly the bias current of a crystal-controlled oscillator. In a high-performance system, separate oscillator, modulator, and RF output stages may be required. In some systems, it may be required to provide additional filtering between the PPM encoder and the RF modulator to comply with FCC regulations. Additional filtering may also be required in computer-controlled systems, where RF transmission can cause interference between channel pulses and frame pulses.

Encoder Applications

The encoder inputs have been designed to accept a wide variety of signal sources. This can range from simple systems using as an input the wiper of a control pot, which is connected between V_{REF} and ground, to complex systems incorporating mixing, exponential processing, and/or control polarity reversing. In all cases it must be remembered that the control inputs to the encoder look like voltage-followers; that is, they draw only very small currents (less than 200nA). The voltage range for these inputs is +1.5V to +5V; however, internal clamps limit the linear control to approximately +1.5V to +3.5V. Channels 4, 5, 6, and 7 analog inputs may be used to select the desired number of output pulses by grounding one of these inputs. That is, by grounding CH4 input, only the first three inputs of the encoder will be used and a three-channel encoder results. Grounding CH5 input results in a four-channel encoder and so on. Thus, any number of channels between 3 and 7 may be selected. The selected channels will continue to be PPM encoded.

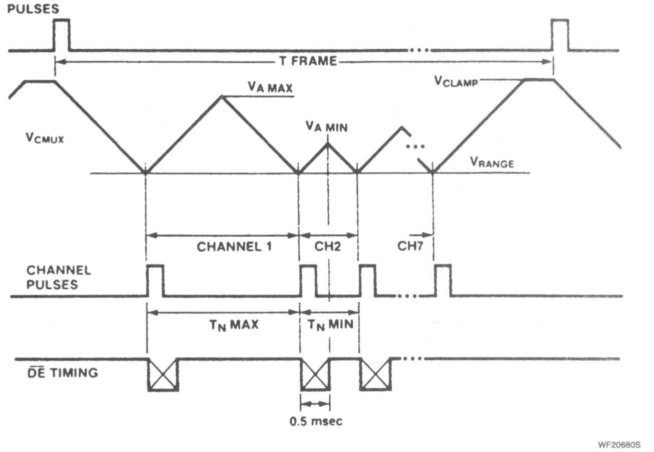

Figure 5. Encoding System Timing Diagram

In the fixed-frame mode, the frame generator functions as an astable multivibrator. In this mode, the total seven-channel time width is included in t_{FRAME} and the synchronization pause is the time difference between the seven-channel time width and t_{FRAME}. In some applications, it may be desirable to allow the synchronization pause, which follows the last channel, to have constant duration. The variable-frame mode simplifies the synchronization pulse detector in the receiver, since the total seven-channel time width is before t_{FRAME}, and the frame pulse generator operates as a monostable multivibrator. Here the synchronization pause is equal to T_{FRAME}. However, the variable-frame mode may complicate the design of the pulse stretchers in the servos. The encoder can be operated as a variable-frame encoder by discharging the C_F capacitor each time the channel pulse output goes High. After the last channel-end output pulse, C_F is allowed to charge fully and the frame generator resets the encoder to channel one.

Decoder

Decoder Block Diagram

Figure 6 shows the block diagram of the decoder. To decode the PPM signal, a serial-to-parallel conversion is required. The decoder separates up to seven channels of serial information into pulse-width modulated outputs. An on-chip voltage regulator, V_R, provides power supply rejection for the decoder as well as a regulated output for a radio receiver if used.

The serial PPM train, after RF detection, is fed into the decoder logic. The channel counter, the gates G1, G2, G3, and the flip-flop, make up the serial-to-parallel decoder. The channel counter is a 3-stage Johnson counter. The pulse-generator monostable provides noise immunity by blanking the input for a fixed time period. The synchronization pause-detector is required to separate successive frames and to initiate the channel count sequence. If a channel is lost due to interference, the system will synchronize again with the next frame without interruption of data. The output from the decoder is a parallel set of pulses. The width of these pulses represents the information for the control channels.

Decoder Circuit Operation

The high-gain input amplifier, $A_V = 60dB$, allows either positive or negative pulses to be used and has input bias currents less than 10nA. Signals as low as $20mV_{P-P}$ can be demodulated. The current generator, I_F, can be used to provide positive feedback, thereby creating hysteresis in the input switching levels. Hysteresis prevents false triggering due to noise or distortion. If positive input pulses are used, the signal is connected to the amplifier non-inverting input. In this case, the input threshold is set by the voltage difference between the amplifier input pins, established externally with a resistive divider network. Negative input signals are coupled to the amplifier inverting input. Each positive edge at the amplifier non-inverting input exceeding the voltage at the amplifier inverting input produces an output signal.

The amplifier output signal, gated by G1, sets the flip-flop. Assume, for the time, that G2 is

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Low. The flip-flop setting and the pulse generator monostable produce a minimum pulse that clocks the counter. The width of this pulse is $t_M = 0.66R_M\ C_M$. With this arrangement, the system will not respond to any next pulse after the present pulse rising edge and before the end of t_M. In effect, the input is turned off for a period equal to t_M following the leading edge of each input pulse. The noise immunity of the decoder is thus enhanced by the ratio of t_M to the period between input pulses, t_N.

The channel counter is clocked each time the flip-flop is set, and the sync pause detector monostable is reset (capacitor C_S is discharged). The sync pause is the time between the last channel pulse in a frame and the first channel pulse of the following frame. When the flip-flop is reset, C_S begins to charge up through R_S. The time constant $t_S = 0.66R_S\ C_S$ is normally much larger than the time between input pulses, so the output of the pause detector remains Low until the last pulse of a given frame is received.

Q_0 will go Low and G2 will go High in a synchronized-frame system after the last channel-end pulse in a frame. Gate G1 disables the decoder input until the pause detector monostable times out; at that time G2 will go Low. This serves two purposes;

1. Establishes synchronization in no more than one frame.
2. Prevents the channel counter from overflowing due to extra noise pulses in a given frame.

Thus, any noise pulses in a frame will only affect the consecutive channels after the present channel, and only in the present frame. If fewer than 7 input channels are used, Q_0 goes High after the last channel-end pulse and the channel counter is reset when the pause detector monostable goes High. Each channel has a totem-pole output stage capable of sourcing 2mA and sinking 1mA.

Decoder Design Equations

The minimum pulse generator and the synchronization pause detector each have time periods given by:

$$t_M = 0.66R_M\ C_M$$
$$t_S = 0.66R_S\ C_S$$

respectively. The constraints on these time periods are:

t_M smaller than the minimum time width between consecutive leading edges of the serial PPM input; $t_{NMIN} = 1$ms in the present robotics application.

t_S greater than the maximum input pulse width; $t_{NMAX} = 2$ms in the robotics application.

t_S smaller than the sync pause.

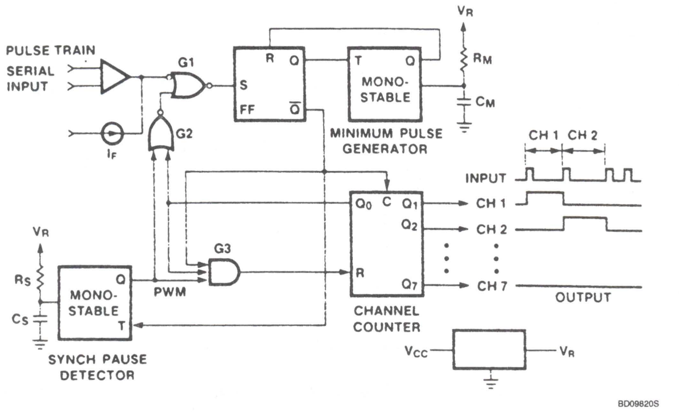

Figure 6. Block Diagram of the Pulse Position Decoder

Servo Amplifier

Servo Amplifier Block Diagram and Circuit Operation

The control servo could be considered the workhorse of the remote-control system, since its function is to translate the pulse information into a usable mechanical form. A block diagram of the servo control IC is shown in Figure 7. This IC is used to convert the pulse-width information into the position of a control surface.

The input pulse width is nominally 15ms for the zero position. It is amplified and directed to a pulse comparator. The leading edge of the input pulse is used to trigger an internal feedback pulse whose length is proportional to the position of the servo control arm.

The width of the input pulse is compared to the width of the internal pulse in the pulse comparator circuit, and the difference, called the error pulse, is fed to a pulse-stretcher and Schmitt-trigger circuit. At the same time, the polarity information resulting from the pulse comparison is stored in a directional flip-flop. This polarity information is then gated by the Schmitt-trigger output for a length of time which is proportional to the error pulse. The gate output actuates a bidirectional motor drive circuit so that the servo motor can be driven in either direction with an amount of drive proportional to the error in the servo position. The position is sensed with a feedback potentiometer wiper that is mechanically coupled to the control surface.

The dynamic behavior of the servo can be adjusted by externally setting the pulse-stretcher gain and the deadband. The circuit, shown in Figure 7, converts pulse width to position.

A similar circuit can be used to convert pulse width to analog voltage. This is shown in Figure 8. In that case, the output pulse is simply integrated and its DC value is fed back to control the timing of the monostable multivibrator. The feedback is negative, and the output voltage adjusts to a value proportional to the input pulse. This circuit can be used, for example, if analog information such as voltage or current is used or displayed directly without digital processing.

Servo Amplifier Timing

For the servo amplifier in Figure 7, a monostable multivibrator was developed that can be used in the linear or in the exponential charge mode. The leading edge of the input pulse starts the process.

In the linear mode, a constant-current source, I_T, charges up the C_T capacitor. The charging is linear and the C_T voltage versus time is a ramp. When the ramp voltage reaches the comparator threshold voltage, V_{TH}, the timing cycle stops. The threshold voltage, V_{TH}, is the negative feedback voltage. The length of the timing cycle for an ideal circuit is given in the following equation:

$$t = V_{TH}\ C_T/I_T$$

The sources of timing error are: the offset voltage and the bias current of the comparator, the saturation resistance of the internal transistor that resets C_T, and the errors in the charging current, I_T. These errors can be kept to less than 0.4% by proper component design, proper process design, and matched component layout. The I_T current source can be programmed by the R_T resistor, from Pin 2 to ground. This adds flexibility since the same time constant can be obtained with a range of different capacitance and current values.

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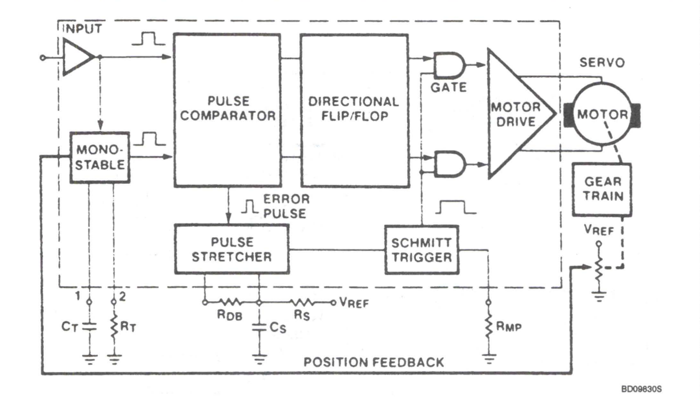


Figure 7. Servo Amplifier Block Diagram and Pulse Width-to-Position Conversion

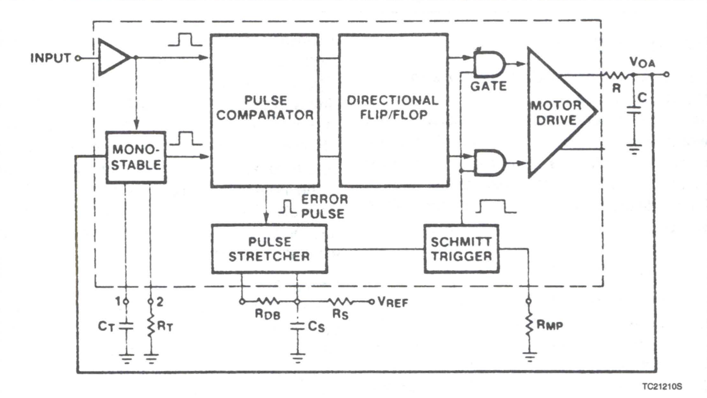


Figure 8. Servo Amplifier and Pulse Width-to-Analog Voltage Conversion

This flexibility also permits the use of the circuit in the exponential charge mode—which might be desirable for low-cost applications. In the exponential charge mode, the R_T resistor is connected from V_{REF} to Pin 1 (see Figure 7). The R_T resistor is charging up the C_T capacitor at Pin 1. The exponential timing response is given by the following equation:

$$t = R_T C_T \ln \frac{V_{REF}}{V_{REF} - V_{TH}}$$

Otherwise, the circuit function is similar to that of the linear mode.

The remaining resistors and capacitors, shown externally to the servo amplifier IC in Figure 7, determine the relationship between the error pulse and the output pulse. This permiting adjustment of the system's dynamic performance for a variety of servo motors and mechanical components.

HOME COMPUTER INTERFACE

Interface Requirements and Hardware

This section examines how the encoder system interfaces to the computer. The encoder interfaces directly with the internal data bus of a home computer by using the peripheral I/O port as shown in Figure 9. Besides the 8-bit bidirectional data lines, D_0 and D_7, four other control lines are required to communicate with the computer. These are: two address lines, A_0 and A_1, a $\overline{\text{Device Select}}$ line, and a Phase Zero Clock line. A_0, A_1, and $\overline{\text{Device Select}}$ are 3-state lines[8]. The hardware interface to the encoder requires only two flip-flops and two OR gates (see Figure 9).

The interface peripheral card plugs into the I/O connector on the computer board. It connects the computer to the joystick console via a 14-wire, 2ft. flat cable. The plug-in card can be modified for different hardware additions, and thus can be used to accommodate various home computer interface requirements.

The hardware implementation of the computer/robot interface contains an 8-bit D/A, an analog-to-PPM converter, flip-flops, gates, one 8-bit latch, seven switches, seven joystick controls, resistors, and capacitors. The D/A output range is 2V to 3V. The 2V corresponds to the digital input word 0, and 3V corresponds to the digital word 255. For manual joystick control, there are seven analog input lines, which access the multiplexer inputs. These input lines can be individually switched between computer control and joystick control.

Interface Signals and Timing

The data flow will be explained with reference to Figures 9 and 10. The P and F flip-flops serve as storage buffers. Synchronous with the computer Phase Zero Clock, they transfer the channel and the frame data from the P and F data lines to the computer. The ribbon cable lines, P and F, tell the computer that an encoder-console pulse is present. A complete frame contains eight channel pulses and starts and ends with a frame pulse. The P line carries the pulse-position data. The P line also serves as the system clock to tell the computer when to write data. Combining these functions simplifies the hardware when compared to a standard data acquisition system where these functions are separate. The QP flip-flop is set by the encoder channel pulses. The QF flip-flop is set by the encoder frame pulses. Both QP and QF flip-flops are reset by the computer write signal, $\overline{DE} = 0$. The $\overline{AE}$ and DTR lines are the read-enable and the data-ready controls for the pulse-to-digital converter.

Figure 11 illustrates the timing sequence of the computer-encoder dialogue. The rising edge of the channel pulse causes the P signal to go High (see arrow 1). To read P, the computer reads the D_4 data line. This line is read when the P flip-flop output is enabled and strobed. For this to occur, both A_1 and $\overline{\text{DEV.SEL.}}$ must be zero. The computer senses P = 1 and starts to prepare data on the D_0 and D_7 lines (see arrow 2). After the new data is on the bus, the computer sends the write signal, $\overline{DE} = 0$, to the encoder (see arrow 3). The new data is latched into the D/A input latch. $\overline{DE} = 0$ resets the QP and QF flip-flops (see arrow 4). QP or QF go Low before the channel or frame pulse disappears. To activate $\overline{DE}$, both A_0 and $\overline{\text{DEV.SEL.}}$ are zero. The D/A input data is designated as the "$D_0 - D_7$ Latch Output" signal in the figure. The idle data latched at the QF reset is erased by the first QP reset, when data for the first channel is latched.

Control System for Home Computer and Robotics Applications AN1341

Two consecutive channel pulses (within the same frame) are spaced from a minimum of 1ms to a maximum of 2ms. The frame pulses and F = 1 settings have a rate of about 50Hz. To read line F, line D_5 is selected. The D_5 line is read when the F flip-flop output is enabled by pulling both A1 and $\overline{\text{DEV.SEL.}}$ Low.

CONTROL SYSTEM APPLICATIONS

General Uses

Figure 12 illustrates the available transmission media for the serial data bus. In the present application, RF transmission was chosen. The figure also represents the consumer's viewpoint. It illustrates that a reduced number of components are needed between the encoder-decoder IC chip set and the home computer, thus keeping the system price low.

Some of the applications of the control concept are listed in Figure 13. A natural use is robotics. The control system concept can be used for home control, alarm and security systems, remote-controlled video games, and remote sensing of variables such as temperature, pressure, position, or motion. Analog data can be transferred and can be used for computer-controlled models. Examples of this last application would be a "smart" mouse that can learn to negotiate a maze and Radio Control models programmed by computer.

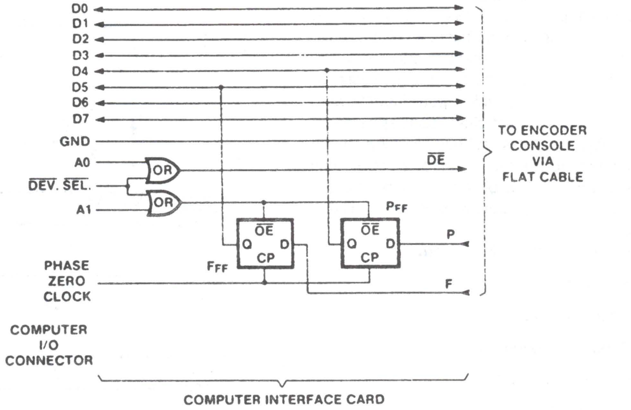

D0
D1
D2
D3
D4
D5
D6
D7
GND
A0
DEV. SEL.
A1
OR
OR
DE
TO ENCODER CONSOLE VIA FLAT CABLE
PFF
OE
Q
D
CP
OE
Q
D
CP
P
PHASE ZERO CLOCK
FFF
F
COMPUTER I/O CONNECTOR
COMPUTER INTERFACE CARD
LD07950S

Figure 9. Computer-Encoder Interface

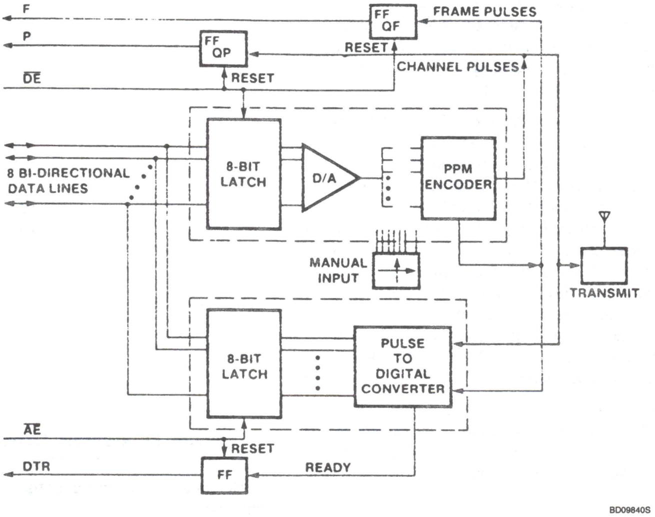

F
FF QF
FRAME PULSES
P
FF QP
RESET
DE
RESET
CHANNEL PULSES
8 BI-DIRECTIONAL DATA LINES
8-BIT LATCH
D/A
PPM ENCODER
MANUAL INPUT
TRANSMIT
8-BIT LATCH
PULSE TO DIGITAL CONVERTER
AE
RESET
DTR
FF
READY
BD09840S

Figure 10. Encoder Console Block Diagram and I/O Data and Control Lines

Control System for Home Computer and Robotics Applications AN1341

Computer-Controlled Robot

The digital proportional system is well-suited to robotics applications because of the multi-channel positioning capability and the possibility for computer remote control. Figure 14 shows the features which were incorporated in the computer-controlled robot application. The objective was to use existing home computers to remotely control a robot. The robot, which has a built-in receiver and decoder, has seven motion capabilities. These are:

1. Forward and backward drive
2. Steering
3. Head rotation
4. Shoulder movement
5. Elbow movement
6. Wrist rotation
7. Hand opening and closing

These motions can be executed in the "play" mode by either keyboard or manual joystick control. In either case, the motion can be recorded and then replayed. In the "record" mode, individual channels can be edited by simultaneously recording these channels while playing back the other channels.

The playback and the recording speed can vary. The max./min. speed ratio is 256/2 = 128. This permits recording in slow motion and playback at normal speed for precise control, or allows special effects such as slow or fast playback. Except for the drive channel, all other channels are closed-loop and can function at variable speed, with the servo motors and the servo amplifiers providing local feedback. The drive channel is open-loop and, when playing back with the drive active, the speed should be the same as the recording drive speed.

A discrete component radio control was used for the wireless robot control. The transmitter frequency and its range are based on standard radio control techniques.

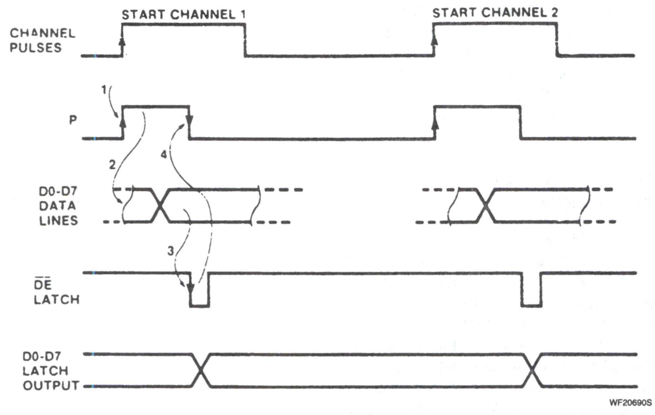


Figure 11. Computer-Encoder Interface Timing Diagram

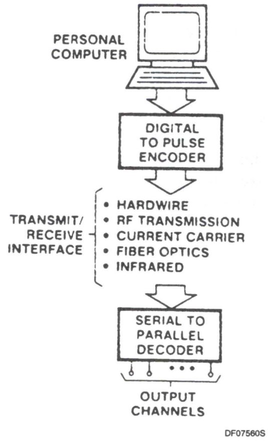


Figure 12. Available Transmission Media for the Serial Data Bus

COMPUTER PROGRAM

Computer-Robot Software Interface

To execute the different operating modes, an efficient software program is essential. The program has to be flexible and fast enough to interact in real-time with the robot. Machine language was used for the speed required to process the data. There are several operation options:

- Keyboard control over any channel combination with positive and negative steps in geometrical progression
- Joystick control over any channel combination
- Parallel recording of any channel combination from joysticks or keyboard. In the "record" mode the PPM-to-digital conversion is done by the software program
- Combined recording and playback, for individual channel editing
- Combined recording and playback, for any channel combination
- Graphic display of the pulse width of all seven channels
- Graphic display of the amount of motion-recording memory used for storage

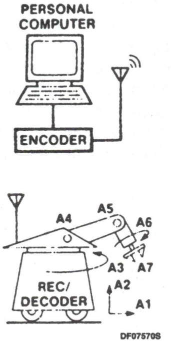
To determine how much time the "record" or the "play" modes would last in a real-time application with a home computer, two things should be defined: the available memory and the speed at which the channel data is stored-in or read-out from this memory. Approximately 19kB of memory is available for recording. One frame has 7 channels and one channel has 8 bits. The total number of frames that may be recorded in memory is: 19,000/7 = 2,714. Data is stored in memory per frame. Because one frame lasts about 20ms, the memory data is addressed at 20ms intervals.

The choice of the recording speed is available. Any speed can be specified by an integer from 1 to 255. This number, Nf,

Control System for Home Computer and Robotics Applications AN1341

- **ROBOTICS**
- **HOME CONTROL**
- **ALARM AND SECURITY SYSTEMS**
- **VIDEO GAMES (REMOTE CONTROL)**
- **REMOTE SENSING**
  - **-TEMPERATURE**
  - **-PRESSURE**
  - **-POSITION, LIGHT, ETC.**
- **ANALOG DATA TRANSFER (VOLTAGE/CURRENT)**
- **COMPUTER CONTROLLED MODELS**

Figure 13. General Control Applications of the Serial Data Bus



- **PLAY MODE**
  - **-COMPUTER (KEYBOARD) CONTROL**
  - **-MANUAL JOYSTICK CONTROL**
- **RECORD MODE**
  - **-EDITING**
  - **-VARIABLE RECORDING SPEED**

REMOTE MOTION CAPABILITIES
A1-FORWARD/BACKWARD MOTION
A2-STEERING (90°C)
A3-HEAD ROTATION (360°C)
A4-SHOULDER (ARM) MOVEMENT (110°C UP/DOWN)
A5-ELBOW MOVEMENT (110°C UP/DOWN)
A6-WRIST ROTATION (360°C)
A7-HAND (CLAW)-OPEN/CLOSE

Figure 14. Features of the Computer-Controlled Robot Application

represents the number of frames to be skipped between memory updates in terms of 20ms increment per frame. The computer will record one out of every Nf + 1 frames, or play the same channel data Nf + 1 times before incrementing to the next set of channel data in memory.

For example, at speed = 1, the memory usage is fast, every 2nd frame or 2 × 20ms = 40ms. The memory capacity is used up after 2,714 × 2 = 5,428 frames or in 5,428 × 20ms = 108s of real-time. At speed 255, the memory usage is slow, every 256th frame or 256 × 20ms = 5.12s. The memory capacity is used up after 2,714 × 256 = 694,784 frames or in 694,784 × 20ms = 3h:51min of real-time. For a 90° mechanical arm rotation, a 1s minimum time was observed. One frame update per second means a speed of 1s/20ms = 50. At this speed, the memory capacity will be used up in 2,714s = 45min real-time.

Real-Time PPM-to-Digital Software Conversion

Pulse-position modulation can be converted directly to binary form by counting the time between channel pulses. The software program divides the 1ms-2ms time interval between two channel pulses into about 190 bits, through a numerical algorithm. The peak counting error is ±2 bits. Clock pulses are counted and the total is adjusted to fit a 0-255 scale.

Floppy disk operations, to save or load data records, are done under a disk-operating software program already written for the particular home computer used. At this time the computer is instructed to perform disk/memory data transfers and not to control the robot. In the present program, configuration disk/memory data transfers and robot control cannot be done at the same time.

System Control Program

The overall program uses both BASIC and machine language. The use of BASIC is confined to the program portion, which takes user inputs for defining the various operating modes. The program sections that control data flow to the robot are written in machine language. This is necessary because, with the PPM-to-digital conversion, less than 50μs are available to present data to the bus after a channel pulse is received. If executed in BASIC, the instruction cycle of the channel play loop would take in excess of 1.5ms which is much too long. Machine language becomes even more essential if a full-duplex system is used, because such a system requires processing of sensor information simultaneously with the execution of a motion program.

The BASIC Program

The BASIC program section takes user inputs to set up the system configuration. Initial options include: playing the channel data program stored in memory, loading an old channel data program from disk into memory, saving the memory program on disk, or recording a new program in memory. If the "record" option is chosen, then the computer asks for the channel numbers to be recorded. Individual play/record channel control allows the user to record one or more channels and play the rest from memory. This feature permits re-recording of individual channels so that an entire seven-channel program doesn't have to be redone because of an error in one channel. Channel data for recording can be entered by joystick or from the keyboard.

Control System for Home Computer and Robotics Applications AN1341

The Assembly Program

Figure 15 shows a flow diagram of the machine language section of the program, and Figure 16 shows the data management sequence. In addition to the main memory locations for channel data storage ($4000 – $9000), two memory buffers are used for input and editing. The keyboard buffer ($300 – $306) holds data entered from the keyboard during a recording sequence, and the scratchpad buffer ($19 – $1F) is used for channel data storage during each frame.

The program sequence begins with a memory pointer set to $4000. When the computer senses a positive-going frame edge, the DE line is pulled Low to reset the QF flip-flop and, when an internal frame counter equals Nf + 1, seven bytes of data are moved from memory (pointer to pointer +6) to the scratchpad buffer. The program uses the time before the first channel pulse arrival to update the screen graphics and scan for keyboard input. The screen display shows a bar graph of the control surface relative position (from –1 to +1 for each channel), and of the storage memory usage. Valid keyboard inputs include channel number, increment or decrement, steps from 0.5% to 10% of the whole 1ms range, and "return". If a "return" is sensed, then the accumulator is loaded with the scratchpad byte for the last keyboard-specified channel number. The last specified increment/decrement amount is implemented and the new data is stored in the appropriate scratchpad location.

The program sets a channel counter equal to zero and waits for the first positive-going pulse edge. Upon sensing the positive-going pulse edge, the computer increments the channel counter and checks whether the first channel has been selected for "play" or "record". If channel one has been specified as "play", the data in the first scratchpad location is loaded onto the data bus and the $\overline{\text{DE}}$ line is pulled Low, latching the data as encoder input. The PPM-encoded data is sent to the robot. If "record" has been specified for channel one, then the counter checks if keyboard or joystick has been specified as an input option. For keyboard recording, the first byte in the keyboard buffer is copied to the first position in the scratchpad buffer. The byte is also put on the data bus and sent to the robot by pulling the $\overline{\text{DE}}$ line Low.

For joystick recording, the computer software must do a PPM-to-digital conversion (A/D). This is initiated by zeroing an internal counter and pulling the $\overline{\text{DE}}$ line Low to reset the QP flip-flop. A small loop alternates between incrementing the counter and scanning for the next positive-going pulse edge. When the positive-going edge is sensed, the loop is broken and the count will be proportioned to the time between pulses. The joystick record sequence is then completed by incrementing the channel counter. The same sequence is followed for each channel. When the channel counter specifies that the eighth pulse has arrived, the seven bytes from the scratchpad buffer memory are copied back into the storage memory (pointer to pointer +6), and the pointer is incremented by seven. The computer waits for the next Nf + 1 positive-going frame edge, after which the entire sequence is repeated. The programming/play sequence ends when either the keyboard scan senses a press on the space bar, or the storage memory capacity has been reached (approximately one and one-half minutes at full speed), or an end marker is read into the first position in the scratch pad buffer. Upon manual termination (space bar press), a zero is stored after the last valid channel as an end marker.

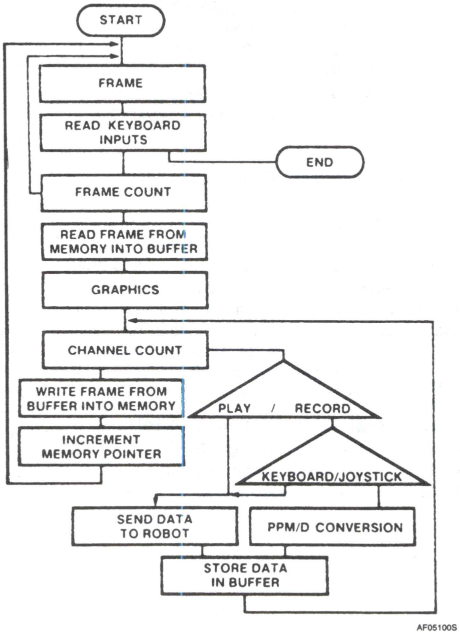


Figure 15. Flow Chart of the Robot Control Computer Program

	FRAME 1	FRAME 2	FRAME 3
STORAGE MEMORY ($HEX)	4000 – – –	4007 – – –	400E – – –

SCRATCHPAD BUFFER ($HEX)	19	1A	1B	1C	1D	1E	1F
CHANNEL NUMBER	1	2	3	4	5	6	7
KEYBOARD BUFFER ($HEX)	300	301	302	303	305	306	

DATA MANAGEMENT SEQUENCE

1. Move data from storage ($4000-4006) to scratchpad ($19-1F).
2. Operate on scratchpad data
    a. Record joystick: PPM-to-digital count = $18,X. X=channel no.
    c. Playback: $18,X-PPM serial to robot.
3. Move scratchpad data back to storage memory pointer: $4000-$4007
4. Increment storage memory pointer
5. Goto 1.

Figure 16. Software Data Management Sequency and Memory Allocation

Signetics

NE544
Servo Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed-loop position control applications. It incorporates a linear one-shot for improved positional accuracy and outputs for external PNP motor drive transistors.

FEATURES

- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

APPLICATIONS

- **Miniature position servo**
- **Robotics**
- **Control devices**
- **Remote positioning**

ORDERING INFORMATION

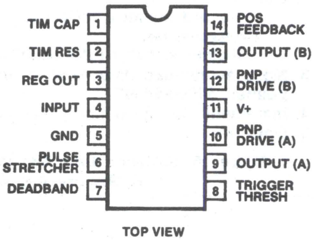
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE544N
16-Pin Plastic SOL Package	0 to +70°C	NE544D

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V+	Supply voltage	6.0	V
I_O	Output current D package N package	 400 500	mA
T_A	Operating temperature	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

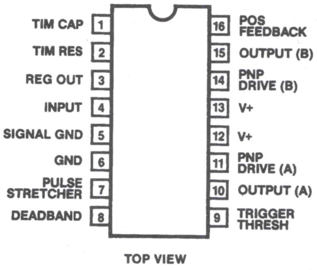
PIN CONFIGURATIONS

N Package


TIM CAP 1
TIM RES 2
REG OUT 3
INPUT 4
GND 5
PULSE STRETCHER 6
DEADBAND 7
14 POS FEEDBACK
13 OUTPUT (B)
12 PNP DRIVE (B)
11 V+
10 PNP DRIVE (A)
9 OUTPUT (A)
8 TRIGGER THRESH
TOP VIEW

CD10480S

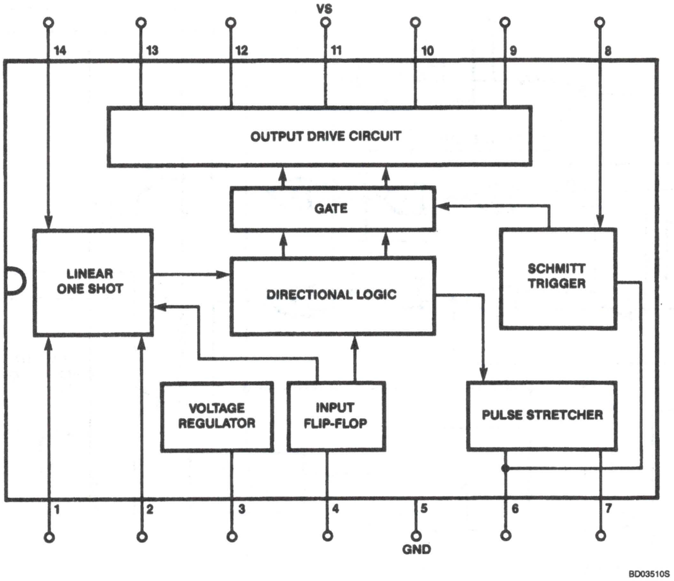
D Package[1]


TIM CAP 1
TIM RES 2
REG OUT 3
INPUT 4
SIGNAL GND 5
GND 6
PULSE STRETCHER 7
DEADBAND 8
16 POS FEEDBACK
15 OUTPUT (B)
14 PNP DRIVE (B)
13 V+
12 V+
11 PNP DRIVE (A)
10 OUTPUT (A)
9 TRIGGER THRESH
TOP VIEW

CD10490S

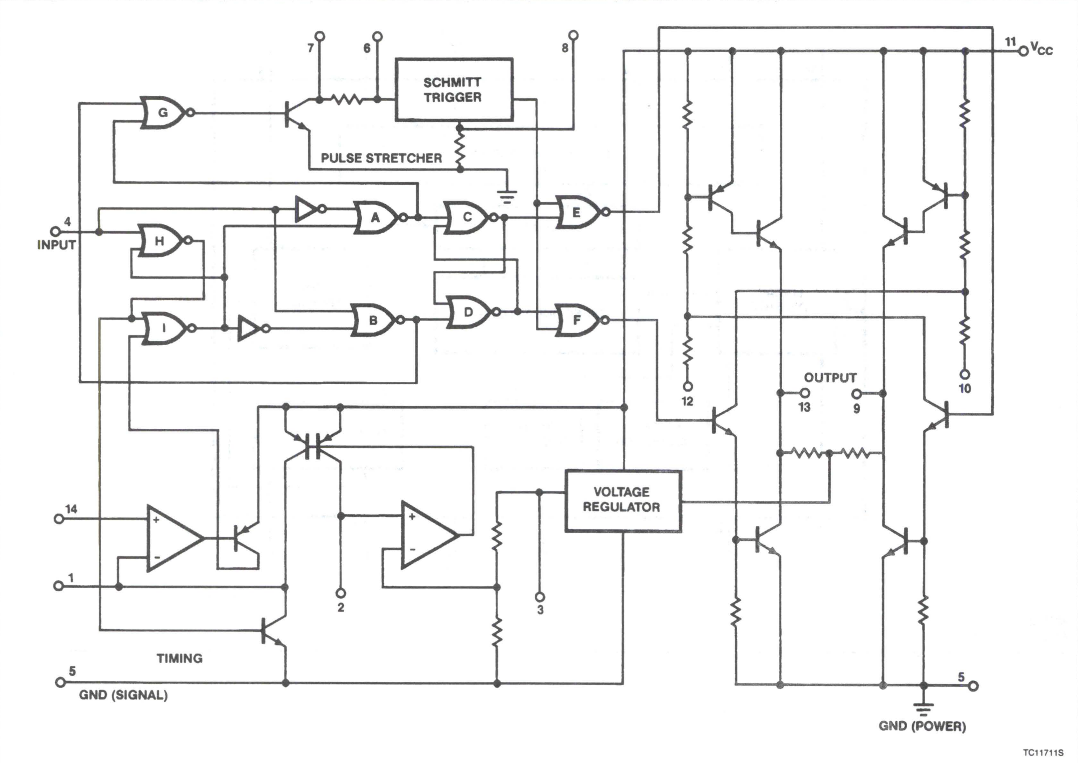
NOTE:
1. SOL and non-standard pinout.

BLOCK DIAGRAM


VS
14
13
12
11
10
9
8
OUTPUT DRIVE CIRCUIT
GATE
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
1
2
3
4
5
6
7
GND
BD03510S

NOTE:
Pinout for N package.

EQUIVALENT SCHEMATIC


7
6
8
SCHMITT TRIGGER
PULSE STRETCHER
G
A
C
E
H
B
D
F
I
4
INPUT
11
V_{CC}
12
OUTPUT
13
9
10
14
1
2
3
VOLTAGE REGULATOR
TIMING
5
GND (SIGNAL)
5
GND (POWER)
TC11711S

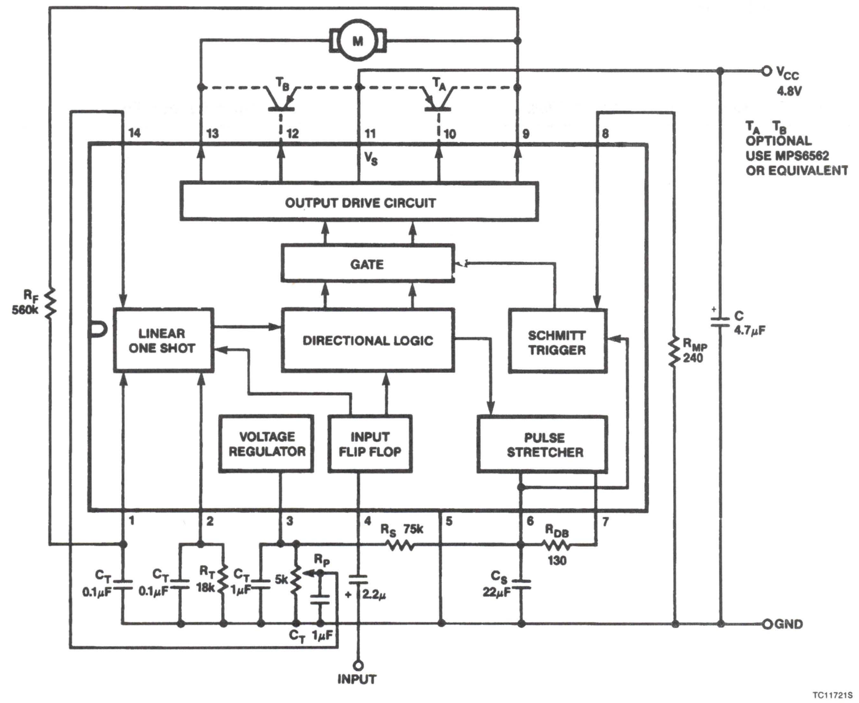
NOTE:
Pinout for N package.

Servo Amplifier NE544

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 4.8V$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC} I_{CC}	Supply voltage Supply current, Pin 11	 Quiescent	3.2 4.2	4.8 5.5	6 10	V mA
V_{TH}	Input threshold, Pin 4 On Off			 1.5 1.4		V
Z_{IN}	Input resistance, Pin 4			18		kΩ
 V_{OL} V_{OH}	Output voltage Low High	Pin 9 or 13. $I_L = 400mA$		 0.3 3.9		V
V_{REG}	Regulated voltage, Pin 3		2.1	2.5	2.9	V
ΔV_{REG}	Regulation, Pin 3 Minimum deadband, Pin 7 One-shot temperature coefficient	$3.9V \leqslant V_{CC} \leqslant 6V$ $R_{DB} = 0$		10 1 0.01		mV/V µs %/°C
	Standby output voltage PNP drive current	Pins 9 and 13 Pins 10 and 12		2.5 20		V mA

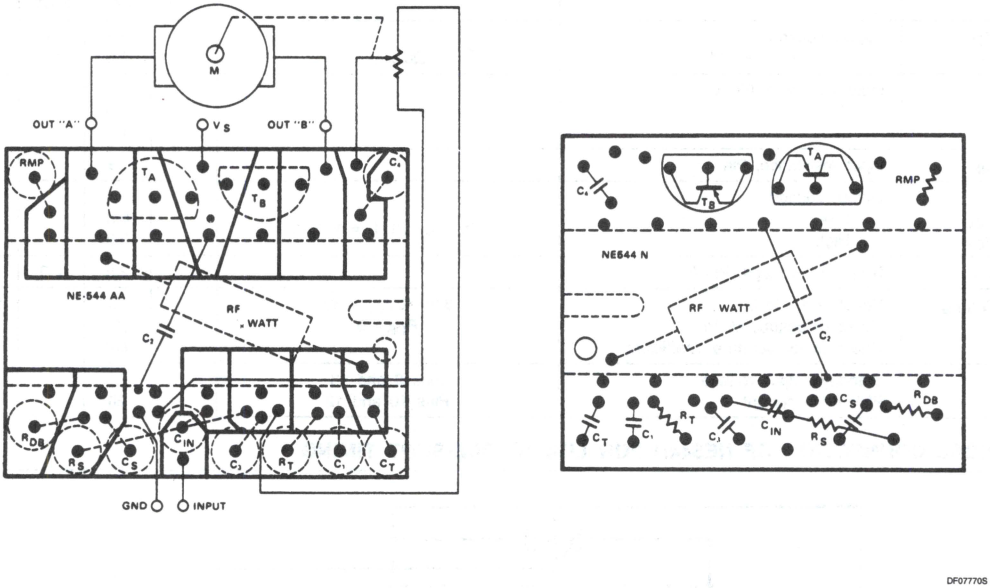
TYPICAL CONNECTION OF NE544N FOR LINEAR ONE-SHOT TIMING


M
TB
TA
14
13
12
11
10
9
8
VS
VCC 4.8V
TA TB OPTIONAL USE MPS6562 OR EQUIVALENT
OUTPUT DRIVE CIRCUIT
GATE
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
VOLTAGE REGULATOR
INPUT FLIP FLOP
PULSE STRETCHER
RF 560k
RMP 240
C 4.7µF
1
2
3
4
5
6
7
RS 75k
RDB 130
CT 0.1µF
CT 0.1µF
RT 18k
CT 1µF
5k
RP
2.2µ
CS 22µF
CT 1µF
INPUT
GND
TC11721S

NOTE:
Pinout for N package

PC BOARD — N PACKAGE

PC BOARD—N PACKAGE

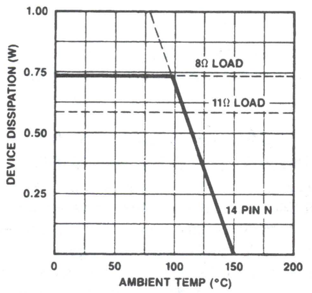

M
OUT "A"
V S
OUT "B"
RMP
T A
T B
C4
NE-544 AA
RF ½ WATT
C2
RDB
RS
CS
CIN
C3
RT
C1
CT
GND
INPUT
C4
T B
T A
RMP
NE544 N
RF WATT
C2
CT
C1
RT
C3
CIN
CS
RS
RDB
DF07770S

Typical PC Board Layout Bottom View

Parts Layout Top View

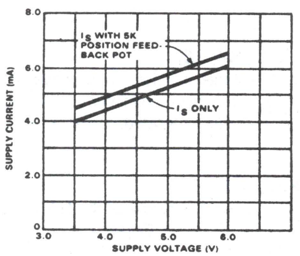
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Dissipation vs Ambient Temperature



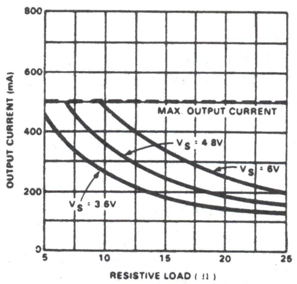
OP19480S

Supply Current vs Supply Voltage



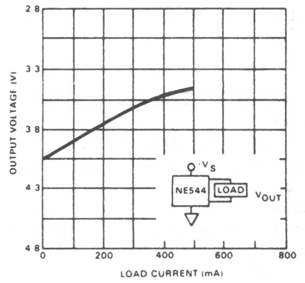
OP19490S

Output Current vs Load Resistance



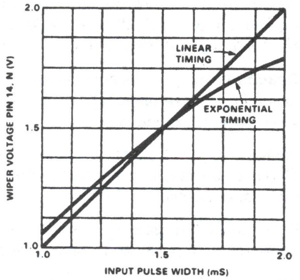
OP19500S

Output Voltage vs Load Current



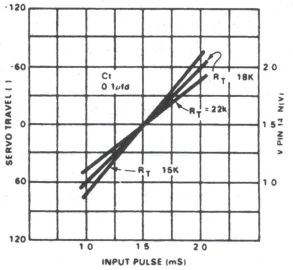
OP19510S

Input Pulse Width vs Feedback Pot Output



OP19520S

Input Pulse vs Servo Travel



OP19530S

Signetics

Linear Products

AN133

Applications Using the NE544 Servo Amplifier

Application Note

DESCRIPTION

The NE544 is a new servo amplifier design for digital proportional RC systems which incorporates the latest state-of-the-art in integrated circuit technology. The basic systems concept was developed in close cooperation with a number of leading manufacturers of radio control equipment.

The design philosophy behind the NE544 was to provide the RC servo systems designer with maximum flexibility in adapting the amplifier performance characteristic to his particular servo system and at the same time to keep the external components count low. To achieve this goal, all the basic servo amplifier functions, such as motor drive, deadband and minimum output pulse, are integrated into the IC, but can be modified over a wide range by using external transistors or padding resistors, respectively. This makes it possible to use the IC for extremely low cost applications as well as for the most sophisticated RC servo systems. Additional features of the circuit are very low standby power drain (typically less than 6mA), an internal voltage regulator for improved power supply rejection and a highly accurate monostable multivibrator. This circuit may be used in 2 different charging modes: linear and exponential. In the linear charging mode, the internally-generated charging current is programmable over a wide range with a resistor to ground. Usable currents range from below 10μA to above 1mA. In the exponential charging mode, the internal current source is simply bypassed with an external resistor from Pin 1 to the regulator output.

The bidirectional power output stage can supply load currents up to 500mA (NE544N package only). Output drive pins for external PNP transistors provide the user with the option of increasing the motor drive by bypassing the internal compound PNP transistors.

The NE544 also provides external pins to adjust deadband and to vary the hysteresis of the Schmitt trigger. This gives the user maximum flexibility in adapting the servo amplifier to a large variety of servo motor and gear train combinations. A dynamic brake integrated into the output stage serves to suppress inductive noise spikes and helps to improve the dynamic performance.

IC PACKAGE

The NE544 has sufficient power dissipation to handle motors with a minimum of 8Ω impedance with the integrated power transistors.

OPERATION

The basic building blocks of the NE544 servo driver are shown in Figure 1.

A positive input signal applied to the input pin (4) sets the input flip-flop and starts the one-shot time period. The directional logic compares the length of the input pulse to that of the internal one-shot and stores the result of this comparison in a directional flip-flop. The exact difference in pulse width between input and internal one-shot pulse, called the error pulse, is also fed to a pulse stretcher, deadband and trigger circuit. These circuits determine 3 important parameters:

1. **Deadband** — The minimum difference between input pulse and internally-generated pulse to turn on the output.
2. **Minimum output pulse** — The smallest output pulse that can be generated from the trigger circuit.
3. **Pulse stretcher gain** — The relationship between error pulse and output pulse.

Proper adjustment of these parameters can be achieved with external resistors and capacitors at Pins 6, 7 and 8. The trigger circuit activates the gate for a precise length of time to provide drive to the bridge output circuitry in proportion to the length of the error pulse.

TYPICAL APPLICATION AS A LINEAR SERVO AMPLIFIER

Figure 2 shows a typical connection of the NE544 as a high performance servo amplifier for remote control servo applications using the 14-pin dual in-line package. The input pulse may be DC-coupled if a reset is used in the receiver decoder. Output drive to the servo motor is applied through Pins 9 and 13 with PNP transistors T_A and T_B optional for high performance applications. The wiper of potentiometer RP is mechanically-coupled to the servo control surface, providing positional feedback. The internal one-shot in this application is operating in the linear charging mode.

LINEAR ONE-SHOT TIMING

In contrast to most conventional servo drivers which use exponential one-shots, the NE544 uses a linear one-shot. This makes it possible to design servo systems with very high positional accuracy and linear pulse width to position transfer functions. The timing of the linear one-shot can best be explained with the help of Figure 3.

The timing cycle starts after the input pulse sets the input flip-flop and releases the reset transistor T_R. This allows current I_C to charge up capacitor C_T in a linear fashion. Current I_R

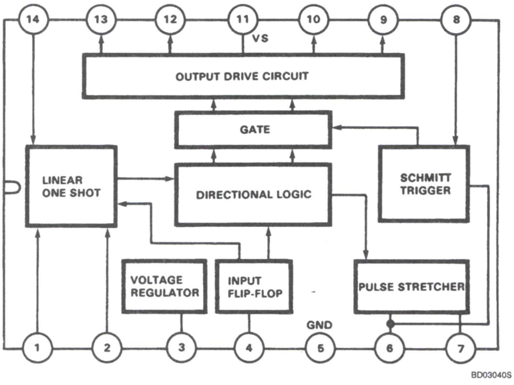


Figure 1. Block Diagram of NE544 Servo Amplifier

Applications Using the NE544 Servo Amplifier

AN133

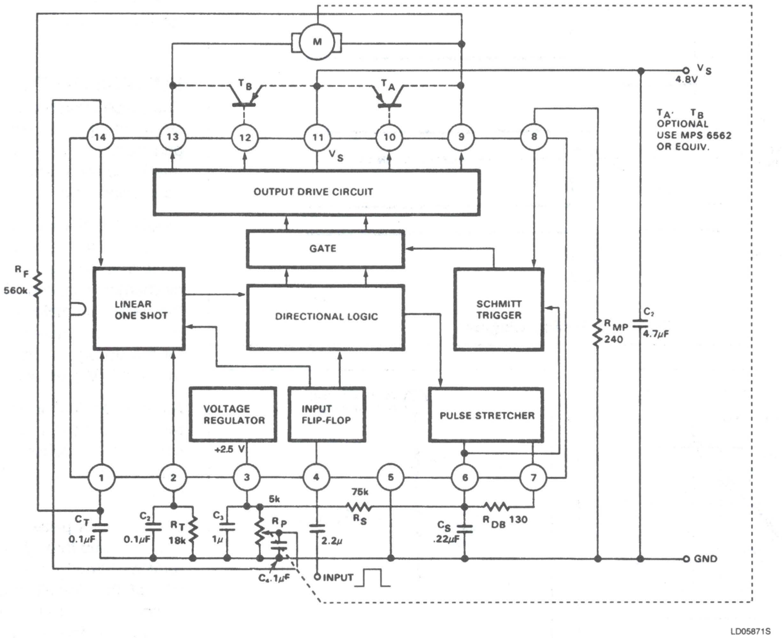

M
T_B
T_A
V_S
4.8V
$T_A \cdot T_B$ OPTIONAL USE MPS 6562 OR EQUIV.
14
13
12
11
10
9
8
V_S
OUTPUT DRIVE CIRCUIT
GATE
R_F
560k
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
R_{MP}
240
C_2
4.7µF
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
+2.5 V
1
2
3
4
5
6
7
5k
75k
R_S
C_T
0.1µF
C_2
0.1µF
R_T
18k
C_3
1µ
R_P
2.2µ
C_S
.22µF
R_{DB} 130
GND
C_4 .1µF
INPUT
LD05871S

Figure 2. Typical Connection of NE544 for Linear One-Shot Timing

is programmed by resistor R_T. The op amp serves as a linear voltage-to-current converter, with the current through R_T and C_T matched identically. The inverting input of the op amp is internally referenced to 1.8V so that the current I_R is given by this equation:

$$I_R = \frac{V_I}{R_T} = \frac{1.8V}{R_T} = I_C$$

The timing period of the internal one-shot is complete when the voltage ramp at Pin 1 reaches the threshold set at Pin 14. This time is given by this equation:

$$T = \frac{C_T V_{14}}{I_R}$$

If we substitute the typical values given in Figure 2 we obtain this equation: ($V_{14} = 1.5V$)

$$T = \frac{(0.1 \times 10^{-6})(1.5V)}{0.1 \times 10^{-3}A} = 1.5 \times 10^{-3}\text{sec}$$

When the internal one-shot has timed-out, the input flip-flop is reset. The reset transistor T_R is clamped to ground as soon as the input pulse goes to zero. Figure 4 shows the relationship of the input pulse, the internal one-shot pulse, the ramp at Pin 1 and the error pulse for a condition where the input pulse is longer than the internal pulse.

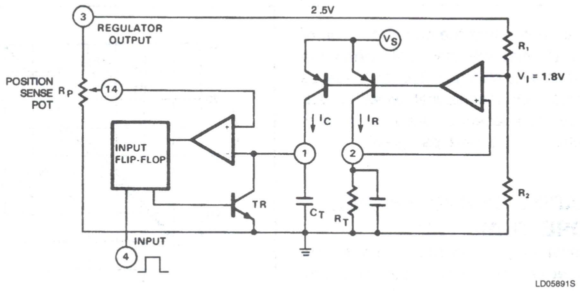

3
REGULATOR OUTPUT
2.5V
V_S
R_1
V_I = 1.8V
POSITION SENSE POT
R_P
14
I_C
I_R
INPUT FLIP-FLOP
1
2
TR
C_T
R_T
R_2
INPUT
4
LD05891S

Figure 3. Simplified Circuit Diagram of Linear One-Shot

In contrast to most conventional designs, the total value of the feedback pot R_P is no longer important, since it serves only as a voltage divider. A reasonable lower limit is 1.5kΩ to keep power consumption low and to prevent loading of the voltage regulator. In the typical application, a 5k pot is used.

ADJUSTMENT OF SERVO TRAVEL

The amount of angular rotation of the feedback pot R_P (or of the servo control surface) can be changed by simply changing the charging current. Figure 5 shows a plot of the servo travel as a function of input pulse width for 3 different values of current setting resistors R_T.

Applications Using the NE544 Servo Amplifier

AN133

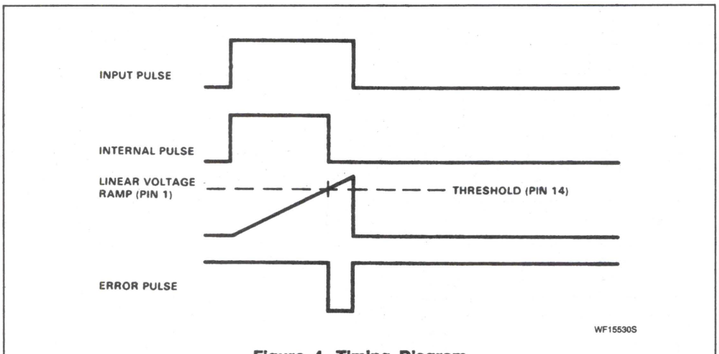


Figure 4. Timing Diagram

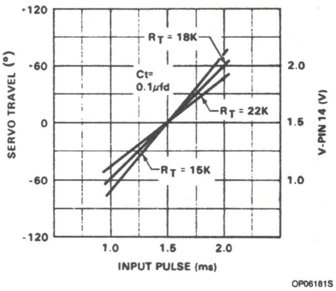


Figure 5. Servo Travel as a Function of Input Pulse for 3 Different Charging Currents

It should be noted that the center position of the wiper (1.5ms) will also shift when the amount of travel is changed. This shift may be compensated by mechanical wiper adjustment or by the addition of padding resistors as described in the next paragraph.

INCREASING SERVO TRAVEL TO MORE THAN 180°

Servo travel may be increased up to the maximum active area of the feedback pot by using padding resistors R_A and R_B as shown in Figure 6.

Figure 7 shows the values of resistors which are required to obtain a desired amount of servo travel.

EXPONENTIAL TIMING OPTION

If an exponential timing characteristic is desired, the circuit shown in Figure 8 may be used.

The time constant of the one-shot in this case is given by this equation:

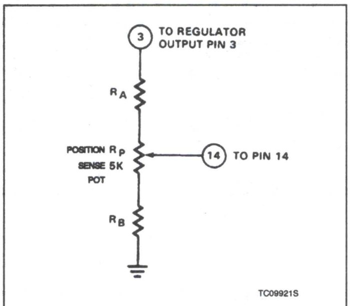


Figure 6. Increased Servo Travel Schematic

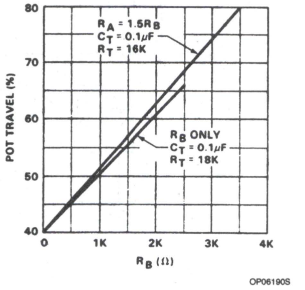


Figure 7. Pot Travel vs R_B

$$T_E = R_{TE}C_T \ln \frac{V_3}{V_3 - V_{14}}$$

Substituting the values shown in Figure 8, where $V_3 = 2.5V$ and $V_{14} = 1.5V$ at the center position, we obtain this equation:

$$T = (16k\Omega)(0.1\mu F)\ln \frac{2.5V}{2.5V - 1.5V} = 1.47ms$$

The center position and servo travel can be changed as described in the previous section for linear operation.

PULSE-STRETCHER

The pulse-stretcher and associated circuitry shown in Figure 9 determine important servo parameters such as minimum output pulse, deadband and error pulse-to-output pulse conversion gain.

Initially, transistor Q_S is off and capacitor C_S is charged to the regulator voltage. An error pulse from gate G turns on transistor Q_S and discharges capacitor C_S to ground through the parallel combination of R_{DB} and R_I. The deadband is determined by the time it takes for the voltage at Pin 6 to reach the trigger threshold (V_1) as shown in Figure 10.

As soon as the Schmitt trigger threshold is reached, transistor Q_S is turned off and the capacitor is discharged through a constant current source I_S until the error pulse disappears.

After the error pulse disappears, capacitor C_S is charged up through resistor R_S. The output remains turned on until the upper threshold (V_2) of the Schmitt trigger is reached. The minimum output pulse is determined by the hysteresis in the Schmitt trigger. This hysteresis may be varied over a wide range by connecting an external resistor R_{MP} from Pin 8 to ground or positive supply.

DEADBAND

Referring to Figure 10, the deadband can be calculated using the equations where T_{DB} is deadband in microseconds, C_S is the pulse stretching capacitor, I_T is the total discharge current, and ΔV is approximately 0.65V. The deadband is determined by the time it takes to discharge capacitor C_S from its initial voltage to the Schmitt trigger threshold.

$$T_{DB} \approx \frac{C_S \Delta V}{I_T}, \text{ and } I_T \approx I_S + \frac{2.2V(R_I\ R_{DB})}{R_I + R_{DB}}$$

The value of the internal deadband resistor R_I is approximately 150Ω. I_T can be calculated with this equation:

$$I_T = 3mA + \frac{2.2V(150R_{DB})}{150 + R_{DB}}$$

For the typical values shown in Figure 2, we obtain this equation:

$$I_T = 3 + 27 = 30mA$$

The deadband can then be calculated using the first equation to obtain this equation:

$$T_{DB} = \frac{(0.22 \times \mu F)\ 0.65V}{30mA} = 4.8\mu s$$

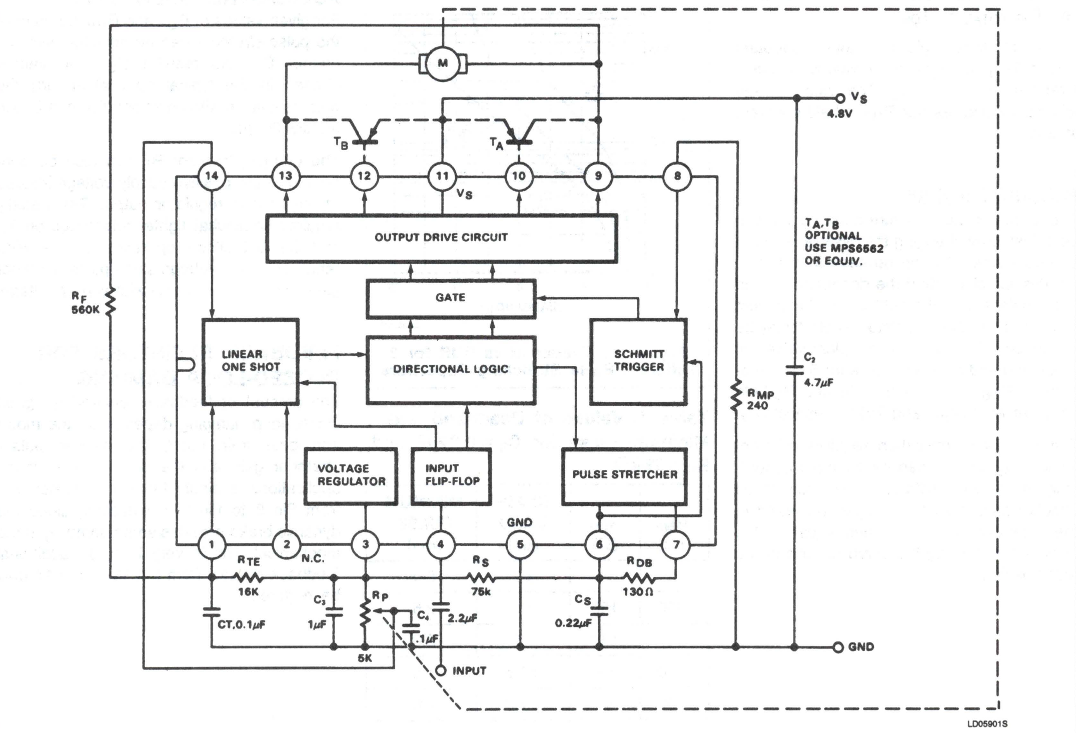

M
TB
TA
VS
4.8V
14
13
12
11
10
9
8
VS
OUTPUT DRIVE CIRCUIT
TA,TB OPTIONAL USE MPS6562 OR EQUIV.
GATE
RF 560K
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
C2 4.7μF
RMP 240
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
GND
1
2
3
4
5
6
7
RTE 16K
N.C.
RS 75k
RDB 130Ω
C3 1μF
RP 5K
C4 2.2μF
CS 0.22μF
CT.0.1μF
.1μF
INPUT
GND
LD05901S

Figure 8. Typical Connection for Exponential Timing Characteristic

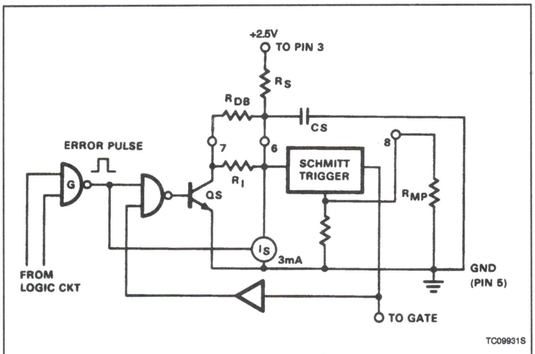

+2.5V TO PIN 3
RS
RDB
CS
ERROR PULSE
7
6
8
G
QS
R1
SCHMITT TRIGGER
RMP
IS 3mA
FROM LOGIC CKT
GND (PIN 5)
TO GATE
TC09931S

Figure 9. Typical Connection of Pulse-Stretcher Circuit

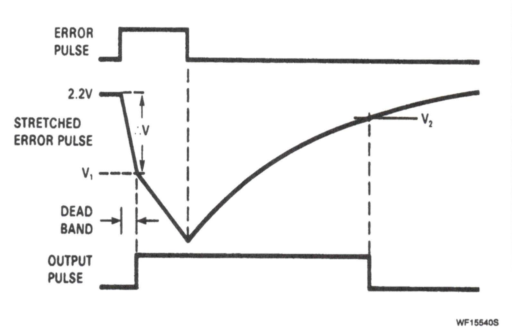


Figure 10. Pulse-Stretcher Waveforms

The total deadband is then twice this value, i.e., $T_{DB\ TOTAL} = \pm T_{DB}$.

Figure 11 shows plots of total deadband versus R_{DB} for 3 different values of pulse stretching capacitor C_S. The value of the minimum pulse resistor R_{MP} is held constant at 240.

MINIMUM PULSE

The length of the minimum output pulse can be adjusted by changing the hysteresis of the Schmitt trigger. As can be seen from Figure 10, this will also affect the deadband. To aid in the selection of the right value of minimum pulse and deadband resistor, Table 1 may be consulted. This table gives typical values of deadband and minimum pulse for 5 combinations of R_{DB} and R_{MP} with C_S and R_S held constant at 0.22μF and 75kΩ, respectively.

If a particular application requires different values, C_S and R_S can be changed accordingly. A capacitor with low series resistance should be used for C_S. If C_S is too resistive, the minimum pulse becomes equal to the error pulse, causing the servo to buzz at the rest position.

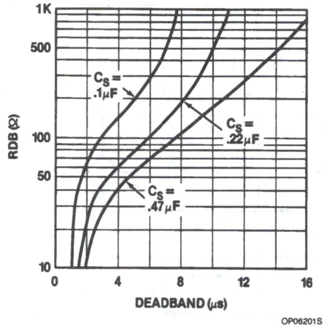


Figure 11. Deadband vs RDB for 3 Different Pulse Stretching Capacitors

Table 1. Values of Deadband and Minimum Pulse for $C_S = 0.22\mu F$ and $R_S = 75k\Omega$

R_{MP} (Ω)	R_{DB} (Ω)	DEADBAND (μs)	MINIMUM PULSE (ms)
		±7	5.0
360	130	±5	2.5
240	130	±5	2.0
160	82	±3.5	1.6
100	51	±2.3	2.0

PULSE-STRETCHER GAIN

For given values of R_{DB} and R_{MP}, the gain of the pulse-stretcher can be adjusted with capacitor C_S and resistor R_S. The values chosen in the typical application turn the outputs fully on with an error pulse of approximately 200μs.

The charging resistor R_S can also be connected to the positive supply voltage instead of the voltage regulator output. This usually requires somewhat tighter tolerances on R_S and C_S, but allows operation over a wide range of supply voltage since pulse-stretcher gain now varies inversely with supply voltage.

FEEDBACK RESISTORS FOR CLOSED-LOOP DAMPING

The amount of feedback required for good closed-loop damping depends on the motor and gear train used, the desired pulse-stretcher gain and the deadband. In many applications, a single feedback resistor, R_F, from Pin 9 to Pin 1 is sufficient, since the dynamic brake provides some damping. If the mechanical gain is very high, an additional feedback resistor from Pin 13 to Pin 14 may be required.

Signetics

NE/SA/SE5570
Brushless DC Motor Controller

Objective Specification

Linear Products

DESCRIPTION

The NE/SA/SE5570 is a three-phase brushless motor controller with a microprocessor-compatible serial input data port; 8-bit monotonic digital-to-analog converter; PWM modulator; oscillator; three Hall sensor inputs and six source/sink phase pre-drivers.

FEATURES

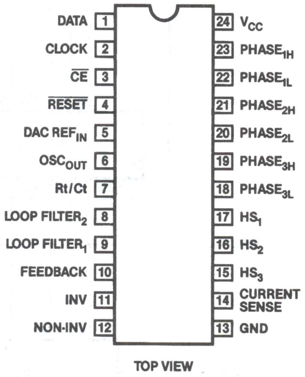
- **8-bit DAC**
- **Serial-to-parallel converter**
- **Output pre-drivers**
- **Entire switch mode conversion**
- **Adaptable to 60° or 120° commutation**
- **Overcurrent protection**

APPLICATIONS

- **Motor controller for three-phase brushless DC motor**
- **Robotics**
- **Computer peripherals**

PIN CONFIGURATION

D[1], F, N Packages


DATA 1
CLOCK 2
$\overline{CE}$ 3
$\overline{RESET}$ 4
DAC REF_{IN} 5
OSC_{OUT} 6
Rt/Ct 7
LOOP $FILTER_2$ 8
LOOP $FILTER_1$ 9
FEEDBACK 10
INV 11
NON-INV 12
24 V_{CC}
23 $PHASE_{1H}$
22 $PHASE_{1L}$
21 $PHASE_{2H}$
20 $PHASE_{2L}$
19 $PHASE_{3H}$
18 $PHASE_{3L}$
17 HS_1
16 HS_2
15 HS_3
14 CURRENT SENSE
13 GND
TOP VIEW

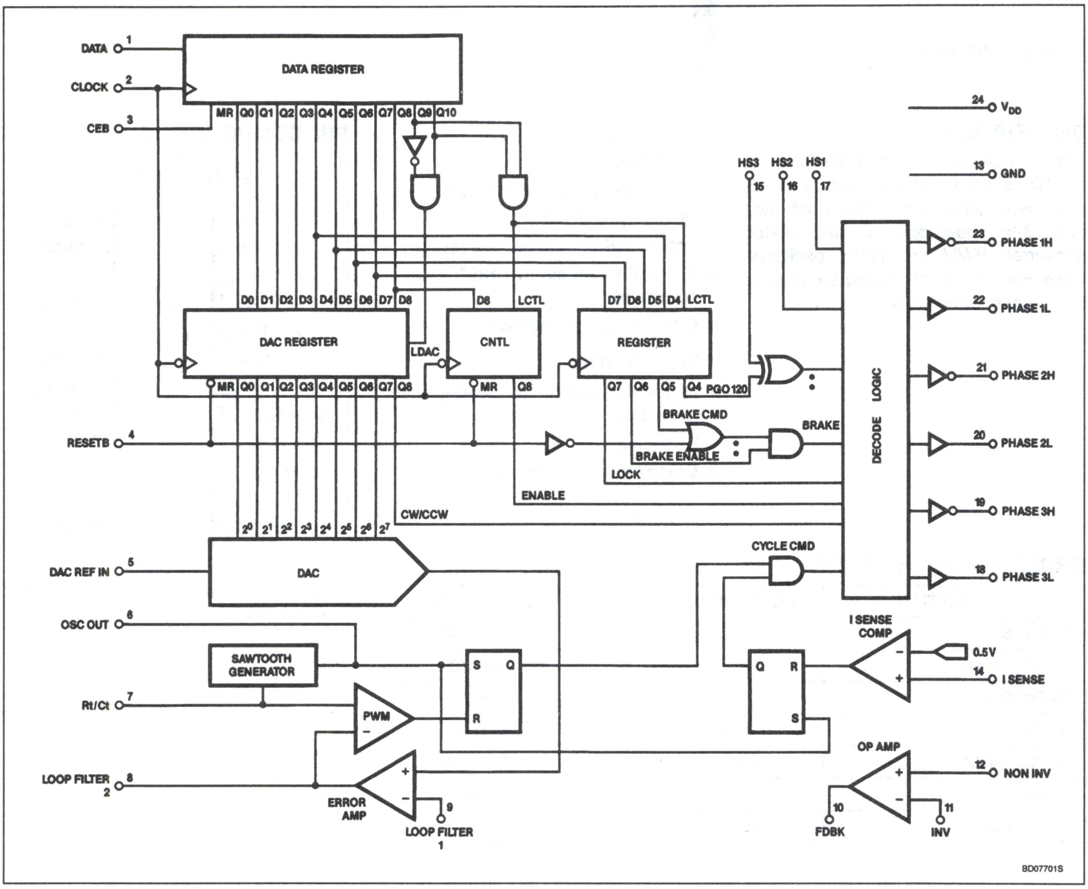
CD11380S

NOTE:
1. Available in SOL.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin SOL	0 to +70°C	NE5570D
24-Pin Cerdip	0 to +70°C	NE5570F
24-Pin Plastic	0 to +70°C	NE5570N
24-Pin Cerdip	-40°C to +85°C	SA5570F
24-Pin Plastic	-40°C to +85°C	SA5570N
24-Pin Cerdip	-55°C to +125°C	SE5570F
24-Pin Plastic	-55°C to +125°C	SE5570N

BLOCK DIAGRAM



DATA 1
CLOCK 2
CEB 3
DATA REGISTER
MR Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10
D0 D1 D2 D3 D4 D5 D6 D7 D8
DAC REGISTER
MR Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
LDAC
D8 LCTL
CNTL
MR Q8
D7 D6 D5 D4 LCTL
REGISTER
Q7 Q6 Q5 Q4 PGO 120
HS3 HS2 HS1
15 16 17
24 VDD
13 GND
DECODE LOGIC
23 PHASE 1H
22 PHASE 1L
21 PHASE 2H
20 PHASE 2L
19 PHASE 3H
18 PHASE 3L
BRAKE CMD
BRAKE
BRAKE ENABLE
LOCK
ENABLE
RESETB 4
CW/CCW
2^0 2^1 2^2 2^3 2^4 2^5 2^6 2^7
DAC REF IN 5
DAC
CYCLE CMD
OSC OUT 6
SAWTOOTH GENERATOR
Rt/Ct 7
PWM
S Q
R
Q R
S
I SENSE COMP
0.5V
14 I SENSE
OP AMP
12 NON INV
LOOP FILTER 2 8
ERROR AMP
9 LOOP FILTER 1
10 FDBK
11 INV
BD07701S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5570	SA5570	SE5570	
	Temperature range				
T_A	Operating ambient	0 to 70	-40 to 85	-55 to 125	°C
T_J	Operating junction	-55 to 150	-55 to 150	-55 to 150	°C
T_{STG}	Storage	-65 to 150	-65 to 150	-65 to 150	°C
V_{CC}	Power supply	15	15	15	V
	Logic inputs, all				
	min	-0.3	-0.3	-0.3	
	max	15	15	15	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient temperature range		
	NE Grade	0 to 70	°C
	SA Grade	−40 to 85	°C
	SE Grade	−55 to 125	°C
T_J	Junction temperature range		
	NE Grade	0 to 90	°C
	SA Grade	−40 to 105	°C
	SE Grade	−55 to 145	°C
V_{CC}	Supply voltage		V

DC AND AC ELECTRICAL CHARACTERISTICS

Limits apply at $V_{CC} = 12V$, $V_{REF} = 5V$ and over operating temperature range unless otherwise specified. Typical data appl

SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Oscillator									
f_O	Frequency initial accuracy	$T_A = 25°C$, $R_T = 2.49k\Omega$, $C_T = 22nF$	19	20	21	19	20	21	kHz
f_C	Frequency drift over temp	$R_T = 2.49k\Omega$, $C_T = 22nF$	18		22	18		22	kHz
	Supply voltage sensitivity	$T_A = 25°C$		±2			±2		%/V
	Output pulse width	$T_A = 25°C$, $R_T = 2.49k\Omega$, $C_T = 22nF$			500			500	ns
Motor Phase Pre-Drivers									
t_R	Rise time	$R_L = 2k\Omega$ to Gnd, $C_L = 2nF$ [1V to 11V]			500			500	ns
t_F	Fall time	$R_L = 2k\Omega$ to V_{CC}, $C_L = 2nF$ [1V to 11V]			500			500	ns
PWM Comparator									
V_{OS}	Offset voltage	$T_A = 25°C$			20			20	mV
I_{BIAS}	Input bias current				1			1	µA
Current Sense Comparator									
I_{BIAS}	Input bias current				1			1	µA
V_{TH}	Current sense trip level			500			500		mV
t_{PD}	Propagation delay to output drivers	$C_L = 2nF$		250			250		ns
Error Amplifier									
I_{BIAS}	Input bias current				1			1	µA
V_{CM}	Input common-mode voltage range		0		5	0		5	V
V_{OL}	Large-signal voltage gain	$V_{OUT} = 1V$ to $11V$	70	90		70	90		dB
PSRR	Power supply rejection ratio		60			60			dB
V_O	Output voltage swing	$V_{IN} = +50mV$, $I_L = -150\mu A$ $V_{IN} = -50mV$, $I_L = +150\mu A$	11.5	11.7 0.2	0.5	11.5	11.7 0.2	0.5	V V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

Limits apply at V_{CC} = 12V, V_{REF} = 5V and over operating temperature range unless otherwise specified. Typical data appl

SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Operational Amplifier									
V_{OS}	Offset voltage		−20	3	+20	−20	3	+20	mV
I_{BIAS}	Input bias current				1			1	μA
V_{CM}	Input common-mode voltage range	T_A = 25°C Over temp.	−0.3 0		5 5	−0.3 0		5 5	V
V_{OL}	Large signal voltage gain	V_{OUT} = 1V to 11V	70	90		70	90		dB
PSRR	Power supply rejection ratio		60	90		60	90		dB
V_O	Output voltage swing	V_{IN} = +50mV, I_L = −150A V_{IN} = −50mV, I_L = +150μA	11.5	11.7 0.2	0.5	11.5	11.7 0.2	0.5	V V
CMRR	Common-mode rejection ratio	R_S = 10kΩ	60	80		60	80		dB
GBW	Gain bandwidth	R_F = 100kΩ		250			250		kHz
V_{NN}	Input noise voltage	F = 1kHz							nV/√Hz
Digital-to-Analog Converter									
	Resolution				8			8	bits
INL	Integral non-linearity error			±1	±2		±1	±2	LSB
DNL	Differential non-linearity error[1]			±0.5	±1		±0.5	±1	LSB
V_{FS}	Full-scale gain error	PWM amp. A_V = 1		±0.2	±0.8		±0.2	±0.8	%FS
	Full-scale temperature drift	V_{REF} T_C = 0ppm/°C		20			20		ppm/°C
V_{ZS}	Zero-scale offset error	PWM amp. A_V = 1		±1	±2		±1	±2	LSB
Z_{IN}	Input impedance (DAC ref. in)			40			40		kΩ
t_S	Settling time to ±0.5 LSB			5			5		μs
t_{PLH}	Propagation delay time (high)			200			200		ns
t_{PHL}	Propagation delay time (low)			200			200		ns
Logic Inputs									
V_{IH}	Input voltage: TTL high		2.0		12	2.0		12	V
V_{IL}	Input voltage: TTL low		0		0.8	0		0.8	V
I_{IH}	Input current: TTL high				±1			±1	μA
I_{IL}	Input current: TTL low				±1			±1	μA

NOTE:

1. Monotonicity guaranteed over operating temperature range.

Signetics

SAA1027
Stepper Motor Driver

Product Specification

Linear Products

DESCRIPTION

The SAA1027 is a bipolar integrated circuit intended for driving a four-phase two-stator motor. The circuit consists of a bidirectional four-state counter and a code converter to drive the four outputs in the sequence required for driving a stepping motor.

FEATURES

- High noise immunity inputs
- Clockwise and counter-clockwise operation
- Reset facility
- High output current
- Outputs protected against damage by overshoot

APPLICATIONS

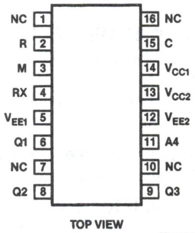
- Automotive industry
- Industrial
- Office equipment
- EDP

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38A)	−20°C to +70°C	SAA1027N

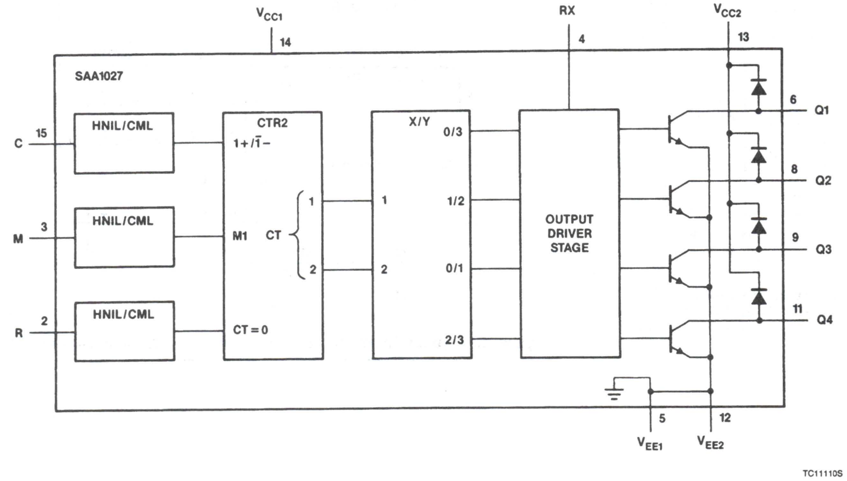
PIN CONFIGURATION

N Package


NC 1
R 2
M 3
RX 4
V_{EE1} 5
Q1 6
NC 7
Q2 8
16 NC
15 C
14 V_{CC1}
13 V_{CC2}
12 V_{EE2}
11 A4
10 NC
9 Q3
TOP VIEW
CD10110S

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Not connected
2	R	Reset input
3	M	Mode input
4	RX	External resistor
5	V_{EE1}	Ground
6	Q1	Output 1
7	NC	Not connected
8	Q2	Output 2
9	Q3	Output 3
10	NC	Not connected
11	Q4	Output 4
12	V_{EE2}	Ground
13	V_{CC2}	Positive supply
14	V_{CC1}	Positive supply
15	C	Count input
16	NC	Not connected

BLOCK DIAGRAM


V_{CC1}
14
RX
4
V_{CC2}
13
SAA1027
C
15
HNIL/CML
M
3
HNIL/CML
R
2
HNIL/CML
CTR2
1+/1̄−
M1 CT
1
2
CT=0
X/Y
0/3
1
1/2
2
0/1
2/3
OUTPUT DRIVER STAGE
6
Q1
8
Q2
9
Q3
11
Q4
5
12
V_{EE1}
V_{EE2}
TC11110S

NOTE:
The blocks marked HNIL/CML are high noise immunity input stages, the block marked CTR2 is a bidirectional synchronous 2-bit (4-state) counter and the block marked X/Y is a code converter. C is the count input, M the mode input to select forward or reverse counting and R is the reset input which resets the counter to content zero.

FUNCTIONAL DESCRIPTION

Count input C (Pin 15)

The outputs change state after each LOW-to-HIGH signal transition at the count input.

Mode input M (Pin 3)

With the mode input the sequence of output signals, and hence the direction of rotation of the stepping motor, can be chosen as shown in Table 1.

Reset Input R (Pin 2)

A LOW level at the R input resets the counter to content zero. The outputs take on the levels shown in the upper and lower line of the table above.

If this facility is not used the R input should be connected to the supply.

External Resistor Pin RX (Pin 4)

The external resistor R4 connected to RX sets the base current of the output transistors. Its value has to be chosen in accordance with the required output current (see Figure 3).

Outputs Q1 to Q4 (Pins 6, 8, 9 and 11)

The circuit has open-collector outputs. To prevent damage by an overshooting output voltage, the outputs are protected by diodes connected to V_{CC2}, Pin 13. High output currents mainly determine the total power dissipation, see Figure 1.

Table 1

COUNTING SEQUENCE	M = L				M = H			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
0	L	H	L	H	L	H	L	H
1	H	L	L	H	L	H	H	L
2	H	L	H	L	H	L	H	L
3	L	H	H	L	H	L	L	H
0	L	H	L	H	L	H	L	H

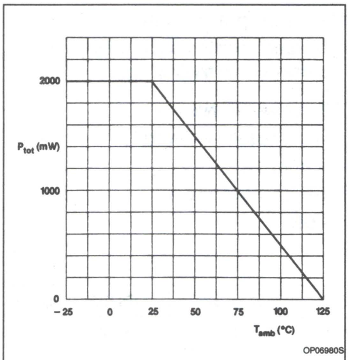


Figure 2. Power Derating Curve

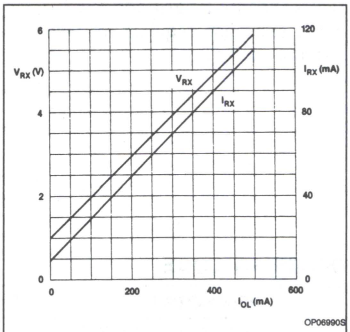


Figure 3. Current I_{RX} Into RX and Voltage V_{RX} on RX as a Function of Required Output Current I_{OL}

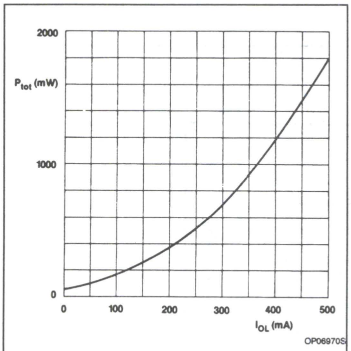


Figure 1. Total Power Dissipation P_{TOT} as a Function of Output Current I_{OL}

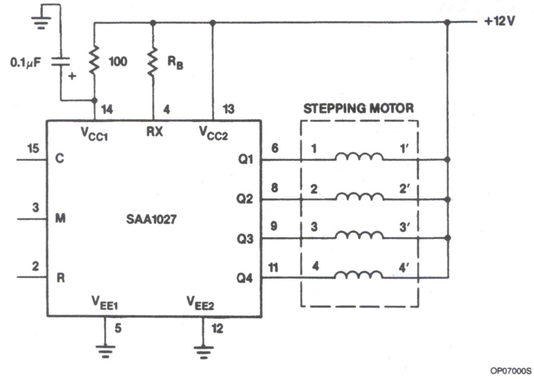


Figure 4. Typical Application of the SAA1027 as a Stepping Motor Driver

Stepper Motor Driver SAA1027

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1}; V_{CC2}	Supply voltage, DC	18	V
V_I	Input voltage, all inputs	18	V
I_{RX}	Current into Pin 4	120	mA
I_{OL}	Output current	500	mA
P_{TOT}	Power dissipation	See Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 9.5$ to 18V; $V_{EE} = 0V$; $T_A = -20$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	9.5		18	V
I_{CC}	Supply current at $V_{CC1} = 12V$; unloaded; all inputs HIGH; Pin 4 open	2	4.5	6.5	mA
Inputs C, M and R (Pins 15, 3 and 2)					
	Input voltage				
V_{IH}	HIGH	7.5			V
V_{IL}	LOW			4.5	V
	Input current				
I_{IH}	HIGH		1		µA
I_{IL}	LOW		30		µA
External Resistor Pin RX (Pin 4)					
V_{RX}	Voltage at RX at $V_{CC} = 12V \pm 15\%$; $R4 = 130\Omega \pm 5\%$	3		4.5	V
Outputs Q1 to Q4					
	Output voltage LOW				
V_{OL}	$I_{OL} = 350mA$		500	1000	mV
V_{OL}	$I_{OL} = 500mA$		700		mV
	Output current				
I_{OL}	LOW			500[1]	mA
I_{OH}	HIGH at $V_Q = 18V$			50	µA

NOTE:

1. See Figures 1 and 2.

Signetics

Linear Products

AN127
Using the SAA1027 With Airpax Four-Phase Stepper Motors

Application Note

INTRODUCTION

Airpax has introduced a range of five new 4-phase stepper motors which can be directly driven by an SAA1027 integrated circuit without the need for discrete power stages or compensating networks. Both the IC and the motors can operate from a single 12V supply. The high noise immunity design of the IC makes the system particularly suitable for use in electrically noisy environments. Use of the new motors and IC will drastically reduce the cost and complexity of stepper motor systems and thereby open up many new areas of application for digital motor control systems.

THE STEPPER MOTORS

The five new stepper motors are similar to our present industrial range with modified stator windings to match them to the output capability of the SAA1027 (350mA each phase). The maximum torque and pull-in rates obtained from the motors when they are driven by the SAA1027 are given in Table 1 for easy reference: the torque/speed characteristic curves and outline drawings of the motors are given in the *Technical Data* section of this publication.

Table 1. Quick Reference Data for the Motors

CATALOG NO.	STEP ANGLE	MAX. TORQUE (mNm)	MAX. PULL-IN RATE (STEPS/S)
9904 112 04002	7° 30'	12	240
9904 112 05001		65	140
9904 112 06001		45	120
9904 112 07005		5	350
9904 112 08001	15°	43	120

Table 2. Brief Data for the SAA1027

Supply voltage	V_P	9.5V to 18V
Load current (Each output)	I_Q	350mA max.
HIGH logic input level	V_{RH}, V_{SH}, V_{TH}	7.5V to V_P
LOW logic input level	V_{RL}, V_{SL}, V_{TL}	0V to 4.5V max.

THE INTEGRATED CIRCUIT

The SAA1027 integrated stepper motor drive circuit is contained in a 16-pin DIL plastic package and is shown in block diagram form in Fig. 1. The circuit comprises three input stages, a logic section, and an output stage for each of the four stator windings of the motor. The three input stages are compatible with high noise immunity logic to ensure correct operation in electrically noisy environments:

- The trigger stage accepts the incoming pulse train which initiates the logic section switching sequence, and thereby controls the speed of rotation and ultimate angular position of the motor drive shaft.
- The set stage accepts a logic level input which overrides the switching sequence of the logic section and sets the output stages to a pre-determined logic state. This facility simplifies the programming of a system by allowing the motor drive shaft to be pre-positioned.
- The cw/ccw* stage accepts a logic level input which reverses the switching sequence of the logic section, thereby reversing the direction of rotation of the motor drive shaft.

The logic section contains a 4-bit bidirectional synchronous counter which switches the four output stages in the correct sequence to cause the motor drive shaft to rotate at the speed, and in the direction, dictated by the input stages.

The four output stages switch the supply current to the four phases of the motor stator. Each output stage is capable of switching a current of 350mA and incorporates an integrated diode for protection against transient spikes caused by switching the stator windings.

Brief data for the SAA1027 is given in Table 2. Further information is given in the *Technical Data* section of this publication.

THE SYSTEM

A practical stepper motor drive system and pulse diagram are given in Fig. 2.

Electrical Requirements

The system is powered from a single 12V supply with a current output compatible with the motor being driven. The current applied to pin 4 of the IC must be adjusted by selection of resistor R_B for each type of motor in accordance with Table 3.

Table 3. Selection Of Resistor R_B

MOTOR	R_B VALUE	I_{SYSTEM} (mA)
9904 112 04002	470 Ω, 0.33W	300
9904 112 05001	220 Ω, 0.67W	620
9904 112 06001	220 Ω, 0.67W	620
9904 112 07005	620 Ω, 0.33W	200
9904 112 08001	220 Ω, 0.67W	620

The relationship between the current at pin 4 of the IC and the output current is given in the *Technical Data* section of this publication.

Trigger Input *T*

The repetition rate and the number of pulses applied to pin 15 of the IC determine the stepping rate and ultimate angular position of the motor drive shaft. The steps are initiated by the positive-going edges of the pulses in the sequence shown in Table 4. The '0' state shown in the table is the logic state of

---

* Clockwise/counter-clockwise

BLOCK DIAGRAM

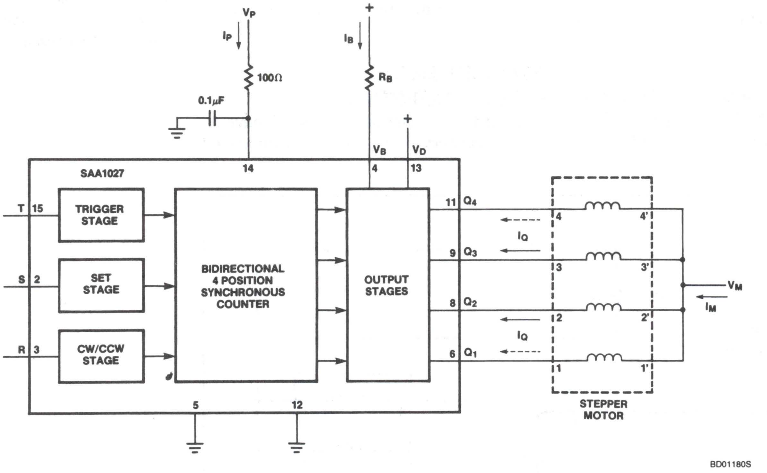


Figure 1. Block Diagram of the SAA1027

the outputs when the 'set' input is operative.

Set Input *S*

The output switching sequence can be set to a predetermined logic state (Q_1 = L, Q_2 = H, Q_3 = L, Q_4 = H), by applying a LOW voltage level to pin 2 of the IC. This input is only effective if the voltage level at the trigger input is HIGH. To achieve maximum noise immunity, this input should be connected permanently to the HIGH voltage level if it is not required.

Direction Of Rotation Input *R*

The output switching sequence of the IC, and therefore the direction of rotation of the motor drive shaft, is determined by the level of the voltage applied to pin 3 of the IC. If the voltage level is HIGH, the drive shaft will rotate counter-clockwise: if the level is LOW, the drive shaft will rotate clockwise. The level of the voltage applied to pin 3 can be changed at any time regardless of the logic state of the other two inputs. To achieve maximum noise immunity, this input must not be left floating if not used, but should be connected to the voltage level appropriate to the required direction of rotation (to pin 14 for counter-clockwise; to pin 5 for clockwise).

Table 4. Output Switching Sequence

S = H									
R = L					R = H				
T	Q_1	Q_2	Q_3	Q_4	T	Q_1	Q_2	Q_3	Q_4
0	L	H	L	H	0	L	H	L	H
1	H	L	L	H	1	L	H	H	L
2	H	L	H	L	2	H	L	H	L
3	L	H	H	L	3	H	L	L	H
0	L	H	L	H	0	L	H	L	H

Precautions to Minimize the Effects of Switching Transients

If the IC and the motor are connected to the same supply source, a simple *RC*-network must be connected in the supply line to the logic part of the IC to prevent the switching sequence from being disturbed by transient spikes caused by switching of the motor windings. This network, which consists of a resistor of 100Ω and a capacitor of 0.1μF, is shown in Fig. 2 and Fig. 3. The capacitor must be located as close as possible to pins 14 and 5(12) of the IC. The connection between the common line of the four integrated clamping diodes (pin 13) and the common line of the four motor windings must be as short as possible.

Minimizing the Dissipation of the IC

The four integrated clamping diodes dissipate the energy which is stored in the motor windings when outputs *Q* are switched off. This dissipation (P_D) is different for each of the motors and adds to the normal dissipation of the IC. If it is necessary to reduce P_D to prevent overheating of the IC, the integrated clamping diodes must be disconnected, by removing the connection from pin 13, and four discrete clamping diodes must be connected to the motor windings as shown in Fig. 3.

TECHNICAL DATA

Electrical Requirements of the Drive System

The various parameters are shown in Fig. 1.

Supply Characteristics

Control circuit supply voltage	V_P	9.5 – 18V (12V typ.)
Control circuit supply current at V_P = 12V	I_P	4.5mA typ.
Output circuit current	I_B	see Fig. 4
Output circuit bias voltage at pin 4	V_B	see Fig. 5
Motor supply voltage	V_m	1.5 – 18V (12V typ.)
Total motor current	I_m	700mA max.
Motor current in one stator	I_Q	350mA max.
Saturation voltage of output transistors at I_Q = 350mA (pins 6, 8, 9 and 11)	V_{sat}	< 1V

Input Levels R, S and T

HIGH	V_{RH}, V_{SH}, V_{TH}	7.5V to V_P
	I_{RH}, I_{SH}, I_{TH}	1μA typ.
LOW	V_{RL}, V_{SL}, V_{TL}	0 – 4.5V max.
	I_{RL}, I_{SL}, I_{TL}	−30μA typ.

Ratings

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).

Using the SAA1027 With Airpax Four-Phase Stepper Motors

Voltages

Voltage to Pins 6, 8, 9, 11, 13 and 14		18V max.
Input voltages *R* (Pin 3), *S* (Pin 2) and *T* (Pin 15)		V_P max.

Currents

Output currents I_{Q1} (Pin 6), I_{Q2} (Pin 8), I_{Q3} (Pin 9) and I_{Q4} (Pin 11)		500mA max.
Bias current into Pin 4	I_B	90mA max.

Thermal Resistance From junction to ambient	θ_{JA}	70°C/W
Junction Temperature	T_J	125°C Max.

STEPPER MOTOR CHARACTERISTICS

Each of the five stepper motors will have its own typical performance when it is connected as shown in Fig. 2 with the value of resistor R_B correctly selected. The typical torque/speed characteristics for the motors under these conditions, together with a typical dimensioned mechanical outline drawing is given in Fig. 6.

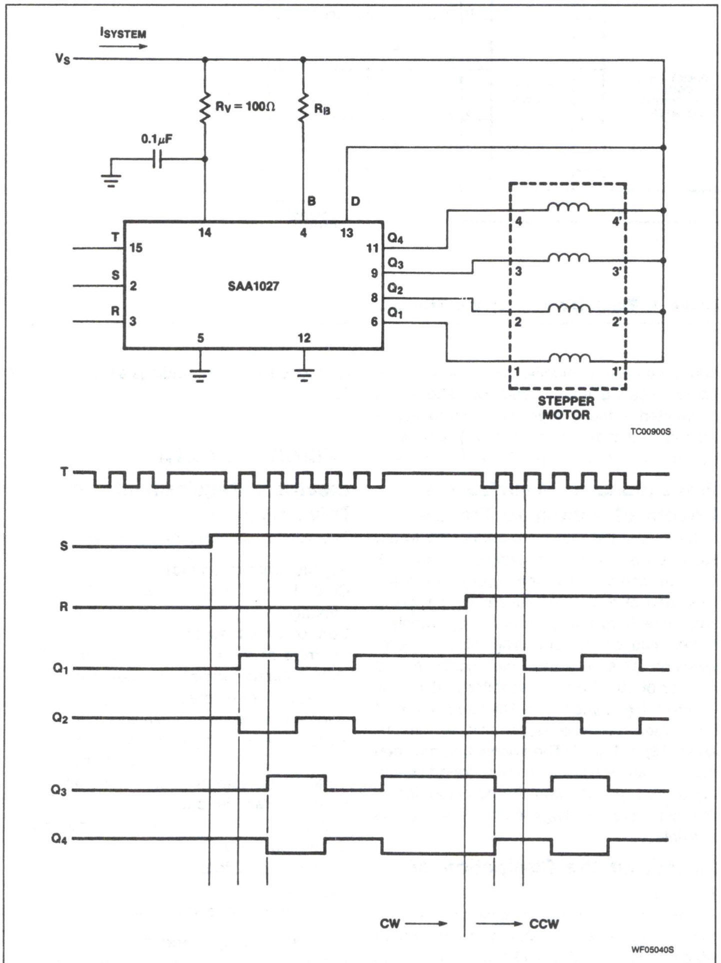

I_{SYSTEM}
VS
RV = 100Ω
RB
0.1μF
B
D
T
S
R
15
2
3
14
4
13
11
9
8
6
Q4
Q3
Q2
Q1
SAA1027
5
12
4
4'
3
3'
2
2'
1
1'
STEPPER MOTOR
TC00900S
T
S
R
Q1
Q2
Q3
Q4
CW
CCW
WF05040S

Figure 2. Connection and Pulse Diagrams for the Drive System

Using the SAA1027 With Airpax Four-Phase Stepper Motors

AN127

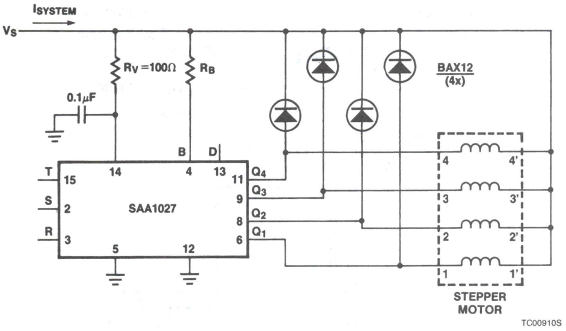

I_SYSTEM
V_S
R_V = 100Ω
R_B
0.1μF
BAX12 (4x)
B
D
T
S
R
15
2
3
14
4
13
11
9
8
6
5
12
SAA1027
Q4
Q3
Q2
Q1
4
4'
3
3'
2
2'
1
1'
STEPPER MOTOR
TC00910S

Figure 3. External Spike Suppression Diodes Being Used to Reduce the Dissipation of the IC

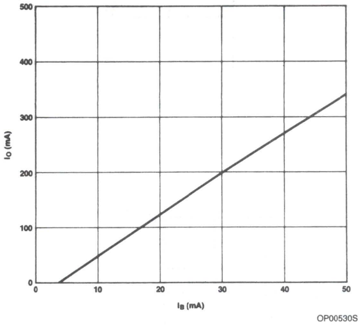


Figure 4. Relationship Between Output Current and Bias Current

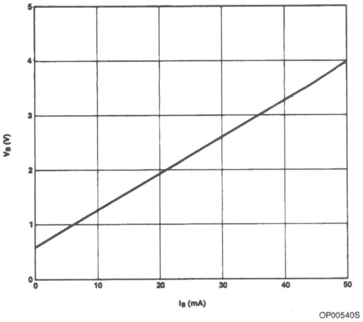


Figure 5. Relationship Between Bias Voltage at Pin 4 and Bias Current

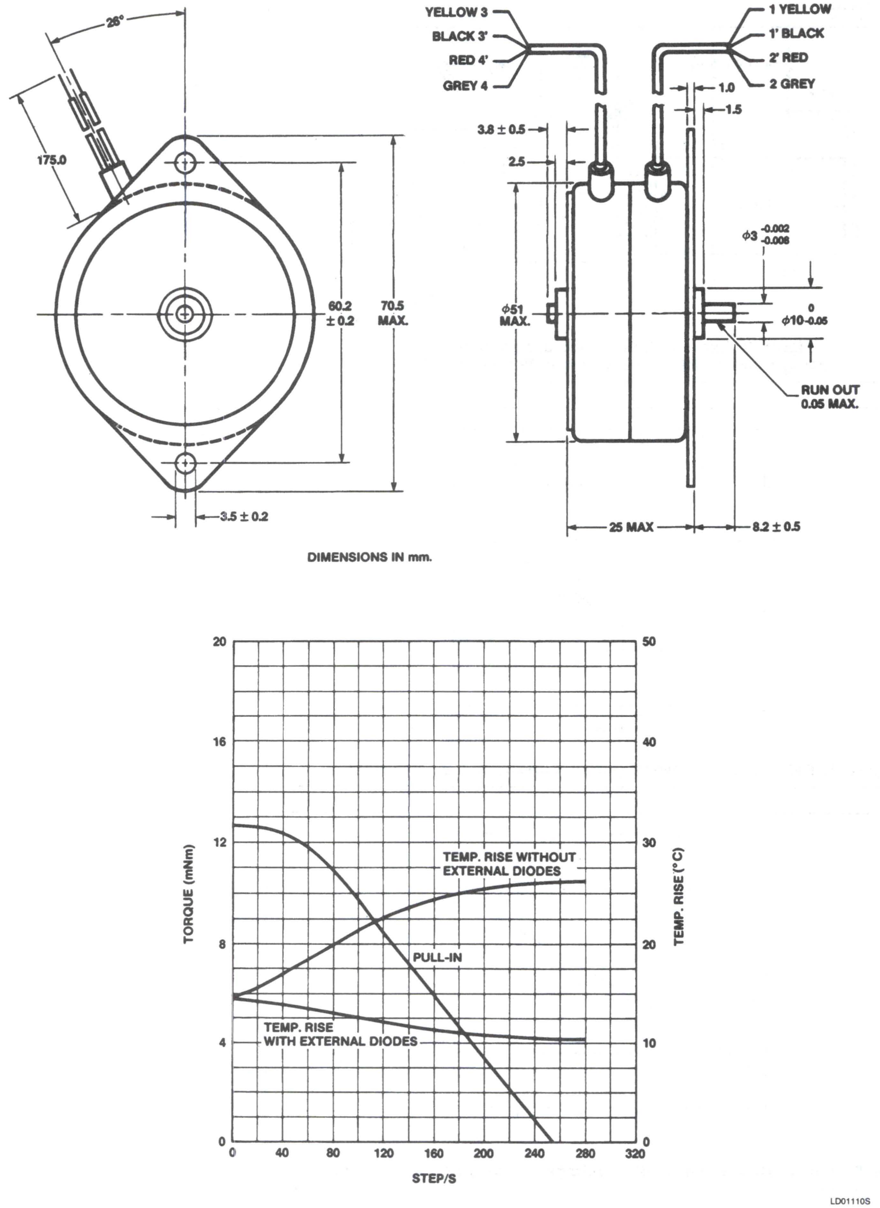


Figure 6. Dimensions and Torque/Speed Characteristic for Stepper Motor 9904 112 04002, and the Temperature Rise of the IC With and Without External Diodes

Signetics

TDA5040T

Brushless DC Motor Driver

Objective Specification

Linear Products

DESCRIPTION

The TDA5040 is designed to operate as a single-phase brushless motor driver in a voltage range of 5 to 16V. Thus a two-phase motor requires two TDA5040Ts and a 3-phase motor will require 3 such devices.

The device contains an internal Hall sensor element for controlling commutation. Motor direction is controlled by logic inputs to C_1 and C_2.

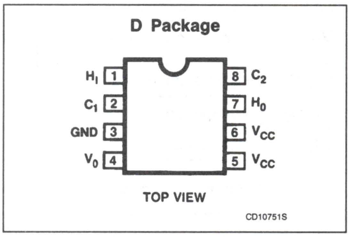
FEATURES

- **Thermal protection**

APPLICATIONS

- **Brushless DC motors**

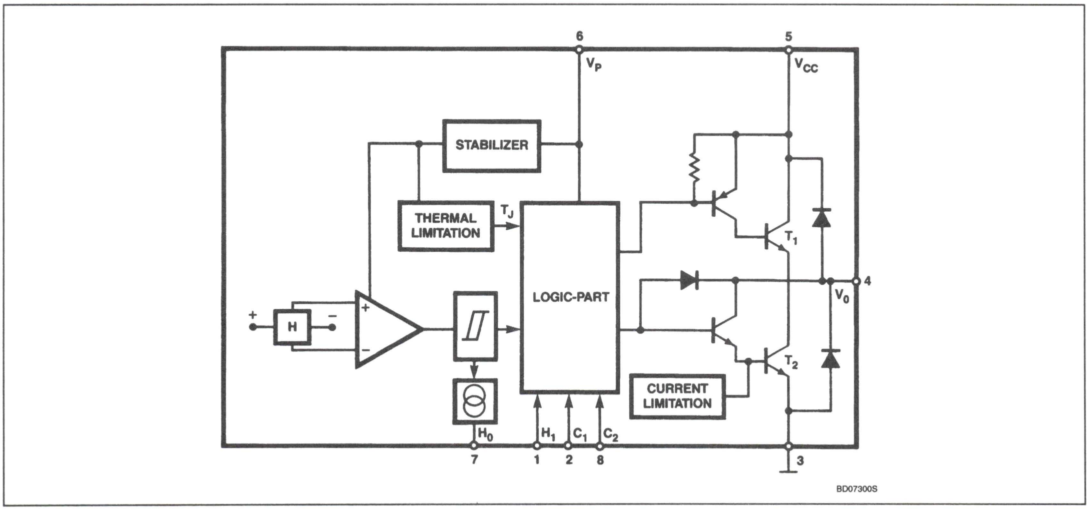
PIN CONFIGURATION


D Package
H_I 1
C_1 2
GND 3
V_0 4
8 C_2
7 H_0
6 V_{CC}
5 V_{CC}
TOP VIEW
CD10751S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO Package	0 to +70°C	TDA5040TD

BLOCK DIAGRAM


6
V_P
5
V_{CC}
STABILIZER
THERMAL LIMITATION
T_J
LOGIC-PART
T_1
T_2
4
V_0
+
H
–
+
–
CURRENT LIMITATION
H_0
H_1
C_1
C_2
7
1
2
8
3
BD07300S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
	Supply voltages			
V_{CC}	Low power stages		−0.5 to 16	V
V_{CC}	Output stage	Under resistance load	−0.5 to 16	V
V_{CC}	Output stage	Under inductive load	0 to 15	V
V_O	Voltage on output	With a maximum of 16V	−0.5 to V_{CC}+1	V
C_1, C_2	Voltage on inputs		−0.5 to 16	V
H_I, H_O	Voltage on Hall output		−0.5 to 16	V
$\pm I_O$	Output current		1.24	A
T_{STG}	Storage temperature		−55 to +150	°C
T_J	Junction temperature	Peak value up to 160°C during 5s	+150	°C

Brushless DC Motor Driver TDA5040T

DC ELECTRICAL CHARACTERISTICS Unless otherwise noted: $5V \leqslant V_{CC} \leqslant 16V$, $-15°C \leqslant T_A \leqslant 60°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Supply voltage						
V_{CC}	Low power stage		5		16	V
V_{CC}	High power stage		0		15	V
Hall-element and trigger circuit						
M_O	Offset		$-15\ 10^{-3}$		$+15\ 10^{-3}$	Tesla
M_H	Hysteresis	Using output H_o or V_o	$2.5\ 10^{-3}$	$4.5\ 10^{-3}$	$6.5\ 10^{-3}$	Tesla
Hall output H_o						
$-IH_oH$	Output current High	$V_p = 12V$ $T_A = 25°C$ $VH_o \leqslant V_p - 0.25V$	10	15	20	µA
IH_oL	Output current Low	$0.7V \leqslant VH_o \leqslant V_p - 0.25V$	10	15	20	µA
$IHo/\Delta T°$	Temperature dependency			0.15		%/°C
$IHo/\Delta V_p$	Voltage dependency			4		%/V
Hall input H_I						
VH_{IH}	Input level High	$I_{HI} > 10\mu A$				
VH_{IL}	Low	$-I_{HI} > 10\mu A$	2.48	2.8	3.15	V
VH_{IS}	Input switching level to drive Output V_O according to truth table	Referred to the calculated switching level $\frac{V_{HIH} + V_{HIL}}{2}$	TBD	0	TBD	mV
Logic inputs C_1 resp. C_2						
V_{IL}	Input voltage Low				1	V
V_{IH}	Input voltage High		2			V
I_{IL}	Input current Low	$V_c = 0.4V$	TBD	19	TBD	µA
I_{IH}	Input current High	$V_c = 16V$			2	µA
Power output stage						
V_{OL}	Output voltage Low	I_o = pulse of 1ms $I_o = 400mA$ duty cycle $\leqslant 1/10$		1	1.25	V
$\Delta V_{OL}/\Delta T°$	Temperature dependency			−0.93		mV/°C
V_{OH}	Output voltage High	$-I_o = 500mA$ duty cycle $\leqslant 1/10$	$V_{cc} - 1.35$	$V_{CC} - 1.1$		V
$\Delta V_{OH}/\Delta T°$	Temperature dependency			+3.6		mV/°C
I_{OL}	Output current Low internally limited		500		1200	mA
I_{OF}	Output current float	$V_o = V_{cc} = 16V$			1	mA
$-I_{OF}$	Output current float	$V_o = 0V$, $V_{cc} = 16V$			1	mA
R_L	Load resistance (across Pins 4 and 5)		6			Ω
Quiescent current						
I_p	Output Low or Float	$I_o = 0$, $V_p = V_{cc} = 16V$		6	TBD	mA
$I_p + I_{CC}$	Output High	$I_o = 0$, $V_p = V_{cc} = 16V$		9	TBD	
Thermal protection						
$T_{JSW\text{-}OFF}$	Switch-off temperature		130		160	°C
$T_{JSW\text{-}ON}$	Switch-on temperature		90		140	°C
T_{JSW}	Hysteresis		20	30	40	°C

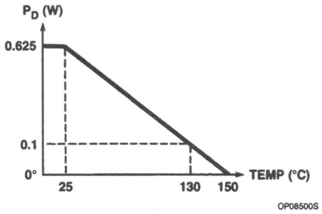


Figure 1. Operating Derating Curve

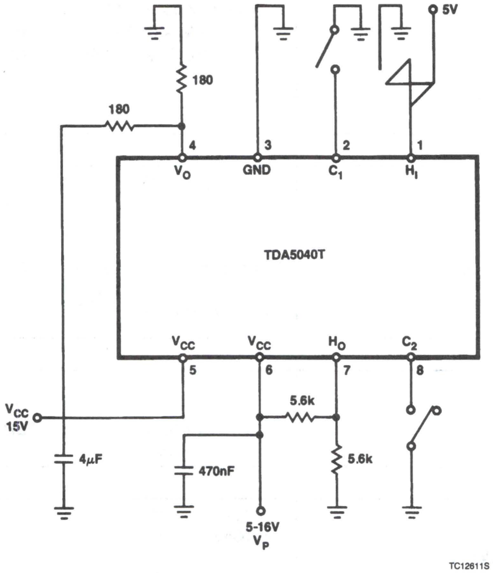

5V
180
180
4
3
2
1
V_O
GND
C_1
H_I
TDA5040T
V_{CC}
V_{CC}
H_O
C_2
5
6
7
8
V_{CC}
15V
5.6k
4μF
470nF
5.6k
5-16V
V_P
TC12611S

Figure 2

THEORY OF OPERATION

C_1 defines the motor rotation direction by connecting it to a high or low voltage level. A low voltage level on C_2 is a float command. Both C_1 and C_2 can be driven by a TTL, CMOS or LOCMOS circuit. Both input characteristics allow up to three inputs to be driven directly by one TTL, CMOS or LOCMOS circuit (e.g., a common float command line for all three ICs in the motor).

The circuit includes a thermal protection which switches the output in the floating state when the chip exceeds the limiting temperature. A hysteresis on this protection avoids degradation of the IC during constant short-circuit of the output. The output power current is limited by a current-limiter in the lower output stage.

A zener diode protects the lower output stage in case the supply voltage V_{CC} is disconnected and the output is inductively loaded. (See Block Diagram.)

TRUTH TABLE

INPUT					OUTPUT	
T_J	M	C_2	C_1	H_I	H_O	V_O
L	N	H	H	H	H	COMMON
L	S	H	H	H	L	H
L	N	H	H	L	H	L
L	S	H	H	L	L	COMMON
L	N	H	L	H	H	COMMON
L	S	H	L	H	L	L
L	N	H	L	L	H	H
L	S	H	L	L	L	COMMON

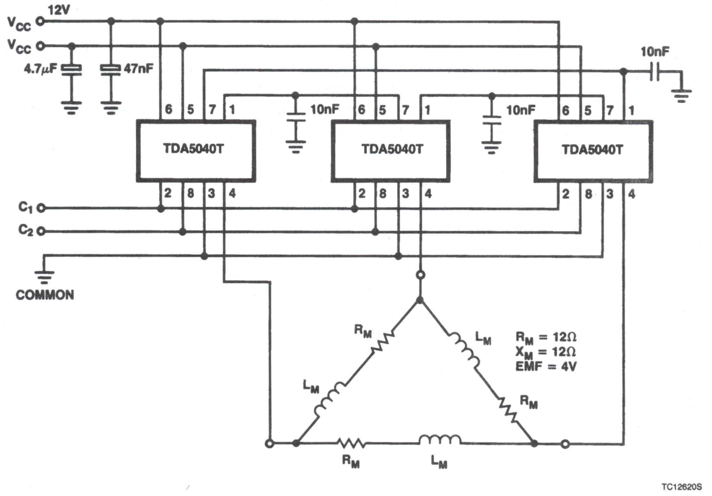
Remarks

T_J = "L" : junction temp. < min. switch on temp.

M = "N" : magnetic north above and south pole below the IC, magnetic field strength > max. offset + ½ max. hysteresis

M = "S" : magnetic south above and north pole below the IC, magnetic field strength > max. offset + ½ max. hysteresis

H_O is H_I compatible



NOTES:
N_{NOM} = 1500RPM
F_{NOM} = 200Hz
T_{NOM} = 2mNm
V_{CC} = 12V
$I_{CC\ NOM}$ = 80mA

Figure 3. Typical Application Circuit

Signetics

Linear Products

AN120
An Overview of Switched-Mode Power Supplies

Application Note

Conceptually, three basic approaches exist for obtaining regulated DC voltage from an AC power source. These are:

- Shunt regulation
- Series linear regulation
- Series switched-mode regulation

All require AC power line rectification.

The series switched-mode regulators will be referred to as switched-mode power supplies or SMPS during the course of this article.

Briefly stated, if all three types of regulation can perform the same function, the following are some of the key parameters to be addressed:

- From an economical point of view, cost of the system is paramount.
- From an operations point of view, weight of the system is critical.
- From a design criteria, system efficiency is the first order of business.

The series and shunt regulators operate on the same principle of sensing the DC output voltage, comparing to an internal reference level and varying a resistor (active device) to maintain the output levels within prespecified limits.

Switched-mode power supplies (SMPS) are basically DC-to-DC converters, operating at frequencies in the 20kHz and higher region. Basically, the SMPS is a power source which utilizes the energy stored during one portion of its operating cycle to supply power during the remaining segment of its operating cycle.

Linear regulators, both shunt and series, suffer when required to supply large currents with resultant high dissipation across the regulating device. Efficiency suffers tremendously. (Efficiencies less than 40% are typical.)

Switched-mode power supplies operate at much higher levels of efficiency (generally in the order of 75% to 80%), thereby reducing significantly the energy wasted in the regulated supply. The SMPS does, however, suffer significantly in the ripple regulation it is able to maintain, as opposed to a much higher degree of regulation available in series (or shunt) linear regulators.

The linear regulators obtain improved regulation by virtue of the series pass elements always conducting, as opposed to SMPS devices having their active devices operative only during a portion of the overall operating period.

Some definitions and comparisons between linear regulators and switched-mode power supplies follow for reference.

REGULATION

Line Regulation — (Sometimes referred to as static regulation) refers to the changes in the output (as a percent of nominal or actual value) as the input AC is varied slowly from its rated minimum value to its rated maximum value (eg. from $105VAC_{RMS}$ to $125VAC_{RMS}$).

Load Regulation — (Sometimes referred to as dynamic regulation) refers to changes in output (as a percent of nominal or actual value) when the load conditions are suddenly changed (eg. minimum load to full load.)

NOTES:
The combination of static and dynamic regulation are cumulative; care should be taken when referring to the regulation characteristics of a power supply.

Thermal Regulation — Referred to as changes due to ambient variations or thermal drift.

TRANSIENT RESPONSE

The ability of the regulator to respond to rapid changes in either line variations, load variations, or intermittent transient input conditions. (This parameter is often referred to as "recovery time.")

AC PARAMETERS

Voltage Limiting — The regulator's ability to "shut down" in the event that the internal control elements fail to function properly.

Current Limiting — Often referred to as "fold-back", where the amplifier segment of the regulator folds back the output current of the device when safe operating limits are exceeded.

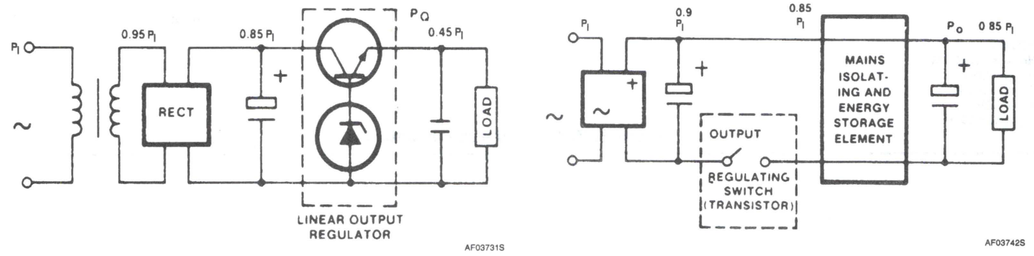
Thermal Shutdown — The regulator's ability to shut itself down when the maximum die temperature is exceeded.

GENERAL PARAMETERS

Power Dissipation — The maximum power the regulator can tolerate and still maintain operation within the safe operating area of its active devices.

Efficiency — The ratio (in percent) of the usable versus total power being dissipated in a regulated supply. (The losses can be AC as well as DC losses.)

EMI/RFI — Generation of ElectroMagnetic/Radio Frequency Interference signals and magnetic field disturbance in SMPS devices. (Transformer and choke design are available which reduce both RFI & EMI to safe acceptance regions.)



a. Conventional Supply — 45% Efficiency **b. Switched-Mode Supply — 80%Efficiency**

Figure 1. Losses in Regulated Power Supplies

An Overview of Switched-Mode Power Supplies

AN120

The balance of this section will be dedicated to the discussion of the general operation of Switched-Mode Power Supplies (SMPS) with emphasis on the Signetics NE5560 Control and Protection Module.

Switched-mode power supplies (SMPS) have gained much popularity in recent years because of the benefits they offer. They are now used on a large scale in desk calculators, computers, instrumentation, etc., and it is confidently expected that the market for this type of supply will grow.

The advantages of SMPS are low weight and small size, high efficiency, wide AC input voltage range, and low cost.

- Low weight and small size are possible because operation occurs at a frequency beyond the audible range; the inductive elements are small.
- High efficiency because, for output regulation, the power transistor is switched rapidly between saturation and cut-off and therefore has little dissipation. This eases heatsink requirements, which contributes to weight and volume reduction. Conventional linear regulator supplies may have efficiencies as low as 50%, or less, but efficiencies of 80% are readily achievable with SMPS (see Figure 1).
- Wide AC input voltage range because the flexibility of varying the switching frequency in addition to the change in transistor duty cycle makes voltage adaptation unnecessary.
- Low overall cost, due to the reduced volume and power dissipation, means that less material is required and smaller semiconductor devices suffice.

Switched-mode power supplies also have slight disadvantages in comparison to linear regulators, namely, somewhat greater circuit complexity, tendency to RFI radiation, slower response to rapid load changes, and less ability to remove output ripple.

HOW SWITCHED-MODE POWER SUPPLIES OPERATE

The switched-mode power supply is a modern version of its forerunner, the electromechanical vibrator, used in the past to supply car radios. But the new concept is much more reliable because of the far greater lifetime of the transistor switch. Figure 2 shows the principle of the AC fed SMPS. In this system, the AC voltage is rectified, smoothed, and supplied to the electronic chopper, which operates at a frequency above the audible range to prevent noise. The chopped DC voltage is applied to the primary of a transformer, and the secondary voltage is rectified and smoothed to give the required DC output. The transformer is necessary to isolate the output from the input. Output voltage is sensed by a control circuit, which adjusts the duty cycle of the switching transistor, via the drive circuit, to keep the output voltage constant irrespective of load and line voltage changes. Without the input rectifier, this system can be operated from a battery or other DC source.

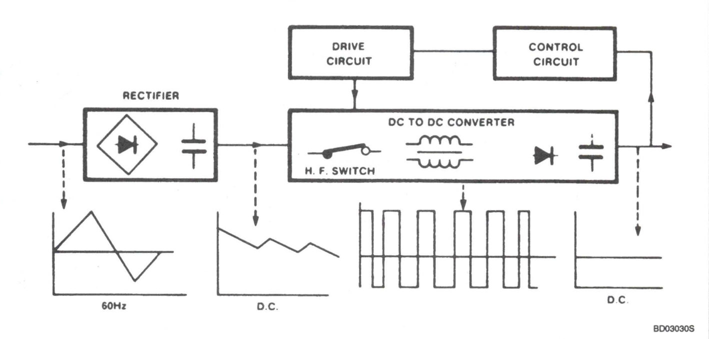


Figure 2. Block Diagram of Switched-Mode Power Supply

Depending on the requirements of the application, the DC-to-DC converter can be one of the three basic types: flyback converter, forward converter, or push-pull (balanced) converter.

The Flyback Converter

Figure 3 shows the flyback converter circuit, and the waveforms of transistor voltage, V_{CE}, and choke current, I_L, reflected to the primary (choke double-wound for line isolation). Cycle time and transistor duty cycle are denoted T and δ, respectively. While Q1 conducts, energy is accumulated in the choke magnetic field (I_L rising and D_1 reverse-biased), and it is discharged into the output capacitor and the load during the flyback period, that is, while Q1 is off (I_L falling and D_1 forward-biased). During Q1 conduction, C_O continues delivering energy to the load, so providing smoothing action. It will be noted that only one inductive element is needed, in distinction to the converter types discussed below, which require two. As the V_{CE} waveform shows, the peak collector voltage is twice the input voltage, V_I, for δ equal to 0.5.

The Forward Converter

A major advantage of the forward converter, particularly for low output voltage applications, is that the high frequency output ripple is limited by the choke in series with the output. Figure 4 illustrates the circuit. During the transistor-on (or forward) period, energy is simultaneously stored in the choke L_O and passed via D_1 to the load. While Q1 is off, part of the energy accumulated in L_O is transferred to the load through free-wheeling diode D_2. Output capacitor C_O smoothes the ripple due to transistor switching. After transistor turn-off, the magnetic energy built up in the transformer core is returned to the DC input via the demagnetizing winding (closely coupled with the primary) and D_3, so limiting the peak collector voltage to twice the input voltage, V_I.

The Push-Pull Converter

This converter type, given in Figure 5, consists of two forward converters operating in push-pull. Diodes D_1 and D_2 rectify the rectangular secondary voltage generated by Q1 and Q2 being turned on during alternate half cycles. Push-pull operation doubles the frequency of the ripple current in output filter L_OC_O and so reduces the output ripple voltage. The peak transistor voltage is $2V_I$.

MAKING THE BEST CONVERTER CHOICE

There exist several versions of the three fundamental circuits described earlier.

These are shown in Figure 6. Circuits IA, IIA and IIIA are the basic types. In the two transistor circuits IB and IIB, transistors Q1 and Q2 conduct simultaneously and diodes D_4 and D_5 limit the peak collector voltage to the level of DC input voltage, V_I. Similarly, in the push-pull circuits IIIB and IIIC, the collector voltage does not exceed V_I; in circuit IIIB, Q1 and Q2 are turned on during alternate half cycles, in circuit IIIC, Q1 and Q4 are turned on in one half cycle and Q2 and Q3 in the next.

Converter choice depends on application and performance requirements. The flyback converter is the simplest and least expensive; it is recommended for multi-output supplies because each output requires only one diode and one capacitor. However, smoothing may be a problem where ripple requirements are severe. The push-pull type has the most complex base drive circuit but it produces the

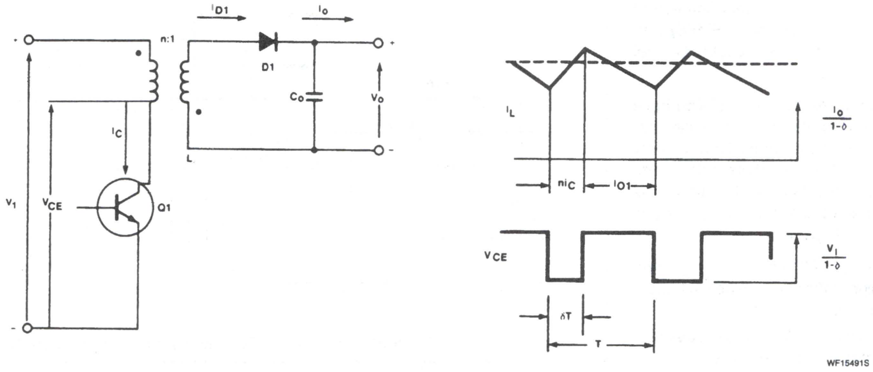


Figure 3. Flyback Converter Circuit Diagram and Waveforms

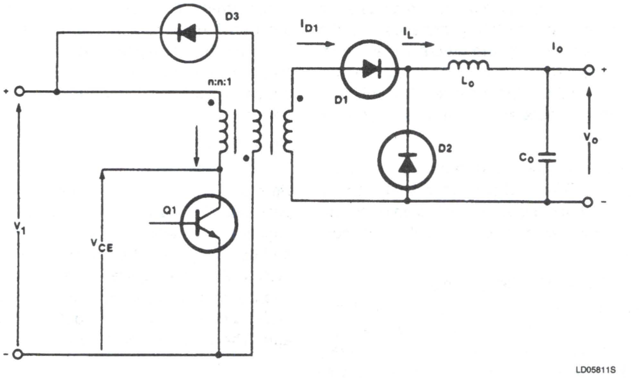


Figure 4. Forward Converter Circuit Diagram

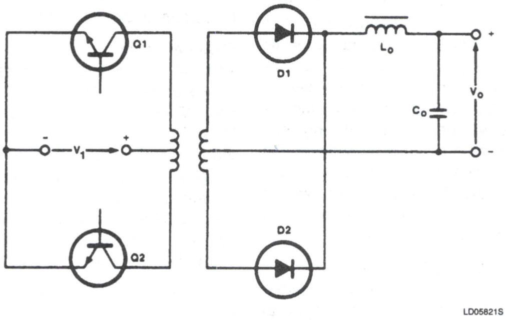


Figure 5. Push-Pull Converter Circuit Diagram

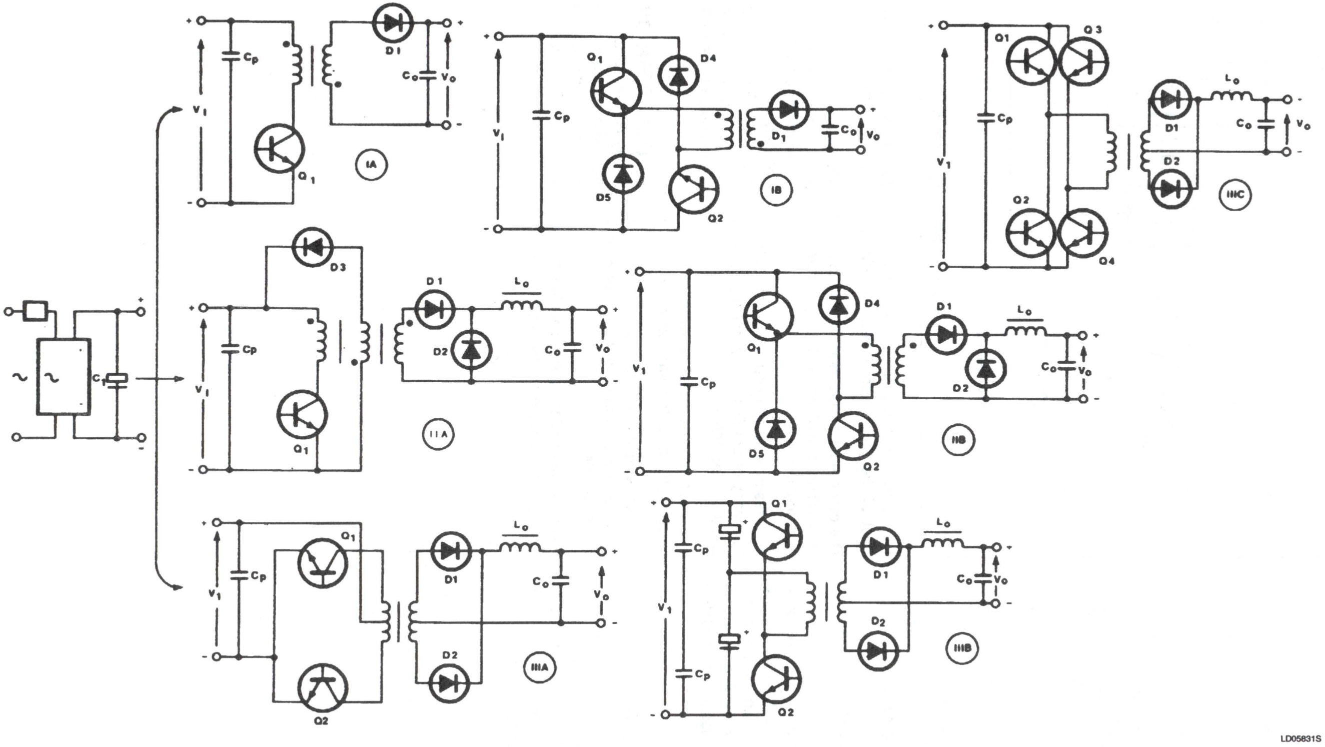
lowest output ripple with given values of L_O and C_O.

Figure 7 is a general guide for the choice of converter type, based on output voltage and power. In the case of the flyback converter, it becomes more and more difficult to keep the percentage output ripple below an acceptable level as the output power increases and the output voltage decreases. For reasons of circuit economy, however, the flyback converter is the best proposition if the output power does not exceed about 10W. For output powers higher than about 1kW, the push-pull converter is preferable.

THE CONTROL AND PROTECTION MODULE

In addition to providing adequate output voltage stabilization against line voltage and load changes, the control module must give fast protection against overload, equipment malfunction, and the effects of switch-on immediately following switch-off. In addition the following features are desirable:

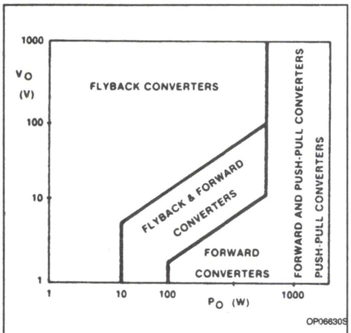
- Soft-Start: a gradual increase of the transistor duty cycle after switch-on causing a slow rise of the output voltage, which prevents an excessive inrush current due to a capacitive load or charging of the output capacitor.
- Synchronization: to prevent interference due to the difference in free-running frequencies (for example, in a system in which a low-power SMPS supplies the base drive circuit of the output switching transistor in a high-power SMPS).


IA
IB
IIA
IIB
IIIA
IIIB
IIIC
Q1
Q2
Q3
Q4
D1
D2
D3
D4
D5
Cp
Co
Cf
Lo
V1
Vo
+
-
LD05831S

NOTES:
Flyback converter family with 1A single-transistor type and 1B two-transistor type.
Forward converter family with 2A single-transistor type and 2B two-transistor type.
Push-pull converter family with 3A conventional type, 3B single-ended type, and 3C bridge type.

Capacitor C_P is a high-frequency bypass (20Hz switching frequency).

Figure 6. Various DC-to-DC Converter Types with Their Rectifier Supply



NOTE:
Converter choice as a function of SMPS output voltage, V_O and output power, P_O.

Figure 7. Converter Type

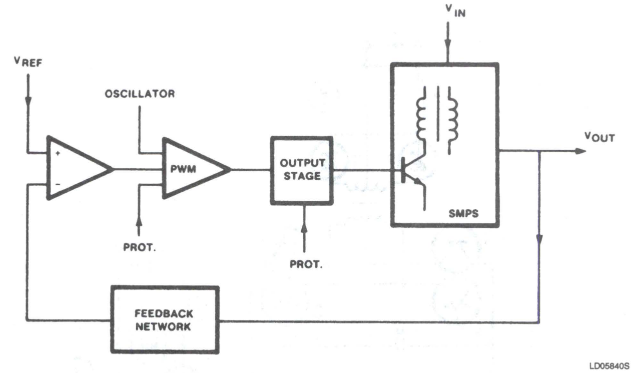


Figure 8. SMPS Control Loop

- Remote switch-on and switch-off: essential for sequential switching of supply units in, for instance, a computer supply system.

The control and protection circuitry of a switched-mode power supply (SMPS) is a crucial and complicated part of the whole supply. Integration of this circuitry on a chip will therefore ease the design of an SMPS considerably.

SMPS CONTROL LOOP

Figure 8 shows the principal control loop of a regulated SMPS. The output voltage V_O is sensed and, via a feedback network, fed to the input of an error amplifier where it is compared with a reference voltage.

The output of this amplifier is connected to an input of the pulse-width modulator, PWM.

The other input of this modulator is used for an oscillator signal, which can be a sawtooth or a triangle.

As a result, a rectangular waveform with the frequency of the oscillator is emerging at the output of the PWM.

The width of this pulse is dictated by the output voltage of the error amplifier.

After passing through an output stage, the pulse can be used to drive the power transistor of the SMPS.

When the width of the pulse is varied, the on-time of this transistor will also vary and consequently the amount of energy taken from the input voltage, V_I.

So, by controlling the duty cycle δ of the power transistor, one can stabilize the output of the SMPS against line and load variations. The duty cycle δ is defined as t_{ON}/T for the power transistor. Protections for overvoltage, overcurrent, etc., can be realized with additional inputs on the PWM or the output stage.

INITIAL TURN-ON

It may be helpful to operate an SMPS open loop with reduced error amplifier gain. This provides an easy way to verify correct operation of control loop elements.

Signetics

Linear Products

NE/SE5560

Switched-Mode Power Supply Control Circuit

Product Specification

DESCRIPTION

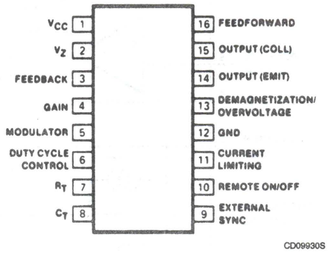
The NE/SE5560 is a control circuit for use in switched-mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched-mode power supplies, including an internal temperature-compensated reference source, internal Zener references, sawtooth generator, pulse-width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse-width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle clamp**
- **Feed-forward control**
- **External synchronization**

PIN CONFIGURATION

D, F, N Packages


V_{CC} 1
V_Z 2
FEEDBACK 3
GAIN 4
MODULATOR 5
DUTY CYCLE CONTROL 6
R_T 7
C_T 8
16 FEEDFORWARD
15 OUTPUT (COLL)
14 OUTPUT (EMIT)
13 DEMAGNETIZATION/ OVERVOLTAGE
12 GND
11 CURRENT LIMITING
10 REMOTE ON/OFF
9 EXTERNAL SYNC
CD09930S

TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to 70°C	NE5560N
16-Pin Plastic Dip	−55°C to 125°C	SE5560N
16-Pin Cerdip	0 to 70°C	NE5560F
16-Pin Cerdip	−55°C to 125°C	SE5560F
16-Pin SO	0 to 70°C	NE5560D

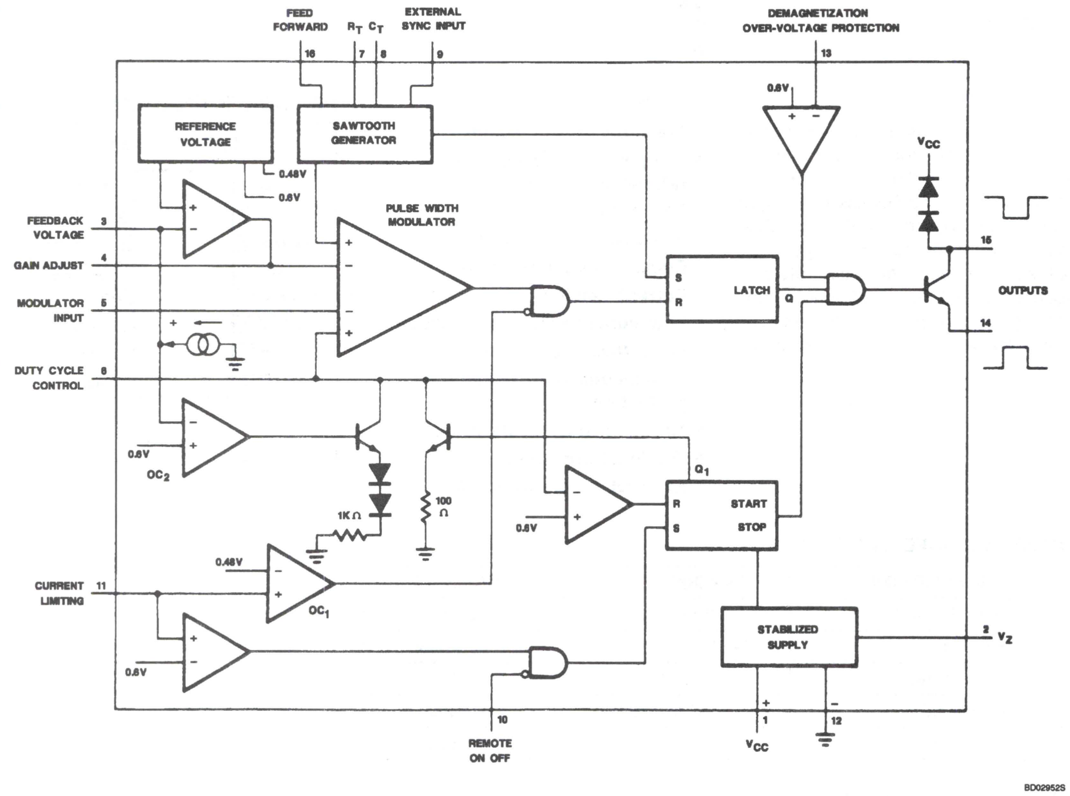
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply[1]		
V_{CC}	Voltage-forced mode	+18	V
I_{CC}	Current-fed mode	30	mA
	Output transistor (at 20 – 30V max)		
I_{OUT}	Output current	40	mA
	Collector voltage (Pin 15)	V_{CC} + 1.4V	V
	Max. emitter voltage (Pin 14)	+5	V
T_A	Operating ambient temperature range		
	SE5560	−55 to +125	°C
	NE5560	0 to 70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Does not include current for timing resistors or capacitors.

Switched-Mode Power Supply Control Circuit NE/SE5560

BLOCK DIAGRAM


FEED FORWARD
R_T
C_T
EXTERNAL SYNC INPUT
16
7
8
9
DEMAGNETIZATION OVER-VOLTAGE PROTECTION
13
0.6V
REFERENCE VOLTAGE
SAWTOOTH GENERATOR
0.48V
0.6V
PULSE WIDTH MODULATOR
V_{CC}
FEEDBACK VOLTAGE 3
GAIN ADJUST 4
MODULATOR INPUT 5
DUTY CYCLE CONTROL 6
S
R
LATCH
Q
15
14
OUTPUTS
0.6V
OC_2
Q_1
1KΩ
100 Ω
0.6V
R
S
START
STOP
0.48V
CURRENT LIMITING 11
OC_1
STABILIZED SUPPLY
2 V_Z
0.6V
10
REMOTE ON OFF
1
12
V_{CC}
BD02952S

NOTE:

1. See Voltage/Current fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
Reference sections									
V_{REF}	Internal reference voltage	25°C Over temperature	3.69 3.65	3.72	3.81 3.85	3.57 3.53	3.72	3.95 4.00	V V
	Temperature coefficient of V_{REF}			−100			−100		ppm/°C
V_Z	Internal Zener reference Temperature coefficient of V_Z	$I_L = -7mA$	7.8	8.4 200	8.8	7.8	8.4 200	8.8	V ppm/°C
Oscillator section									
	Frequency range	Over temperature	50		100k	50		100k	Hz
	Initial accuracy oscillator	$R = 5k\Omega$		5			5		%
	Duty cycle range	$f_O = 20kHz$	0		98	0		98	%
Modulator									
	Modulation input current	Voltage at Pin 5 = 2V Over temperature		0.2	20		0.2	20	μA
Housekeeping function									
I_{IN}	Pin 6, input current	At 2V Over temperature		0.2	20		0.2	20	μA
	Pin 6, duty cycle limit control	For 50% max duty cycle 15kHz to 50kHz/41% of V_Z	40	50	60	40	50	60	% of duty cycle
	Pin 1, low supply voltage protection thresholds		8	9.0	10.5	8	9.0	10.5	V
	Pin 3, feedback loop protection trip threshold		400	600	720	400	600	720	mV
I_{IN}	Pin 3, pull-up current	At 2V	−7	−15	−35	−7	−15	−35	μA
	Pin 13, demagnetization/over-voltage protection trip on threshold	Over temperature	470	600	720	470	600	720	mV
	Pin 13, input current	At 0.25V 25°C Over temperature		−0.6	−10 −20		−0.6	−10 −20	μA
	Pin 16, feed-forward duty cycle control	Voltage at Pin 16 = $2V_Z$	30	40	50	30	40	50	% original duty cycle
	*Pin 16, feed-forward input current	At 16V, $V_{CC} = 18V$ 25°C		0.2	5		0.2	5	μA
		Over temperature			10			10	μA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
External synchronization									
	Pin 9 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
	Sink current	Voltage at Pin 9 = 0V, 25°C		−65	−100		−65	−125	μA
		Over temperature			−125			−125	μA
Remote									
	Pin 10 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
	Sink current	At 0V 25°C		−85	−100		−85	−125	μA
		Over temperature			−125			−125	μA
Current limiting									
I_{IN}	Pin 11 Input current	Voltage at Pin 11 = 250mV 25°C		−2	−20		−2	−20	μA
		Over temperature			−40			−40	μA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	μs
OC_1	Trip Levels: Shut down, slow start, low level		0.500	0.600	0.700	0.500	0.600	0.700	V
OC_2	Current limit, high level		0.400	0.480	0.560	0.400	0.560	0.500	V
ΔOC	Low Level in terms of high level, OC_1		0.750	0.800	0.850	0.750	0.800	0.850	V
Error amplifier									
V_{OH}	Output voltage swing		6.2		9.5	6.2		9.5	V
V_{OL}	Output voltage swing				0.7			0.7	V
	Open-loop gain		54	60		54	60		dB
R_F	Feedback resistor		10k			10k			Ω
BW	Small-signal bandwidth			3			3		MHz
Output stage									
	$V_{CE}(SAT)$ $I_C = 40mA$				0.5			0.5	V
	Output current (Pin 15)		40			40			mA
	Max. emitter voltage (Pin 14)		5	6		5	6		V
Supply voltage/current[1]									
I_{CC}	Supply current	$I_Z = 0$, voltage-forced, $V_{CC} = 12V$, 25°C			10			10	mA
		Over temp.			15			15	mA
V_{CC}	Supply voltage	$I_{CC} = 10mA$ current-fed	20		23	19		24	V
V_{CC}	Supply voltage	$I_{CC} = 30mA$ current-fed	20		30	20		30	V

NOTE:

1. Does not include current for timing resistors or capacitors.

MAXIMUM PIN VOLTAGES

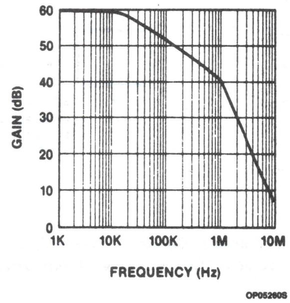
NE5560		
Pin No	**Function**	**Maximum Voltage**
1	V_{CC}	See Note 1
2	V_Z	Do not force (8.4V)
3	Feedback	V_Z
4	Gain	
5	Modulator	V_Z
6	Duty Cycle Control	V_Z
7	R_T	Current force mode
8	C_T	
9	External Sync	V_Z
10	Remote On/Off	V_Z
11	Current Limiting	V_{CC}
12	GND	GND
13	Demagnetization/Overvoltage	V_{CC}
14	Output (Emit)	V_Z
15	Output (Collector)	$V_{CC} + 2V_{BE}$
16	Feed-forward	V_{CC}

NOTE:

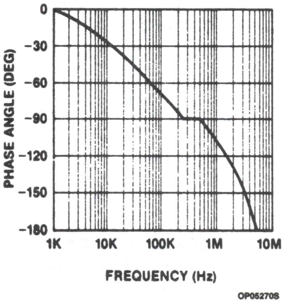
1. When voltage-forced, maximum is 18V; when current-fed, maximum is 30mA. See voltage-/current-fed supply characteristic curve.

TYPICAL PERFORMANCE CHARACTERISTICS

Error Amplifier Open-Loop Gain



Error Amplifier Open-Loop Phase

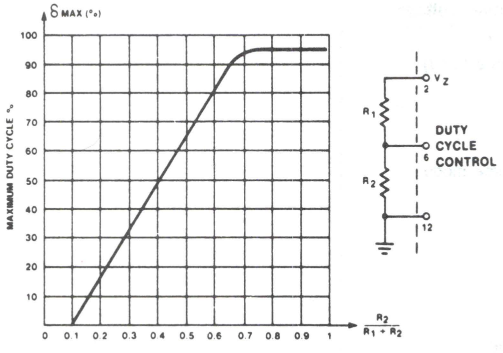


Switched-Mode Power Supply Control Circuit

NE/SE5560

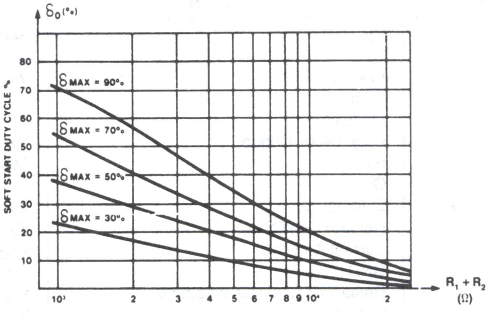
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Graph for Determining δ_{MAX}



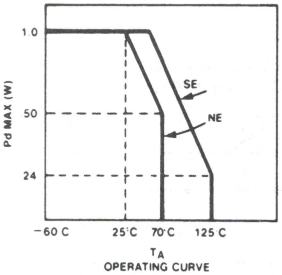
OP05280S

Soft-Start Min. Duty Cycle vs $R_1 + R_2$



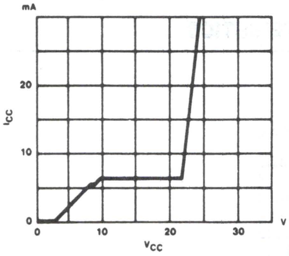
OP05290S

Power Derating Curve



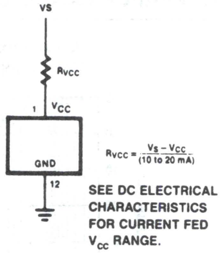
OP05300S

NE5560 Voltage-/Current-Fed Supply Characteristics



OP05310S

Current-Fed Dropping Resistor

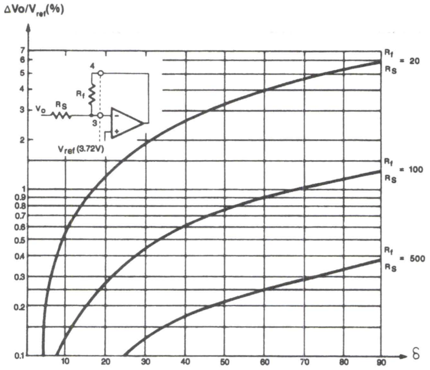


$R_{VCC} = \frac{V_S - V_{CC}}{(10 \text{ to } 20 \text{ mA})}$

SEE DC ELECTRICAL CHARACTERISTICS FOR CURRENT FED V_{CC} RANGE.

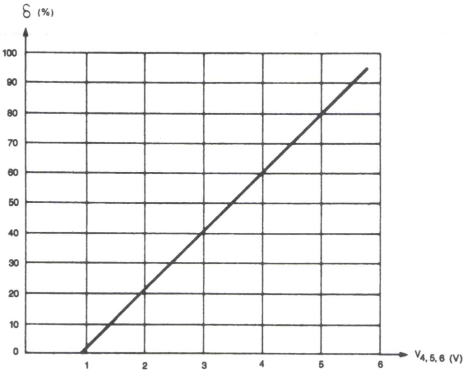
TC08780S

Regulation vs Error Amp Closed-Loop Gain



OP05320S

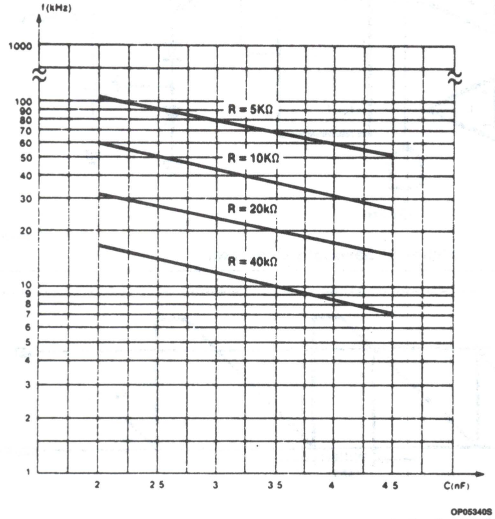
Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage



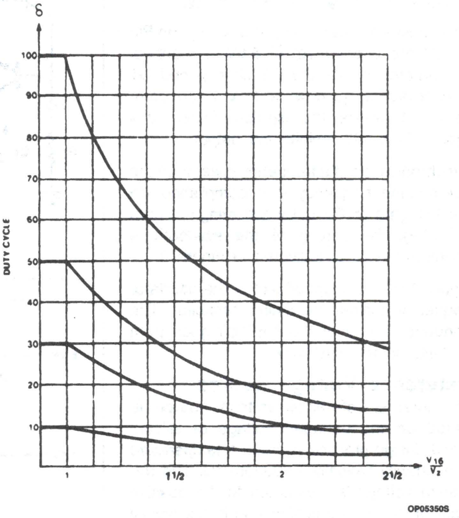
OP05330S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Typical Frequency Plot vs R_T and C_T



Duty Cycle Sensitivity to Feed-Forward Voltage (Pin 16)



THEORY OF OPERATION

The following functions are incorporated:

- A temperature-compensated reference source.
- An error amplifier with Pin 3 as input. The output is connected to Pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (Pins 7, 8, 9).
- A pulse-width modulator with a duty cycle range from 0 to 95%.

The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ_{MAX}

Pin 5 gives a direct access to the modulator, allowing for real constant-current operation:

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore Pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at Pin 10, also operating via the start-stop circuit.
- An inhibit input at Pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (Pin 15) and the emitter (Pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage- or current-driven (Pins 1 and 12). The internally-generated stabilized output voltage V_Z is connected to Pin 2.
- A special function is the so-called feed-forward at Pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim 1/V16$.
- Loop fault protection circuits assure that the duty cycle is reduced to zero or a low value for open- or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5V.

This voltage V_Z is also present at Pin 2 and can be used for precise setting of δ_{MAX} and to supply external circuitry. Its max. current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current-driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage: typical 23V for 10mA and max. 30V for 30mA.

The low supply voltage protection is active when $V_{(1-12)}$ is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and $R_{(7-12)} \geqslant 20k\Omega$.

The Sawtooth Generator

Figure 2 shows the principal circuitry of the oscillator. A resistor between Pin 7 and Pin 12 (GND) determines the constant current that charges the timing capacitor $C_{(8-12)}$.

This causes a linear increasing voltage on Pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS flip-flop and Q1 discharges $C_{(8-12)}$ down to 1.1V, where comparator L resets the flip-flop. During this flyback time, Q2 inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on Pin 9. By activating this gate ($V^9 < 2V$), the setting of the sawtooth is prevented. This is indicated in Figure 3.

Figure 4 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the NE5560 goes from < 50Hz up to > 100kHz.

Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency typically ± 100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amplifier Compensation

For closed-loop gains less than 40dB, it is necessary to add a simple compensation capacitor as shown in Figures 4 and 5.

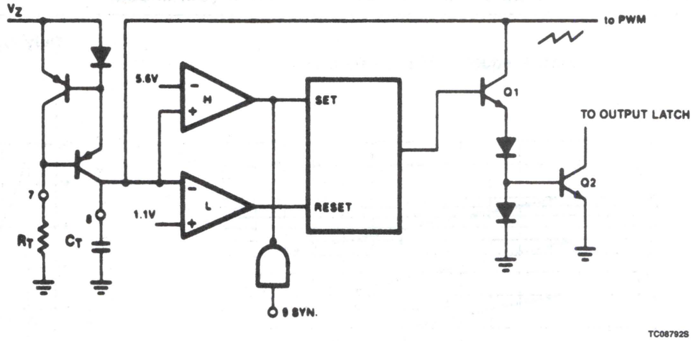


Figure 2. Sawtooth Generator

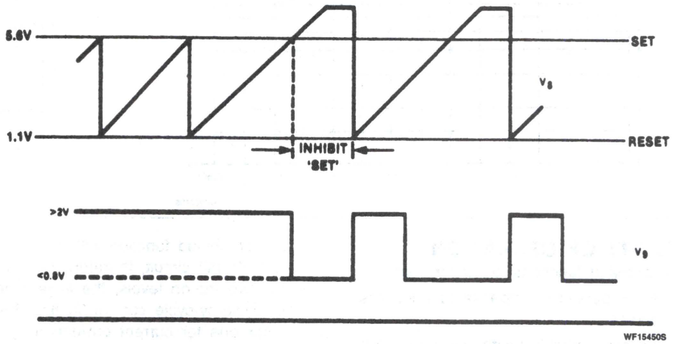


Figure 3. Sawtooth Oscillator Synchronization

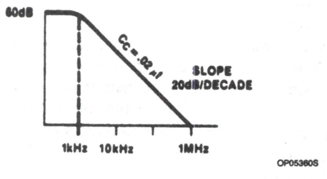


Figure 4. Error Amplifier Compensation Open-Loop Gain

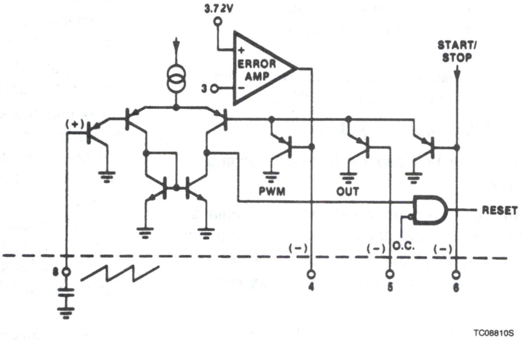


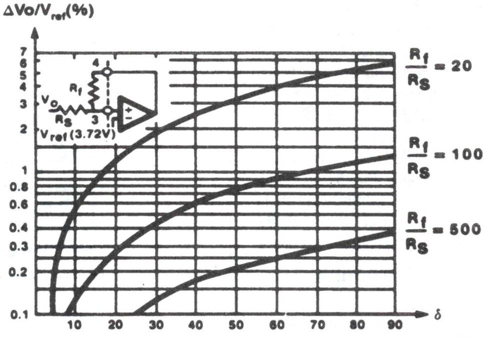
Figure 5. Error Amplifier

Error Amplifier with Loop-Fault Protection Circuits

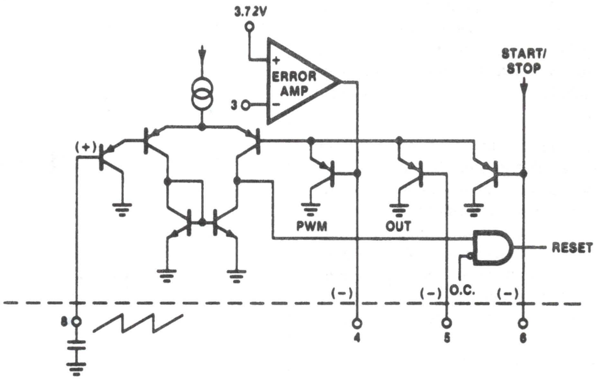
This operational amplifier is of a generally used concept and has an open-loop gain of typically 60dB. As can be seen in Figure 5, the inverting input is connected to Pin 3 for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to Pin 4, so that the required gain can be set with R_S and $R_{(3-4)}$. This is indicated in Figure 5, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, Pin 4 can be used for phase shift networks that improve the loop stability.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via $R_{(3-4)}$. This would result in a large duty cycle. A current source on Pin 3 prevents this by pushing the input voltage high via the voltage drop over $R_{(3-4)}$. As a result, the duty cycle will become zero, provided that $R_{(3-4)} > 100k$. When the feedback loop is short-circuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore, an additional comparator is active for feedback voltages at Pin 3 below 0.6V. Now an internal resistor of typically 1k is shunted to the impedance on the δ_{MAX} setting Pin 6. Depending on this impedance, δ will be reduced to a value δ_0. This will be discussed further.



a. Duty Cycle — δ — % Regulation



b. Pulse-Width Modulation

Figure 6

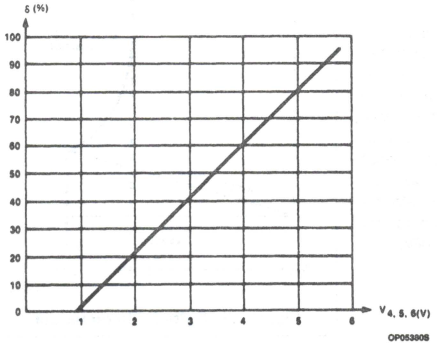


Figure 7. Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

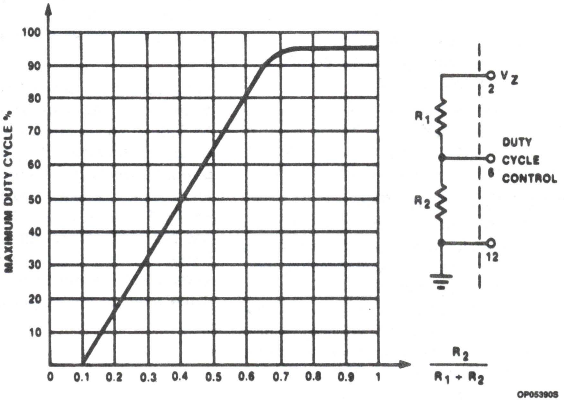


Figure 8. Graph for Determining δ_{MAX}

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 6, the PWM circuit in the NE5560 is a long-tailed pair in which the sawtooth on Pin 8 is compared with the LOWEST voltage on either Pin 4 (error amplifier), Pin 5, or Pin 6 (δ_{MAX} and slow-start). The transfer graph is given in Figure 7. The output of the PWM causes the resetting of the output bistable.

Limitation of the Maximum Duty Cycle

With Pins 5 and 6 not connected and with a rather low feedback voltage on Pin 3, the NE5560 will deliver output pulses with a duty cycle of ≈ 95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the maximum duty cycle is a must.

A DC voltage applied to Pin 6 (PWM input) will set δ_{MAX} at a value in accordance with Figure 7. For low tolerances of δ_{MAX}, this voltage on Pin 6 should be set with a resistor divider from V_Z (Pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider from V_Z, so forming a bridge configuration with the δ_{MAX} setting is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 8 can be used for determining the tap on the bleeder for a certain δ_{MAX} setting.

As already mentioned, Figure 9 gives a graphical representation of this. The value δo is limited to the lower and the higher side;

- It must be large enough to ensure that at maximum load and minimum input voltage the resulting feedback voltage on Pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop fault occurs. In practice, a value of 10 – 15% will be a good compromise.

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: Pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{MAX} information. This is necessary when the SMPS must have a real constant-current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components. When not used, Pin 5 should be tied to Pin 6.

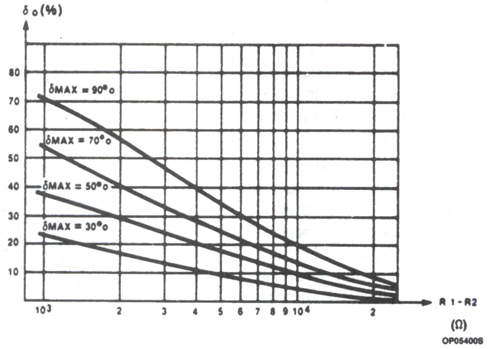


Figure 9. Soft-Start Minimum Duty Cycle vs $R_1 + R_2$

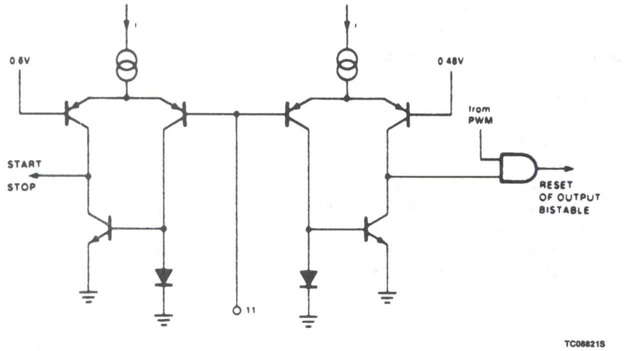


Figure 10. Current Protection Input

Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant-current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the NE5560 in an economical way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to Pin 11. As can be seen in Figure 10, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

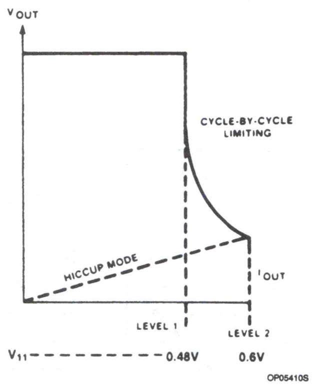


Figure 11. Output Characteristic

When activated, it will immediately reset the output flip-flop, so reducing the duty cycle. The effectiveness of this cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator activates the start-stop circuit and causes an immediate inhibit of the output pulses. After a certain deadtime, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 11.

The Start-Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead-time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode effectively limits the energy during fault conditions. The realization and the working of the circuit are indicated in Figures 12 and 13. The dead time and the soft-start are determined by an external capacitor that is connected to Pin 6 (δ_{MAX} setting).

An RS flip-flop can be set by three different functions:

1. Remote on/off on Pin 10.
2. Overcurrent protection on Pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the flip-flop, the output pulses are blocked via the output gate. In the same time transistor Q1 is forward-biased, resulting in a discharge of the capacitor on Pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q1. The voltage at Pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the flip-flop is reset. The output stage is no longer blocked and Q1 is cut off. Now V_Z will charge the capacitor via R1 to the normal δ_{MAX} voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty cycle of the output pulse now gradually increases to a value determined by the feedback on Pin 3, or by the static δ_{MAX} setting on Pin 6.

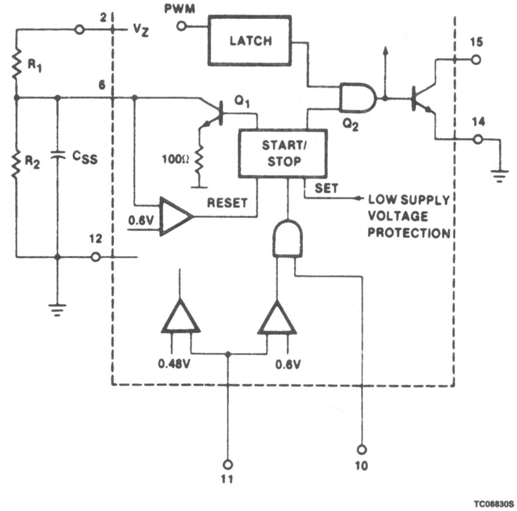


Figure 12. Start-Stop Circuit

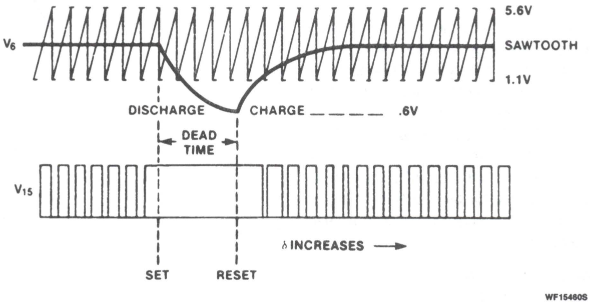


Figure 13. Start-Stop Circuit

Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on Pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage > 2V is applied. Start-up occurs via the slow-start circuit.

The Output Stage

The output stage of the NE5560 contains a flip-flop, a push-pull driven output transistor, and a gate, as indicated in Figure 14. The flip-flop is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected to respectively Pin 15 and Pin 14, allowing for normal or inverted output pulses. An internally-grounded emitter would cause untolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \cong 0.4V$. An internal clamping diode to the supply voltage protects the collector against overvoltages. The max. voltage at the emitter (Pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (Pin 13) operates also via this base.

Demagnetization Sense

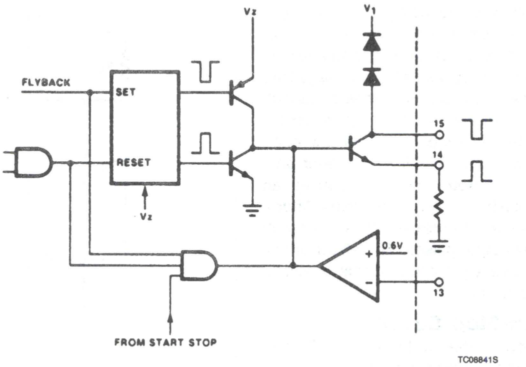
As indicated in Figure 14, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to Pin 13. A specific application for this function is to prevent saturation of forward-converter transformers. This is indicated in Figure 15.

Feed-Forward (Pin 16)

The basic formula for a forward converter is

$$V_{OUT} = \frac{dV_{IN}}{n} \quad \text{(n = transformer ratio)}$$

This means that in order to keep V_{OUT} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim 1/V_{IN}$ can ease the feedback-loop design.



NOTE:
The signal V_{13} can be derived from the demagnetizing winding in a forward converter as shown below.

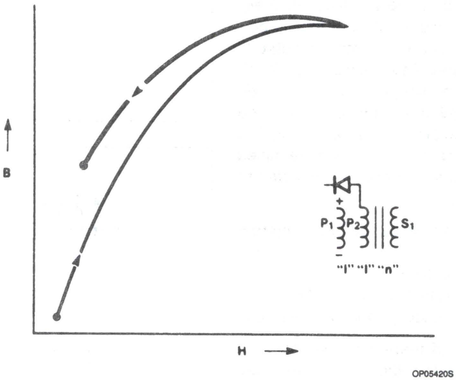


Figure 14. Output Stage

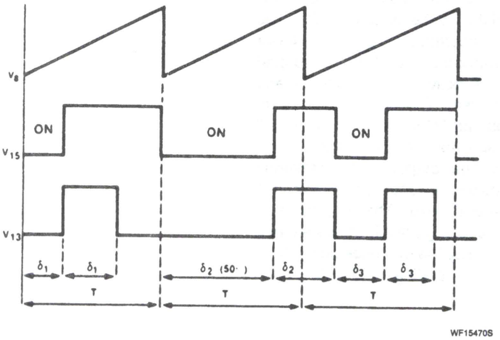


Figure 15. Output Stage Inhibit

This loop now only has to regulate for laod variations which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the max. inductance is determined by $\delta_{MAX} \times V_{IN}$ max. A regulation of $\delta_{MAX} \sim 1/V_{IN}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim 1/V_{IN}$ can be realized by using Pin 16 of the NE5560.

Figure 16 shows the electrical realization. When the voltage at Pin 16 exceeds the stabilized voltage V_Z (Pin 2), it will increase the charging current for the timing capacitor on Pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the δ_{MAX} voltage on Pin 6 remains constant because it is set via V_Z. Figure 17 visualizes the effect on δ_{MAX} and the normal operating duty cycle δ. For $V_{16} = 2 \times V_Z$, these duty cycles have halved. The graph for $\delta = f(V_{16})$ is given in Figure 18.

NOTE:
V_{16} must be less than Pin 1 voltage.

APPLICATIONS

NE/SE5560 Push-Pull Regulator

This application describes the use of the Signetics NE/SE5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 19 and 20.

Input voltage range is +12V to +18V for a nominal output of +30V and −30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed-forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation < 1% for an input range of +13V to +18V and load regulation to positive output of < 3% for $\Delta I_L(+)$ of 0.1 to 1A.

The main pulse-width modulator operates to 48kHz with power switching at 24kHz.

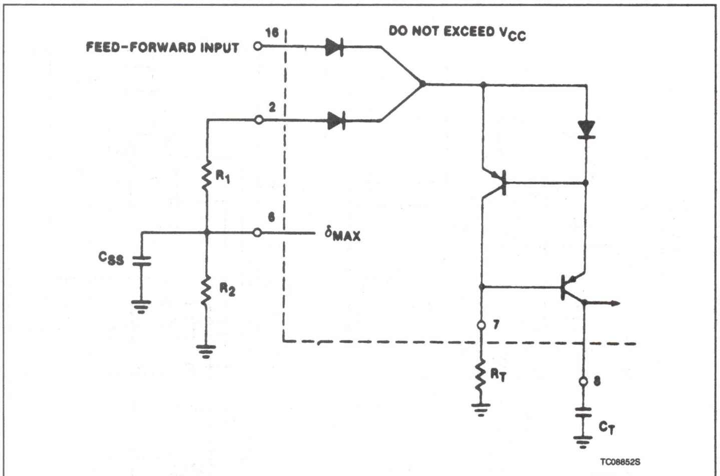


Figure 16. External δ Maximum Control

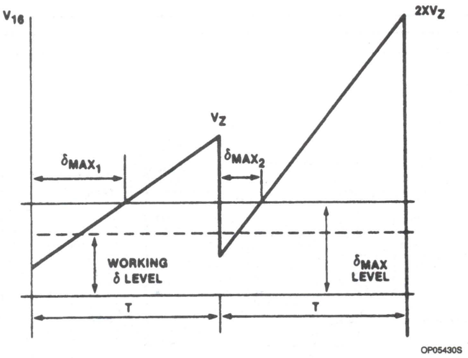


Figure 17. Feed-Forward Circuitry

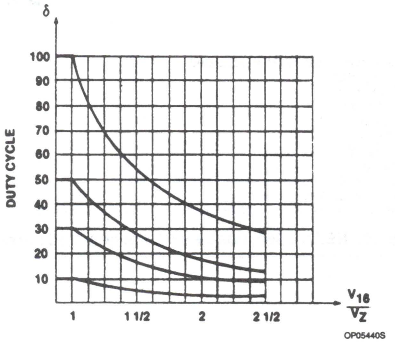
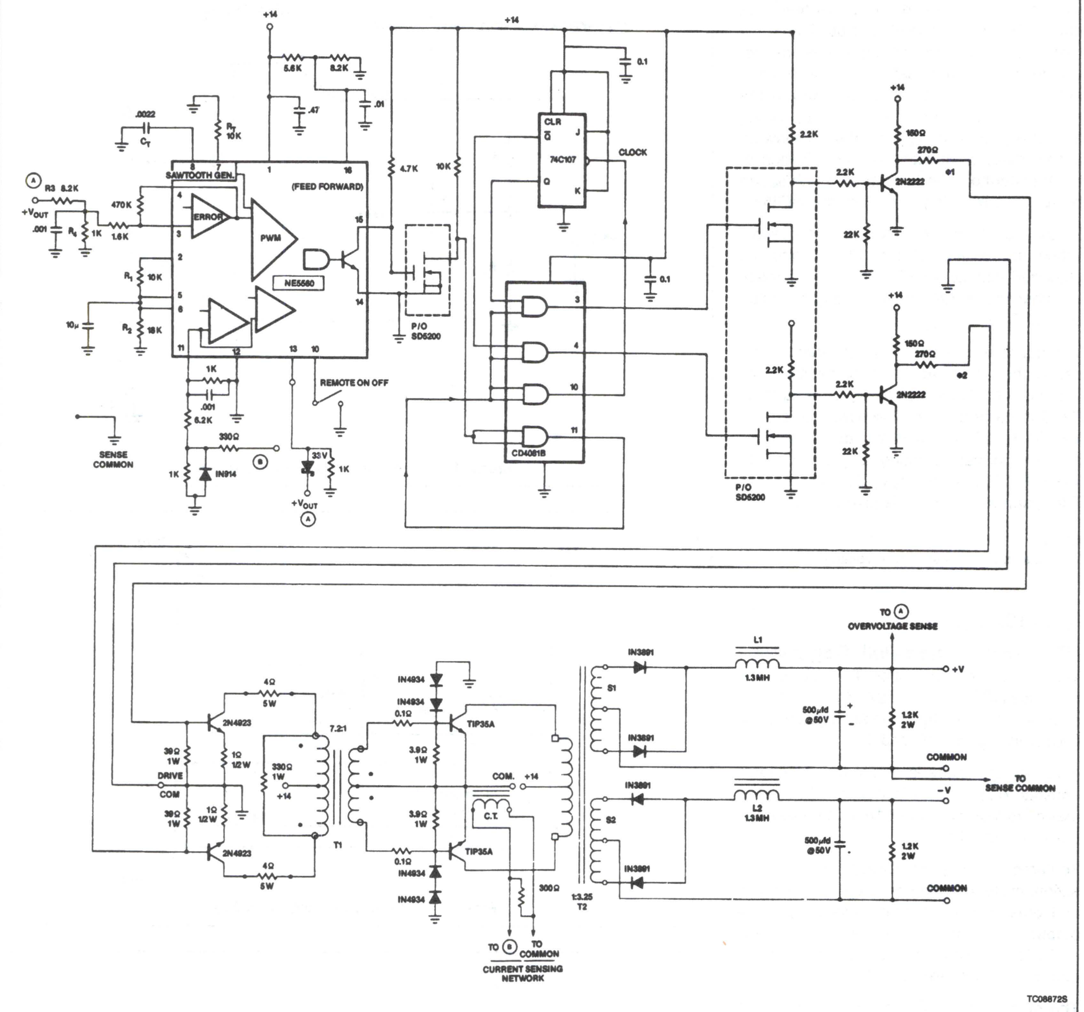
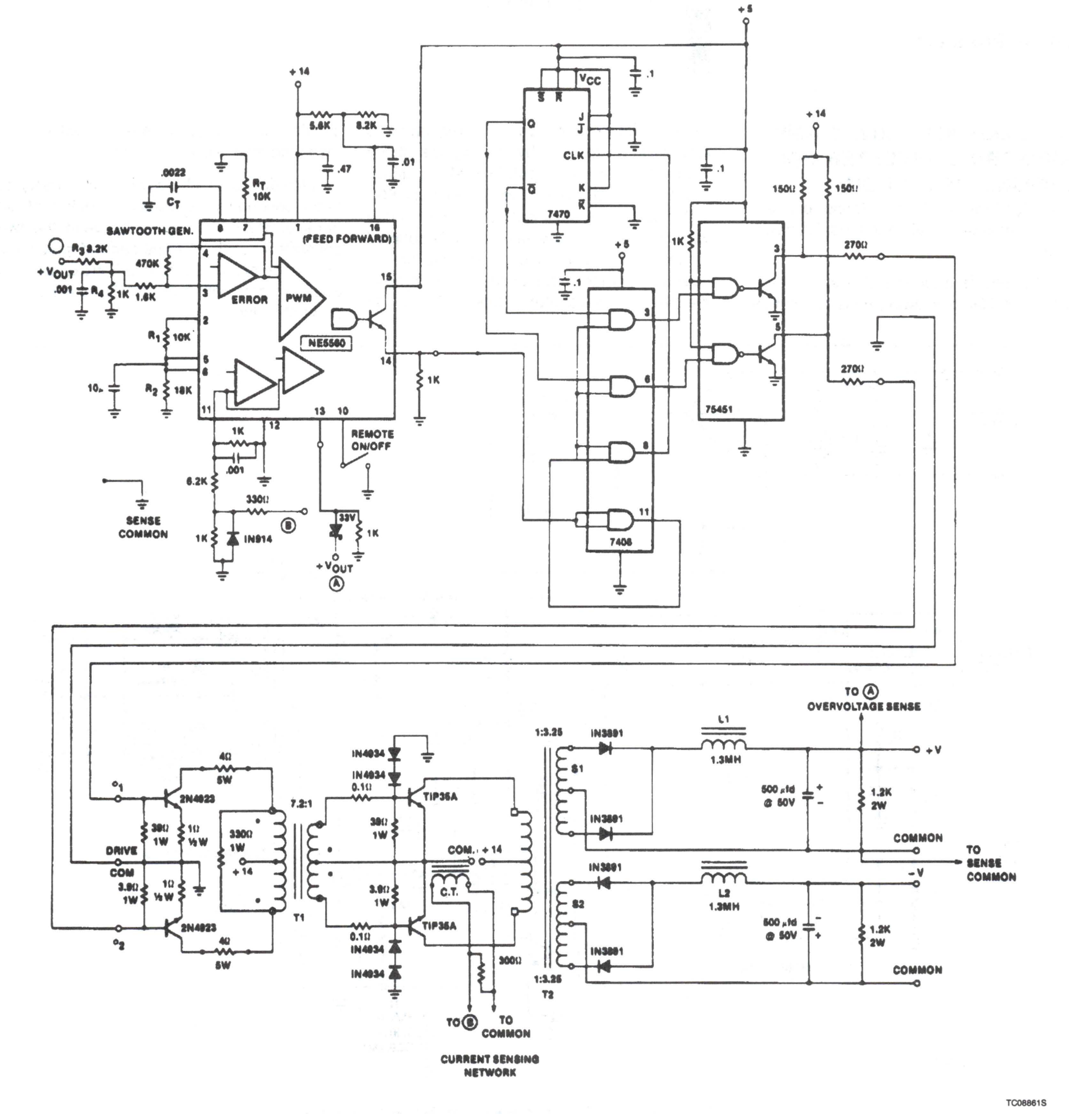


Figure 18. Feed-Forward Regulation


+14
5.6K
8.2K
.47
.01
.0022
C_T
R_T 10K
SAWTOOTH GEN.
(FEED FORWARD)
ERROR
PWM
NE5560
R3 8.2K
$+V_{OUT}$
470K
1K
1.6K
R_1 10K
R_2 18K
10μ
4.7K
10K
P/O SD5200
REMOTE ON OFF
1K
.001
6.2K
330Ω
IN914
33V
SENSE COMMON
CLR
$\overline{Q}$
J
K
Q
74C107
CLOCK
0.1
CD4081B
2.2K
22K
150Ω
270Ω
2N2222
Φ1
Φ2
TO A OVERVOLTAGE SENSE
L1 1.3MH
L2 1.3MH
IN3891
S1
S2
+V
-V
500μfd @50V
1.2K 2W
COMMON
TO SENSE COMMON
4Ω 5W
2N4923
39Ω 1W
1Ω 1/2W
DRIVE
COM
330Ω 1W
7.2:1
T1
IN4934
0.1Ω
3.9Ω 1W
TIP35A
COM. +14
C.T.
300Ω
1:3.25 T2
TO B
TO COMMON
CURRENT SENSING NETWORK
TC08872S

NOTES:
Power ground and signal ground must be kept separated
T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 19. NE/SE5560 Push-Pull Switched-Mode Regulated Supply With CMOS Drive Conversion Logic


+14
5.6K
8.2K
.47
.01
.0022
C_T
R_T 10K
SAWTOOTH GEN.
8 7 1 16
(FEED FORWARD)
R_3 8.2K
+V_{OUT}
470K
.001
R_4 1K
1.8K
4 3 2 5 6 11
ERROR
PWM
NE5560
15
14
1K
R_1 10K
10
R_2 18K
13 10 12
REMOTE ON/OFF
1K
.001
6.2K
330Ω
B
1K
IN914
SENSE COMMON
33V
1K
+V_{OUT}
A
+5
.1
V_{CC}
S R
Q
J
J
CLK
Q
K
K
7470
+5
.1
3 6 8 11
7406
+14
150Ω
150Ω
1K
3 5
270Ω
270Ω
75451
TO A
OVERVOLTAGE SENSE
L1
1.3MH
+V
1:3.25
IN3891
S1
IN3891
500 µfd @ 50V
1.2K 2W
COMMON
TO SENSE COMMON
IN3891
L2
1.3MH
−V
S2
IN3891
500 µfd @ 50V
1.2K 2W
COMMON
1:3.25
T2
4Ω 5W
o_1
2N4923
39Ω 1W
1Ω ½W
330Ω 1W
+14
DRIVE
COM
3.9Ω 1W
1Ω ½W
2N4923
o_2
4Ω 5W
7.2:1
T1
IN4934
IN4934
0.1Ω
TIP35A
39Ω 1W
COM. +14
3.9Ω 1W
C.T.
0.1Ω
TIP35A
IN4934
IN4934
300Ω
TO B
TO COMMON
CURRENT SENSING NETWORK
TC08861S

NOTES:

Power ground and signal ground must be kept separated

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 20. NE/SE5560 Push-Pull Switched-Mode Regulated Supply With TTL Drive Conversion Logic

Signetics

Linear Products

AN121
Forward Converter Application Using the NE5560

Application Note

DUAL OUTPUT ±50V, 1 AMP, FORWARD CONVERTER FOR OFF-LINE OPERATION

A straightforward 100W off-line converter, with transformer isolation to load, is shown in Figure 1.

The NE5560 is operated at a switching frequency of 75kHz allowing minimum magnetics and component size. Line regulation is also greatly improved by making use of Pin 16, the feed-forward input. Typical transformer design recommended is: T_1: Primary 60T #24, Secondary 20T #26 on a Ferroxcube #2616 (3C8) pot core wound tightly coupled for minimum leakage inductance and having adequate primary inductance for low droop in the base drive waveform. Base drive to Q2 should approach 0.5A peak for fast turn-on response and minimum losses.

T_2 provides 2.4:1 stepdown from primary to each secondary. A primary winding of 60 turns of #26 wire wound between the two secondaries with 25 turns each of #20 wire. The recommended core is a Ferroxcube-type 3622 pot core with a 25 mil (1/1000 in.) gap to prevent saturation.

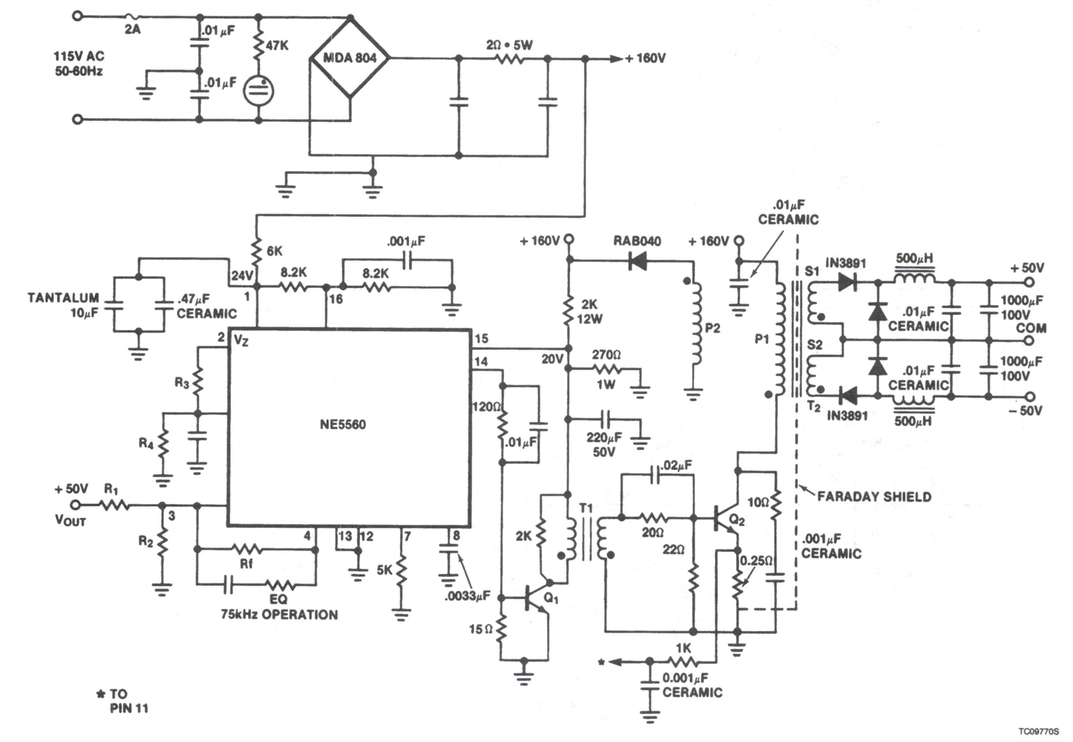

2A
.01µF
47K
115V AC
50-60Hz
.01µF
MDA 804
2Ω • 5W
+160V
.01µF
CERAMIC
+160V
RAB040
+160V
6K
.001µF
24V
8.2K
8.2K
TANTALUM
10µF
.47µF
CERAMIC
1
16
2
VZ
15
14
20V
2K
12W
270Ω
1W
P2
P1
S1
IN3891
500µH
+50V
.01µF
CERAMIC
1000µF
100V
COM
S2
.01µF
CERAMIC
1000µF
100V
T2
IN3891
500µH
−50V
R3
R4
NE5560
120Ω
.01µF
220µF
50V
.02µF
+50V
R1
VOUT
3
R2
4
13
12
7
8
Rf
EQ
75kHz OPERATION
5K
.0033µF
2K
T1
Q1
15Ω
20Ω
22Ω
Q2
10Ω
0.25Ω
FARADAY SHIELD
.001µF
CERAMIC
1K
0.001µF
CERAMIC
* TO
PIN 11
TC09770S

Figure 1. ±50V Feed-Forward Switched-Mode Converter

Signetics

AN122

NE5560 Push-Pull Regulator Applicator

Application Note

Linear Products

INTRODUCTION

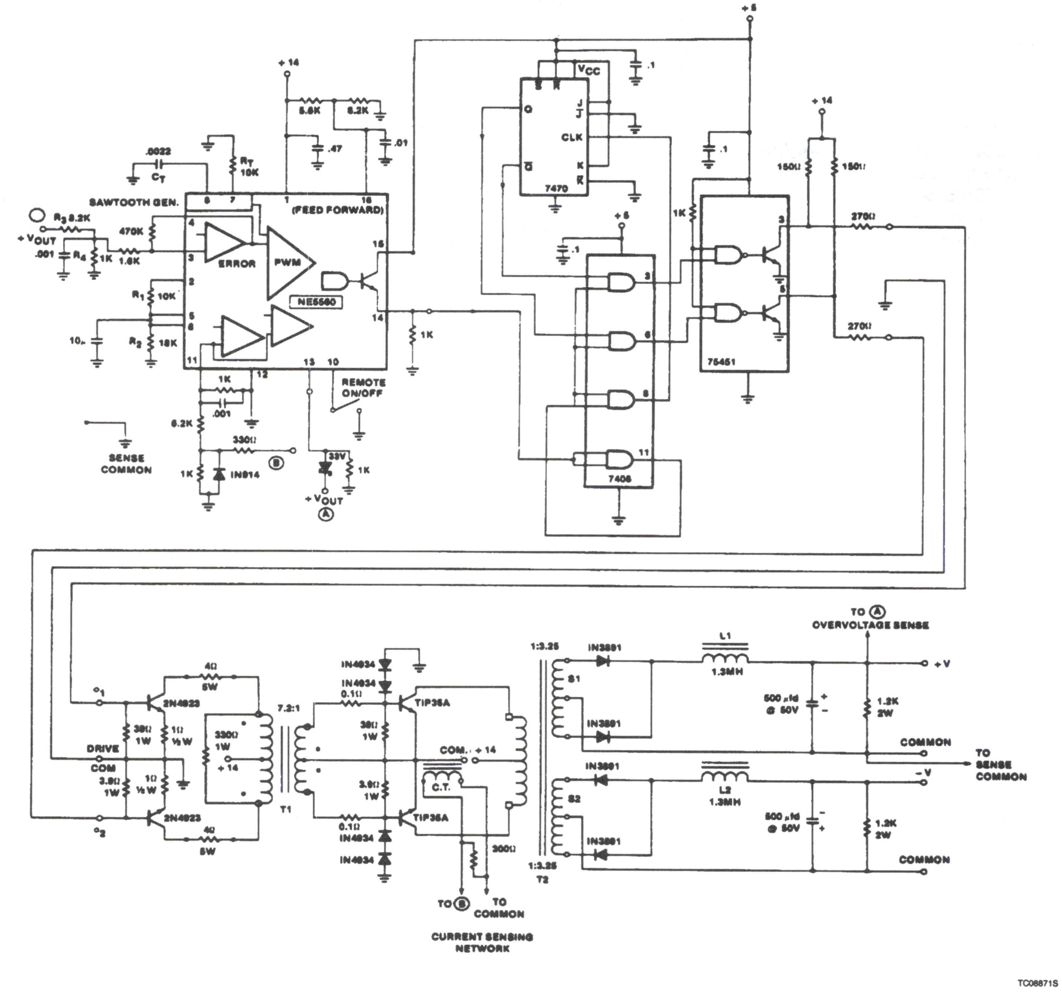
NE/SE5560 Push-Pull Regulator

This application describes the use of the Signetics NE/SE5560 adapted to function as a push-pull switched-mode regulator, as shown in Figures 1 and 2.

Input voltage range is +12 to +18V for a nominal output of +30 and −30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed-forward input compensation, cycle-by-cycle drive current protection and overvoltage sensing, line regulation (to positive output) < 1% for an input range of +13 to +18V and load regulation to positive output of < 3% for $\Delta I_L(+)$ of 0.1 to 1 Amp.

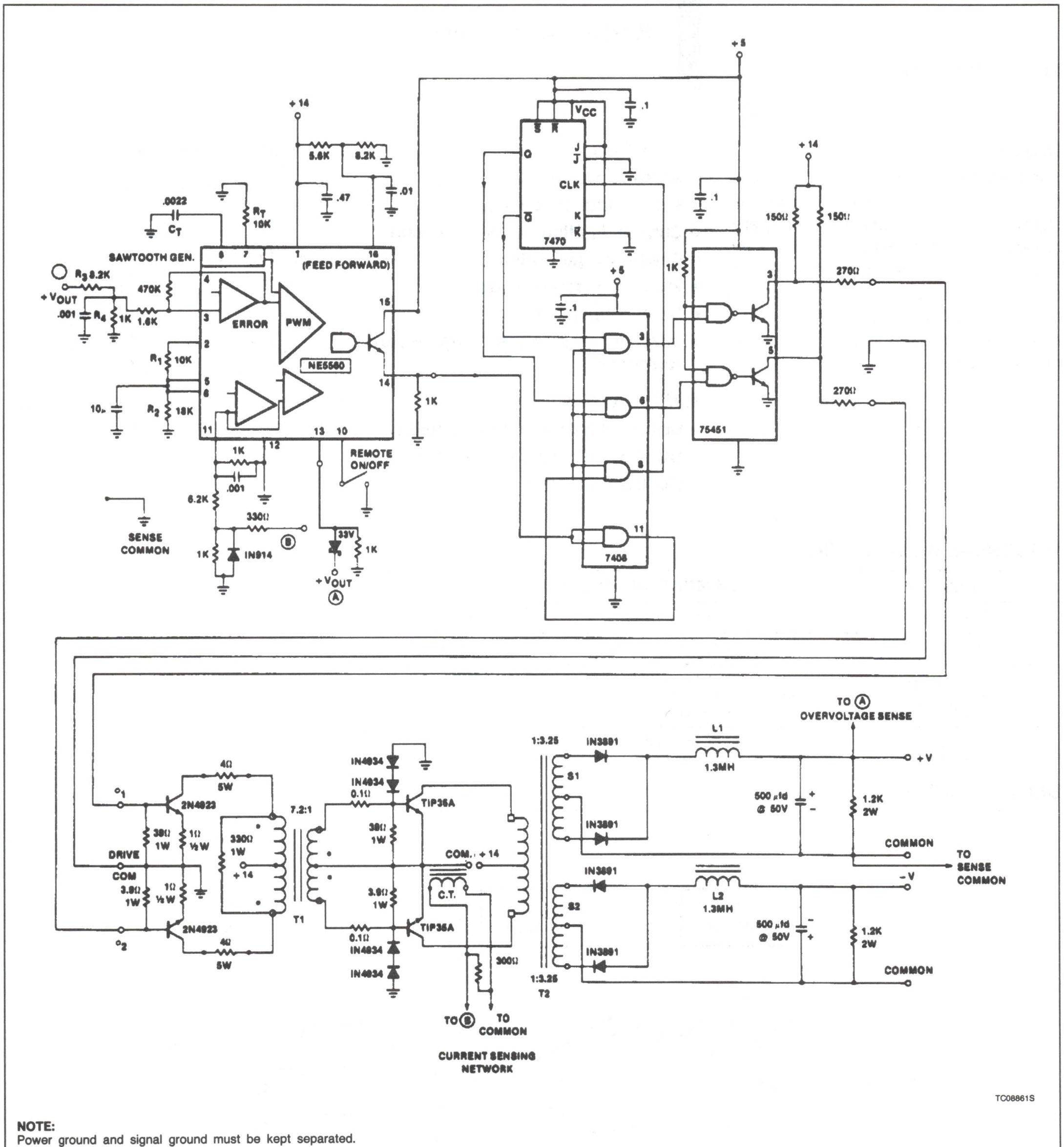
The main pulse-width modulator operates to 48kHz with power switching at 24kHz.


+14
5.6K
8.2K
.47
.01
.0022
C_T
R_T 10K
SAWTOOTH GEN.
6
7
1
16
(FEED FORWARD)
R_3 8.2K
+V_{OUT}
.001
R_4
1K
1.6K
470K
4
3
ERROR
PWM
15
2
R_1 10K
5
6
10μ
R_2 18K
NE5560
14
1K
11
12
13
10
REMOTE ON/OFF
1K
.001
6.2K
330Ω
Ⓑ
1K
IN914
SENSE COMMON
33V
1K
+V_{OUT}
Ⓐ
+5
.1
V_{CC}
S
R
Q
J
J
CLK
K
K
Q
7470
+5
.1
3
6
8
11
7408
+14
.1
1K
150Ω
150Ω
3
5
270Ω
270Ω
75451
TO Ⓐ OVERVOLTAGE SENSE
1:3.25
IN3891
S1
IN3891
L1
1.3MH
+V
500 μfd @ 50V
1.2K 2W
COMMON
TO SENSE COMMON
IN3891
–V
S2
L2
1.3MH
IN3891
500 μfd @ 50V
1.2K 2W
COMMON
1:3.25
T2
$○_1$
2N4923
4Ω 5W
38Ω 1W
1Ω ½W
DRIVE
COM
3.9Ω 1W
1Ω ½W
330Ω 1W
+14
$○_2$
2N4923
4Ω 5W
7.2:1
T1
IN4934
IN4934
0.1Ω
TIP35A
38Ω 1W
COM. +14
C.T.
3.9Ω 1W
0.1Ω
TIP35A
IN4934
IN4934
300Ω
TO Ⓑ
TO COMMON
CURRENT SENSING NETWORK
TC08871S

NOTE:
Power ground and signal ground must be kept separated.

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T_2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material

Figure 1. NE/SE5560 Push-Pull Switched-Mode Regulated Supply With CMOS Drive Conversion Logic


+5
+14
5.6K
8.2K
.47
.01
.0022
C_T
R_T 10K
SAWTOOTH GEN.
(FEED FORWARD)
R_3 8.2K
470K
$+V_{OUT}$
.001
R_4
1K
1.6K
ERROR
PWM
NE5560
R_1 10K
R_2 18K
10μ
1K
13 10
12
REMOTE ON/OFF
.001
6.2K
330Ω
Ⓑ
33V
1K
IN914
SENSE COMMON
$+V_{OUT}$ Ⓐ
V_{CC}
S R
Q
$\bar{Q}$
J
K
CLK
7470
.1
7408
75451
150Ω
270Ω
1K
o_1
o_2
DRIVE
COM
4Ω 5W
2N4923
39Ω 1W
1Ω ½W
330Ω 1W
3.9Ω 1W
+14
7.2:1
T1
IN4934
0.1Ω
TIP35A
COM. +14
C.T.
300Ω
TO Ⓑ
TO COMMON
CURRENT SENSING NETWORK
1:3.25
T2
S1
S2
IN3891
L1
L2
1.3MH
500 μfd @ 50V
1.2K 2W
+V
−V
COMMON
TO Ⓐ OVERVOLTAGE SENSE
TO SENSE COMMON
TC08861S

NOTE:
Power ground and signal ground must be kept separated.

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T_2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material

Figure 2. NE/SE5560 Push-Pull Switched-Mode Regulated Supply With TTL Drive Conversion Logic

Signetics

NE/SE5561

Switched-Mode Power Supply Control Circuit

Product Specification

Linear Products

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched-mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, overcurrent sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

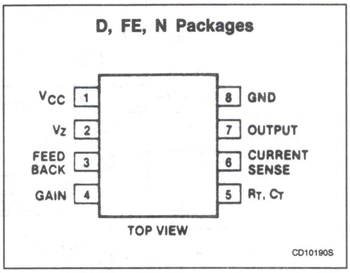
FEATURES

- **Micro-miniature (D) package**
- **Pulse-width modulator**
- **Current limiting (cycle-by-cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature-compensated reference**

APPLICATIONS

- **Switched-mode power supplies**
- **DC motor controller inverter**
- **DC/DC converter**

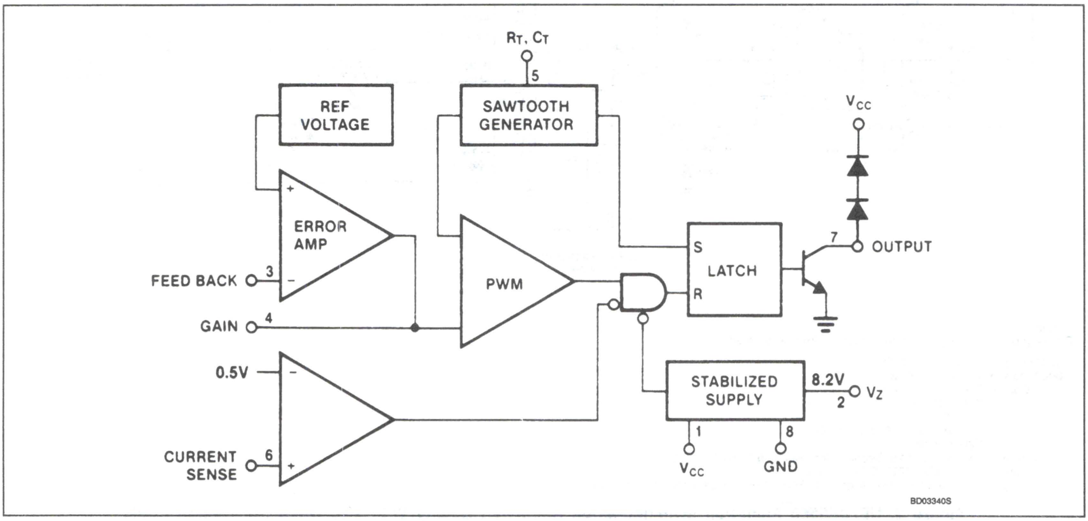
PIN CONFIGURATION


D, FE, N Packages
VCC 1
VZ 2
FEED BACK 3
GAIN 4
8 GND
7 OUTPUT
6 CURRENT SENSE
5 RT, CT
TOP VIEW
CD10190S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5561N
8-Pin Plastic DIP	-55 to +125°C	SE5561N
8-Pin Cerdip	0 to +70°C	NE5561FE
8-Pin Cerdip	-55 to +125°C	SE5561FE
8-Pin SO	0 to +70°C	NE5561D

BLOCK DIAGRAM


RT, CT
5
REF VOLTAGE
SAWTOOTH GENERATOR
VCC
ERROR AMP
+
−
PWM
S
LATCH
R
7
OUTPUT
FEED BACK 3
GAIN 4
0.5V
CURRENT SENSE 6
STABILIZED SUPPLY
8.2V
2
VZ
1
8
VCC
GND
BD03340S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply[1] Voltage-forced mode Current-fed mode	 +18 30	 V mA
 I_{OUT} V_{OUT}	Output transistor (at 20-30V max) Output current Output voltage Output duty cycle	 40 V_{CC} + 1.4V 98	 mA V %
P_D	Maximum total power dissipation	0.75	W
T_A	Operating temperature range SE5561 NE5561	 −55 to +125 0 to 70	 °C °C

NOTE:

1. See Voltage-Current-fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 12V$, $T_A = 25°C$, unless otherwise specified.

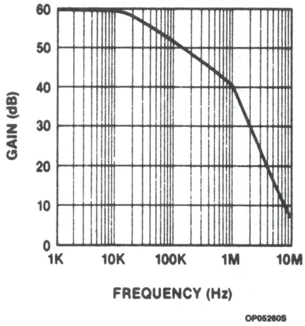
SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference section										
V_{REF}	Internal ref voltage	$T_A = 25°C$		3.69	3.75	3.84	3.57	3.75	3.96	V
		Over temperature		3.65		3.88	3.55		3.98	V
V_Z	Internal zener ref	$^*I_L = 7mA$		7.8	8.2	8.8	7.8	8.2	8.8	V
	Temp. coefficient of V_{REF}				±100			±100		ppm°C
	Temp. coefficient of V_Z				±200			±200		ppm/°C
Oscillator section										
	Frequency range	Over temperature		50		100k	50		100k	Hz
	Initial accuracy				12			12		%
	Duty cycle range	$f_O = 20kHz$		0		98	0		98	%
Current limiting										
I_{IN}	Input current	Pin 6 = 250mV	$T_A = 25°C$		−2	−10		−2	−10	μA
			Over temp.			−20			−20	μA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	$I_{OUT} = 20mA$		0.88	1.10		0.88	1.10	μs
			$I_{OUT} = 40mA$		0.7	0.8		0.7	0.8	μs
	Current limit trip level			.400	.500	.600	.400	.500	.600	V
Error amplifier										
	Open-loop gain				60			60		dB
	Feedback resistor			10k			10k			Ω
BW	Small-signal bandwidth				3			3		MHz
V_{OH}	Output voltage swing			6.2			6.2			V
V_{OL}	Output voltage swing					0.7			0.7	V
Output stage										
I_{OUT}	Output current	Over temperature		20			20			mA
V_{CE}	Sat	$I_C = 20mA$, Over temp.				0.4			0.4	V

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 12V$, $T_A = 25°C$, unless otherwise specified.

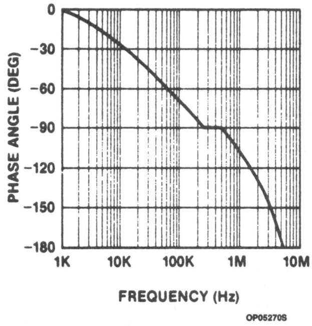
SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Supply voltage/current										
I_{CC}	Supply current	$I_Z = 0$, voltage-forced	$T_A = 25°C$			10.0			10.0	mA
			Over temp.			13.0			13.0	mA
V_{CC}	Supply voltage	$I_{CC} = 10mA$, current-fed		20.0	21.0	22.0	19.0	21.0	24.0	V
		$I_{CC} = 30mA$ current		20.0		30.0	20.0		30.0	V
Low supply protection										
	Pin 1 threshold			8	9	10.5	8	9	10.5	V

TYPICAL PERFORMANCE CHARACTERISTICS

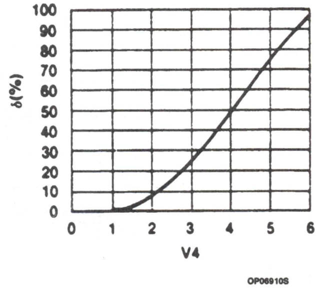
Error Amplifier Open-Loop Gain



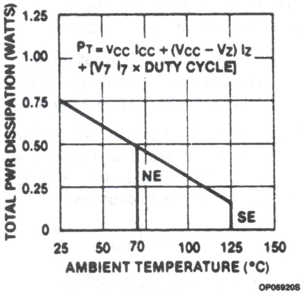
Error Amplifier Open-Loop Phase



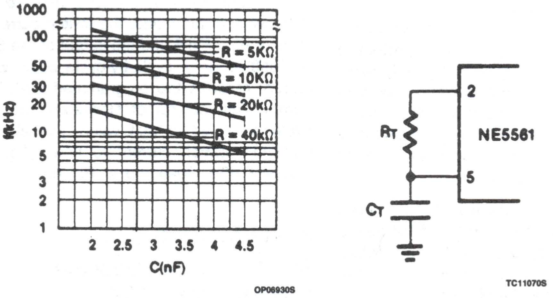
Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage



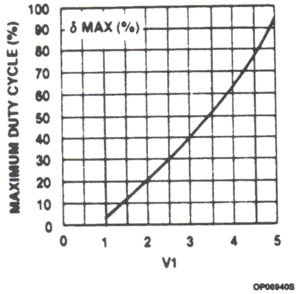
Power Derating Curve



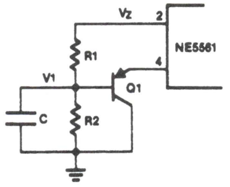
Typical Frequency Plot vs R_T and C_T



Maximum Duty Cycle vs Base Voltage on Q1



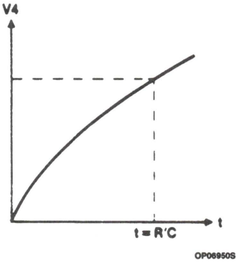
Start-Up Circuit



δ max is a function of f $\left[\frac{R2}{R1+R2} V_Z + V_{BE\,Q1}\right]$

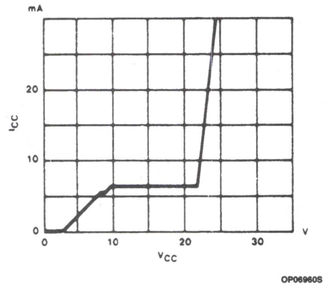
TC11080S

Slow-Start Voltage

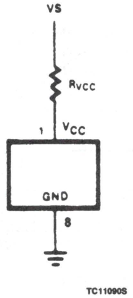


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE5561 Voltage-Current-Fed Supply Characteristics



Current-Fed Dropping Resistor



$$R_{VCC} = \frac{V_S - V_{CC}}{(10 \text{ to } 20\text{mA})}$$

NOTE:
See DC Electrical Characteristics for Current Fed V_{CC} Range.

NE5561 Start-Up

The start-up, or initial turn-on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum ($\delta > 90\%$). Either overcurrent limit or slow-start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used, if desired.

To implement slow-start, the start-up circuit can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp-up slowly when power is applied, causing the duty cycle to ramp-up simultaneously.

Overcurrent limit may be used also. To limit duty cycle in this mode, the switch current is monitored at Pin 6 and the output of the 5561 is disabled on a cycle-by-cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value, just allowing maximum switch current to flow. (Approximately 0.50V measured at Pin 6.)

APPLICATIONS

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor.

Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{MAX} circuit is required, as evidenced by Q1. The δ_{MAX} limit may be calculated by using the relationship:

$$\frac{R2}{R1 + R2}(8.2V) = V\delta_{MAX}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, with R1 and R2 being defined from the desired conditions.

Signetics

AN123
NE5561 Applications

Application Note

Linear Products

INTRODUCTION

5V, 0.5A Buck Regulator Operates From 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor. Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{MAX} circuit is required, as evidenced by Q1. The δ_{MAX} limit may be calculated by using the relationship.

$$\frac{R2}{R1 + R2}(8.2V) = V\delta_{MAX}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, and R1, R2 are defined from the desired conditions. (See Figure 2.)

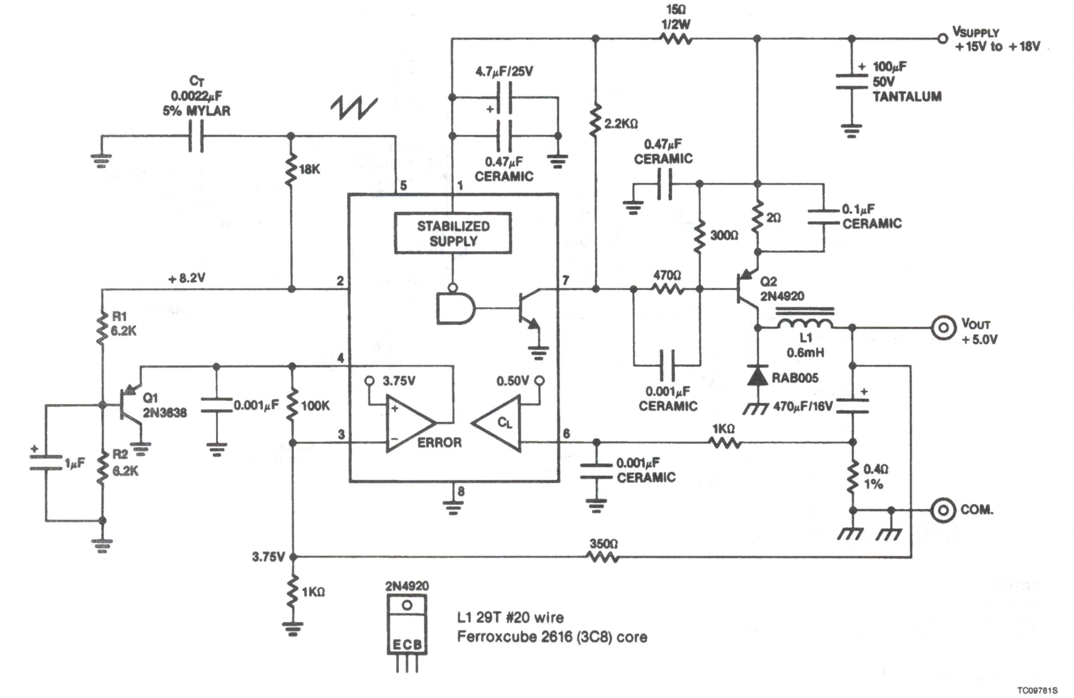
NE5561 Boost Converter With Output Variable (18V to 30V, 0.2A)

The circuit shown uses the NE5561 SMPS controller in a non-isolated boost converter operating from a 15V line. The addition of three transistors and one diode is necessary to complete the design (see Figure 3).

Operation is as follows. Q1 is a combination slow start and max duty cycle limit transistor. When power is first applied to the circuit, C7 in a discharged state begins to charge toward the divider voltage, V_δ. This $V_\delta + V_{BE}$ controls the voltage on Pin 4, the error amp output, causing the duty cycle to be limited initially to δ_0, then to gradually approach its normal operating range, δ. The base divider is fed from V_Z, which is nominally 8.2V.

Output regulation starts at the error amplifier, with gain set by R2 (adj) and R5 combination. The error amp is stable for closed loop gain in excess of 40dB (×100), for which the regulation will be approximately 1%. C4 is added to the output to insure stability at gain below 40dB. C4 creates a dominant pole at approximately 1kHz, descending at 6dB per octave to unity near 1MHz. Input to the error amplifier is referenced to 3.75V and must reach this reference level for the output of the NE5561 to be active. Output voltage is then the quantity 3.75V times the divider ratio from V_{OUT} to Pin 3 as set by R2.

If the ratio is, for instance, 10:1, the output will be ≃ 37V. If the ratio is 5:1, the output will be ≃ 18.5V, etc.



15Ω
1/2W
VSUPPLY
+15V to +18V
4.7µF/25V
+
100µF
50V
TANTALUM
CT
0.0022µF
5% MYLAR
2.2KΩ
0.47µF
CERAMIC
18K
0.47µF
CERAMIC
5
1
2Ω
0.1µF
CERAMIC
STABILIZED
SUPPLY
300Ω
+8.2V
2
7
470Ω
Q2
2N4920
R1
6.2K
L1
0.6mH
VOUT
+5.0V
4
3.75V
0.50V
RAB005
Q1
2N3638
0.001µF
100K
ERROR
CL
0.001µF
CERAMIC
470µF/16V
3
6
1KΩ
1µF
R2
6.2K
8
0.001µF
CERAMIC
0.4Ω
1%
COM.
3.75V
350Ω
1KΩ
2N4920
ECB
L1 29T #20 wire
Ferroxcube 2616 (3C8) core
TC09781S

Figure 1. NE5561 5V/0.5A Buck Converter

NE5561 Applications

AN123

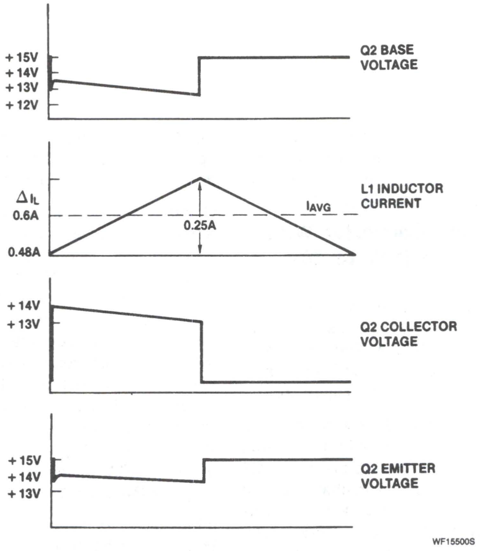
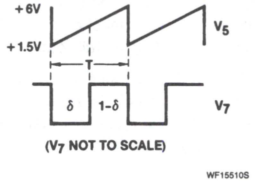
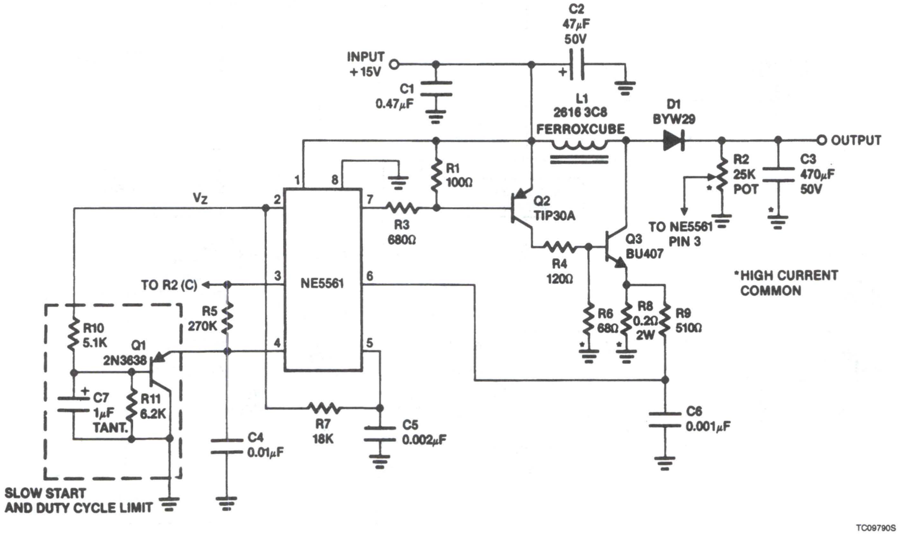


Figure 2. Typical Buck Converter Waveforms

Output to Q2 base is a square wave of variable duty cycle as determined by load demand. The internal transistor is open-collector and must have a pull-up resistance; in this application the base circuit of Q2. The duty cycle δ is a fraction between 0 and 1. The actual on time is proportional then to δ × T, where T is the period of the free-running frequency of the sawtooth generator internal to the NE5561. Frequency is set by the RC combination, R7 × C5 with charging current supplied from V_Z (8.2V). The stabilizing effect of the internal zener supply gives a constant frequency. The sawtooth waveform is related to duty cycle as shown below.




C2
47μF
50V
INPUT
+15V
C1
0.47μF
L1
2616 3C8
FERROXCUBE
D1
BYW29
OUTPUT
R1
100Ω
R2
25K
POT
C3
470μF
50V
V_Z
1
8
2
7
R3
680Ω
Q2
TIP30A
TO NE5561 PIN 3
Q3
BU407
R4
120Ω
*HIGH CURRENT COMMON
TO R2 (C)
3
NE5561
6
R5
270K
R10
5.1K
Q1
2N3638
4
5
R6
68Ω
R8
0.2Ω
2W
R9
510Ω
C7
1μF
TANT.
R11
6.2K
R7
18K
C5
0.002μF
C4
0.01μF
C6
0.001μF
SLOW START AND DUTY CYCLE LIMIT
TC09790S

NOTES:
C5 is the timing capacitor
L1 is Ferroxcube 2616
3C8 with 14 turns of #18 enameled wire (0.14 mH)

$$\delta f_{MAX} \text{ is a function of } f\left[\frac{R11}{R10+R11}(V_Z)+V_{BE}\right]$$

Figure 3. DC-to-DC SMPS Using NE5561 Variable 18V to 30V Out at 0.2A

Q3 is switched on during the saturated portion of the output waveform from Pin 7 of the NE5561, termed δ, and is switched off during the remainder of the cycle (1 – δ).

The sawtooth frequency is set at approximately 22kHz in this example. The NE5561 is capable of operation to 100kHz, however.

Pin 6 of the NE5561 operates an overcurrent protective feature which resets the output on Pin 7 if the instantaneous Pin 6 voltage exceeds 0.50V. In this case, R8 determines the peak current of Q3 emitter circuit prior to shutdown. The operation of the overcurrent circuit is on a pulse-to-pulse basis, returning to normal as soon as the Pin 6 voltage falls below 0.50V. As is noted, a small degree of filtering is needed to eliminate short switching transient, allowing only the primary current wave form to be sensed.

Switching circuit operation proceeds as follows. Q3 turns on, causing magnetization current to begin increasing in L1, the switching indicator. After initial start-up, C3 is charged to the output, thus with Q3 on, Diode D1 is reverse-biased and does not conduct during the duty cycle, δ. C3, the output capacitor, sustains the full load current during this part of the cycle. When Q3 turns off, the magnetic field energy previously stored in L1 is discharged through D1, which is now forward-biased. The output capacitor is incrementally charged, restoring its depleted voltage. The ripple voltage is a function of the size of C3 and its internal resistance. For minimum ripple, a low ESR (Equivalent Series Resistance) capacitor must be used, since previously-mentioned peak load current flows in C3.

Single Transistor 100V, 250mA Buck Converter (Off-Line)

With a single 15V zener diode to limit package dissipation, the NE5561 controller may be operated directly from the rectified AC line. The following example shows the simplicity of such a converter which is capable of a nominal 100V output (see Figure 5). A base drive transformer is used to gain high voltage isolation between the NE5561 and the switching transistor, and to provide adequate base drive. A low power PNP transistor is used in an auxiliary slow-start and duty cycle limiting circuit to prevent over-excitation (Q1).

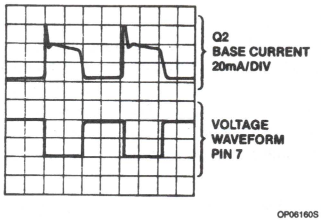


Figure 4. Switching Waveforms

Operation is as follows. Drive from the NE5561 output is fed to the primary of T1, base drive transformer, with a pulse-width modulated signal causing Q2 (BU407) to switch current to inductor, L1. As the current

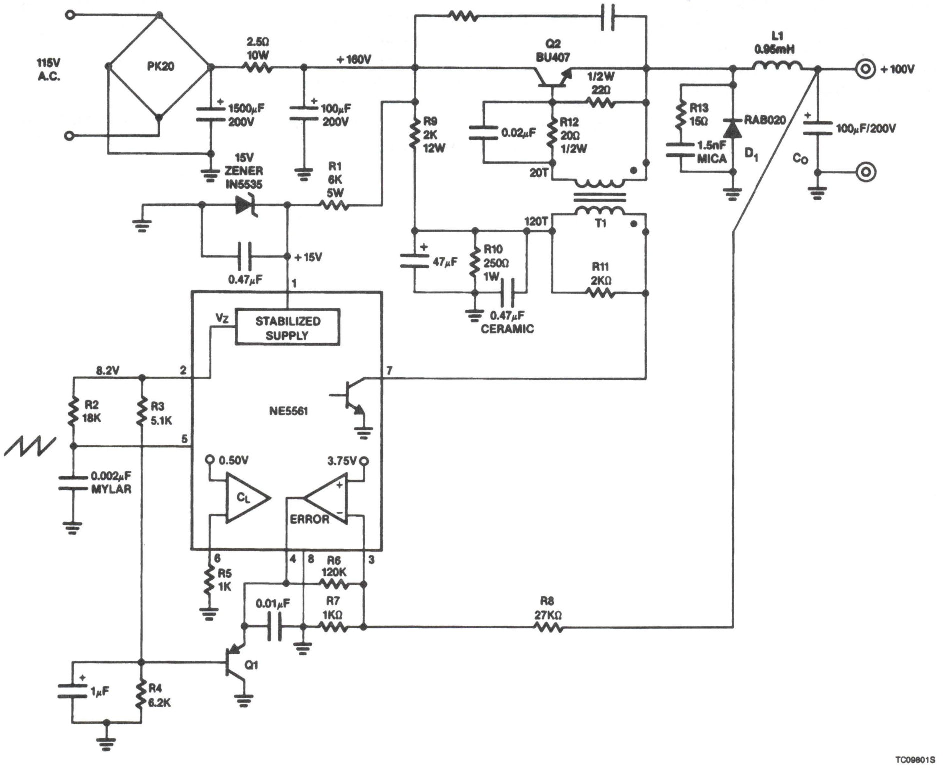

115V
A.C.
PK20
2.5Ω
10W
+160V
1500µF
200V
100µF
200V
15V
ZENER
IN5535
R1
6K
5W
0.47µF
+15V
1
Vz
STABILIZED
SUPPLY
NE5561
8.2V
2
R2
18K
R3
5.1K
5
0.002µF
MYLAR
0.50V
CL
3.75V
ERROR
7
6
R5
1K
4
8
R6
120K
3
0.01µF
R7
1KΩ
R8
27KΩ
Q1
1µF
R4
6.2K
Q2
BU407
1/2W
22Ω
R9
2K
12W
0.02µF
R12
20Ω
1/2W
20T
120T
T1
47µF
R10
250Ω
1W
0.47µF
CERAMIC
R11
2KΩ
L1
0.95mH
+100V
R13
15Ω
1.5nF
MICA
RAB020
D1
100µF/200V
CO
TC09801S

Figure 5. NE5561 100V/0.25A Switched-Mode Converter

builds up, energy is stored in L1, coincident with the saturation period (δ) of the NE5561 output stage. During this period, current also flows through L1 to C_O and the load. When Q2 cuts off, the choke field collapses and D1 conducts as the load is sustained by the inductor-stored energy.

V_{OUT} is sampled by the divider R7 and R8, rising until the junction of the divider is forced to 3.75V. Load variations are thus translated to duty cycle variations to maintain constant voltage at the output. The measured efficiency at 0.5A load is in excess of 72%. Line regulation is good from approximately 93V to 120V.

The base current waveform driving Q2 is shown in Figure 4. This indicates that the BU407 base current rises initially to 60mA to obtain fast turn-on, then settles to about 40mA for the remainder of the duty cycle, δ. Reverse-biasing of the emitter-base junction occurs to enhance turn-off.

Snubber networks are necessary, as shown across Q2 and commutation diode D1, to prevent component failure during fast switching. It is critical that these networks be placed physically adjacent to the respective components they protect, and that low inductance capacitors and resistors be used as snubbers (ceramic or dura mica caps and carbon resistors).

The base drive transformer is constructed using a Ferroxcube 2616-3C8 core, with primary of 120 turns of #26 wire, and 20 turns of #26 on secondary. The primary is wound in a simple solenoidal manner, first on the bobbin, followed by a layer of mylar tape to provide voltage isolation. Next, the secondary winding is added. Primary inductance measures 45mH with a leakage inductance of 120μH. It is important to have sufficient primary inductance to prevent excessive droop in base drive current. Also, leakage reactance must be kept reasonably low to minimize ringing.

DC Motor Drive with Fixed Speed Control

The circuit shown in Figure 7 incorporates a simple switched-mode approach to DC motor control, which is efficient and free of the dissipation problems inherent in linear drives. The NE5561 provides pulse-proportional drive and speed control based on DC tachometer feedback. A simple switching circuit consisting of one transistor (2N4920 PNP) and a commutation diode is used to deliver programmed pulse energy to the motor.

A frequency of approximately 20kHz is used to eliminate audio noise present in some switching drives. The DC tach in this example delivers 2.7V/1000 RPM. Its output is such that negative feedback occurs when this voltage is applied to the error amplifier of the NE5561, Pin 3, through a suitable divider. Note that the voltage to Pin 3 must be 3.75V in order to obtain servo lock. Thus, the divider from the tach output must be appropriate to maintain the proper ratio for speed control to occur.

As shown in the waveform pattern (Figure 6), duty cycle varies directly with load torque demand. No load current is ≃ 0.3A and full load is 0.6A. Current and voltage waveforms at 0.6A are shown in Figure 6. If desired, torque limiting may be set by feeding a derivative of motor return current back to Pin 6 of the NE5561.

Operating range is 12V to 18V input for a tach output nominal variation of less than 20mV, and approximately 4.35V for the divider values shown. The motor is a Globe 100A 565 rated at $12V_{DC}$.

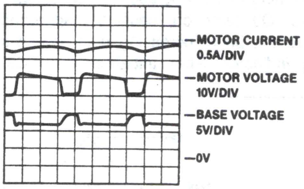


Figure 6. Switching Waveforms

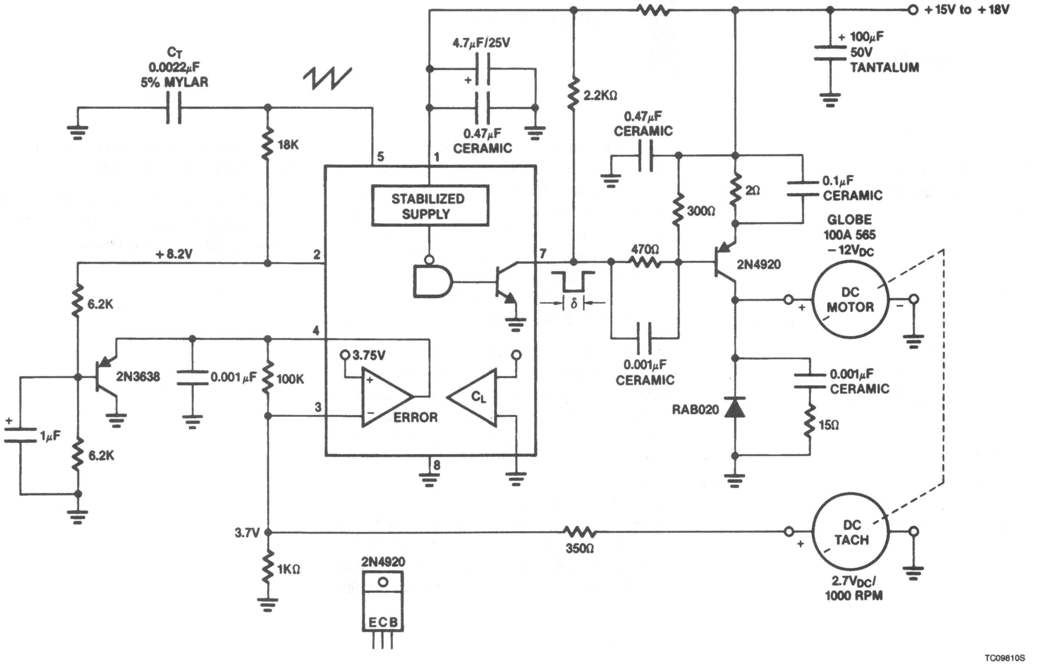

+15V to +18V
+ 100µF
50V
TANTALUM
4.7µF/25V
+
0.47µF
CERAMIC
C_T
0.0022µF
5% MYLAR
18K
2.2KΩ
0.47µF
CERAMIC
5
1
STABILIZED
SUPPLY
300Ω
2Ω
0.1µF
CERAMIC
GLOBE
100A 565
−12V_{DC}
+8.2V
2
7
470Ω
2N4920
DC
MOTOR
+
−
δ
6.2K
4
3.75V
+
2N3638
0.001µF
100K
C_L
0.001µF
CERAMIC
0.001µF
CERAMIC
3
−
ERROR
RAB020
15Ω
+
1µF
6.2K
8
3.7V
350Ω
DC
TACH
+
1KΩ
2N4920
ECB
2.7V_{DC}/
1000 RPM
TC09810S

Figure 7. NE5561 Pulse-Width Modulated Motor Drive (Constant Speed)

Signetics

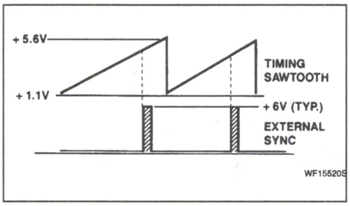
Linear Products

AN124

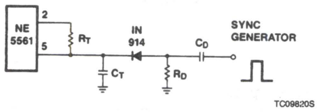
External Synchronization for the NE5561

Application Note

Synchronization of the 5561 can be accomplished by forcing the timing pin (Pin 5) above the 5.6V sawtooth limit comparator for a short time.



This can be accomplished with a simple diode-coupled narrow pulse source with fairly low source impedance:



A drawback to this approach is that when the 5.6V threshold is reached, a discharge transistor is turned on to quickly pull the timing capacitor to ground and will also attempt to pull the pulse generator to ground. This condition can be avoided by keeping the pulse width very narrow (0.1μs) or by placing a differentiator network between the pulse generator and the diode.

The differentiator will now produce a positive-going spike with the positive edge of the sync pulse, resetting the sawtooth without passing too much current through the discharge transistor. The negative spike produced by the falling edge of the clock will be blocked by the diode and will have no effect on the sawtooth ramp. A narrow sync pulse is no longer necessary while a sharp-*edged* pulse is. The value of C_D should be sufficient to ensure that a 10V pulse will drive the capacitor, C_T, high enough to trip the 5.6V comparator according to:

$$C_T \Delta V_{CT} = C_D(\Delta V_{CT} - V_D)$$

This relates the magnitude of the spike to the size of the pulse. Also assume $R_D C_D < 1\mu s$.

The free-running frequency of the slaved 5561 should be slightly lower than the sync frequency for proper operation.

Signetics

Linear Products

NE/SE5562

Switched-Mode Power Supply Control Circuit

Product Specification

DESCRIPTION

The NE/SE5562 is a single-output control circuit for switched-mode power supplies. This single monolithic IC contains all control and protection features needed for full-featured switched-mode power supplies.

The 100mA source/sink output is designed to drive power FETs directly. The associated output logic is designed to prevent double pulsing or cross-conduction current spiking on the output.

All of the control and protect features work cycle-by-cycle up to the maximum operating frequency of 600kHz.

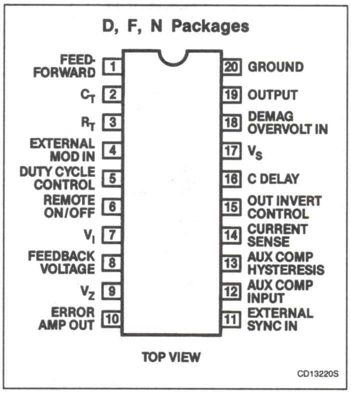
For ease of interface, all digital inputs are TTL or CMOS compatible.

The NE5562 is supplied in 20-pin glass/ceramic (Cerdip), plastic DIP, and plastic SO packages. The NE grade part is characterized and guaranteed over the commercial ambient temperature range of 0°C to +70°C and junction temperature range of 0°C to +85°C. The SE5562 is supplied in the glass/ceramic (Cerdip) package. The SE grade part is characterized and guaranteed over the ambient temperature range of −55 to +125°C and junction temperature range of −55 to +135°C.

FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting (2 levels)**
- **Auxiliary comparator, with adjustable hysteresis**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Duty cycle adjust and clamp**
- **Feed-forward control**
- **External synchronization**
- **Total shutdown after adjustable number of overcurrent faults**
- **Soft-start**

PIN CONFIGURATION

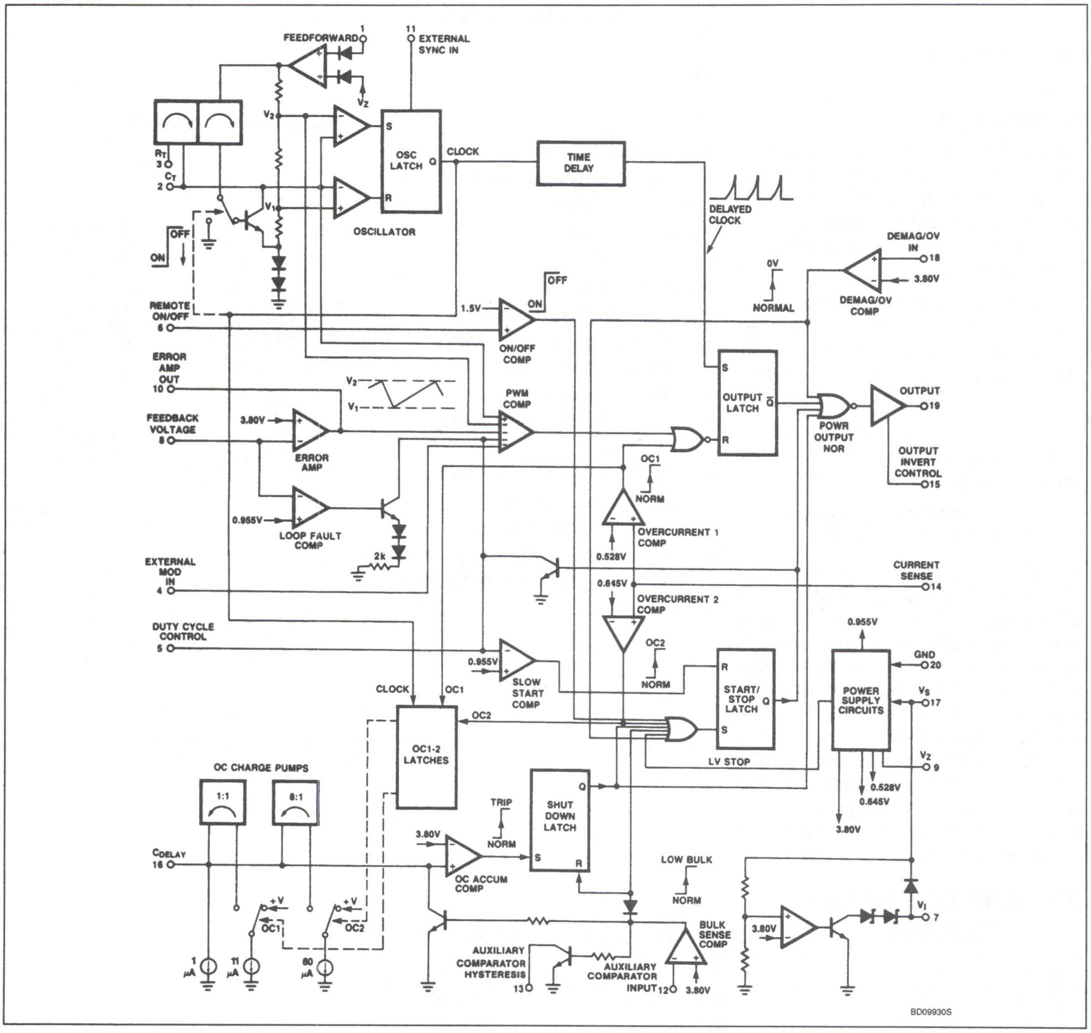

D, F, N Packages
FEED-FORWARD 1
C_T 2
R_T 3
EXTERNAL MOD IN 4
DUTY CYCLE CONTROL 5
REMOTE ON/OFF 6
V_I 7
FEEDBACK VOLTAGE 8
V_Z 9
ERROR AMP OUT 10
20 GROUND
19 OUTPUT
18 DEMAG OVERVOLT IN
17 V_S
16 C DELAY
15 OUT INVERT CONTROL
14 CURRENT SENSE
13 AUX COMP HYSTERESIS
12 AUX COMP INPUT
11 EXTERNAL SYNC IN
TOP VIEW
CD13220S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SO	0 to +70°C	NE5562D
20-Pin Ceramic DIP	0 to +70°C	NE5562F
20-Pin Plastic DIP	0 to +70°C	NE5562N
20-Pin Ceramic DIP	−55°C to +125°C	SE5562F

Switched-Mode Power Supply Control Circuit NE/SE5562

BLOCK DIAGRAM


FEEDFORWARD
1
11
EXTERNAL SYNC IN
V_Z
V_2
V_1
S
R
OSC LATCH
Q
CLOCK
OSCILLATOR
TIME DELAY
DELAYED CLOCK
R_T 3
C_T 2
OFF
ON
REMOTE ON/OFF 6
1.5V
ON
OFF
ON/OFF COMP
ERROR AMP OUT 10
FEEDBACK VOLTAGE 8
3.80V
ERROR AMP
PWM COMP
0.955V
LOOP FAULT COMP
2k
EXTERNAL MOD IN 4
DUTY CYCLE CONTROL 5
0.955V
SLOW START COMP
CLOCK
OC1
OC2
OC1-2 LATCHES
OC CHARGE PUMPS
1:1
8:1
C_{DELAY} 16
+V
OC1
OC2
1 µA
11 µA
80 µA
3.80V
OC ACCUM COMP
TRIP
NORM
SHUT DOWN LATCH
S
R
Q
AUXILIARY COMPARATOR HYSTERESIS 13
AUXILIARY COMPARATOR INPUT 12
3.80V
0V
NORMAL
OUTPUT LATCH
S
R
$\overline{Q}$
DEMAG/OV IN 18
3.80V
DEMAG/OV COMP
OUTPUT 19
POWR OUTPUT NOR
OUTPUT INVERT CONTROL 15
OC1
NORM
OVERCURRENT 1 COMP
0.528V
0.645V
OVERCURRENT 2 COMP
OC2
NORM
CURRENT SENSE 14
START/STOP LATCH
LV STOP
0.955V
GND 20
POWER SUPPLY CIRCUITS
V_S 17
V_Z 9
0.528V
0.645V
3.80V
LOW BULK
NORM
BULK SENSE COMP
3.80V
V_I 7
BD09930S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply		
V_S	voltage-fed mode (Pin 17)	16	V
I_{CC}	current-fed mode (Pin 7)	30	mA
	Output transistor output current	100	mA
	Sync (Pin 11)	V_S	V
	Duty cycle control (Pin 5)	V_Z	V
	Remote on/off (Pin 6)	V_S	V
	Output invert control (Pin 15)	V_S	V
	Feedback pin (Pin 8)	V_Z	V
	C_{DELAY} (Pin 16)	V_Z	V
	External mod in (Pin 4)	V_S	V
FF	Feed-forward (Pin 1)	V_S	V
	Demag/overvoltage in (Pin 18)	V_Z	V
	Current sense (Pin 14)	V_S	V
	Low supply sense and hysteresis (Pins 12, 13)	V_S	V
T_J	Operating junction temperature	135	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec)	300	°C

NOTES:
1. Ground Pin 20 must always be the most negative pin.
2. For power dissipation, see the application section which follows.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
	Supply		
	voltage-fed	10 to 16	V
	current-fed	15	mA
T_A	Ambient temperature range		
	NE grade	0 to +70	°C
	SE grade	−55 to +125	°C
T_J	Junction temperature range		
	NE grade	0 to +85	°C
	SE grade	−55 to +135	°C

DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Internal reference										
V_{REF}	Reference voltage	Internal	T_A = 25°C	3.76	3.80	3.84	3.76	3.80	3.84	V
V_{REF}	Reference voltage	Internal	Over temp.	3.72	3.8	3.90	3.725	3.8	3.870	V
	Temperature stability	Internal			30			30		ppm/°C
	Long-term stability	Internal			0.5			0.5		µV/ 1000hrs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC} = 12V$, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference										
V_Z	Zener voltage	9	$I_L = 7mA$, $T_A = 25°C$	7.35	7.60	7.75	7.35	7.6	7.75	V
V_Z	Zener voltage	9	$I_L = 7mA$, Over temp.	7.25		7.80	7.20		7.78	V
$\triangle V_Z/\triangle T$	Temperature stability	9	$I_L < 1mA$		50			50		ppm/°C
Low supply shutdown										
	Comparator threshold voltage	Internal	$T_A = 25°C$	8.30	8.45	8.75	8.30	8.45	8.75	V
	Comparator threshold voltage	Internal	Over temp.	8.00	8.45	8.90	8.00	8.45	8.90	V
	Hysteresis	Internal		25	50	8.00	25	50	800	mV
Oscillator										
f_{MIN}	Frequency range, minimum	1, 2, 3, 11	$R_T = 42.7k\Omega$, $C_T = 0.47\mu F$		60	80		60	80	Hz
f_{MAX}	Frequency range, maximum	1, 2, 3, 11	$R_T = 2.87k\Omega$, $C_T = 380pF$	600			600			kHz
	Initial accuracy	1, 2, 3, 11	$f_O = 52kHz$, $R_T = 16k\Omega$ and $C_T = 0.0015\mu F$, $T_A = 25°C$	48.6	54	59.4	48.6	54	59.4	kHz
	Voltage stability	1, 2, 3, 11, 17	$10V < V_S < 18V$		−215			−215		ppm/V
	Temperature stability	1, 2, 3, 11			300	500		300	500	ppm/°C
	Sawtooth peak voltage	2, 3	$T_A = 25°C^1$	5.00	5.25	5.40	5.00	5.25	5.40	V
		2, 3	Over temp.	4.80	5.25	5.60	4.80	5.25	5.60	V
	Sawtooth valley voltage	2, 3	$T_A = 25°C$	1.25	1.70	2.00	1.25	1.70	2.00	V
		2, 3	Over temp.	1.0	1.7	2.1	1.25	1.7	2.0	V
	Sync. in high level	11		2.0		V_Z	2.0		V_Z	V
	Sync. in low level	11		0.0		0.8	0.0		0.8	V
	Sync. in bias current	11	(Sourced), $V_{11} < 0.8V$		0.50	10.0		0.50	10.0	μA
	Feed-forward ratio, maximum	1			2			2		
	Feed-forward duty cycle reduction	1	$V_{FF} = 2V_Z$, $T_A = 25°C$	11	13.5	19	11	13.5	19	%
		1	Over temp.	6	13.5	22	8		22	%
	Feed-forward reference voltage	9			V_Z	V_S		V_Z	V_S	V
	Feed-forward bias current	1			2.5	50.0		2.5	50.0	μA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Error amp										
I_{BIAS}	Input bias current	8			1.0	5.0		1.0	5.0	μA
A_{VOL}	DC open-loop gain	8, 10	$R_L > 100k\Omega$	60	86		60	86		dB
V_{OH}	High output voltage	10	I_{SOURCE} = 1mA	5			5			V
V_{OL}	Low output voltage	10	I_{SINK} = 1mA			2.0			2.0	V
	PSRR from V_Z and V_S	Internal	$f_O < 300kHz$		−40			−40		dB
BW	Small-signal gain bandwidth product				8			8		MHz
	Feedback resistor range			1		240	1		240	kΩ
I_{SINK}	Output sink current		V8 = V10 = 5V			10			10	mA
I_{SOURCE}	Output source current		V8 = 3V, V10 = 1V			5			5	mA
	Sawtooth feedthrough		A_V = 100, 0% duty cycle		200			200		mV
PWM comparator and modulator										
	Minimum duty cycle	19	@$V_{COMP} <$, f = 300kHz	0			0			%
	Maximum duty cycle	19	@$V_{COMP} >$, f = 300kHz, V15 = 0V	95		98	95		98	%
A_{CC}	Duty cycle	10, 19	f = 15kHz to 200kHz, $V_{IN} = 0.472\ V_Z$	41	49	55	41	49	55	%
t_{PD}	Propagation delay to output	2, 19	$V_{15} = 0$		400			400		ns
I_{BIAS}	Bias current, external modulator input	4	(Sourced)		0.20	20		0.20	20	μA
I_{BIAS}	Bias current, duty cycle control	5	(Sourced)		0.20	20		0.20	20	μA
	Soft-start trip voltage	5		.910	0.955	0.990	0.922	0.955	0.988	V
Remote on/off (shutdown)										
	Output enabled	6		0		0.80	0		0.80	V
	Output disabled	6		2		V_Z	2		V_Z	V
I_{BIAS}	Bias current	6			1	10		1	10	μA
V_{IN}	Maximum input voltage	6		V_Z			V_Z			V
	Delay to output(s)	6, 19			400			400		ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 12V$, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Current limit comparator(s)										
	Shutdown, OC2	14		.593	0.645	.697	0.593	0.645	0.697	V
	Minimum duty cycle, OC1	14		.486	0.528	.570	0.486	0.528	0.570	V
I_{BIAS}	Bias current	14	(Sourced)		0.5	50		0.5	50	µA
OC_1	C_{DELAY} charge current	16		−18.2	−13	−6.5	−18.2	−13	−7.8	µA
OC2	C_{DELAY} charge current	16		−770	−550	−250	−770	−550	−330	µA
C_{DELAY}	Discharge current	16	$V12 = V_Z$	0.4	1.4	4.0	0.8	1.4	2.0	µA
C_{DELAY}	Shut off trip level	16	$T_A = 25°C$	3.75	3.86	3.97	3.75	3.86	3.97	V
Auxiliary comparator with shutdown										
I_{BIAS}	Bias current	12	(Sourced)		1	10		1	10	µA
	Threshold voltage	12		3.69	3.80	3.91	3.69	3.80	3.91	V
C_{DELAY}	Discharge current	12	$V_{IN} = 3V$	5	10		5	10		mA
	Hysteresis	12, 13			10			10		mV
Demagnetization overvoltage comparator										
I_{BIAS}	Bias current	18			2	10		2	10	µA
	Threshold voltage	18		3.62	3.80	3.91	3.69	3.80	3.91	V
	Hysteresis	18			10			10		mV
Output stage										
V_{OH}	High output voltage	19	$I_{SOURCE} = 100mA$	$V_S - 2.5$	$V_S - 1.9$		$V_S - 2.5$	$V_S - 1.9$		V
V_{OL}	Low output voltage	19	$I_{SINK} = 2mA$		0.16	0.4		0.16	0.4	V
V_{OL}		19	$I_{SINK} = 100mA$, $T_A = 25°C$		1.4	2.0		1.4	2.0	V
		19	$I_{SINK} = 100mA$, over temp.			2.25			2.25	V
	I_{SINK} max	19		100			100			mA
	I_{SOURCE} max	19		100			100			mA
t_R	Rise time	19	$C_L = 2000pF$		160			160		ns
t_F	Fall time	19	$C_L = 2000pF$		80			80		ns
Supply current/voltage										
I_{CC}	Supply current	17	$10V < V_S < 16V$ (Voltage-fed mode), $V_I < V_S$		9	15		9	15	mA
V_S	Input voltage	7, 17	$I_I = 15mA$, (Current-fed mode) V_S = meter	14.2	15.3	16.7	14.2	15.3	16.7	V
Operating frequency range for all functions but feed-forward working cycle-by-cycle										
f_{MIN}	Minimum frequency	All	$R_T = 42.7kΩ$, $C_T = 0.47µF$		60	80		60	80	Hz
f_{MAX}	Maximum frequency	All	$R_T = 2.87kΩ$, $C_T = 380pF$	600	1000		600	1000		kHz

NOTE:

1. Sawtooth peak and valley voltages were designed to be temperature-dependent to provide the frequency independence of temperature.

Switched-Mode Power Supply Control Circuit NE/SE5562

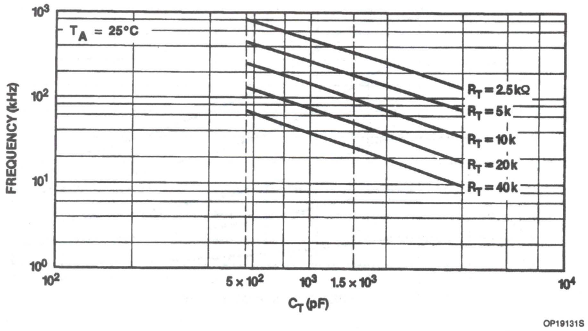


Figure 1. Frequency vs R_T, C_T NE/SE5562

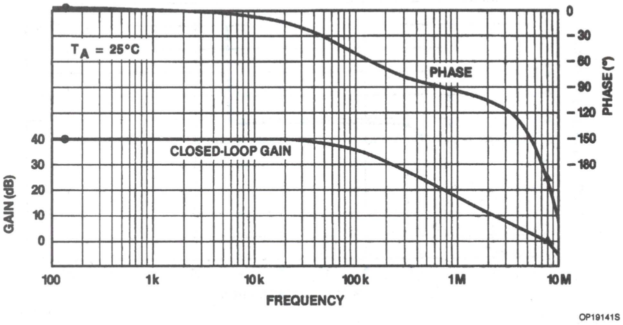


Figure 2. Error Amplifier Closed-Loop Response

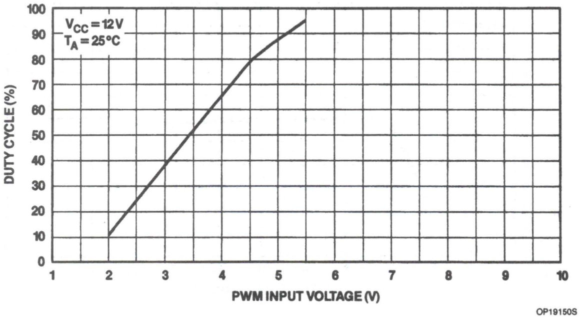


Figure 3. Duty Cycle vs PWM Input Voltage

8

Switched-Mode Power Supply Control Circuit

NE/SE5562

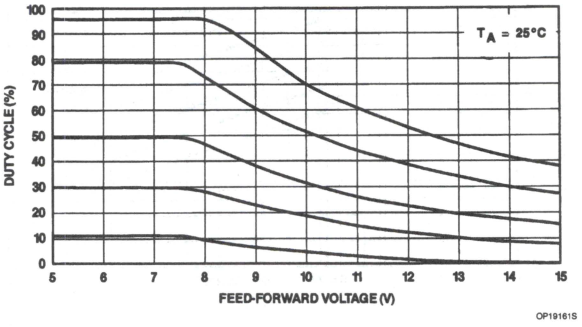


Figure 4. Duty Cycle vs Feed-forward Voltage

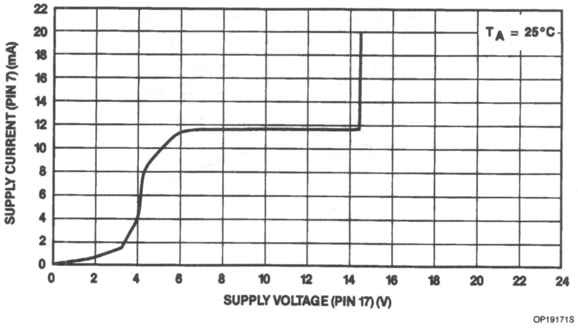


Figure 5. Current-Feed Characteristics

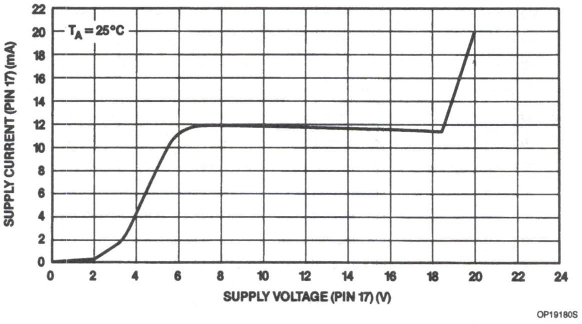


Figure 6. Voltage-Feed Characteristics

THE NE/SE5562 THEORY OF OPERATION

INTRODUCTION

Switched-mode power conversion relies on the principle of pulsed energy storage in an inductive or capacitive element. Capacitive switched converters are typically used with low power systems for which only tens of milliamperes are required. Medium and high power converters tend to use inductive storage elements as shown in Figures 7 – 9 with which a single switch may be moved around to create step-up (flyback) positive or negative polarity and step-down (forward or buck) conversion from a fixed-voltage source. The relationship between input and output voltage in each case is controlled by the switching on-to-off ratios, which is termed duty cycle. Duty cycle modulation is the common factor in this basic type of power control mechanism. By adding a high-gain operational amplifier, having one input tied to a stable DC reference voltage, configured in a negative feedback loop to maintain a constant output voltage as shown in Figure 10, the switched-mode controller becomes a dynamic voltage regulator. It is this single-switch topology that is most readily adapted to the NE/SE5562 SMPS Control IC.

The ability to switch inductor currents at rates up to 600kHz with state-of-the-art power FETs makes the design of small, efficient switching power converters an attainable reality. Protective features such as programmable slow-start and cycle-by-cycle current limiting allow safe, maintenance-free power supplies to be mass-produced at reduced cost to the manufacturer. Integrated technology makes long-term reliability a predictably achievable goal.

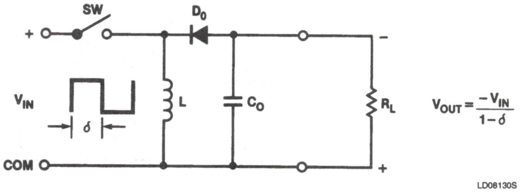

SW
D0
+
VIN
δ
L
CO
RL
$V_{OUT} = \frac{-V_{IN}}{1-\delta}$
COM
−
+
LD08130S

Figure 7. Negative Output Flyback Converter

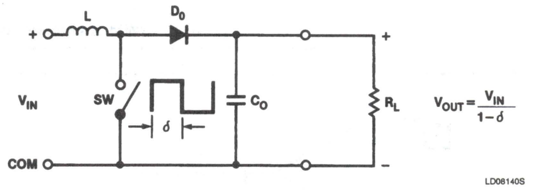

L
D0
+
VIN
SW
δ
CO
RL
$V_{OUT} = \frac{V_{IN}}{1-\delta}$
COM
+
−
LD08140S

Figure 8. Positive Output Flyback Converter

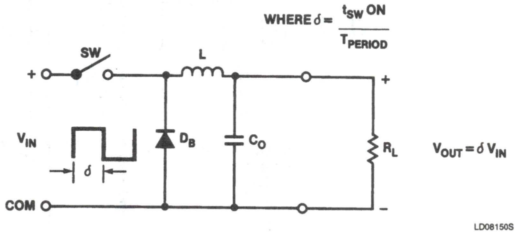

$\text{WHERE } \delta = \frac{t_{SW}\text{ ON}}{T_{PERIOD}}$
SW
L
+
VIN
δ
DB
CO
RL
$V_{OUT} = \delta V_{IN}$
COM
+
−
LD08150S

Figure 9. Forward Converter (Single Inductor) Step Down

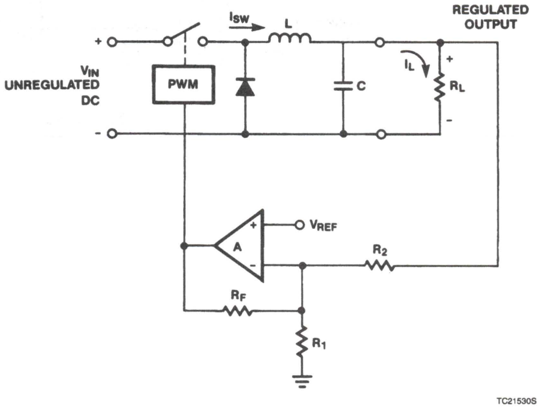

ISW
L
REGULATED OUTPUT
+
VIN UNREGULATED DC
PWM
C
IL
RL
+
−
−
VREF
A
+
−
R2
RF
R1
TC21530S

Figure 10. The Forward (Buck) Converter ($V_{OUT} = V_{IN}(\delta)$)

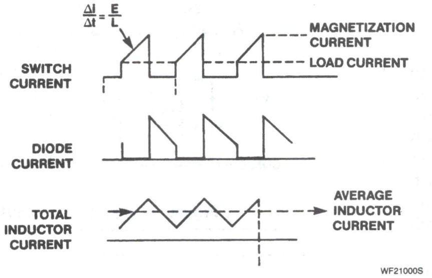
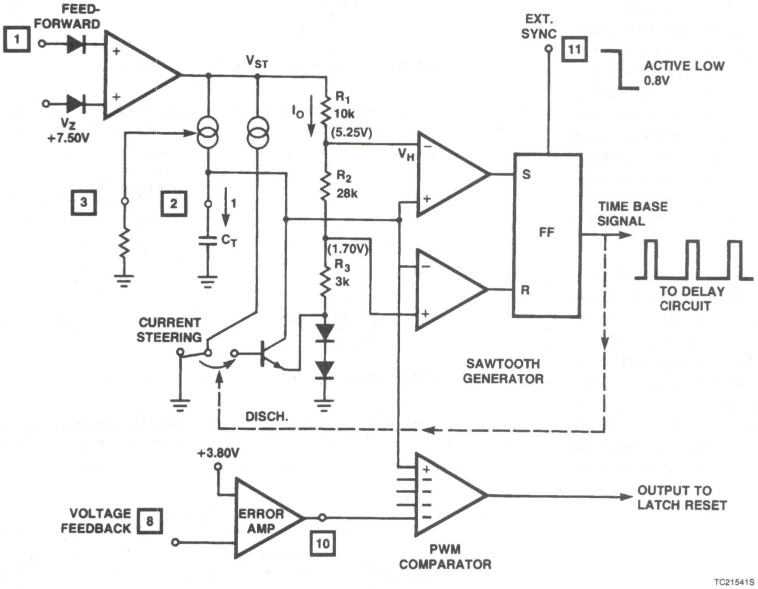


Figure 11. PWM Switching Waveforms



FEED-FORWARD
1
V_Z +7.50V
V_{ST}
I_O
R_1 10k
(5.25V)
V_H
R_2 28k
3
2
1
C_T
(1.70V)
R_3 3k
CURRENT STEERING
EXT. SYNC
11
ACTIVE LOW 0.8V
S
FF
R
TIME BASE SIGNAL
TO DELAY CIRCUIT
SAWTOOTH GENERATOR
DISCH.
+3.80V
VOLTAGE FEEDBACK
8
ERROR AMP
10
PWM COMPARATOR
OUTPUT TO LATCH RESET
TC21541S

Figure 12

THE NE/SE5562 THEORY OPERATION

The Sawtooth Oscillator

The sawtooth oscillator consists of a gated charge-discharge capacitor circuit with threshold comparators setting the peak and valley voltages of the ramp. The resistor divider R1 – 3 is supplied with a source voltage derived from either V_Z (7.50V) minus two diode drops, or, when feed-forward is in control, a voltage greater than V_Z and proportional to the main supply voltage. The nominal upper threshold voltage is 5.25V and the lower threshold 1.70V. These then determine the sawtooth peak and valley voltages, respectively.

Operation

Beginning with the charge cycle, ramp voltage builds up on the timing capacitor due to a constant current supplied to the node at Pin 2. When capacitor voltage reaches the upper threshold, comparator A switches, setting the latching flip-flop. The output of the latch goes high, generating a clock pulse. The discharge transistor is simultaneously turned on, reducing charge on the timing capacitor to the point at which the lower threshold voltage, 1.70V, is reached. The lower comparator is then activated, resetting the latch and terminating the clock pulse. Note that the discharge transistor is referenced to the same return diodes as the threshold resistor divider and the discharge current is made to track with the charge current. This charge and discharge tracking results in a true sawtooth waveform even at extended frequencies. Figure 15 shows a family of curves which explains the relationship between R_T, C_T, and the frequency of the sawtooth generator. The data sheet shows the initial accuracy of the oscillator at 60Hz and 600kHz.

THE PULSE WIDTH MODULATOR AND ERROR AMPLIFIER

The PWM consists of a multi-input voltage comparator (Figure 13) having its positive input tied to the sawtooth ramp voltage and the various negative inputs referenced to ORed control signal nodes. The primary control signal is the error amplifier output voltage node which sets the active duty cycle termination point of the PWM output waveform. As the error amplifier input signal derived from the power supply load voltage varies, for instance in a negative direction, the amplifier output moves upward, raising the PWM comparator toward longer duty cycles at the output on Pin 19. The start-up sequence begins with zero voltage at the input to the error amplifier. Since this could signal an open feedback loop, the loop fault comparator on Pin 8 clamps the PWM duty cycle until the feedback voltage exceeds 0.955V. A second comparator monitors the duty cycle control, Pin 5, with the same threshold level, inhibiting the output via the start-stop latch (Figure 14).

The charging of the slow-start capacitor provides a controlled ramp-up of the output duty cycle and a resultant gradual increase in energy fed to the output magnetics.

The dynamic response of the PWM comparator is shown in the simulated waveform drawing of Figure 15. The error amplifier output voltage is depicted as sloping positive (increasing) with time as referenced to the sawtooth waveform. This causes the duty cycle to increase with time. This is an indication of an increasing load on the power supply as output voltage is decreasing. The Pin 5 (δ_{MAX}) control voltage is also superimposed midway on the sawtooth, indicating the limits of duty cycle increase as the output waveform no longer increases in duty cycle after the δ_{MAX} threshold is crossed. A hypothetical overcurrent pulse (Pin 14) is shown to illustrate cycle termination immediately at the output (Pin 19).

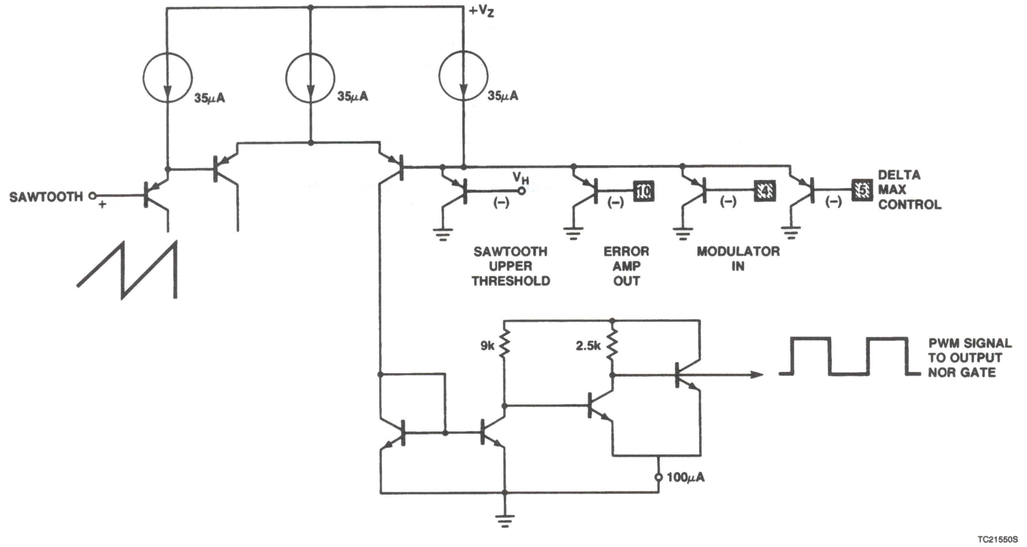


Figure 13. PWM Comparator

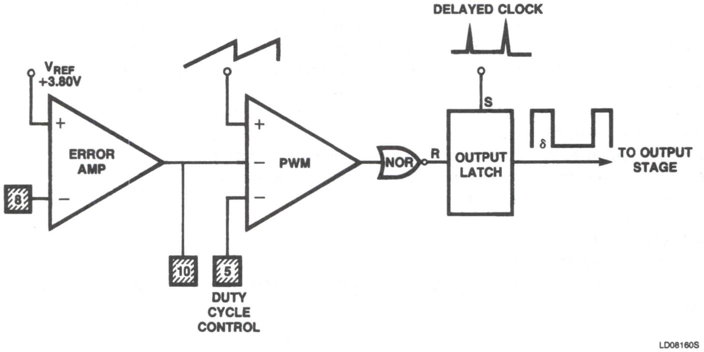

DELAYED CLOCK
VREF +3.80V
+
−
ERROR AMP
8
+
−
−
PWM
10
5
DUTY CYCLE CONTROL
NOR
R
S
OUTPUT LATCH
δ
TO OUTPUT STAGE
LD08160S

Figure 14. The Duty Cycle Control Circuit, Pulse Width Modulator, and Error Amplifier, Reference, and Output Latch

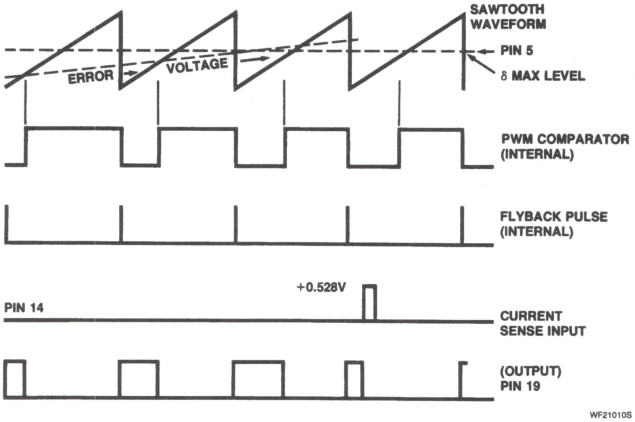

SAWTOOTH WAVEFORM
PIN 5
δ MAX LEVEL
ERROR
VOLTAGE
PWM COMPARATOR (INTERNAL)
FLYBACK PULSE (INTERNAL)
+0.528V
PIN 14
CURRENT SENSE INPUT
(OUTPUT) PIN 19
WF21010S

Figure 15. Duty Cycle vs Feedback Error and Overcurrent Sense

The error amplifier's non-inverting input is tied to a bandgap reference of 3.80V, accurate to ± 2% at 25°C. The temperature stability of the voltage reference is 30ppm/°C.

The error amplifier is designed for an open-loop gain of 86dB having a small-signal unity gain bandwidth of 3MHz. Closed-loop gain is stable to 10dB, as shown in Figure 17. The DC output excursion of the amplifier is capable of controlling the full PWM range of 0 to 95%. The amplifier can sink 10mA and source 5mA. The nominal DC output for 50% duty cycle is 3.55V. Feedback control resistor value may range from 1kΩ to 240kΩ without overload or instability. However, low closed-loop gains must be compensated by lag lead network techniques for optimum stability. Loop compensation networks may intersect the open-loop gain curve with a slope 2 closure and must then be compensated to maintain overall phase and gain margin (Figure 16).

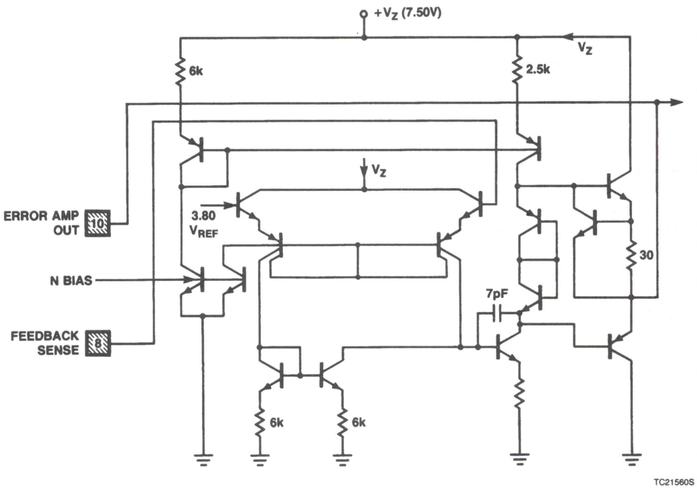


Figure 16. Error Amplifier

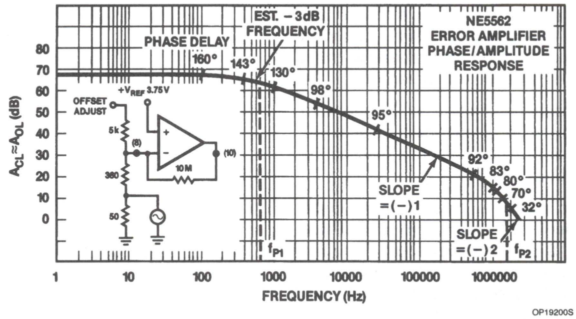


Figure 17. Error Amp, Response

Feed-Forward Compensation (Pin 1)

To provide a means of automatically improving line-to-load voltage regulation, a technique called feed-forward regulation is made a part of the NE/SE5562 active mechanism. Referring back to the diagram for the sawtooth oscillator, note that Pin 1 is capable of changing the internal supply voltage to the charging circuit for the timing capacitor, C_t. With a nominal duty cycle of 30%, for instance, increasing Pin 1 voltage by 1V from 10.3 to 11.3 will reduce the output duty cycle by approximately 5%. Thus, a primary has caused a decrease in volt-seconds (duty cycle X primary volts) of 5/30 or 16% (Figure 4). The result is a small over-compensation in the output energy, but an overall safe margin in transformer flux.

NOTE:

Figure 18 shows a delta V_1 of 7.5V.

The mechanism which produces inverse duty cycle modulation is shown in Figure 18. Increasing Pin 1 voltage beyond the value of V_Z (7.50V) increases the charge rate on C_T, causing the duty cycle to be terminated earlier for each cycle that input voltage is increased. The threshold voltages at the sawtooth limit comparator reference inputs are changed with Pin 1 also in order to offset any change in oscillator frequency.

The secondary benefit of using feed-forward is the attenuation of any low-frequency AC riding on the DC supply before it reaches the regulated output.

Note that a start delay circuit is added to the Pin 1 divider in order to prevent internal race conditions during initial power-up. Once the turn-on transient has decayed, normal operation of the feed-forward circuit is assured. Figure 19 shows an RC delay placed in a base clamping circuit to provide reliable starting.

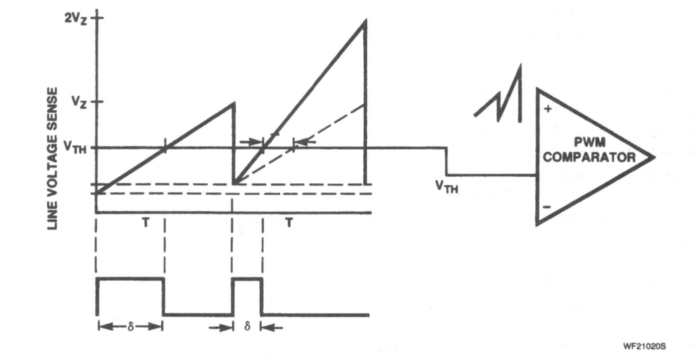


Figure 18. Feed-forward

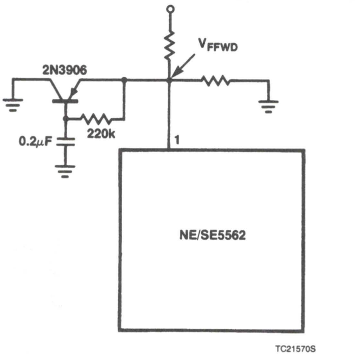


Figure 19. Feed-forward Turn-On Delay Circuit

SYNCHRONIZATION

The synchronization of the sawtooth oscillator to an external pulse of negative-going polarity is shown in Figure 20. When the sync input pulse crosses the 1.5V threshold, negative, the sawtooth oscillator is prevented from discharging the timing capacitor, causing the charge voltage on the capacitor to remain high (5.25V) until the sync pulse again goes above 1.5V, allowing reset. This action stretches the period of the oscillator and results in a lower frequency undersynchronization control than the free-running frequency.

NOTE:
See oscillator schematic, Figure 12, for sync circuit details.

The following relationship holds —

$f_{\text{free-run}} > f_{\text{sync}}$

$$f_{\text{sync}} = \frac{1}{t_0 + \tau}$$

A typical recommended starting point in calculating frequency for synchronous operation is to set the free-run frequency approximately 10% higher than the sync frequency. Then set the pulse width, τ, to 10% of t_0, the free-run period, with the desired new frequency determined by the sum as above.

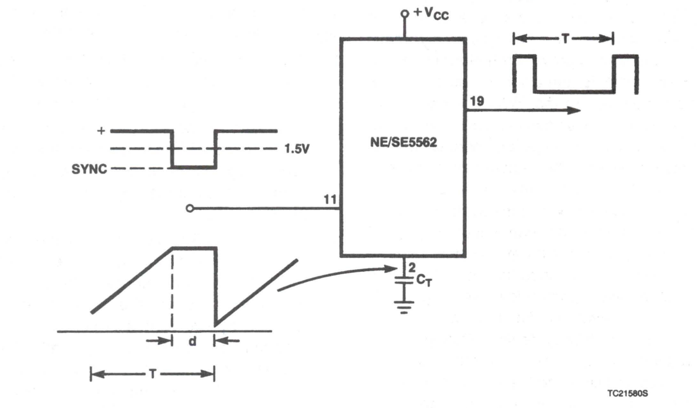


Figure 20. Synchronization Signals

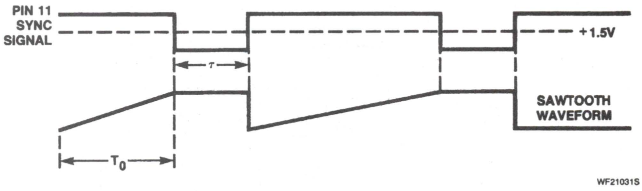


Figure 21. Sync Signal Relationship to Controlled Sawtooth Waveform

DUTY CYCLE LIMIT (PIN 5)

The forward or buck converter, and even the flyback converters, may require an automatic duty cycle limit to prevent transformer saturation or unstable behavior. A special input provides access to the PWM comparator for this purpose. As discussed previously in regard to the error amplifier, increasing load demand may drive the system current beyond safe limits. A simple solution is the placement of a duty cycle limit within the system dynamic response before this can occur. Figure 13 shows the PWM comparator with its multiple input ports. All are inverting in polarity and provide a lowest priority level sensing circuit. The lowest level on Pin 4, 5, or 10 gains control of the duty cycle limit. During normal operation, the δ_{MAX} circuit sends a continuous threshold signal to the PWM comparator, setting a fixed limit on how much the error amplifier is allowed to increase the duty cycle in response to load demand. Figure 22 shows the circuit within the NE/SE5562 which actually controls duty cycle as listed below:

1. Duty cycle ramp-up (slow-start) during power-up. Time constant controlled by external R, C ramp voltage at Pin 5.
2. Slow-start if remote ON/OFF is actuated, if OC2 threshold trips, demagnetization/overvoltage is sensed, or low supply voltage to the internal regulator is sensed ($V_S \leqslant 8.45V$).
3. Note that Pin 8 is monitored by the loop fault comparator. When the regulated supply feedback drops below this threshold level (0.955V), the duty cycle is clamped by two diodes in series with a 2kΩ load across Pin 5 to ground. This implies a minimum duty cycle condition as long as the low output level remains.

Referring to the graph in Figure 23, the designer may choose a divider ratio which, when referenced to V_Z, 7.5V, provides an easy duty cycle limit control. For example, a 50% limit results in a ratio of 0.48. Setting R_2 at a nominal value between 10 and 20kΩ and solving for R_1, the proper limit is obtained.

Example:

A duty cycle limit of 50% is required for a forward converter.

$R_2 = 10k\Omega$, find R_1

$$\frac{R_2}{R_1 + R_2} = 0.48$$

$$\therefore R_2 = 0.48\ (R_1 + R_2)$$

$$0.48R_1 = R_2 - 0.48R_2$$

$$\therefore R_1 = \frac{R_2(1 - 0.48)}{0.48}$$

$$= \frac{10k\Omega(0.52)}{0.48}$$

$$= 10.8k\Omega$$

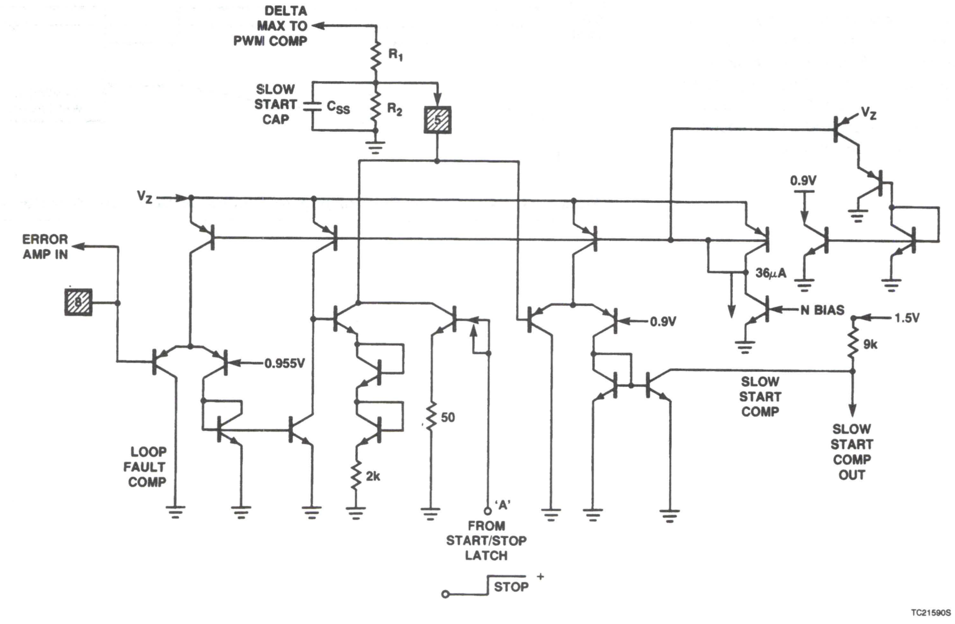


Figure 22. Duty Cycle Limit Control

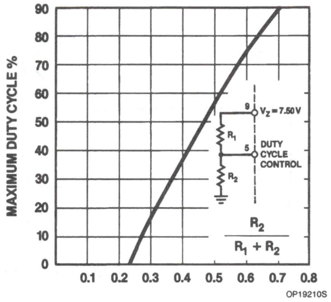


Figure 23. Maximum Duty Cycle

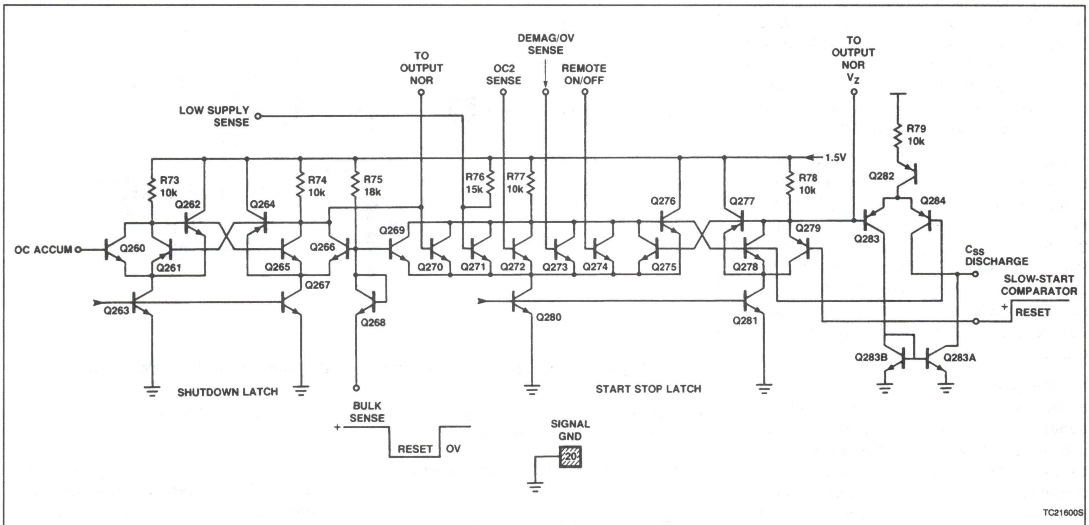

DEMAG/OV SENSE
TO OUTPUT NOR
OC2 SENSE
REMOTE ON/OFF
TO OUTPUT NOR V_Z
LOW SUPPLY SENSE
1.5V
R73 10k
R74 10k
R75 18k
R76 15k
R77 10k
R78 10k
R79 10k
OC ACCUM
Q260
Q261
Q262
Q263
Q264
Q265
Q266
Q267
Q268
Q269
Q270
Q271
Q272
Q273
Q274
Q275
Q276
Q277
Q278
Q279
Q280
Q281
Q282
Q283
Q284
Q283B
Q283A
C_{SS} DISCHARGE
SLOW-START COMPARATOR
+
RESET
SHUTDOWN LATCH
BULK SENSE
+
RESET
OV
SIGNAL GND
20
START STOP LATCH
TC21600S

Figure 24. Start-Stop/Shutdown Latches

THE START-STOP CONTROL SEQUENCE

The start-up circuit involves a sequential set of conditions which progresses as follows: power-up after OFF condition or remote ON after OFF. Initially, 0V exist on the supply output, causing zero feedback volts on Pin 8. The slow-start capacitor is discharged, forcing Pin 5 to 0V, having been clamped by the internal discharge transistor. Internal supply regulator input exceeds 8.45V, releasing low voltage shutdown condition with Pin 5 below 0.955V. The slow-start comparator output goes high, resetting the start/stop latch, sending a low output signal to the output stage power NOR gate. The PWM signal is then enabled to feed the output drive circuits, starting energy flow through the magnetics. However, instantaneously the power supply output is still below 0.955V and the loop fault comparator forces the PWM to remain at a minimum duty cycle. The equivalent circuit at this instant in the start-up cycle which exists at Pin 5 is shown in Figure 26.

The actual minimum duty cycle is determined by the parallel source resistance of R_1 and R_2 combined with the shunt loading internal to Pin 5. High values of divider resistance, 20 – 30kΩ, will supply less shunt current to Pin 5 and create a lower modulator duty cycle, while lower values of R_1 and R_2 (5 – 10kΩ) will generate a higher modulator voltage and a greater resultant minimum duty cycle.

As the power conversion circuits become active and Pin 8 feedback voltage increases above 0.955V, the duty cycle network is unclamped; duty cycle increases, controlled by the RC time constant $R_1 \| R_2 . C_{SS}$, and as output voltage brings the feedback voltage up to equal the reference voltage, 3.80V, the error amplifier takes control and the supply is in regulation.

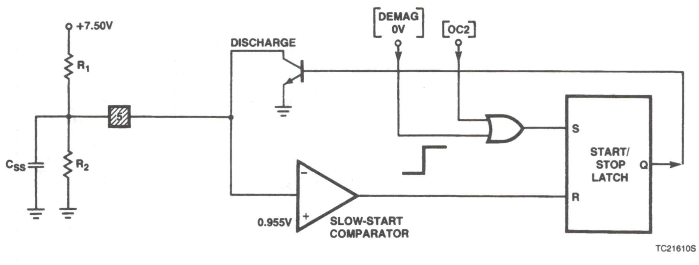


Figure 25. Slow-Start Comparator

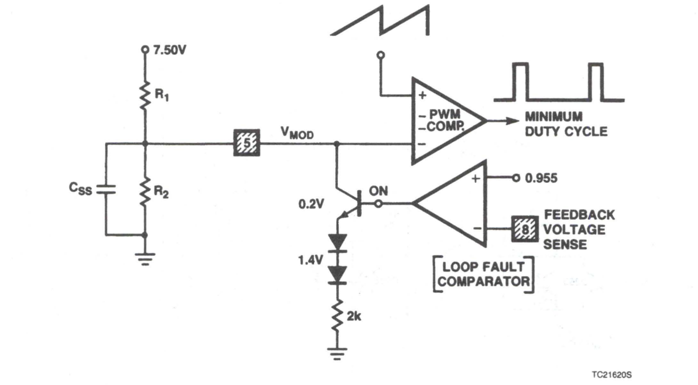


Figure 26. Loop Fault Comparator and Minimum Duty Cycle Clamp

The stop or shutdown sequence is initiated by any of the following conditions:

a. Supply voltage (bulk) sense below 3.80V at Pin 12.

b. Pin 17 below 8.45V or Pin 7 current below level (less than 9mA).

c. Remote ON/OFF voltage at Pin 6 greater than 2V.

d. Sustained OC2 causing C_{DLY} to charge above 3.80V (current sense on Pin 14 continuously above 0.645V peak).

DUAL-LEVEL OVERCURRENT COMPARATORS

The overcurrent sensing circuit (Figure 27) consists of a single PNP input buffer with emitter-follower tied to V_Z, 7.50V, feeding into the base of an NPN split-emitter transistor. This forms the input node to a set of dual-level voltage comparators with references of 0.528 and 0.645V, respectively. Current sources for the comparator are fixed biased NPNs.

The typical transition time delay for an overcurrent fault is 300ns. Bias current at the input averages 500nA.

If the overcurrent sense feature is not used, it is recommended that Pin 14 be tied to ground.

When used for sensing current-derived voltage impulses from the primary driver, a high-speed, low-impedance transient filter network is advised. An example is shown in Figure 28. Keep C_F close to the NE/SE5562.

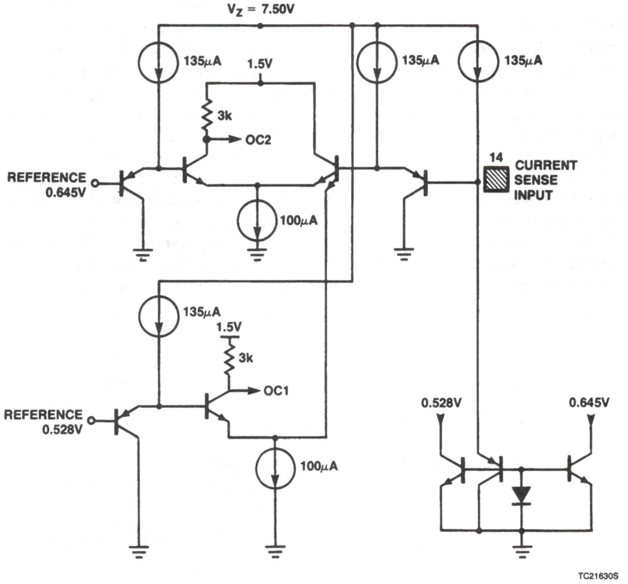

V_Z = 7.50V
135μA
1.5V
135μA
135μA
3k
OC2
14
CURRENT SENSE INPUT
REFERENCE 0.645V
100μA
135μA
1.5V
3k
OC1
REFERENCE 0.528V
0.528V
0.645V
100μA
TC21630S

Figure 27. NE/SE5562 Overcurrent Comparator

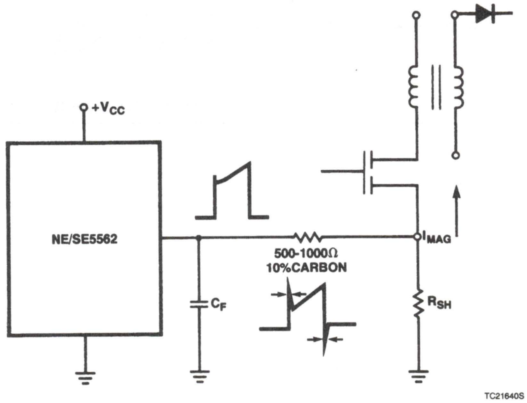

+V_CC
NE/SE5562
500-1000Ω 10%CARBON
I_MAG
C_F
R_SH
TC21640S

Figure 28. Transient Suppression

THEORY — OC1 AND OC2

Overcurrent Logic and Delay Capacitor Operations

The circuit takes a voltage input from Pin 14 and compares the level to a dual reference comparator with trips at 0.53 and 0.65V. The lower trip point actuates cycle-by-cycle shutdown of the output stage with an intrinsic delay of 400ns. The second level actuates the slow-start function. In addition, there exists a separate housekeeping circuit whose function is to terminate operation of the output stage if its threshold is exceeded. This involves a time delay circuit based on two separate switchable current sources, OC1 and OC2. The time delay capacitor allows the user to program shutdown of the system after a predetermined number of overcurrent cycles have occurred within the period set by the ramp-up of the delay capacitor. Once shutdown has occurred in this manner, external reset is required to restart the system. Referring to the logic block Figure 29, which controls the gating of the two charge pumps into the delay capacitor at Pin 16, the complete signal flow may be traced. Logic signals from the overcurrent 1 and 2 comparators are gated by the clock and delayed clock signals generated by the sawtooth oscillator. The complete sequence for an overcurrent fault may be understood by referring to Figure 30 for OC2. Here it is shown that an OC2 signal exists indicating that the 0.65V threshold has been exceeded by a signal at Pin 14.

Note that an overcurrent pulse within a particular clock frame turns on the respective OC2 charge ramp during the entire next clock frame. Consecutive overcurrent pulses of either OC1 or OC2 magnitude will activate the selected charge pump for the total duration that such overcurrent occurs. The charging cycle will continue until the delay capacitor reaches the 3.86V trip level.

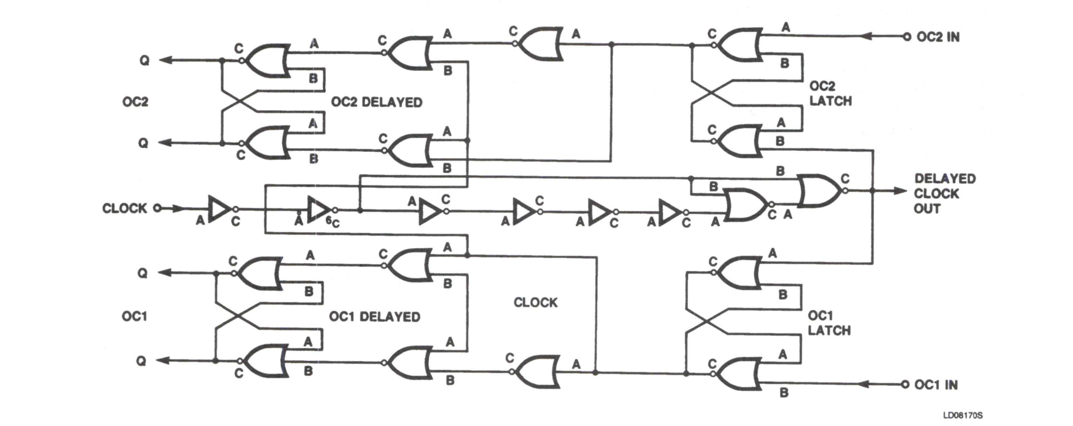


Figure 29. Overcurrent Logic

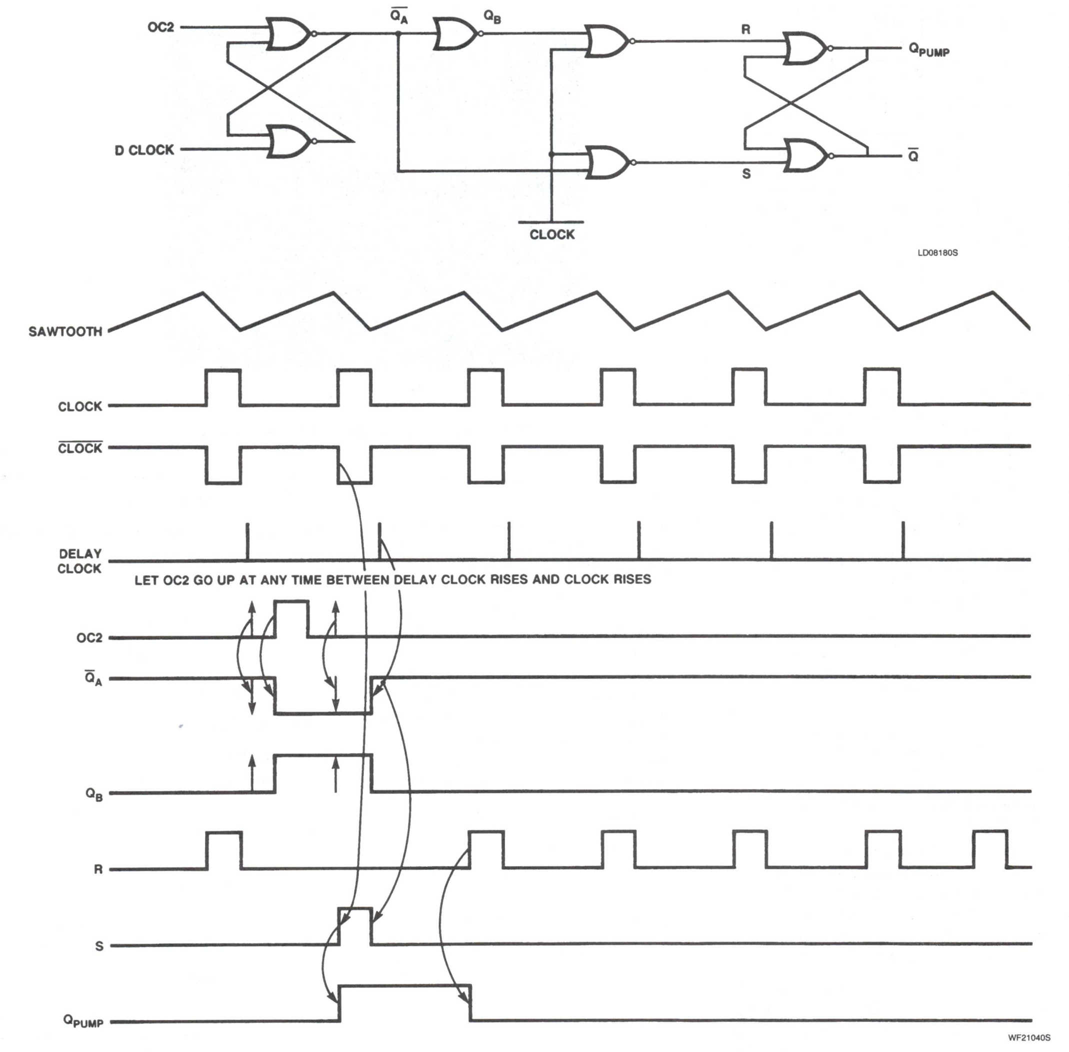

OC2
D CLOCK
$\overline{Q}_A$
Q_B
R
S
Q_{PUMP}
$\overline{Q}$
CLOCK
LD08180S
SAWTOOTH
CLOCK
$\overline{CLOCK}$
DELAY CLOCK
LET OC2 GO UP AT ANY TIME BETWEEN DELAY CLOCK RISES AND CLOCK RISES
OC2
$\overline{Q}_A$
Q_B
R
S
Q_{PUMP}
WF21040S

Figure 30. OC2 Fault Cycle

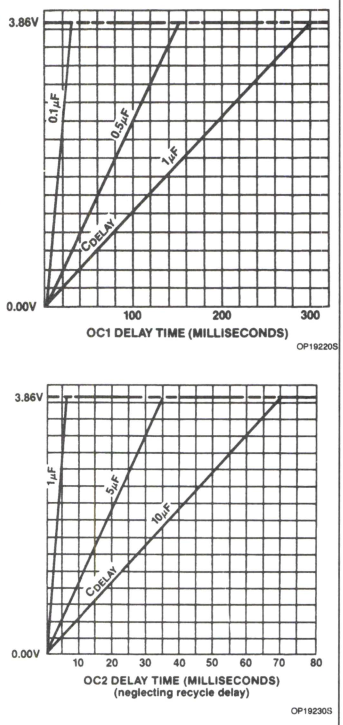


Figure 31. Overcurrent Shutdown Function

CALCULATING THE DELAY CAPACITOR

Actual delay time for a given capacitor value at Pin 16 may be estimated using the graphs in Figure 31 for OC1 and OC2. By first determining the allowable overcurrent time product for a particular power converter, a capacitor delay value may be calculated.

Note that the OC1 charge pump is typically 13μA while OC2 pumps 550μA into the capacitor. If the exact value is to be calculated for a particular delay requirement, use the following procedure:

1. Determine the level of overcurrent — OC1 or OC2.
2. Find the maximum delay time which the supply may safely sustain for this continuous overcurrent condition. Note that OC1 may be activated on every cycle if OC2 is not reached, causing continuous charging of C-Delay. However, OC2 overcurrent detection causes the supply to go into slow-start shutdown (hiccup mode), on the first such pulse. OC2 delays are based on an interrupted charging cycle with total cycle time determined by the external slow-start delay capacitor duty cycle maximum divider — time constant.

For a continuous OC1 overcurrent:

$$C_{DLY} = \frac{(13 \times 10^{-6})(\text{Delay time — sec})}{3.86V} \qquad (1)$$

For a continuous OC2 overcurrent:

$$C_{DLY} = \frac{(550 \times 10^{-6})(\text{Delay cycles} \times 1 / f_{SW})}{3.86V} \qquad (2)$$

Some downward adjustment of the OC2 capacitor value may be necessary to compensate for the 1 – 2μA of discharge current at Pin 16 during the delay cycles.

Example: A maximum of 100 OC2 current fault cycles is allowed.

f_{SW} = 400kHz, find C_{DLY}

$$C_{DLY} = \frac{(550 \times 10^{-6})(100 \times \frac{1}{4} \times 105)}{3.86V}$$

$$= 0.036\mu F$$

Example: OC2/C_{DLY}

Find number of OC1 cycles before shutdown with 0.036μF C_{DLY}.

$$\text{Delay Time} = \frac{3.6 \times 10^{-8}F)(3.86V)}{13 \times 10^{-6}A}$$

$$= 10.7ms$$

$$\text{Total cycles to shutdown} = \frac{10.7 \times 10^{-3}}{2.5 \times 10^{-6}}$$

$$= 4280$$

Figure 33 shows an actual OC1 charging cycle for continuous fault current sensed at Pin 14 and a DLY = 1μF.

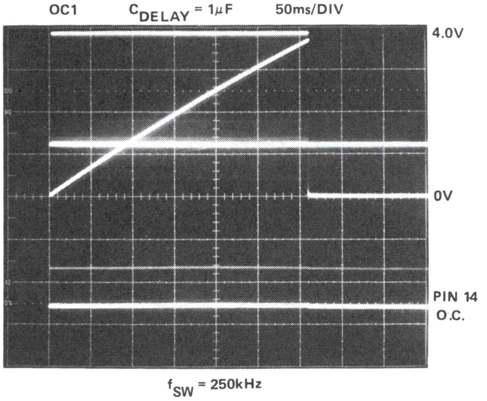


Figure 32. OC1 Ramp and Shutdown Delay

BULK-SENSE AUXILIARY COMPARATOR WITH SHUTDOWN

This circuit is intended to act as an automatic low-line detection mechanism. As shown in Figure 33, a voltage divider is connected from the main unregulated DC supply to Pin 12. The lower divider resistor may be a potentiometer of 5 – 10kΩ resistance with center-tap connected to Pin 13. The comparator which senses Pin 12 voltage is referenced to 3.80V and Pin 12 divider voltage must be greater than this voltage by a sufficient margin to operate within the prescribed low-line limits. For instance, if a line voltage drop of 25% is considered the shutdown threshold, then V_{12} should be calculated for a nominal operating voltage as shown in Figure 33.

When the line voltage drops more than 25%, the output stage is disabled. With the hysteresis connected as shown and the pot adjusted near midway, the line voltage will have to exceed $V_{NOMINAL}$ before the supply will restart. The hysteresis control may then be calibrated for the desired overexcursion before restart. This prevents unstable circuit chatter.

The reset switch provides a means for resetting the shutdown latch after overcurrent faults have charged C_{DLY} to its trip threshold. This also provides a discharge path for the delay capacitor. Figure 34 shows internal circuit.

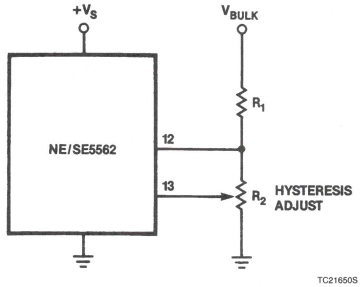

+VS
VBULK
R1
NE/SE5562
12
13
R2
HYSTERESIS ADJUST
TC21650S

Figure 33. Bulk-Sense Comparator Divider

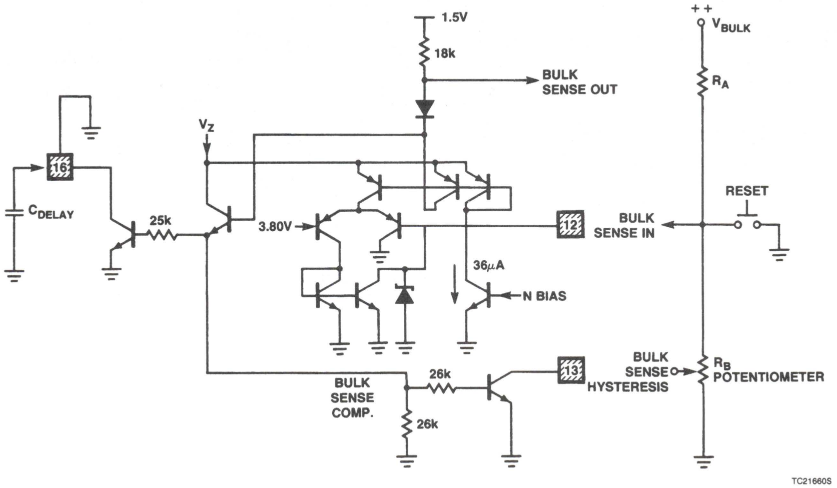

1.5V
18k
BULK SENSE OUT
++
VBULK
RA
VZ
16
CDELAY
25k
3.80V
RESET
12
BULK SENSE IN
36μA
N BIAS
13
BULK SENSE HYSTERESIS
RB POTENTIOMETER
BULK SENSE COMP.
26k
26k
TC21660S

Figure 34. Bulk-Sense Comparator

Switched-Mode Power Supply Control Circuit NE/SE5562

THE OUTPUT DRIVE STAGE

The output stage contains the power NOR inhibit gate, invert logic function, and source-sink drivers. The driver stage is capable of sourcing and sinking 100mA at frequencies up to 600kHz. The output transistors are Schottky clamped to prevent saturation and the resultant switching delay due to stored charge. A 2.5Ω current sense resistor in the emitter of Q419 serves to drive active clamp Q427 when the output sources more than 200mA. This places a limit on the peak current available during instantaneous charging of a power MOS FET gate. This feature protects the output stage from inadvertent catastrophic overload.

When sinking current, the output is clamped to a maximum of 1.4V. Output swing for positive output is typically $V_S - 1.9V$ at 100mA sourcing. Rise time for a 2000pF load at Pin 19 is typically 160ns with a fall time of 80ns.

The power NOR gate provides a fast response inhibit function to shutdown the output in the event of a number of different fault conditions. All inputs are internal to the device and do not appear directly on the external pins as is shown on Figure 35.

The additional flexibility of an invert control allows the polarity at the output during duty cycle to be reversed. This provides a simple means of designing with P-channel power MOS FETs without adding external inverters. The invert logic is controlled by a simple logic signal at Pin 15. Grounding will cause the output to be a normal positive output and a high level gives inverted output.

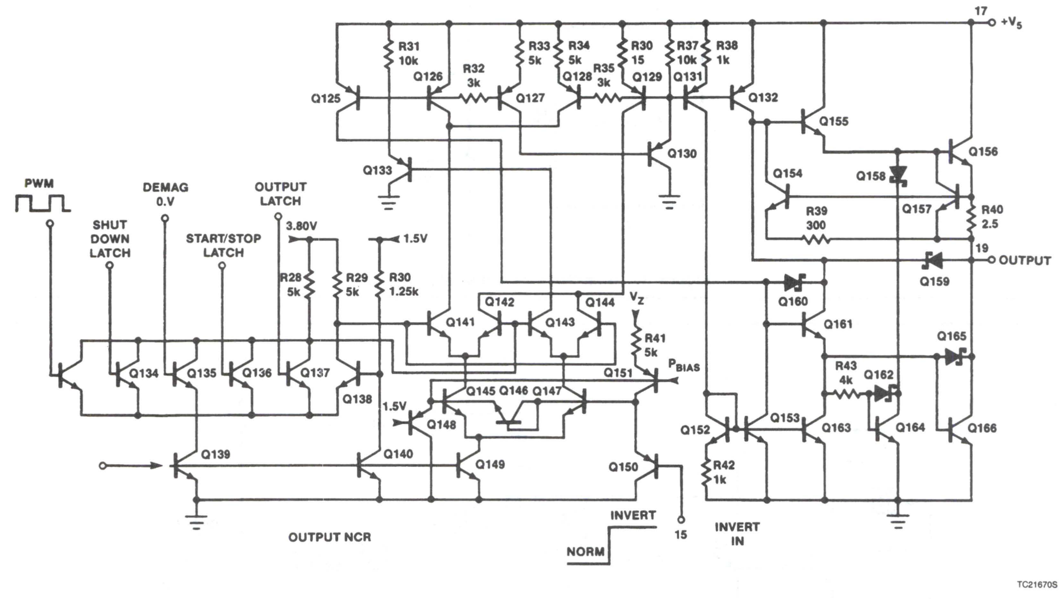

17
+V_S
R31 10k
R32 3k
R33 5k
R34 5k
R35 3k
R30 15
R37 10k
R38 1k
Q125
Q126
Q127
Q128
Q129
Q131
Q132
Q155
Q130
Q156
Q133
Q154
Q158
R39 300
Q157
R40 2.5
19
OUTPUT
Q159
PWM
DEMAG 0.V
OUTPUT LATCH
SHUT DOWN LATCH
START/STOP LATCH
3.80V
1.5V
R28 5k
R29 5k
R30 1.25k
Q142
Q144
VZ
Q160
Q141
Q143
Q161
R41 5k
Q165
PBIAS
Q134
Q135
Q136
Q137
Q138
Q151
R43 4k
Q162
Q145 Q146 Q147
1.5V
Q148
Q152
Q153
Q163
Q164
Q166
Q139
Q140
Q149
Q150
R42 1k
INVERT
15
NORM
INVERT IN
OUTPUT NCR
TC21670S

Figure 35. Output Driver Schematic

THE INTERNAL VOLTAGE REGULATOR

The internal regulator is configured to provide for external supply to the NE/SE5562 from either a voltage feed or a current feed.[1]

For the current-fed mode, a series-dropping resistor may be used to power the device from voltages greater than 18V with current supply of 15 to 25mA. Note that supply current stated in the data sheet is for the device only without load on the output or V_Z. Drive currents also are pulse-related and thus reflect frequency components onto the current-feed circuit. These must be filtered out at Pin 7 with adequately large capacitors in order to prevent motor-boating (see Figure 36 and Figure 37).

Input current to Pin 7 flows through Zeners Z_1 and Z_2, and short regulator transmitter QR. A differential amplifier with 3.80V reference provides feedback to regulate V_S to 15V.

In the voltage-fed mode using Pin 17, the Zeners prevent current flow through QR for input voltages less than 19V.

Power dissipation of the device must stay within the allowable package limits. These limits are derived from the thermal characteristics of the particular package chosen. The NE5562N plastic package is capable of operating within the temperature range (ambient) of 0 to +70°C. This rating applies to the surface-mount product NE5562D also. Obviously, the power dissipation of the "D" package is lower than the standard DIP. Thermal resistance for the various packages are:

20-Pin plastic — NE5562N/SE5562N: θ_{JA} 61°C/W

20-Pin glass/ceramic — NE5562F/SE5562F: θ_{JA} 90°C/W

20-Pin SO: −55 to +85°C/W (board-dependent)

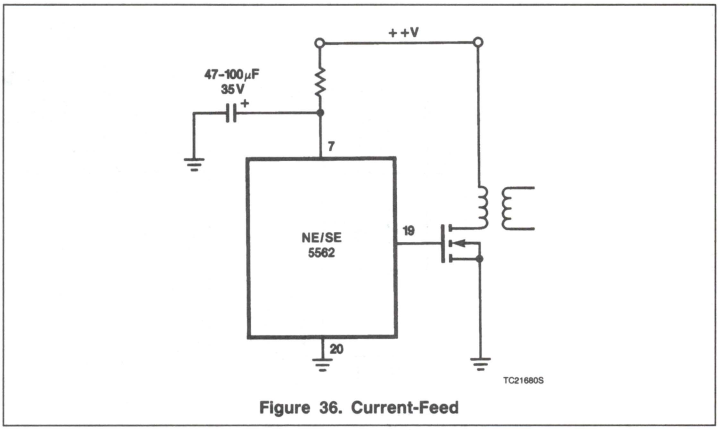


Figure 36. Current-Feed

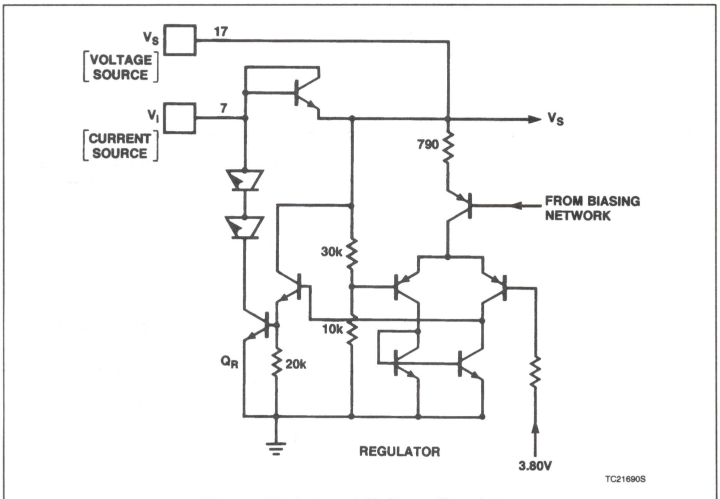


Figure 37. Internal Voltage Regulator

Design Example — An NE5562N is operated at 40°C ambient in the voltage-fed mode with V_S = 15V; assume I_S = 22mA average:

$$\therefore P_D = (22 \times 10^{-3})(15)$$
$$= 330\text{mW}$$

Solving for the temperature rise from ambient to the IC functions:

$$\text{Temperature rise} = 61°\text{C/W} \times 0.33\text{W}$$
$$= 20.1°\text{C}$$

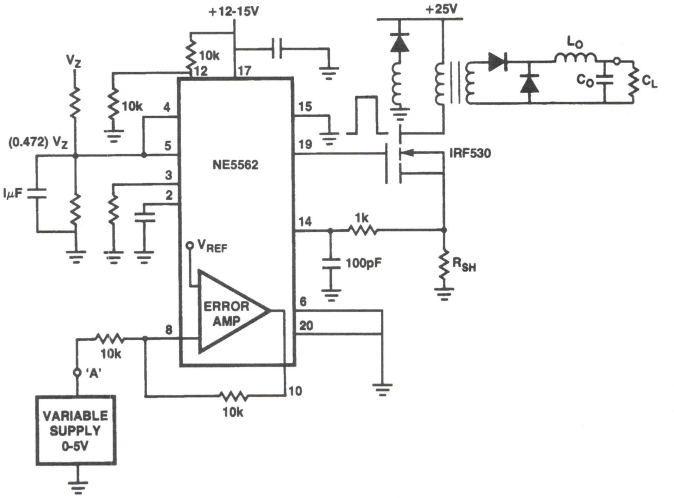
Junction temperatures will be 20.1°C above average ambient temperatures which is 40°C.

$$T_J = 40°\text{C} + 20.1°\text{C} = 60.1°\text{C}$$

The allowable maximum junction temperature is 150°C. 125°C is more conservative. The conditions of this example are safe.

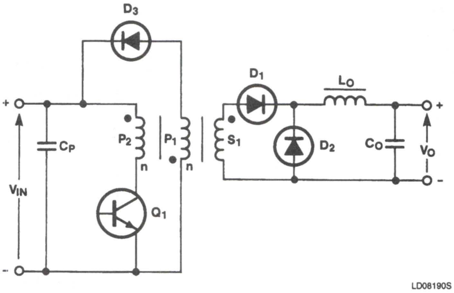
NOTE:

[1] See Figures 5 and 6 for Internal Regulator Response Curves.


+12-15V
+25V
10k
12
17
V_Z
10k
4
15
(0.472) V_Z
5
19
NE5562
IRF530
3
2
1μF
14
1k
V_{REF}
100pF
R_{SH}
ERROR AMP
6
20
8
10k
'A'
10
10k
VARIABLE SUPPLY 0-5V
L_O
C_O
C_L
TC21701S

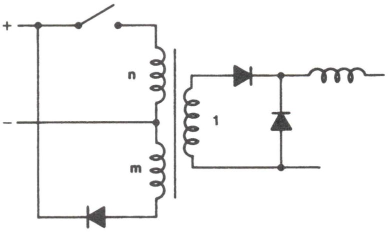
NOTES:
1. Supply will become active as point 'A' reaches the level of V_{REF}, 3.80V.
2. Monitor Pin 19 and Pin 2 on dual-trace scope with voltmeter connected to supply output.

Figure 38. Open-Loop Test Setup


D_3
D_1
L_O
+
C_P
P_2
P_1
S_1
D_2
C_O
V_O
n
n
V_{IN}
Q_1
-
+
-
LD08190S

NOTE:
The P_1 clamp winding prevents collector voltage from exceeding 2X V_{IN} during off time.

Figure 39. Forward Converter



To Prevent Core Saturation Due to Flux Staircasing

$$\boxed{\delta_{max} < 1 - \frac{m}{m+n}}$$ if $m = n$ $\delta_{max} < .5$

Demagnetization of Core

$$\boxed{V_{CE\ max} = V_{I\ max} \times \frac{m+n}{m} \quad (V)}$$

Maximum Voltage Across Transistor

Figure 40. Forward Converter Design Formulas

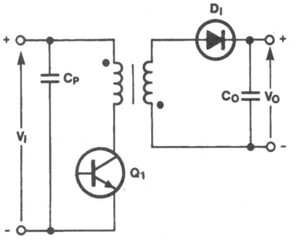


Figure 41. Isolated Secondary

Flyback Converter Design

Flyback Converter

Advantages:

- Simple circuit. Only one inductive component even with line isolation.
- Economic. Low component count, low cost.
- Work over large input voltage variations.
- Can accommodate multiple outputs.

Disadvantages:

- Large output ripple current due to discontinuous energy transfer.
- Large output capacitor; has to supply part of the load current.
- Low leakage inductance required to prevent high voltage spikes at the switching transistors.
- Relatively large core volume for the output power. Core driven in one direction only.

Design Parameters for Flyback Inductor

Input

- Minimum input voltage
- Maximum input voltage

Output

- Output voltage or voltages
- Output current or currents
- Output load

Frequency of Operation

Estimate of Overall Efficiency. (η)

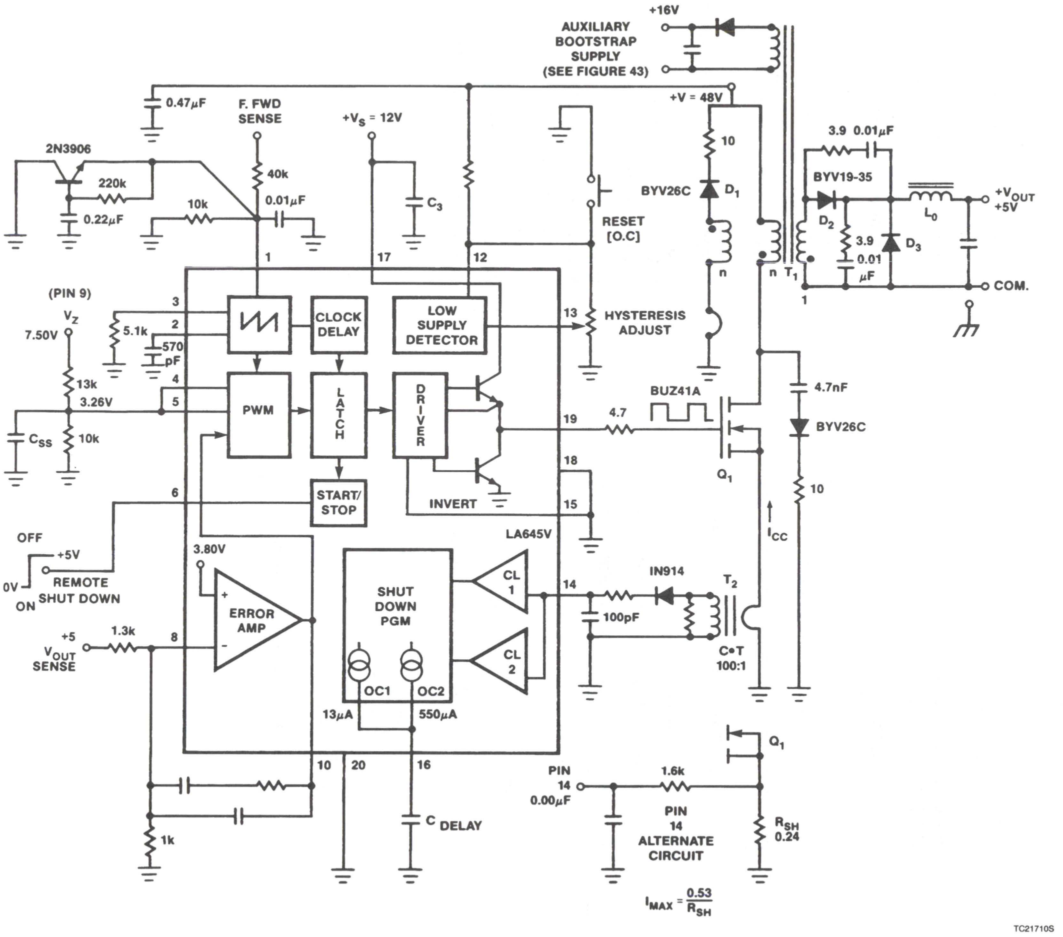

AUXILIARY BOOTSTRAP SUPPLY (SEE FIGURE 43)
+16V
+V = 48V
0.47μF
F. FWD SENSE
+V_S = 12V
2N3906
220k
0.22μF
10k
40k
0.01μF
C3
10
BYV26C
D1
RESET [O.C]
n
n
T1
3.9
0.01μF
BYV19-35
D2
3.9
0.01 μF
D3
L0
+V_OUT +5V
COM.
1
(PIN 9)
V_Z
7.50V
5.1k
570 pF
13k
3.26V
C_SS
10k
CLOCK DELAY
LOW SUPPLY DETECTOR
HYSTERESIS ADJUST
PWM
LATCH
DRIVER
START/ STOP
INVERT
BUZ41A
4.7
4.7nF
BYV26C
10
Q1
I_CC
LA645V
OFF
+5V
0V
ON
REMOTE SHUT DOWN
3.80V
ERROR AMP
SHUT DOWN PGM
CL 1
CL 2
OC1
OC2
13μA
550μA
IN914
100pF
T2
C•T 100:1
+5
V_OUT SENSE
1.3k
1k
C DELAY
1
17
12
3
2
4
5
6
8
13
19
18
15
14
10
20
16
PIN 14
0.00μF
1.6k
Q1
R_SH 0.24
PIN 14 ALTERNATE CIRCUIT
I_MAX = 0.53/R_SH
TC21710S

Figure 42. Forward Converter, 100W – 5V

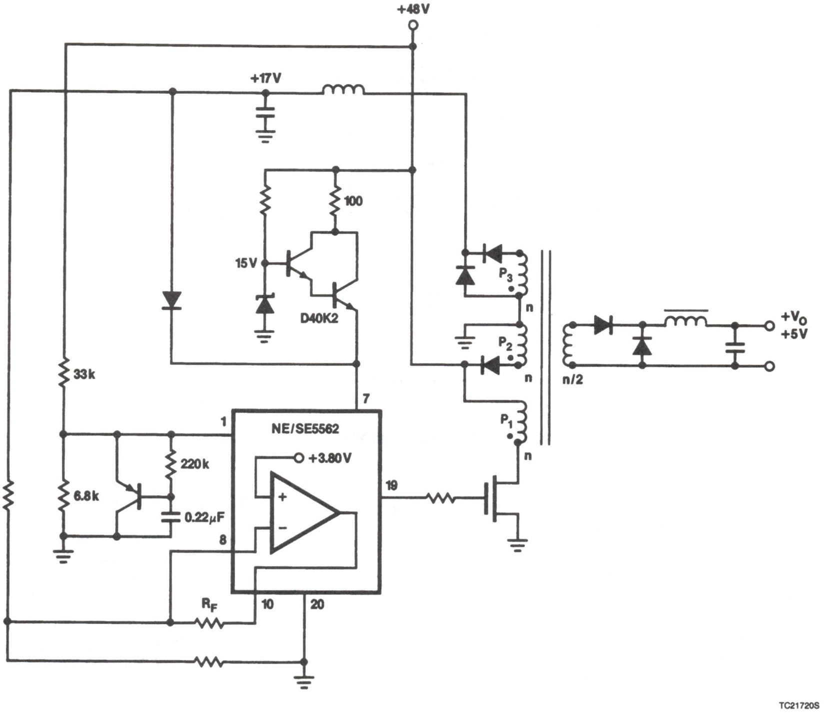
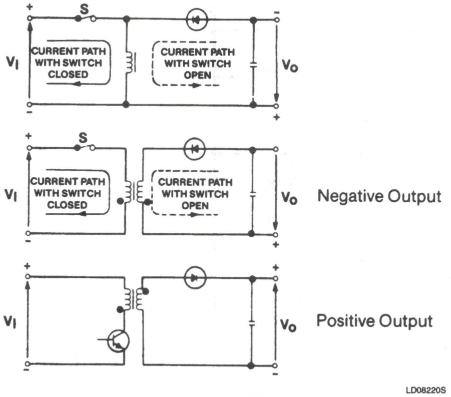
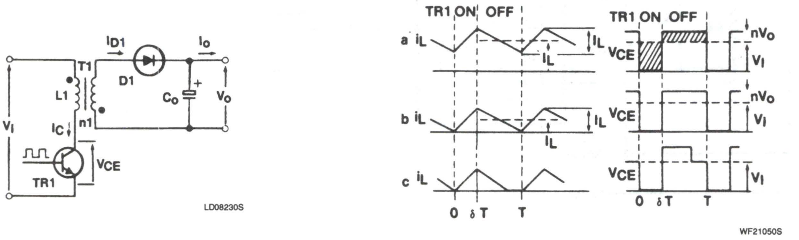

+48V
+17V
100
15V
D40K2
33k
6.8k
220k
0.22μF
NE/SE5562
+3.80V
+
−
1
7
8
19
10
20
R_F
P_3
P_2
P_1
n
n
n
n/2
$+V_O$
+5V
TC21720S

Figure 43. Shunt-Regulated Output With Bootstrap Supply


S
CURRENT PATH WITH SWITCH CLOSED
CURRENT PATH WITH SWITCH OPEN
V_I
V_O
Negative Output
Positive Output
LD08220S

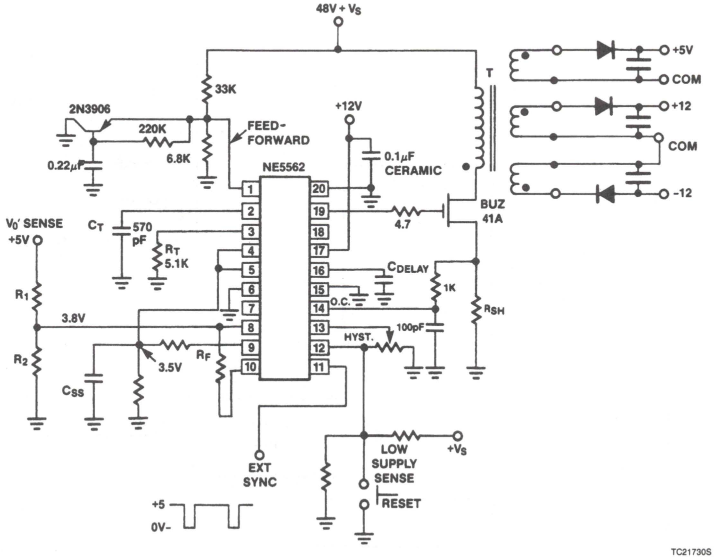
Development of Practical Flyback Converter Circuit


I_{D1}
I_o
D1
T1
L1
n1
C_o
V_o
V_I
I_C
V_{CE}
TR1
LD08230S
TR1 ON OFF
a i_L
b i_L
c i_L
Î_L
Ī_L
0 δT T
V_{CE}
nV_o
V_I
WF21050S

Flyback Converter and Current and Voltage Waveforms

NOTES:
a. Uninterrupted choke current
c. Interrupted choke current

Figure 44


48V + V_S
33K
2N3906
220K
6.8K
0.22µF
FEED-FORWARD
NE5562
+12V
0.1µF CERAMIC
T
+5V
COM
+12
COM
-12
BUZ 41A
4.7
V_0' SENSE +5V
C_T
570 pF
R_T 5.1K
R_1
3.8V
R_2
C_{SS}
3.5V
R_F
C_{DELAY}
1K
O.C.
R_{SH}
100pF
HYST.
1 2 3 4 5 6 7 8 9 10
20 19 18 17 16 15 14 13 12 11
EXT SYNC
+5
0V-
LOW SUPPLY SENSE
+V_S
RESET
TC21730S

NOTE:
400kHz operation with feed-forward line regulation and cycle-by-cycle current limiting.

Figure 45. NE5562 Flyback Converter

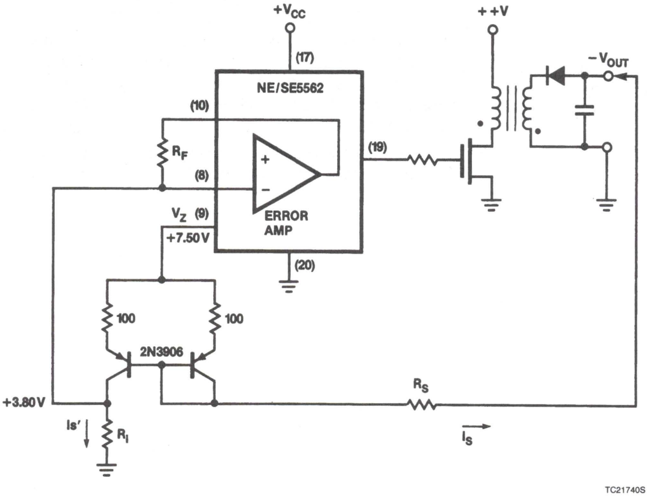

+V_{CC}
(17)
NE/SE5562
(10)
R_F
(8)
V_Z (9)
+7.50V
ERROR AMP
(19)
(20)
+ +V
-V_{OUT}
100
100
2N3906
+3.80V
Is'
R_I
R_S
I_S
TC21740S

Figure 46. Negative Output Regulator Using Current Mirror

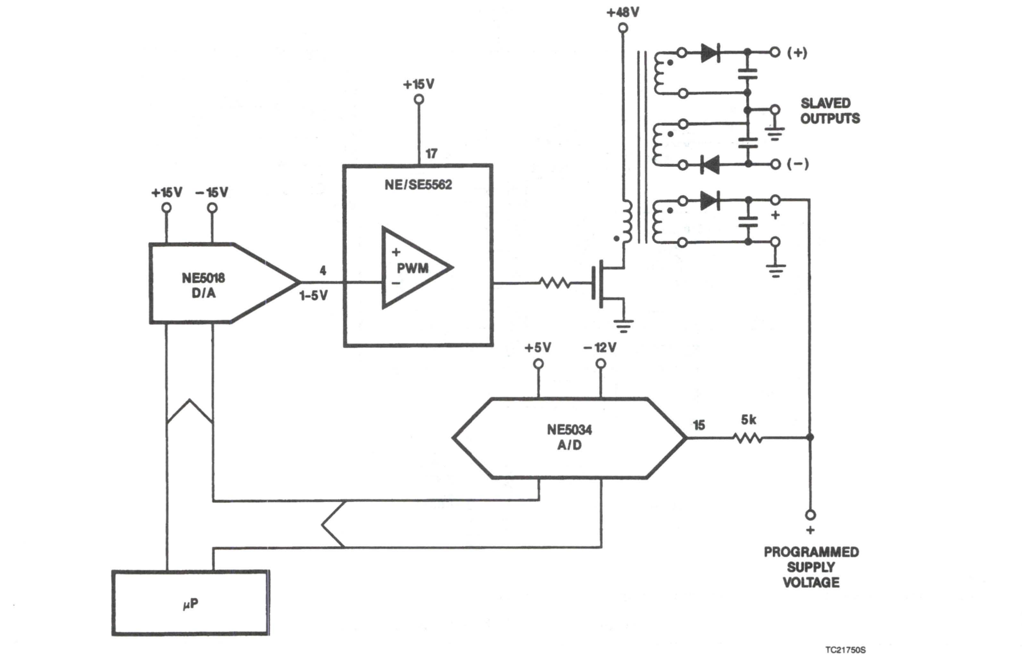

+48V
+15V
17
NE/SE5562
PWM
+15V −15V
NE5018
D/A
4
1-5V
(+)
SLAVED
OUTPUTS
(−)
+5V −12V
NE5034
A/D
15
5k
μP
PROGRAMMED
SUPPLY
VOLTAGE
TC21750S

Figure 47. Microprocessor-Controlled SMPS

REFERENCES

1. R.D. Middlebrook and Slobadan Ćuk, *Advances in Switched Mode Power Conversion*, Volumes I and II, TESLA Co., Pasadena, CA, 1983.
2. Rudolf P. Stevens and Gordon E. Bloom, *Modern DC to DC Switchmode Power Convertor Circuits*, Van Nostrand Reinhold/Computer Science and Engineering Series, 1985.
3. H. Dean Venable, *Stability Analysis Made Simple,* Venable Industries, Inc., 1981.
4. J. Jongsma and L.P.M. Bracke, *High Frequency Ferrite Power Transformer and Choke Design*, N. V. Philips ELCOMA Publications, Eindhoven, the Netherlands, September 1982.
5. Edwin S. Oxner, *Power FETs and Their Applications*, Prentice-Hall, 1982.

Signetics

Linear Products

NE5568
Switched-Mode Power Supply Controller

Product Specification

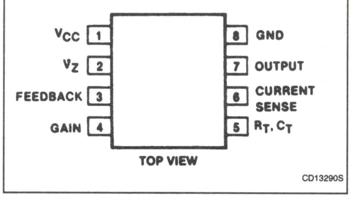
DESCRIPTION
The NE5568 is a control circuit for use in switched mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required. The NE5568 is a selected version of the NE5561.

FEATURES
- **Micro-miniature (D) package**
- **Pulse width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double-pulse protection**
- **Internal temperature-compensated reference**

APPLICATIONS
- **Switch mode power supplies**
- **DC motor controller inverter**
- **DC/DC converter**

PIN CONFIGURATION

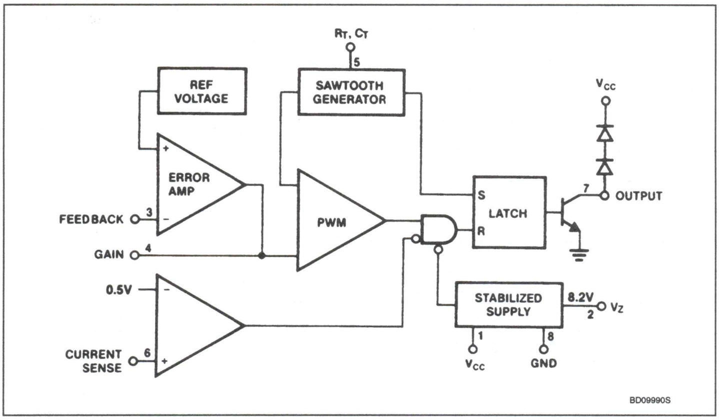
D, FE, N Packages


V_CC 1
V_Z 2
FEEDBACK 3
GAIN 4
8 GND
7 OUTPUT
6 CURRENT SENSE
5 R_T, C_T
TOP VIEW
CD13290S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5568N
8-Pin Cerdip	0 to +70°C	NE5568FE
8-Pin SO package	0 to +70°C	NE5568D

BLOCK DIAGRAM


R_T, C_T
5
REF VOLTAGE
SAWTOOTH GENERATOR
V_CC
ERROR AMP
+
−
FEEDBACK 3
GAIN 4
PWM
S
LATCH
R
7
OUTPUT
0.5V
CURRENT SENSE 6
STABILIZED SUPPLY
8.2V
2
V_Z
1
V_CC
8
GND
BD09990S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
I_{OUT}	Output current	40	mA
	Output duty cycle	98	%
P_D	Max total power dissipation	0.75	W
T_A	Operating temperature range	0 to 70	°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 12V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		NE5568			UNIT
				Min	Typ	Max	
Reference section							
V_{REF}	Internal reference voltage	$T_A = 25°C$		3.69	3.75	3.84	V
		Over temperature		3.66		3.87	V
V_Z	Internal zener ref	$I_L = 7mA$		7.8	8.2	8.8	V
	Temperature coefficient of V_{REF}				± 100		ppm/°C
	Temperature coefficient of V_Z				± 200		ppm/°C
Oscillator section							
f	Frequency range	Over temperature		50		100k	Hz
	Initial accuracy				12		%
	Duty cycle range	$f_o = 20kHz$		0		98	%
Current limiting							
I_{IN}	Input current	Pin 6 = 250mV	$T_A = 25°C$		−2	−10	μA
			Over temp.			−20	μA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	$I_{OUT} = 20mA$		0.88	1.10	μs
			$I_{OUT} = 40mA$		0.7	0.8	μs
	Current limit trip level			0.400	0.500	0.600	V
Error amplifier							
	Open-loop gain				60		dB
	Feedback resistor			10k			Ω
BW	Small-signal bandwidth				3		MHz
V_{OH}	Output voltage swing			6.2			V
V_{OL}	Output voltage swing					0.7	V
Output stage							
I_{OUT}	Output current	Over temperature		20			mA
V_{CE}	Saturation	$I_C = 20mA$, over temperature				0.4	V
		$I_C = 40mA$, over temperature				0.5	V
Supply voltage/current							
I_{CC}	Supply current	$I_Z = 0$, voltage-fed	$T_A = 25°C$			10.0	mA
			Over temp.			13.0	mA
V_{CC}	Supply voltage	I_S=10mA, current-fed		19.0	21.0	24.0	V
		$I_{CC} = 30mA$, current-fed		20.0		30.0	V
Low supply protection							
	Pin 1 threshold			8.0	9.0	10.5	V

NOTE:
All curves and applications of NE5561 apply exactly.

Signetics

Linear Products

SG1524C/2524C/3524C

Switched-Mode Power Supply Control Circuits

Preliminary Specification

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications.

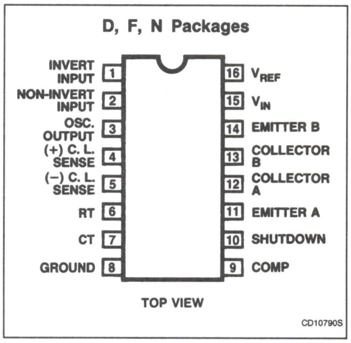
FEATURES

- **Fully interchangeable with standard SG1524 family**
- **Precision reference internally trimmed to within 1% and guaranteed**
- **High-speed current limit function**
- **Low supply protection with hysteresis**
- **200mA of output current**
- **60V output capability**
- **Wide common-mode input range for both error amp and current limit comparator**
- **Very good CMRR & PSRR for both error amp and current limit comparator**
- **Superior logic design using ECL circuits for glitch-free high-speed operation and fault protection**

APPLICATIONS

- **Switched-mode power supplies**
- **Motor control circuitry**

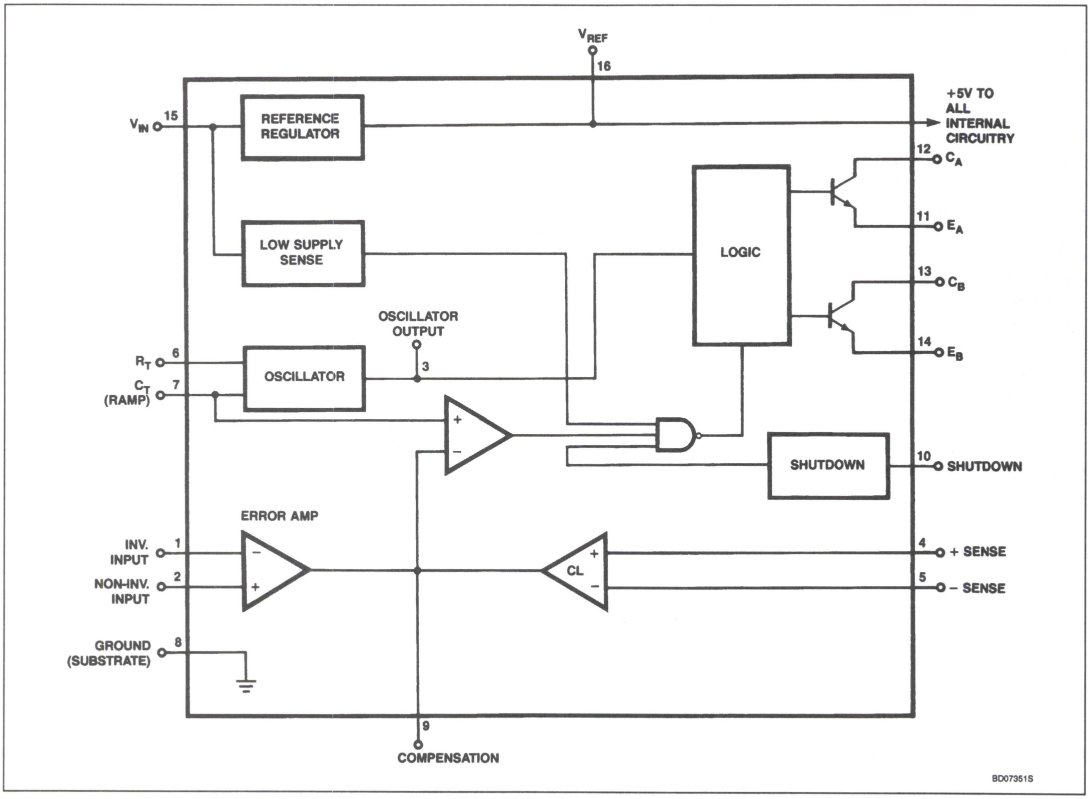
PIN CONFIGURATION


D, F, N Packages
INVERT INPUT 1
NON-INVERT INPUT 2
OSC. OUTPUT 3
(+) C. L. SENSE 4
(−) C. L. SENSE 5
RT 6
CT 7
GROUND 8
16 V_REF
15 V_IN
14 EMITTER B
13 COLLECTOR B
12 COLLECTOR A
11 EMITTER A
10 SHUTDOWN
9 COMP
TOP VIEW
CD10790S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	SG3524CN
16-Pin Ceramic DIP	0 to +70°C	SG3524CF
16-Pin Plastic SO	0 to +70°C	SG3524CD
16-Pin Plastic DIP	-40°C to +85°C	SG2524CN
16-Pin Ceramic DIP	-40°C to +85°C	SG2524CF
16-Pin Plastic SO	-40°C to +85°C	SG2524CD
16-Pin Plastic DIP	-55°C to +125°C	SG1524CN
16-Pin Ceramic DIP	-55°C to +125°C	SG1524CF

BLOCK DIAGRAM


VREF
16
+5V TO ALL INTERNAL CIRCUITRY
VIN 15
REFERENCE REGULATOR
12 CA
11 EA
13 CB
14 EB
LOGIC
LOW SUPPLY SENSE
OSCILLATOR OUTPUT
3
RT 6
CT (RAMP) 7
OSCILLATOR
SHUTDOWN
10 SHUTDOWN
ERROR AMP
INV. INPUT 1
NON-INV. INPUT 2
CL
4 + SENSE
5 – SENSE
GROUND (SUBSTRATE) 8
9
COMPENSATION
BD07351S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Supply voltage	40	V
V_C	Collector supply voltage	60	V
I_O	Output current (each output)	250	mA
I_{REF}	Reference output current[1]	50	mA
V_{REF}	Externally forced reference voltage	5.5	V
	Error amp inputs	$V_{IN}-3$	V
	Error amp max diff. voltage[2]	0.5	V
	Oscillator charging current	5	mA
	Current limit sense inputs	V_{IN}	V
	Current limit max. diff. voltage	40	V
	Shutdown inputs	5.5	V
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[3, 4] F package N package D package	 1190 1450 1090	 mW mW mW
T_J	Operating junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Short-circuit protected.
2. Inputs are clamped by two diodes. Resistors should be used to limit input current to less than 1mA maximum.
3. The power dissipation can be calculated from $P_D = I_{SB}V_{IN} + 2$ duty cycle $(I_{OUT}\ V_{CE\ ON}) + I_{REF}\ (V_{IN} - 5V) + 2I_{CT}\ (V_{IN} - 3.6)$.
4. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Supply voltage	7 to 40	V
V_C	Collector supply voltage (with emitters grounded)	0 to 60	V
I_O	Output current (each output) ($V_{CE} < 2.5V$)	0 to 200	mA
I_{REF}	Reference load current	0 to 20	mA
V_{CM}	Error amp common-mode input	1.5 to ($V_{IN} - 4$)	V
V_{CM}	Current limit amp common-mode input	0 to ($V_{IN} - 4$)	V
	Oscillator charging current	0.02 to 2	mA
R_T	Oscillator timing resistor	2 to 150	kΩ
T_A	Operating ambient temperature range		
	SG1524C	−55 to 125	°C
	SG2524C	−40 to 85	°C
	SG3524C	0 to 70	°C
T_J	Operating junction temperature range		
	SG1524C	−55 to 150	°C
	SG2524C	−40 to 125	°C
	SG3524C	0 to 125	°C
$-C_T$	Oscillator timing capacitor	0.47 to 100	nF
f_{OSC}	Oscillator frequency	0.1 to 400	kHz

DC AND AC ELECTRICAL CHARACTERISTICS Minimum and maximum limits apply over recommended operating junction temperature range, typical data applies at $T_J = 25°C$, and $V_{IN} = V_C = 20V$, $R_T = 2.7k\Omega$, $C_T = 0.01\mu F$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SG1524C/2524C			SG3524C			UNIT
			Min	Typ	Max	Min	Typ	Max	
Turn-on characteristics									
V_{IN}	Input minimum voltage	After turn-on	7		40	7		40	V
	Turn-on input voltage		4.9	6	6.5	4.9	6	6.5	V
	Input voltage hysteresis		100	240	360	100	240	360	mV
V_{REF}	Turn-on reference voltage		4.3	4.60	4.8	4.3	4.60	4.8	V
	Reference voltage hysteresis		100	240	360	100	240	360	mV
Reference section[1]									
V_{OUT}	Output voltage	Over temperature	4.9		5.1	4.9		5.1	V
V_{OUT}	Output voltage	$T_J = 25°C$	4.95	5.00	5.05	4.915	5.00	5.105	V
	Temperature stability			15	50		15	50	mV
	Line regulation	$V_{IN} = 7$ to 40V		1.0	15		1.0	15	mV
	Load regulation	$I_L = 0$ to 20mA		10	20		10	20	mV
	Total output variation	$7V < V_{IN} < 40V$, $0mA < I_L < 20mA$	4.90	5.0	5.10	4.90	5.0	5.10	V
I_{OUT}	Maximum output current	$V_{REF} = 0V$	−120	−60	−25	−120	−60	−25	mA
	Output noise voltage	$10Hz < f < 10kHz$, $T_A = 25°C$		170			170		μV_{RMS}
	Long-term stability	$T_A = 25°C$, 1khrs		20			20		mV
RR	Ripple rejection	$T_A = 25°C$, $f = 2400Hz$		60			60		dB
Oscillator section									
	Initial frequency		38	41	44	38	41	44	kHz
	Frequency temp. stability				2			2	%
	Voltage stability	$V_{IN} = 7$ to 40V		0.5	1.0		0.5	1.0	%
	Sawtooth peak voltage	$V_{IN} = 40V$	3.2	3.5	3.8	3.2	3.5	3.8	V
	Sawtooth valley voltage	$V_{IN} = 7V$	0.5	.75	1.0	0.5	.75	1.0	V
	Clock amplitude		2.85	3.4		2.85	3.4		V
	Clock pulse width	Measured level = 2.0V	.25	0.5	.75	.25	0.5	.75	μs
f_{MIN}	Minimum frequency	$R_T = 150k\Omega$, $C_T = 0.1\mu F$		100			100		Hz
f_{MAX}	Maximum frequency	$R_T = 2k\Omega$, $C_T = 470pF$, $T_J = 25°C$		550			550		kHz
f_{MAX}	Maximum frequency	$R_T = 2k\Omega$, $C_T = 470pF$	400			400			kHz
f_{MAX}	Maximum frequency	$R_T = 2k\Omega$, $C_T = 1nF$	290			290			kHz
I_{CT}	CT charging current	$I_{RT} = -2mA$[4]	−2.0	−1.86	−1.7	−2.0	−1.86	−1.7	mA
	Saturation voltage	$I_{CT} = 5mA$, $V_P3 = 5V$	.55	0.72	1.0	.55	0.72	1.0	V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

Minimum and maximum limits apply over recommended operating junction temperature range, typical data applies at $T_J = 25°C$, and $V_{IN} = V_C = 20V$, $R_T = 2.7k\Omega$, $C_T = 0.01\mu F$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SG1524C/2524C			SG3524C			UNIT
			Min	Typ	Max	Min	Typ	Max	
Error amplifier section[2]									
V_{OS}	Input offset voltage	$R_S = 2k\Omega$		1.0	5.0		1.0	10	mV
I_{BIAS}	Input bias current	$R_S = 1k\Omega$		1.0	5.0		1.0	10	µA
I_{OS}	Input offset current	$R_S = 1k\Omega$		0.04	1.0		0.04	1.0	µA
CMRR	Common-mode rejection ratio	$V_{CM} = 1.5$ to $12.5V$	75	85		75	85		dB
PSRR	Supply voltage rejection ratio	$V_{IN} = 7$ to $40V$	80	93		80	93		dB
	DC open-loop gain	$C_L = 0.01\mu F$ $V_9 = 1$ to $4V$	60	79		60	79		dB
	Gain bandwidth product	$T_A = 25°C$, $A_V = 0B$	2	5		2	5		MHz
	Output low level	$I_{SINK} = 100\mu A$, $V_{CC1}1 - V_{CC2} > 0.15V$		0.3	0.5		0.3	0.5	V
	Output high level	$I_{SOURCE} = 100\mu A$, $V_2 - V_1 > 0.15V$	5.0	5.6	6.0	5.0	5.6	6.0	V
	Output sink current	$V_1 - V_2 > 0.15V$, $V_9 = 2.5V$	100	136	170	100	136	170	µA
	Output source current	$V_2 - V_1 > 0.15V$, $V_9 = 2.5V$	−170	−140	−100	−170	−140	−100	µA
PWM comparator section									
	Minimum duty cycle	$V_2 = 0.5V$, $V_9 = V_1$			0			0	%
	Maximum duty cycle	$V_2 = 3.9V$, $V_9 = V_1$	45	48.7	50	45	48.7	50	%
	Duty cycle for max. freq.	$V_2 - V_1 > 0.15V$, $Rt = 2k\Omega$, $C_T = 470pF$	32		42	32		42	%
I_{BIAS}	Input bias current	$I_{RT} = 0mA$, $V_2 = 2.5V$, $V_9 = V_1$	−5.0		0	−5.0		0	µA
	Propagation delay to output			0.5			0.5		µs
Current-limiting section[2]									
	Sense voltage		180		220	170		230	mV
I_{BIAS}	Input bias current	$R_S = 10k\Omega$, $V_2 - V_1 > 0.15V$	−5		0	−5		0	µA
CMRR	Common-mode rejection ratio	$V_{CM} = 0$ to $12.5V$	50	90		50	90		dB
PSRR	Power supply rejection ratio	$V_{IN} = 7$ to $40V$	50	90		50	90		dB
V_{OL}	Output low voltage	$V_2 - V_1 > 0.15V$, $V_4 - V_5 > 0.3V$	0	0.28	0.2	0	0.28	0.2	V
t_{PD}	Propagation delay to output			0.7			0.7		µs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Minimum and maximum limits apply over recommended operating junction temperature range, typical data applies at $T_J = 25°C$, and $V_{IN} = V_C = 20V$, $R_T = 2.7k\Omega$, $C_T = 0.01\mu F$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SG1524C/2524C			SG3524C			UNIT
			Min	Typ	Max	Min	Typ	Max	
Shutdown input									
I_{BIAS}	Input bias current	$T_J = 25°C$, $V_{10} = 1V$	10		200	10		200	µA
	Shutdown threshold voltage	$T_J = 25°C$	0.6	0.8	1.0	0.6	0.8	1.0	V
	Shutdown threshold voltage		0.4		1.3	0.4		1.3	V
t_{PD}	Propagation delay to outputs			0.5			0.5		µs
Output section (each output)									
V_{CE}	Collector emitter voltage	$I_C = 100\mu A$	60	75		50	75		V
	Collector leakage current	$V_{CE} = 60V$, $V_{10} = 1.5V$		0.1	20		0.1	20	µA
	Collector saturation voltage	$I_C = 20mA$		0.2	0.4		0.2	0.4	V
	Collector saturation voltage	$I_C = 200mA$		1.2	2.0		1.2	2.0	V
	Emitter output voltage	$I_E = 20mA$	17.5	18		17.5	18		V
	Emitter output voltage	$I_E = 200mA$	16.5	17.5		16.5	17.5		V
t_R	Collector rise time Emitter rise time	$T_A = 25°C$, $I_C = I_E = 10mA$, $C_L = 15pF$		0.5 0.1	0.6 0.2		0.5 0.1	0.6 0.2	µs µs
t_F	Collector fall time Emitter fall time	$T_A = 25°C$, $I_C = I_E = 10mA$, $C_L = 15pF$		0.1 0.1	0.2 0.2		0.1 0.1	0.2 0.2	µs µs
Total supply current^3									
I_{SB}	Standby supply current	$V_{IN} = 40V$, $I_{RT} = 0mA$, $V_{10} = 1.5V$		9.0	11.0		9.0	11.0	mA
I_{CC}	Operating supply current	$V_{IN} = 40V$, $I_C = I_E = 10mA$		11	15		11	15	mA

NOTES:
1. Unless otherwise specified, $I_L = 0mA$.
2. Unless otherwise specified, $V_{CM} = 2.5V$.
3. Unless otherwise specified, $I_{REF} = 0mA$.
4. I_{RT} is the current into Pin 6.

Signetics

AN1261

High-Frequency Ferrite Power Transformer and Choke Design

Application Note

Linear Products

Authors:
L. P. M. Bracke,
F. C. Geerlings, and
J. Jongsma

PART 1: SWITCHED-MODE POWER SUPPLY MAGNETIC COMPONENT REQUIREMENTS

In switching power supplies, problems often arise with the design of the magnetic components, the ferrite-cored transformers, and chokes. The interaction between electronic and magnetic design deserves particular attention. Firstly, in switched-mode power supplies (SMPS), the power transformer and choke, and the electronic circuitry, are so interdependent that design is hardly possible without the magnetic aspects being constantly taken into account. Secondly, by combining magnetic and electronic design, a far better insight is gained into the operation of the circuit, with a consequent improvement in the design itself.

This application note covers most aspects of switching power supply design, with emphasis on the magnetic aspects. Here, the basic electrical relationships for SMPS are given for forward, push-pull, and flyback converters. Practical formulas are given for inductance and effective-current values; auxiliary outputs and other special features are also covered. Some aspects of control are treated. All treatments are related to the magnetic design.

THE FORWARD CONVERTER

Non-isolated

Principle of Operation

Figure 1 shows the outline circuit of a forward converter. The basic operation of an ideal converter is described by

$$V_O = \delta V_I \tag{1}$$

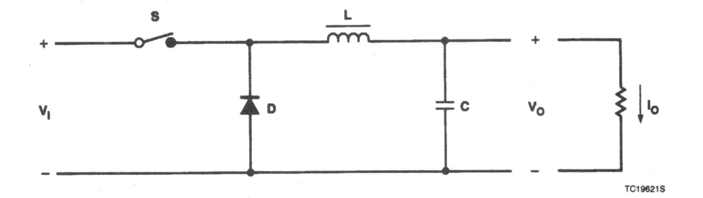


Figure 1. Outline Circuit of a Forward-Converter Switched-Mode Power Supply

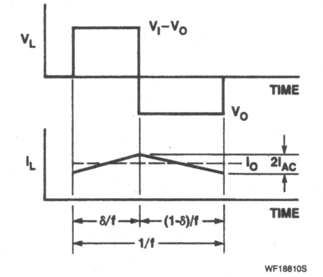


Figure 2. Voltage Waveform Across the Power Choke in a Forward-Converter SMPS, and the Associated Current Waveform

Figure 2 shows the voltage waveform across the inductance and the associated current waveforms.

NOTE:
All symbols for quantities used here are listed in the Table.

Minimum Choke Inductance

For continuous-mode operation (uninterrupted current flow through the choke) — otherwise, regulation deteriorates — output current I_O must always be greater than half the choke ripple current $2I_{AC}$. This is ensured by using a minimum value for the choke inductance

$$L_{MIN} = \frac{1}{2f}\,\frac{V_O}{I_{O\,MIN}}\left(1 - \delta_{MAX}\,\frac{V_{I\,MIN}}{V_{I\,MAX}}\right) \tag{2}$$

An increase in δ as a result of a sudden load increase will cause a temporary increase in choke ripple current. As long as the ripple component is much smaller than the DC component, which is usually the case, this does not affect the design of the choke.

Choke Design

Output choke L carries a direct current equal to the DC current in the load. Thus, to avoid saturation, an airgap is required in the core. The design steps are:

- Determine $I_M = \sigma I_{O\,MAX} + I_{AC}$
- Calculate $I_M^2 L_{MIN}$
- Proceed to Part 4 of this series.

For core loss, see Part 2.

Deriving Auxiliary Power from the Choke

During the flywheel period (1 – δ)/f, that is, while the power switch is not conducting, the voltage across the choke is stabilized. By adding secondary windings to the choke, auxiliary stabilized low voltages can be obtained as shown in Figure 3.

High-Frequency Ferrite Power Transformer and Choke Design

AN1261 Part 1

LIST OF SYMBOLS

SYMBOL	UNIT*	DEFINITION
A_{CP}	m^2	Core center-pole cross-sectional area
$A_{CP\,MIN}$	m^2	Minimum core center-pole cross-sectional area
A_e	m^2	Effective core cross-sectional area
B_{AC}	T	Flux-density sweep; half the peak-to-peak flux density excursion
$B_{AC\,OPT}$	T	Optimum center pole peak flux density sweep for maximum throughput power
B_{CF}	mm	Coil former (or winding window) breadth
dV/dt	V/s	Maximum permissible rate of voltage increase
f	Hz	Operating frequency
f_R	Hz	Resonant frequency of transformer primary and slow-rise capacitor combination
H_{CF}	mm	Height of coil former or winding window
I_{AC}	A	Half peak-to-peak current ripple
I_E	A	RMS current at full load
I_M	A	Peak choke current
I_{magM}	A	Maximum (peak) transformer magnetizing current
I_{maxM}	A	Maximum peak inductor current
I_O	A	Power supply output (load) current
$I_{O\,MIN}$	A	Minimum required output (load) current
$I_{O\,MAX}$	A	Maximum required output (load) current
$I_{I\,M}$	A	Peak primary current
k	–	$P_{AUX}/P_{AUX\,MAX}$
ℓ_{AV}	m	Average turn length
ℓ_e	m	Effective magnetic path length in a core
L	H	Choke inductance
L_{AUX}	H	Inductance of choke with auxiliary winding
L_{MIN}	H	Minimum required value of L
L_s	H	Stray inductance of power supply output circuit
m	–	Ratio of demagnetizing (energy-recovery) winding turns to secondary winding turns
n	–	Number of turns
N	–	Number of turns in a winding portion
N_D	–	Number of turns in main choke winding
N_{PRIM}	–	Integral, rounded number of primary turns
P	W	Power
P_C	W	Total transformer core loss
P_E	W	Eddy-current loss in a core
P_H	W	Hysteresis loss in a core
P_{IN}	W	Converter input power
P_L	W	Power absorbed in a choke
$P_{O\,MAX}$	W	Maximum output power used for choke design
$P_{O\,MIN}$	W	Minimum output power used for choke design
P_{TH}	W	Transformer throughput power
P_W	W	Dissipation in transformer windings
r	–	Transformer turns ratio
θ_{JC}	°C/W	Transformer or choke thermal resistance with winding creepage distance incorporated
θ_{JN}	°C/W	Transformer or choke thermal resistance for a winding without creepage distance
t_C	s	Commutation time
t_F	s	Turn-off (fall) time of power switch
V_{AUX}	V	Voltage on auxiliary winding
V_{CEM}	V	Maximum voltage across power switch
V_{CESM}	V	Maximum collector-emitter voltage for a power-switching transistor with the base-to-emitter voltage $V_{BE} \leqslant 0$
V_e	m^3	Effective volume of a core
V_F	V	Voltage drop across output choke and leads
V_I	V	Steady state (DC) input voltage to a converter
$V_{I\,BO}$	V	'Brown-out' converter input voltage
$V_{I\,MAX}$	V	Maximum (peak) converter input voltage
$V_{I\,MIN}$	V	Minimum (trough) converter input voltage (including drop-out)
V_{IR}	V	Peak-to-peak converter input-voltage ripple
V_O	V	Output (load) voltage
$V_{O\,MAX}$	V	Maximum output voltage
V_R	V	Voltage drop of output rectifier
V_R	V	Overshoot (ringing) voltage allowance
x	%	Feedforward factor. The maximum % increase in duty factor allowed by the control in response to a sudden load change
z	–	Proportionality factor
α	–	Ratio of core saturation flux to working flux allowed: for transient response without saturation
β	–	Voltage-limiting factor
δ	–	Duty factor of power switch
δ_{MAX}	–	Maximum permitted duty factor
δ_{MIN}	–	Minimum duty factor
$\delta_{O\,MAX}$	–	Maximum duty factor under steady-state conditions
δ_{TR}	–	Transient duty factor
ΔI_O	A	Step change in load current
ΔT	°C	Temperature rise above ambient
ϵ	–	Unbalance factor
μ_a	–	Amplitude permeability at a stated mean flux density and for a stated variation
μ_e	–	Effective relative permeability
μ_0	H/m	Permeability of free space: $4\pi \times 10^{-}$ H/m
σ	–	Ratio of setting of overcurrent trip to rated output current

SUBSCRIPTS

1	Pertains to a transformer primary or (in winding design) primary winding portion
2	Pertains to a transformer secondary or (in winding design) secondary winding portion
AUX	Pertains to an auxiliary winding
CP	Pertains to center pole of an E or EC core, or to the wound leg of a U core
e	Effective value
L	Pertains to choke

SUPERSCRIPT

′	(as in r′) a preliminary (not rounded) value

* unless otherwise stated.

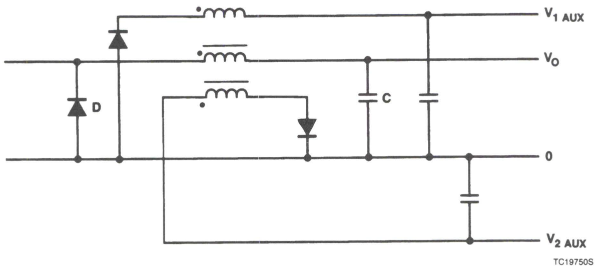


Figure 3. Auxiliary Low-Voltage Outputs can be Obtained by Adding Windings to the Choke of a Forward Converter

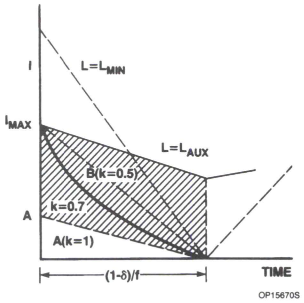


Figure 4. Current Through a Forward-Converter Choke With Auxiliary Windings

These auxiliary voltages are rectified by diodes that conduct during the flywheel period. Since auxiliary loads decrease the amount of energy recovered by flywheel diode D, the amount of auxiliary power that can be derived is limited to 20 – 30% of the total output power.

In order to store sufficient energy in the choke to supply an auxiliary load, inductance L_{MIN} calculated from Equation 2 must be increased to L_{AUX}. This might lead to the use of a larger core: see Part 4.

The relationship between L_{MIN} and L_{AUX} is

$$L_{AUX} > L_{MIN}/\left\{1-\left((0.3 \text{ to } 0.4)\ \frac{1}{1-\delta_{MAX}}\right)\right\} \tag{4}$$

The factor (0.3 to 0.4) corresponds to an auxiliary load being 20 – 30% of the total. If output ripple is not important, a higher proportion of auxiliary load can be drawn.
The turns ratio

$$r \approx V_O/V_{AUX} = N_D/N_{AUX} \tag{5}$$

During forward conversion, during the period δ/f, the input power

$$P_{IN} = \delta V_I I_O$$

Similarly, the throughput power

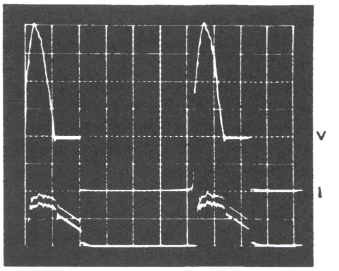
$$P = \delta V_O I_O$$

The difference is the power stored in and then removed from the choke:

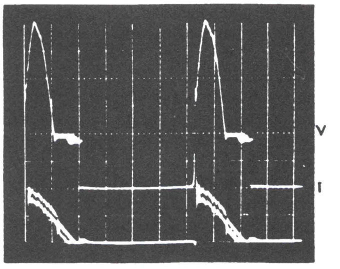
$$P_L = P_{IN} - P = \delta I_O\ (V_I - V_O)$$

From Equation 1,

$$\begin{aligned} P_L &= \delta I_O\ (V_I - \delta V_I) \\ &= \delta V_I I_O\ (1 - \delta) \\ &= P_{IN}\ (1 - \delta) \end{aligned}$$



a. L > L_{AUX}



b. L < L_{AUX}

NOTE:
These oscillograms were taken from a TV power supply, hence the voltage peaks.

Figure 5. Oscillogram of Choke Waveforms

High-Frequency Ferrite Power Transformer and Choke Design

AN1261 Part 1

If, during flywheel period $(1-\delta)/f$, the choke current is divided between output and flywheel diodes as indicated in Figure 4 by line A, P_{AUX} is maximum ($P_{AUX\ MAX}$). The current below A is that through the flywheel diode of the primary output. Figure 5 shows some waveforms.

Due to leakage induction, flywheel diode current does not begin at A, but at I_{MAX}, as the auxiliary output currents are then zero. This decreases the value of $P_{AUX\ MAX}$. If the current is shared according to line B in Figure 4, $P_{AUX} = kP_{AUX\ MAX}$, where $k = 0.5$. In practice, k will be somewhat higher: a value of $k = 0.7$ is reasonable.

If $L = L_{MIN}$, no auxiliary power can be drawn. From these considerations it follows that the auxiliary power that can be obtained is limited and depends on k, δ, and L, such that

$$P_{AUX} \leqslant k(1-\delta)\ (1-L_{AUX}/L_{MIN})\ P_{IN}$$

The required value of L_{AUX} is obtained from

$$L_{AUX} > L_{MIN}/\{1-\frac{P_{AUX}}{kP_{TOT}(1-\delta_{MAX})}\}$$

Substituting $k = 0.7$ and $P_{AUX}/P_{TOT} = (0.2$ to $0.3)$ yields Equation 4.

$$(P_{TOT} = P_{TH} - I_O(V_F + V_R + V_O))$$

Single Forward-Converter With Isolating Transformer

Principle of Operation

The outline circuit of a forward-converter with power line isolation is given in Figure 6.

The magnetic energy stored in the transformer while S is ON must be removed while S is OFF, otherwise the energy stored and removed during a complete switching cycle would not be zero and the transformer core would rapidly saturate. A solution involving minimum power loss is to add a winding, closely coupled to the primary, and a diode D_3 such that a flow of magnetizing current is ensured while S is OFF.

The operation of the transformer-isolated forward-converter is described by the same basic expression, Equation 1, as was used for the non-isolated version. The transformer also adds an extra degree of freedom of choice of output voltage for practical values of δ. This output voltage becomes

$$V_O = \frac{\delta V_I}{r} \tag{6}$$

Voltage and current waveforms for a transformer-isolated forward-converter are given in Figure 7.

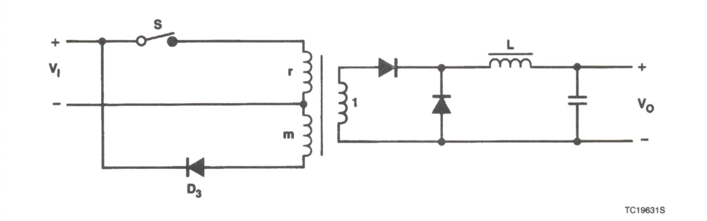


Figure 6. Outline Circuit of a Power Line-Isolated Forward-Converter SMPS

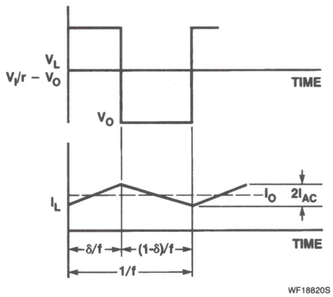


Figure 7. Output Circuit Waveforms for the Power Line-Isolated Forward-Converter

Duty Factor

The maximum allowable duty factor at which the core will not saturate due to flux staircasing depends on r and m:

$$\delta_{MAX} < 1 - \frac{m}{m+r} \tag{7}$$

The maximum voltage across the power switch (here, a transistor) is then

$$V_{CEM} = V_{I\ MAX}\frac{m+r}{m} \tag{8}$$

When using a transistor with $V_{CESM} = 850V$ in a forward-converter with a maximum (rectified) input voltage of 375V, it is usually adequate to limit V_{CE} to $2 \times 375 = 750V$. Thus, with $m = r$, there is 100V to spare for ringing and integrated supply voltage surges.

The effective duty factor depends on frequency, turns ratio, r, rated load current, the leakage inductance of the transformer and the inductance of the leads to the output diodes.

As a guide for power line operated SMPS, decrease the conduction time so that

$$\delta_e/f = \delta/f - rI_O \times 1.2 \times 10^{-9} \tag{9}$$

The inductance of the leads to the output diodes is reflected into the primary as the square of the turns ratio. With large turns ratios, combined with high switching currents, the loss due to communication delay becomes substantial. The effect is as if the available duty factor is decreased.

In Figure 8a,

$$t_C \approx I_O r L_S / V_I$$

Now, L_S is about 1 nH/mm of leads and, for a 220V power line supply, $V_{I\ MIN} \approx 200V$. With the shortest possible leads to the output diodes, experiment shows that the commutation delay is

$$t_C \approx 1.2 I_O r \times 10^{-9}$$

This is an important reason for not operating low-voltage high-current SMPS at high frequencies, but, rather, to use a frequency just above the audible range.

Preliminary Turns Ratio and Core Selection

The preliminary turns ratio

$$r' = \frac{\delta_{E\ MAX}\ V_{I\ MIN}}{V_{O\ MAX} + V_F + V_R} \tag{10}$$

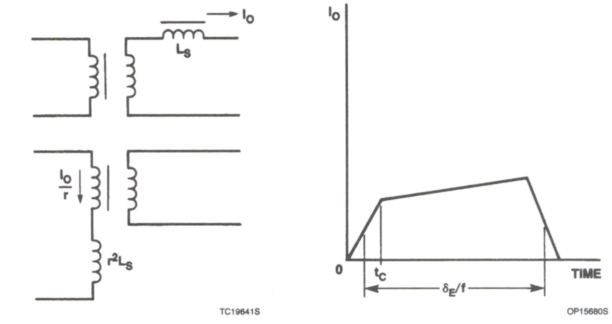
For transformer core selection, see Part 2.

Multiple-Output Transformers

Additional outputs at any DC level can be obtained simply by adding further secondaries of the appropriate number of turns to the output transformer. The regulation of the additional outputs will be better than with a flyback converter. However, each output needs two diodes and a power choke, against the single diode needed with a flyback converter.

Warning: the flywheel diode *must* always conduct when the forward diode does not. Otherwise, peak forward-conversion rectification occurs and the output voltage could rise to the peak value of the forward-conversion voltage, which might be much higher than the nominal voltage, with disastrous results. So, ensure that the appropriate minimum load is always present at each output.

With several different outputs, it is necessary to find that value of volts-per-turn for the transformer that allows each output voltage to be obtained within the permitted tolerance



a. Inductance in the Secondary is Reflected Back into the Primary as the Square of the Turns Ratio

b. There is a Delay, t_C, During Which Neither Output Diode Conducts

Figure 8. Effect of Stray Inductances in the Output Circuit of an Isolated Forward-Converter

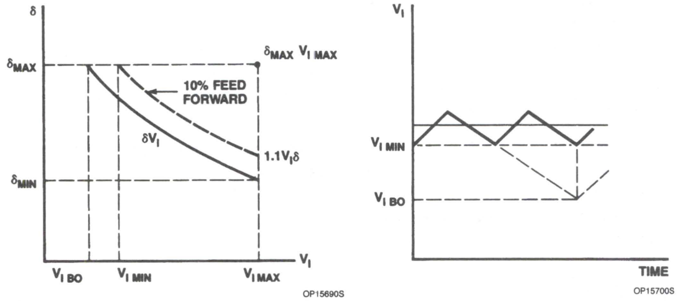


Figure 9. Input Voltage and Duty Factor Combinations Under Transient Load Conditions for Feedback and Feed-forward Control

with an integral number of turns. The procedure for this is described in Part 3.

Control Method

The function of the control circuit is to stabilize the output against variations in input voltage and load by adjusting the duty factor of the switching device. However, the effect of step load changes cannot be corrected immediately because some time is needed for the current through the choke to assume the new value of the load current.

A momentary change in output voltage is thus inevitable. The time required for resumption of the desired level of output voltage after the sudden load change depends greatly on the properties of the control system. Two basic control characteristics can be distinguished (See Figure 9).

Feedback — A step increase in load current causes the power switch duty factor to increase instantly to its maximum value δ_{MAX}, regardless of the level of input voltage. It is thus possible for $(\delta V_I)_{MAX} = \delta_{MAX}V_{I\ MAX}$.

Feed-forward — A step rise in load current causes the power switch duty factor to increase to a value x% higher than its steady-state value for a constant load.

The $(\delta V_I)_{MAX}$ product in response to a step load increase will be higher with feedback control. This results in a shorter delay in adjusting to the new load because the choke current is forced to increase at a maximum rate. However, the output transformer must be so designed that it is able to cope with the product $\delta_{MAX}V_{I\ MAX}$ without saturating.

With feed-forward control,

$$(\delta V_I)_{MAX} = (1 + \frac{x}{100})\,\delta_{MIN}V_{I\ MAX}$$

The corresponding value of α for the transformer design is

$$\alpha = 1 + \frac{x}{100}$$

Difficulties may be encountered with converter starting at full load with minimum power line voltage (15% below nominal). If the duty factor is close to maximum, all the output current will flow into the load and little or no current will be available to charge the output capacitor. Starting will be improved if the steady-state value of the duty factor is 10% below its maximum allowable value.

One disadvantage of feedback control is that a larger transformer core is generally required to avoid saturation.

Primary Inductance and De-Saturation

The primary inductance is given by

$$L_1 = \mu_0\mu_a n_1^2 A_e/\ell_e \qquad (11)$$

where the value of μ_a is obtained from the core data.

The maximum, peak, primary magnetizing current is

$$I_{magM} = \frac{(\delta V_I)_{MAX}}{L_1 f} \qquad (12)$$

The peak primary current is

$$I_{1M} = \frac{1}{r}(I_O + \frac{I_{O\ MIN}}{2}) + I_{magM} \qquad (13)$$

Primary inductance L_1 together with slow-rise dV/dt capacitor C (Figure 10) across the switch forms a resonant circuit with a natural frequency

$$f_r = 1/\{2\pi\sqrt{(L_1C)}\} \qquad (14)$$

The value of C used should satisfy the relationship

$$\frac{I_{1M}t_F}{2V_{CESM}} = C > I_{1M}/(dV/dt)$$

It is recommended that $f_r > f$. At a lower value of f_r, the core might fail to desaturate and flux staircasing could occur, with disastrous results. A higher f_r offers sufficient safety margin under all conditions; a ratio $mf_r/(rf)$ of about 1.2 is a good compromise. An electronic solution to the problem can be found in some control ICs (e.g., TDA1060) where there is a facility for reducing the duty factor when core saturation is possible.

High-Frequency Ferrite Power Transformer and Choke Design

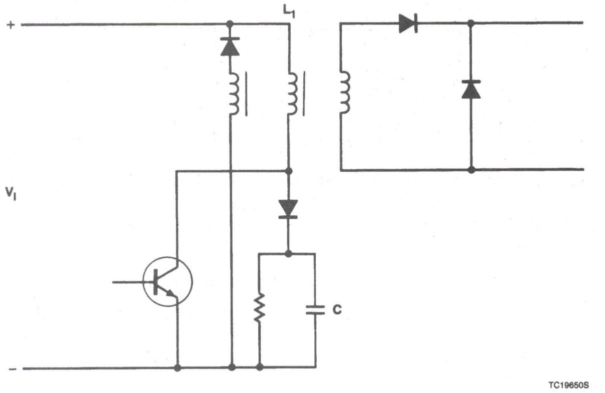


Figure 10. Forward-Converter Transformer With Magnetizing (Energy Recovery) Winding, and a Slow-Rise Capacitor in the Primary

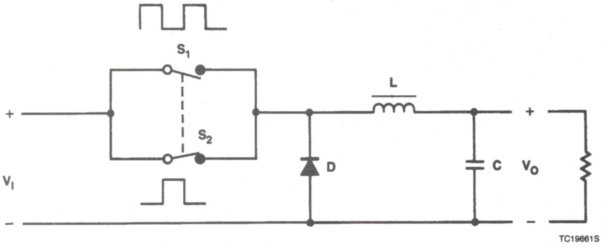


Figure 11. Outline Circuit of a Double-Forward SMPS Converter. Switches S_1 and S_2 Operate Alternately

The value and spread of L_1 may be reduced by introducing an airgap in the core; the penalty is higher magnetizing current. The spacer thickness required is generally smaller than the range for which the I^2L curves discussed in Part 4 apply. For these small values of spacer thickness S (total airgap 2S), the value of μ_e (and, thus, L_1) can be obtained for cores of *constant cross-sectional area* from

$$s = \frac{\ell_e}{2}\left(\frac{1}{\mu_e} - \frac{1}{\mu_a}\right) \qquad (16)$$

If it is not possible to decrease L_1 sufficiently to make $f_r > f$, the addition of a sensor winding on the transformer to generate a signal to prevent premature switch-on should be considered.

Transformer Currents

The ripple in the output choke is, in general, only a few percent of the DC load current. For this reason, the transformer current can be regarded as a square wave for the purposes of winding loss calculation.

The maximum RMS current values are given, approximately, for the primary and secondary by

$$I_{e1} = \frac{I_O}{r}\sqrt{\delta_{OMAX}} = \frac{I_{e2}}{r} \qquad (17)$$

where

$$\delta_{O\ MAX} = \delta_{MAX}\frac{V_I}{V_{I\ AV\ MIN}} \qquad (18)$$

Duty factor $\delta_{O\ MAX}$ is used in these calculations for the following reason.

For 220V power line, the minimum line voltage is roughly $185V_{RMS}$. Using an input filter capacitor of about 2μF/W (to cope with a mains drop-out of 10ms), the peak-to-peak ripple at 185V power line input is about 20V. Under these conditions the minimum average (steady-state) input voltage

$$V_{I\ AV\ MIN} = \sqrt{2}V_{I\ MIN} - \tfrac{1}{2}V_{IR} \qquad (19)$$
$$= 252V.$$

However, δ_{MAX} is set so that the converter can handle a 10ms drop-out. But mains drop-out is not a steady-state condition, so that $\delta_{O\ MAX}$ should be used to calculate I_e and, thus, the loss and consequent temperature rise of the transformer.

Choke Design

To determine the minimum required choke inductance and for the choke design, see the Principle of Operation.

Transient Response Time

The transient response time required for a forward-converter to adjust to a step in the load current of ΔI_O is

$$t_R = (\Delta I_O L)/\{(V_O + V_F + V_R)(\frac{\delta_{tr}}{\delta} - 1)\} \qquad (20)$$

The Double Forward Converter

Principle of Operation

The equivalent circuit diagram of a double forward converter is shown in Figure 11. It comprises two forward converters in parallel, with flywheel diode D and filter LC common to both. Switches S_1 and S_2 operate alternately, which doubles the ripple frequency of the choke current. Since energy is pumped twice per converter period, the output voltage is

$$V_O = 2\delta V_I \qquad (21)$$

Choke Inductance

The minimum choke inductance is calculated in a similar way to that for the single forward converter. However, since there are now two charges and two discharges per converter period,

$$L > \frac{V_O}{4fI_{O\ MIN}}\left(1 - \frac{2\delta_{MAX}V_{IMIN}}{V_{I\ MAX}}\right) \qquad (22)$$

Further choke design proceeds as in section on Single Forward-Converter.

Preliminary Transformer Turns Ratio

The transformer is designed in a similar way to that for the single forward converter, except that now the turns ratio is twice as great. The preliminary turns ratio of a double forward converter transformer is

$$r' = 2\frac{\delta_{E\ MAX}V_{I\ MIN}}{V_{O\ MAX} + V_F + V_R} \qquad (23)$$

Transient Response Time

The transient response time required for a double forward converter to adapt to a step in the load current of ΔI_O is

$$t_R = (\Delta I_O L)/2\{(V_{O\ MAX} + V_F + V_R)\left(\frac{\delta_{TR}}{\delta} - 1\right)\} \qquad (24)$$

THE FLYBACK CONVERTER

Non-Isolated Inverting Converter

The outline circuit of an inverting flyback converter is given in Figure 12. The basic operation of an ideal inverting flyback converter is described by

$$V_O = \frac{\delta}{1-\delta}V_I \qquad (25)$$

The voltage waveform across inductance L and the associated current waveforms under steady-state conditions are given in Figure 13.

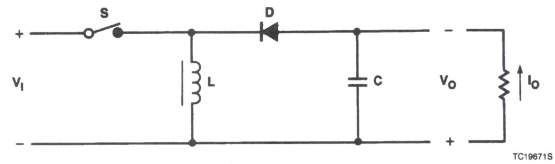


Figure 12. Outline Circuit of a Non-Isolated, Inverting Flyback Converter

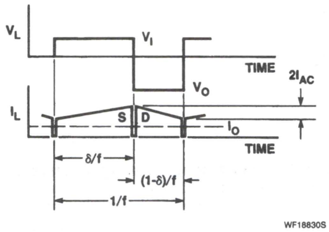


Figure 13. Voltage and Current Waveforms for the Choke of a Non-Isolated, Inverting Flyback Converter

Power Inductor

The minimum inductance required to ensure continuous-mode operation at minimum load $P_{O\ MIN}$ is

$$L > \frac{(\delta_{MIN}V_{I\ MAX})^2}{2fP_{O\ MIN}} \qquad (26)$$

NOTE: use of P_O allows output diode loss to be neglected.

The maximum peak current through the inductor is $I_M = I_{DC\ MAX} + 2I_{AC}$, and

$$I_M = \frac{\sigma P_{O\ MAX}}{\delta_{MAX}V_{I\ MIN}} + \frac{\delta_{MAX}V_{I\ MIN}}{2fL} \qquad (27)$$

For inductor design, see Part 4.

It is evident that the value of the inductor is inversely proportional to the minimum load. On the other hand, the choke must not saturate at maximum load if the supply voltage is minimum. Thus, continuous choke current with large output power variations is not always practical. The alternatives are:

- Pre-load the supply to decrease the ratio $P_{O\ MAX}/P_{O\ MIN}$.
- Change the operating frequency.
- Accept a discontinuous choke current at the expense of higher peak current through switch and output capacitor.

In the last case, the choke current waveform will be triangular rather than trapezoidal. For a triangular current waveform, Equations (26) and (27) become

$$L > \frac{(\delta_{MIN}V_{I\ MAX})^2}{2fP_{O\ MIN}} \qquad (28)$$

and

$$I_M = 2\frac{\sigma P_{O\ MAX}}{\delta_{MAX}V_{I\ MIN}} \qquad (29)$$

Proceed now with Part 4.

Non-Inverting Boost Converter

Principle of Operation

The outline circuit of a boost converter is shown in Figure 14. Its operation is described by

$$V_O = \frac{V_I}{1-\delta}$$

The voltage waveform across inductor L and the associated current waveforms under steady-state conditions are shown in Figure 15.

Power Inductor

The minimum inductance required to ensure continuous-mode operation of the choke at load $P_{O\ MIN}$ is

$$L > \frac{2}{27}\frac{V_O{}^2}{fP_{O\ MIN}} \qquad (30)$$

The maximum peak inductor current is

$$I_{MAX\ M} = \frac{\sigma P_{O\ MAX}}{V_{IMIN}} + \frac{\delta_{MAX}V_{I\ MIN}}{2fL} \qquad (31)$$

Proceed now with Part 4.

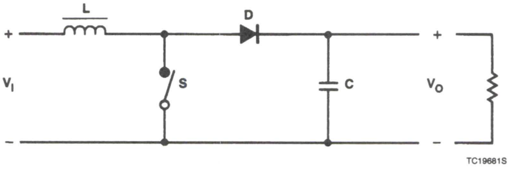


Figure 14. Outline Circuit of a Boost Flyback Converter

High-Frequency Ferrite Power Transformer and Choke Design

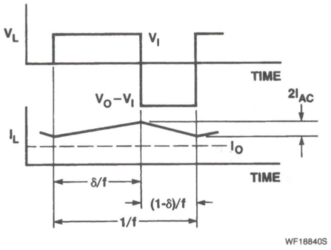


Figure 15. Voltage and Current Waveforms for the Choke of a Boost Flyback Converter

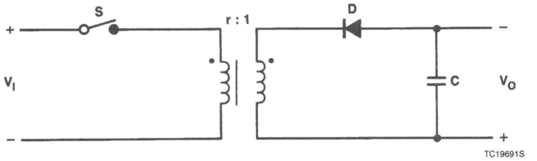


Figure 16. Outline Circuit Diagram of a Transformer-Isolated Flyback Converter

Transformer-Isolated Flyback Converter

Principle of Operation

For high-voltage low-current supplies, a useful variant of the inverting flyback converter is obtained by adding secondary windings to the choke to form a transformer, Figure 16. A further benefit of this arrangement is power line isolation.

Turns Ratio

In order to protect the switching devices, the turns ratio

$$r < \frac{V_{CESM} - (V_{IMAX} + V_r)}{V_O + V_F + V_R} \tag{32}$$

At high voltages, such as rectified power line, a good compromise between inductor size, switching-transistor peak current, and diode peak current can usually be obtained by one of the following procedures. At moderate input voltage range,

$$\frac{V_{I\ MAX}}{V_{I\ MIN}} < 2$$

take $\delta_{MIN} = 0.3$. This yields

$$\delta_{MAX} = 1/\{1 + \frac{7}{3}(V_{I\ MIN}/V_{I\ MAX})\} \tag{33}$$

so that

$$r' = \frac{3}{7}\{V_{I\ MAX}/(V_O + V_F + V_R)\} \tag{34}$$

At large input voltage range, that is,

$$\frac{V_{I\ MAX}}{V_{I\ MIN}} > 2$$

take

$$r' = \frac{1}{V_O + V_F + V_R}\sqrt{(V_{I\ MAX}V_{I\ MIN})} \tag{35}$$

This yields

$$\delta_{MIN} = 1/\{1 + \frac{V_{I\ MAX}}{r'(V_O + V_F + V_R)}\} \tag{36}$$

NOTE: If $\delta_{MIN} > 0.3$, take $\delta_{MIN} = 0.3$ and proceed as for a small input voltage range, otherwise

$$\frac{1}{\delta_{MAX}} = 1 + (1 - \delta_{MIN})\,V_{I\ MIN}/\delta_{MIN}V_{I\ MAX}$$

A *voltage limiting winding* with turns ratio between primary and limiting winding r/m limits switching device voltage to $\beta V_{I\ MAX}$. The maximum duty factor must then be such that

$$\delta_{MAX} < 1 - \frac{1}{\beta} \tag{37}$$

where

$$\delta_{MIN} = 1/\{1 + \frac{(1 - \delta_{MAX})V_{I\ MAX}}{\delta_{MAX}V_{I\ MIN}}\} \tag{38}$$

and

$$r' = \frac{\delta_{MIN}V_{I\ MAX}}{(1 - \delta_{MIN})(V_O + V_F + V_R)} \tag{39}$$

with

$$m = \frac{r}{(\beta - 1)} \tag{40}$$

Power Inductor

To ensure continuous-mode operation, design the choke primary for minimum load.

$$L < \frac{(\delta_{MIN}V_{I\ MAX})^2}{2fP_{O\ MIN}} \tag{41}$$

The maximum peak current through the primary

$$I_{MAX\ M} = \frac{\sigma P_{O\ MAX}}{\delta_{MAX}V_{I\ MIN}} + \frac{\delta_{MAX}V_{I\ MIN}}{2fL}$$

Proceed with Part 4. The number of turns on the choke secondary, together with r, are found in Part 3.

Multiple Output

Additional output voltages at any DC level can be obtained by simply adding additional secondaries of the appropriate numbers of turns. Note that, if the range of DC output voltages is large, leakage inductance will increase and regulation deteriorate.

The design procedure is covered in the following section.

Effective Currents

The maximum value of the RMS current through the primary winding is

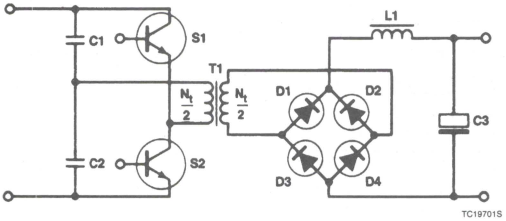
$$I_{e1} = \frac{P_{O\ MAX}\sqrt{\delta_{O\ MAX}}}{\delta_{O\ MAX}V_{I\ MIN}}\sqrt{\{1 + \frac{1}{3}\left(\frac{P_{O\ MIN}}{P_{O\ MAX}}\right)^2\}} \tag{42}$$

and through secondary x,

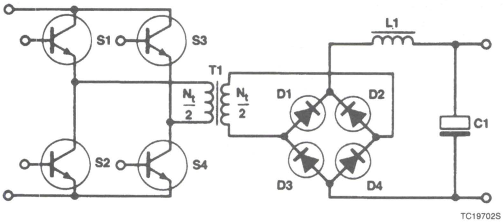
$$I_{ex} = \frac{r_xP_{OX\ MAX}\sqrt{(1 - \delta_{O\ MAX})}}{\delta_{O\ MAX}V_{I\ MIN}} \times \sqrt{\{1 + \frac{1}{3}\left(\frac{P_{O\ MIN}}{P_{O\ MAX}}\right)^2\}} \tag{43}$$

where

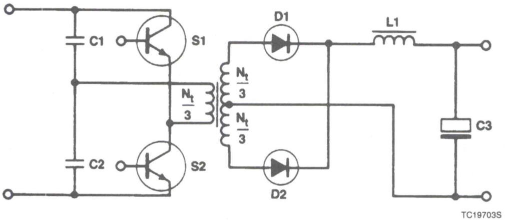
$$\delta_{O\ MAX} = 1/\left\{1 + \frac{V_{I\ AV\ MIN}}{r(V_O + V_F + V_R)}\right\}$$


L1
C1
S1
T1
$\frac{N_t}{2}$
$\frac{N_t}{2}$
D1
D2
C3
C2
S2
D3
D4
TC19701S

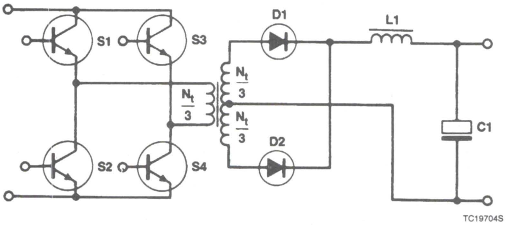
a. Two-Winding (1 + 1) Transformer in a Single-Ended Push-Pull Converter With a Bridge-Rectified Output


S1
S3
L1
T1
$\frac{N_t}{2}$
$\frac{N_t}{2}$
D1
D2
C1
S2
S4
D3
D4
TC19702S

b. Two-Winding (1 + 1) Transformer in a Bridge Converter With a Bridge-Rectified Output

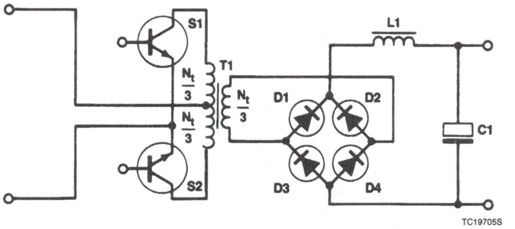

D1
L1
C1
S1
$\frac{N_t}{3}$
$\frac{N_t}{3}$
$\frac{N_t}{3}$
C3
C2
S2
D2
TC19703S

c. Three-Winding (1 + 2) Transformer in a Single-Ended Push-Pull Converter With a Bi-Phase Output

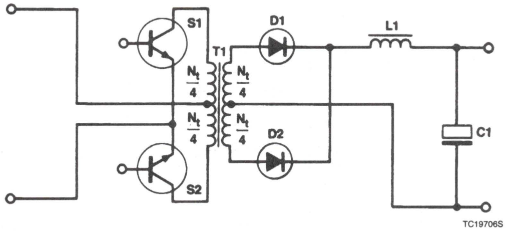

D1
L1
S1
S3
$\frac{N_t}{3}$
$\frac{N_t}{3}$
$\frac{N_t}{3}$
C1
D2
S2
S4
TC19704S

d. Three-Winding (1 + 2) Transformer in a Bridge Converter With a Bi-Phase Output

Figure 17. The Basic Configurations of Push-Pull Converters


S1
T1
$\frac{N_t}{3}$
$\frac{N_t}{3}$
$\frac{N_t}{3}$
S2
L1
D1
D2
D3
D4
C1
TC19705S

e. Three-Winding (1 + 2) Transformer in a Push-Pull Converter With a Bridge-Rectified Output


S1
T1
D1
L1
$\frac{N_t}{4}$
$\frac{N_t}{4}$
$\frac{N_t}{4}$
$\frac{N_t}{4}$
D2
C1
S2
TC19706S

f. Four-Winding (2 + 2) Transformer in a Push-Pull Converter With a Bi-Phase Output

Figure 17. The Basic Configurations of Push-Pull Converters (Continued)

THE PUSH-PULL CONVERTER

Principle of Operation

Outline circuits of the various basic configurations of push-pull converters are shown in Figure 17.

Since energy is pumped twice per converter period, the basic operation of a push-pull converter is described by

$$V_O = \frac{z\,\delta\,V_I}{2} \qquad (44)$$

For full bridge and conventional push-pull converters, z = 4; for half bridge push-pull converters z = 2.

The voltage waveform across the choke and the associated current waveforms are shown in Figure 18.

Duty Factor

With the equal conduction times per converter cycle, the maximum allowable duty factor is 0.5, but a more practical value is 0.45. In practice, wiring and transformer stray inductances result in a finite commutation time between output diodes. As a result, the interval during which energy is supplied to the output is shorter, and the effective duty factor smaller. This effective duty factor depends on operating frequency, transformer ratio, load current, and the stray inductance of the leads to the rectifier diodes.

To compensate for the increased commutation time, the energy transfer period δ/f should be decreased to about

$$\delta_e f = \delta/f - 1.2 r I_O \times 10^{-9} \qquad (45)$$

Transformer Turns Ratio

The preliminary turns ratio is

$$r' = \frac{2\delta_{E\ MAX} V_{I\ MIN}}{V_O + V_F + V_R} \qquad (46)$$

Power Choke Inductance

The minimum choke inductance that ensures continuous choke current, and, thus, continuous-mode operation is

$$L > \frac{V_O}{4fI_{AC}}(1 - 2\delta_{MAX}\frac{V_{I\ MAX}}{V_{I\ MIN}}) \qquad (47)$$

Here,

$$I_{AC} = I_{O\ MIN} - I_{MAG\ M} \qquad (48)$$

and

$$I_{MAGM} = \frac{r\delta_{MAX} V_{I\ MIN} \ell_e}{2n_I^2 \mu_O \mu_e A_e f} \qquad (49)$$

During transistor conduction, Figure 19, the magnetizing current changes from $+I_{MAG\ M}$ to $-I_{MAG\ M}$. While both transistors are off, during the interval (½f – δf) the transformer primary is open circuit. This forces the magnetizing current to flow through the output diodes in series. Thus, the load and magnetizing currents converge in one diode and cancel in the other.

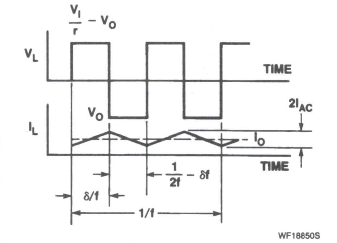


Figure 18. Voltage Waveform Across the Choke of a Push-Pull Converter Together with the Associated Current Waveforms

If, at low output current, one diode ceases to conduct, there is no path for the magnetizing current, which is then diverted through the conducting diode and the output choke to the output capacitor. This causes the output voltage to rise. From this, it follows that the minimum load current that can be drawn from the converter without one diode ceasing to conduct in this way is

$$I_{O\ MIN} = I_{MAGM} + I_{AC}$$

The magnetizing current flowing through the output diodes is

$$I_{MAGM} = \frac{\delta_{MAX} V_{I\ MIN} r}{2L_1 f}$$

where

$$L_1 = n_1^2 \mu_O \mu_e \ell_e / A_e$$

These two expressions together yield equation 49.

From Figure 19, the peak current through the power choke is

$$I_M = \sigma(I_{O\ MAX} + I_{O\ MIN} + I_{MAGM}) \qquad (50)$$

Further choke design proceeds with Part 4.

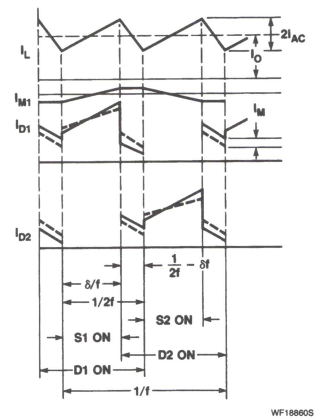


Figure 19. Waveform for Calculating the Peak Choke Current of a Push-Pull Converter

Transformer Currents

In a push-pull transformer, only one half of the double winding conducts at a time. The peak current through each half of the double winding is

$$I_{1M} = I_M/r$$

The effective primary current in each winding half is

$$I_{e1} \approx \frac{I_O}{r}\sqrt{\delta_{O\ MAX}} \qquad (52)$$

and, in the secondary,

$$I_{e2} \approx I_O\sqrt{\delta_{O\ MAX}} \qquad (53)$$

where

$$\delta_{O\ MAX} = \frac{\delta_{MAX} V_{I\ MIN}}{V_{I\ AV\ MIN}}$$

Transient Response Time

The transient response time required for a push-pull converter to adjust to a step in the load current of ΔI_O is

$$t_r = (\Delta I_O L)/2\ (V_O + V_F + V_R)\ (\frac{\delta_{tr}}{\delta} - 1) \qquad (54)$$

PART 2: SWITCHED-MODE POWER SUPPLY MAGNETIC CONSIDERATIONS AND CORE SELECTION

CORE SELECTION

Available ferrite core types cater for a wide range of SMPS application requirements. The preferred grade of ferrite for high-frequency power applications is Ferroxcube 3C8: a range of cores in this material is listed in Table 1, together with the principal data required by a designer. All symbols for quantities used are listed in the Table below.

If the proper core for a given application is to be selected, a number of factors should be taken into account. The type of converter circuit used, for example, determines to a large extent the throughput power capacity of a transformer wound on a given core type.

The discussion here assumes that no premagnetization — magnetic bias by a permanent magnet — is applied to the core.

The selection charts given here are mainly intended for cores for push-pull and forward-converter transformers. The design procedure for flyback converter transformers differs considerably, and the selection charts given here are mainly intended as a check on the core selected in Part 4.

Core Selection for Forward and Push-Pull Transformers

Selection charts 1, 2 and 3 show the throughput power as a function of frequency for a number of ferrite cores in the frequency range 10kHz to 100kHz. Note that the transformer throughput power must exceed the output power by an amount set by the efficiency of the output circuit, as discussed in Part 1.

Table 1. Principal Data for Cores for High-Frequency Power Applications

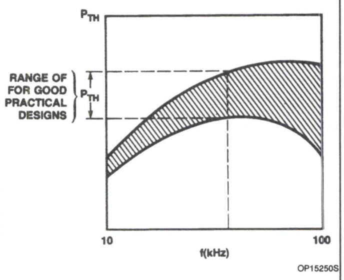
CATALOG NUMBER[1]	CORE TYPE	$A_{CP\ MIN}$ (mm^2)	A_e (mm^2)	V_e ($mm^3 \times 10^3$)	l_e (mm)	B_{CF} (mm)	H_{CF} (mm)	l_{AV} (mm)	θ_{JN} (°C/W)	θ_{JC}[2] (°C/W)
4322 020 52500	EC35/17/10	66.5	84.3	6.53	77.4	21.4	4.6	53	17.4	20.0
4322 020 52510	EC41/19/12	100	121	10.8	89.3	24.4	5.5	62	15.5	17.0
4322 020 52520	EC52/24/14	134	180	18.8	105	28.2	7.5	70	10.3	11.9
4322 020 52530	EC70/34/17	201	279	40.1	144	41.3	11.5	96	7.1	7.8
4312 020 34070	EE20/20/5	23.5	31.2	1.34	42.8	10.5	3.0	38	35.4	
4312 020 34020	EE25/25/7	52.0	55.0	3.16	57.5				30.0	
4312 020 34550	EE30/30/7	46.0	59.7	4.00	66.9	16.3	4.8	56	23.4	
4312 020 34110	EE42/42/15	172	182	17.6	97.0	26.2	6.8	93	10.4	12.2
4312 020 34120	EE42/42/20	227	236	23.1	98.0	26.2	6.8	103	10.0	11.5
4312 020 34170	EE42/54/20	227	236	28.8	122	35.3	6.8	103	8.3	9.8
4312 020 34190	EE42/66/20	227	236	34.5	146	50.0	6.8	103	7.3	8.1
4312 020 34100	EE55/55/21	341	354	43.7	123	32.5	7.7	116	6.7	7.4
3122 134 90210	EE55/55/25	407	420	52.0	123	32.5	7.7	124	6.2	6.8
4312 020 34380	EE65/66/27	517	532	78.2	147	38.6	10.2	150	5.3	6.1
3122 134 90690	UU15/22/6	30.0	30.0	1.44	48.0	10.0	4.0	45	33.3	
3122 134 90300	UU20/32/7	52.2	56.0	3.80	68.0	14.5	5.5	57	24.2	
3122 134 90460	UU25/40/13	100	100	8.60	86.0	19.0	7.0	75	15.7	
3122 134 90760	UU30/50/16	157	157	17.4	111	26.0	9.0	104	10.2	
3122 134 91390	UU64/79/20	289	290	61.0	210			110/98[3]	5.4	6.2

NOTES:
1. Core material 3C8.
2. For IEC class 2 insulation.
3. Wound on both legs.

High-Frequency Ferrite Power Transformer and Choke Design

AN1261 Part 2

Each core is represented as a shaded area, as shown in Figure 1.



NOTE:
In the core selection charts, the power-handling capability of each core is plotted as a shaded area extending from 10kHz to 100kHz. The vertical boundaries of this area represent the upper and lower limits of throughput power capacity achievable by good design, but depending on conductor type and power line insulation requirements.

Figure 1. Power Handling Capability

The actual throughput power obtainable with a given core depends to a large extent on the following characteristics:

- The flux density sweep
- The winding configuration (simple or split/sandwiched windings, sensor or demagnetization windings, see Part 3)
- Conductor type (solid, strip, Litz, see Part 3)
- Single or multiple output
- Power line insulation requirements

The upper limit of the shaded area for each core refers to a transformer design with optimized flux-density sweep, maximum use of the winding window, and Litz wire for minimum AC resistance. The lower limit refers to a design with 8mm creepage distance for IEC 435 power line insulation, optimized flux-density sweep, a (1 + 2) winding configuration (Part 1), and optimized but solid-wire windings. In addition, the following general conditions were assumed in the calculation of both boundaries:

- The hot-spot (peak) temperature of the core is 100°C; the temperature rise is 40°C
- The maximum flux-density sweep is limited to 1/1.72 of the maximum permissible flux density for the core material (0.32T for FXC 3C8) to cope with transient conditions
- The thermal behavior of wound cores, but without potting or additional heatsinking, was assumed
- Core flux densities are calculated assuming minimum cross-sectional areas.

Thus, the selection charts are based on worst-case conditions. Where the ambient temperature is lower than 60°C, when feedforward (Part 1) is used to ease the restriction on maximum flux density, or when heatsinking or potting are employed to improve heat transfer, throughput power capacity will be increased.

It may happen that, at a given power level, more than one type of core may be used. The following criteria may be used to make a choice:

- copper foil secondary windings are preferable for low-voltage, high-current supplies; thus, for ease of winding, a core with a round center pole should be chosen
- coil formers and mounting hardware are not available as standard for all core types
- production logistics may be improved if one core type is used for both transformer and choke.

Where these considerations do not apply, the choice of core should be guided by the discussion of Section 2.

Core Selection for Flyback Converters and Chokes

The magnetic design of flyback transformers and output chokes for forward and push-pull converters is essentially the same: the main design parameter is the energy to be stored. Core selection, therefore, is made on the basis of energy stored, $\frac{1}{2}I_M^2L$. A selection procedure based on energy to be stored is given in Part 4. This leads directly to spacer thickness and number of turns. Once a core has been chosen from Part 4, use charts 4 and 5 to check that the core chosen satisfies the throughput power requirements. If not, choose a larger core size for the design procedure in Part 4.

OPERATING FLUX DENSITY

When determining operating flux density, a distinction must be made between transformers and chokes. For chokes, and flyback-converter transformers (which also function as chokes), the most important parameter is the maximum peak flux density. The flux density sweep follows from the inductance value required.

For push-pull and forward-converter transformers, both AC and DC components of flux density must be taken into account from the start of the design process.

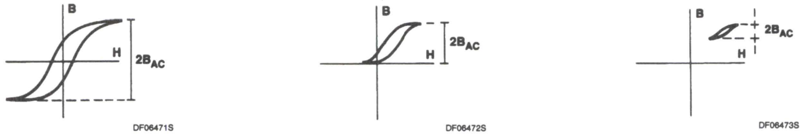
Flux-Density Levels for Forward and Push-Pull Transformers

The operating flux density of a transformer can seldom approach the maximum permissible flux density in practice since an allowance must be made for transient conditions, such as sudden load increases.

Unless special electronic measures (Part 1) are taken, a transient factor is required to cope with sudden load changes. This factor is related to the ability of the power supply to accept a range of input voltages. The input voltage range of power line operated power supplies may be 215V to 370V, or 200V to 340V; for telephone supplies, 40V to 70V; and for mobile supplies, 9V to 15.5V. The usual transient factor is 1.72.

For symmetrical excitation of the core (push-pull), the maximum possible flux-density sweep (Figure 2) is, in principle, twice that for asymmetrical excitation. In practice, however, allowance has to be made for unbalance when determining the operating flux density.

The maximum operating flux density depends on the protection circuitry. One source of unbalance is unequal flux linkage between two halves of a center-tapped winding. For this reason, bifilar windings are to be preferred. However, this is not possible in power line operated supplies since the voltage across the winding might be greater than the maximum voltage between adjacent turns.



a. Push-Pull Converter Transformers

b. Forward-Converter Transformer (With Slow-Rise Capacitor) or Ringing-Choke Flyback Converter

c. Flyback Converter Choke

Figure 2. Flux-Density Excursions and the Corresponding Flux-Density Sweeps

Table 2. Maximum Values of Flux-Density Sweep for Various Converter Types and Control Circuits

BOUNDARY CONDITIONS	FLUX-DENSITY SWEEP $B_{AC\ CP}$ (T)	
	Forward	**Push-pull**
Maximum sweep for FXC 3C8 (100°C)	0.16	0.32
At transient factor α	$\frac{0.32}{2\alpha}$	$\frac{0.32}{\alpha}$
With unbalance factor ϵ		$\frac{0.32}{\epsilon\alpha}$
With x% feed-forward	$\frac{0.32}{2(1 + x/100)}$	
With unbalance factor ϵ and x% feed-forward		$\frac{0.32}{\epsilon(1 + x/100)}$

The major reason for asymmetry is unequal conduction times or saturation voltages of the power switches in a push-pull converter. Storage effects can result in different switch-off delays. Core saturation occurring due to a delay decreases the primary inductance so that the magnetizing current rises steeply. This may lead to the destruction of the power switches. As a further safeguard, the maximum operating flux density should be decreased by an additional factor that depends on the efficiency of the protection circuit. A practical guide is a 15% allowance for a fully protected converter (unbalance factor $\epsilon = 1.15$), but a 100% allowance for an unbalanced push-pull converter ($\epsilon = 2$).

In forward converters, remanence should, in theory, also be allowed for. However, to obtain the correct primary inductance, some airgap is often useful. This airgap, together with the slow-rise capacitor (Part 1), results in the whole first quadrant of the BH loop being useful in practice, as is shown in Figure 2.

Where feedforward control is used, the transient factor can be reduced considerably and a higher flux-density sweep can often be applied.

The actual transient factor is determined by the feed-forward percentage used. Note, however, that application of feed-forward reduces the transient response of the power supply.

Practical flux-density and sweep limits are summarized for various converter types in Table 2. The curves of Figure 3, show the optimum flux-density sweep, where throughput power is maximum, for a range of cores in the frequency range 10kHz to 100kHz. Horizontal lines indicate the maximum allowable sweep for various converter types. Further lines can be added for other boundary conditions with the aid of Table 2. The given curves are calculated for a transformer temperature rise of 40°C.

The converter operating frequency is set by the required output voltage and current, and by the type of switch to be used. Once this frequency is known, the optimum flux-density sweep can be found for any core type.

Where the frequency is more or less fixed, and two core types could be used (Section 1), preference should be given to that core type for which the intersection of the optimum sweep curve with the set frequency is closest to the maximum flux density sweep.

Where frequency can be chosen freely, the frequency corresponding to the intersection of the optimum sweep curve with the line for the maximum flux-density sweep represents the optimum use of the core material.

Operation at the optimum sweeps represented by the curves of Figure 3 means that core loss and permissible winding loss are in optimum proportion. Deviation from the optimum proportion of core and winding loss, results in a lower throughput power. When the design is limited by saturation flux density, deviation is inevitable. The effect of deviation from the optimum flux density is plotted in Figure 4. This plot, which applies to any frequency, gives a rough indication of the reduction in throughput power from the optimum value. Once the optimum flux density sweep has been determined for the core and converter combination, the number of turns can be calculated as shown in the next section.

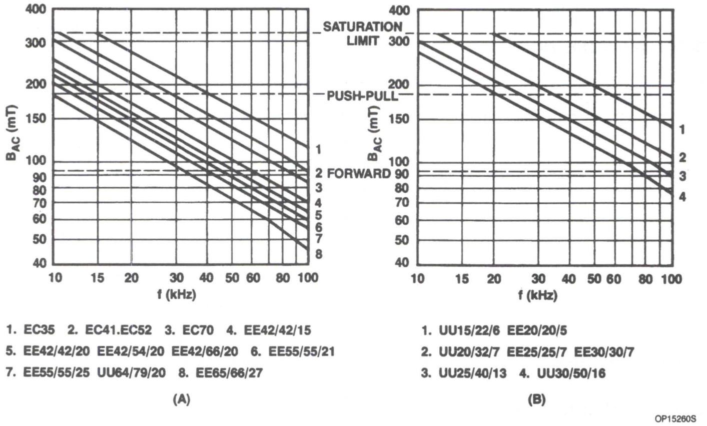
Flux Densities for Chokes and Flyback Transformers

The maximum flux density is taken into account in the design procedures given in Parts 1 and 4. The design centres around the maximum stored energy $\frac{1}{2}I_M^2L$ in the choke, which, in turn, is related to the inductance value from which follows the number of turns.

The flux-density sweep in chokes is generally relatively low, and so, in consequence, is the core loss. It may happen, however, especially in ringing choke flyback converters, that the flux-density sweep is comparable to that in forward converters. Core loss is not then negligible and should be calculated as shown in the section on core loss.

Once core type, spacer thickness, and number of turns have been established, the peak flux-density sweep can be calculated:

$$B_{AC\ CP} = \frac{LI_{AC}}{N_{PRIM}\ A_{CP}}$$



NOTE:
Horizontal lines indicate the limits for various converter types, with $\propto = 1.72$. The curves are calculated for a transformer temperature rise of 40°C.

Figure 3. Optimum Peak Center-Pole Flux Density Sweeps $B_{AC\ OPT}$ for a Variety of Cores for SMPS Applications

where I_{AC} is found during the design process (Part 1). In the case of a flyback transformer, all quantities refer to the primary.

If I_{AC} is relatively high, core loss will be significant.

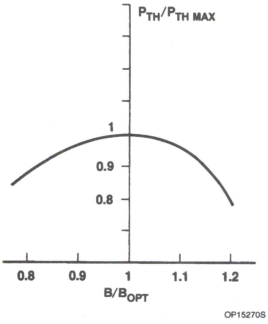


Figure 4. The Effect on Throughput Power Capacity of a Deviation in B_{AC} from the Optimum Value Indicated in Figure

NUMBER OF TURNS

Once the flux-density sweep is known, the number of turns can be determined.

Forward and Push-Pull Converter Transformers

The *minimum* number of turns in the secondary

$$n_{2\,MIN} = \frac{\delta V_I}{r' A_{CP\ MIN} B_{AC\ CP} f z}$$

$z = 2$ for forward and half-bridge push-pull converters;

$z = 4$ for full-bridge push-pull converters.

The values of δ and V_I are obtained from $\delta V_I = \delta_{MAX} V_{I\ MIN} = \delta_{MIN} V_{I\ MAX}$ (this and r′ are found in Part 1).

$n_{2\ MIN}$ will generally not be an integer and must be rounded. If the value of $n_{2\ MIN}$ is small, rounding will change the flux density sweep significantly. To prevent saturation, rounding should be to the next higher integer. The effect of rounding can be counteracted by changing the operating frequency.

Where operating frequency is not fixed, iteration will result in a satisfactory design. When the actual flux-density sweep is within 10% of the optimum, throughput power will be within 5% of its maximum.

Use the flux-density sweep obtained after rounding to determine core loss.

Flyback Converters and Chokes

Flyback converters and output chokes: the number of turns is derived and rounded in the choke design procedure given in Part 4.

Flyback transformers: the rounded number of primary turns is found in the choke design procedure of Part 4. The value of r′ is calculated in Part 1.

CORE LOSS

At frequencies approaching 100kHz, core loss has two main components: hysteresis loss and eddy-current loss. The hysteresis loss in Ferroxcube 3C8 at 100°C is

$$P_H \approx 16.7\ f^{1.3} B^{2.5}{}_{AC\ EM} V_e$$

This expression applies between 10kHz and 100kHz for both symmetrical and asymmetrical excitation, and for both sine and square wave fields.

The eddy-current loss for Ferroxcube 3C8, under the same conditions, is

$$P_E \approx 0.8 f^2 B^2{}_{AC\ EM} A_e V_e$$

The contribution of eddy-current loss in the core is greatly dependent on core size, frequency and flux density sweep. Below 100kHz, eddy-current loss may be neglected for small cores. However, for the larger cores, such as the E65 and EC70, eddy-current loss becomes important at much lower frequencies.

For very large cores, with center-pole diameters exceeding 35mm, the expressions for both P_H and P_E do not hold, even below 100kHz.

In the above expressions, $B_{AC\ EM}$ is the peak effective flux density sweep. It is related to $B_{AC\ CP}$ by

$$B_{AC\ CP} A_{CP} = B_{AC\ EM} A_e$$

For cores of constant cross sectional area, such as most E and U cores, $B_{AC\ CP}$ and $B_{AC\ EM}$ are similar in value, but they differ significantly for EC cores.

High-Frequency Ferrite Power Transformer and Choke Design

AN1261
Part 2

THERMAL RESISTANCE

In order to determine the maximum permissible dissipation of a transformer or choke, its thermal behavior must be known. This depends on core size, conductor form, and insulation requirements. Table 1 gives two values for thermal resistance: with and without creepage distance allowance at the ends of the winding.

These thermal resistances were measured with the transformer mounted on a printed circuit board with no local heat sources. They are referred to the hot-spot temperature in the middle of the center leg of the core (as deduced from the measured value on the ferrite surface).

For hot-spot temperatures up to 100°C, the maximum permissible winding dissipation may be obtained from:

$$P_W = \frac{\Delta T}{\theta_J} - P_C$$

This expression may be used for any ratio of core to winding dissipation.

In a choke with a large DC component of current, where core loss is negligible, $P_W = \Delta T/\theta_J$.

The temperature rise should be checked again once the winding design is complete. Winding design is treated in Part 3 for transformers and Part 4 for chokes. If the actual temperature rise is too high, the estimated throughput capacity was optimistic and a larger core should be used.

DATA NECESSARY FOR WINDING DESIGN

Before it is possible to move to the design of the windings, the following data should be available.

Forward and push-pull converters

- Core type(s)
- Coil former dimensions
- Power line insulation requirements
- Preliminary turns ratio (Part 1)
- Rounded number of secondary turns
- Operating frequency
- Secondary current and waveform
- Winding dissipation permitted
- Other windings — auxiliary outputs or sensor windings.

Flyback Transformers

- Core types (Part 4)
- Coil former dimensions
- Number of primary turns (Part 4)
- Preliminary turns ratio (Part 1)
- Operating frequency (Part 3)
- Primary and secondary currents and waveforms
- Other windings — sensor or auxiliary outputs
- Winding dissipation permitted
- Core loss
- Power line insulation requirements

Output and Flyback Chokes

- Core loss

Proceed to Part 4 for remaining design.

CORE SELECTION CHARTS

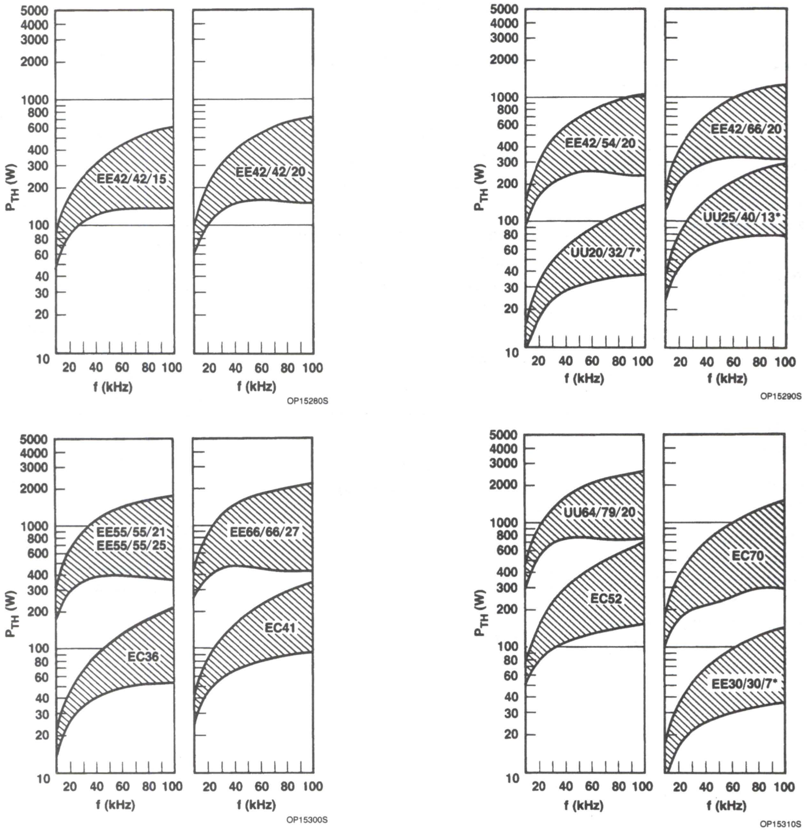
These charts allow an initial selection to be made of the appropriate ferrite core for a particular SMPS application. The upper limit of the shaded areas represents the performance of the core under ideal conditions: Litz wire windings and the whole of the winding window devoted to power transfer windings. Thus, there are no auxiliary windings, such as energy-recovery (demagnetizing) windings, and no allowance for creepage distance. The lower limit of the shaded area corresponds to the minimum performance to be expected from a basic, practical design. Thus, allowance is made for creepage distance, 30% of the remaining window is assumed to be occupied by auxiliary windings (non-power transfer windings), and the winding design is assumed to be optimized as shown in Part 3 of this series, but of simple construction. For both boundaries, optimum flux-density sweep is assumed.

NOTE:

*Cores marked with an asterisk have insufficient winding breadth for creepage distance for IEC 435 power line isolation.

THROUGHPUT POWER CORE SELECTION CHART 1

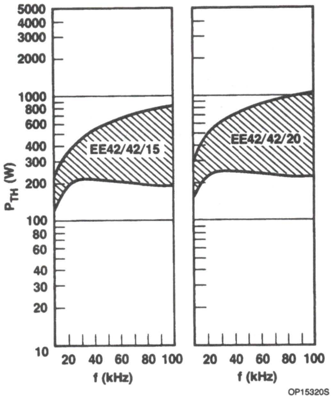
Forward Converter

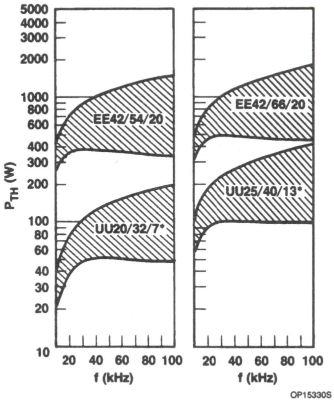


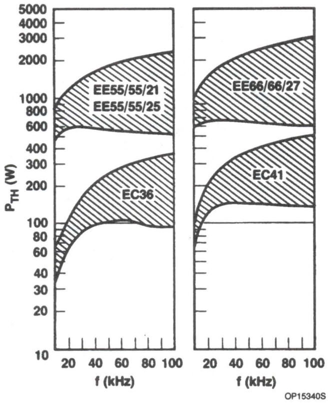
NOTE:
*Without creepage allowance.

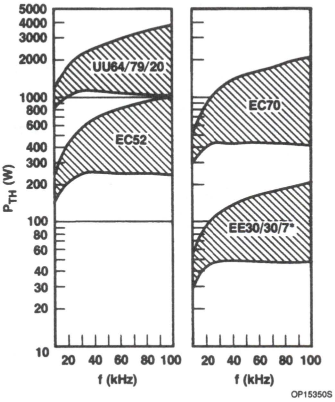
THROUGHPUT POWER CORE SELECTION CHART 2

Balanced Push-Pull Converter









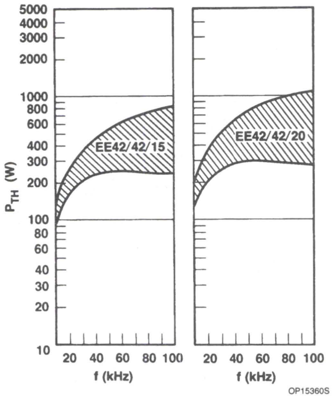
NOTES:

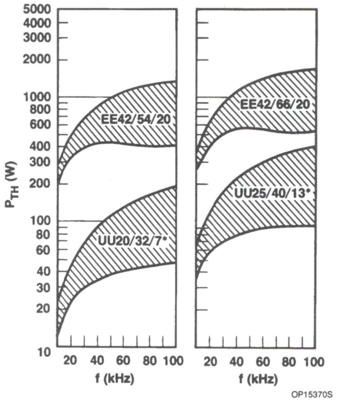
In order to obtain the performance indicated here, great care in both converter design and transformer winding layout is required to ensure that core excitation remains symmetrical. Any asymmetry could result in saturation of the core and destruction of the power switches in the converter.

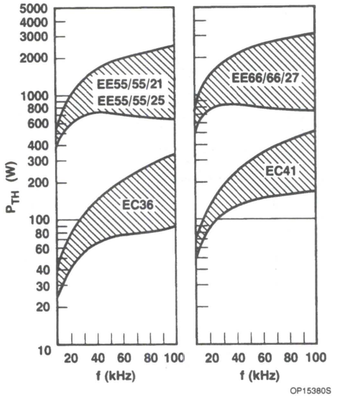
*Without creepage allowance.

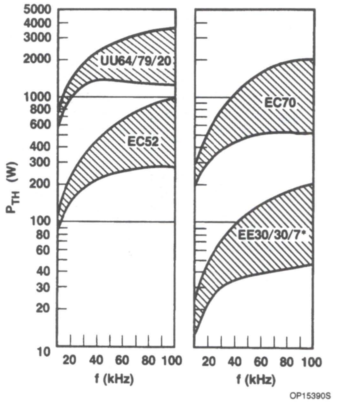
THROUGHPUT POWER CORE SELECTION CHART 3

Unbalanced Push-Pull Converter





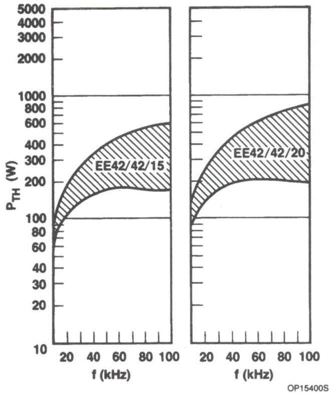


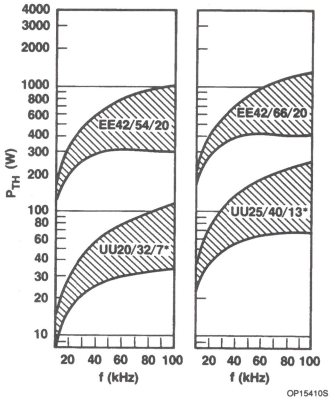


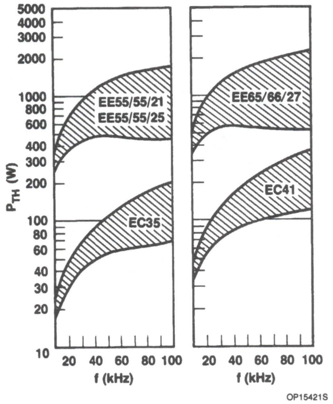
NOTE:
*Without creepage allowance.

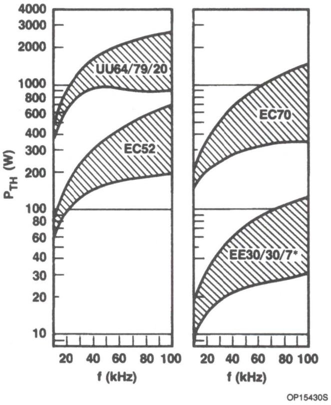
THROUGHPUT POWER CORE SELECTION CHART 4

Flyback $\gamma = 1^{+}$









NOTES:

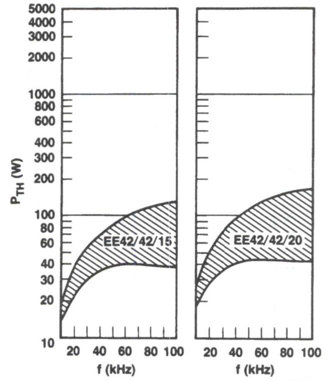
These charts are intended as a guide only: the choke selection procedure in Part 4, based on stored energy, should be used to make the choice of core. These charts can be used to check that choice.

$^{+}$ γ is the ratio of minimum to maximum load current for good regulation at constant duty factor.

*Without creepage allowance.

THROUGHPUT POWER CORE SELECTION CHART 5

Flyback $\gamma = 0.25^{+}$



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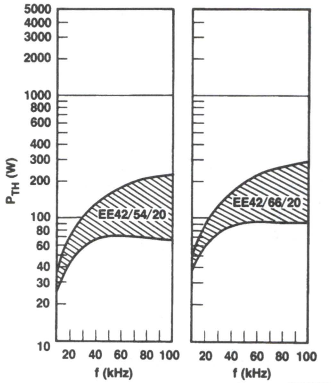

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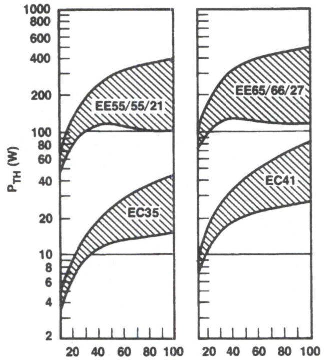
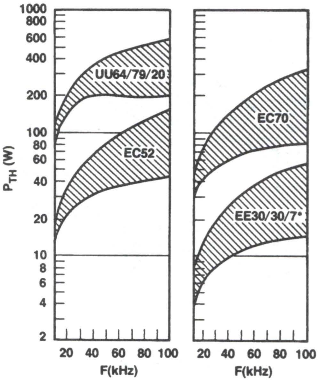


OP15461S



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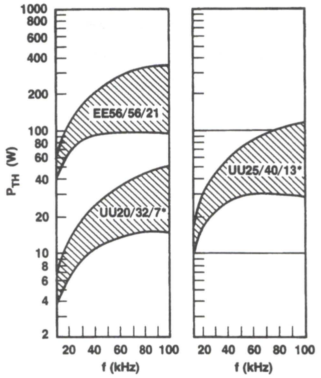

OP15480S

NOTES:

$^{+}$ γ is the ratio of minimum to maximum load current for good regulation at constant duty factor.

*Without creepage allowance.

High-Frequency Ferrite Power Transformer and Choke Design

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Part 3

PART 3: TRANSFORMER WINDING DESIGN

INTRODUCTION

At ultrasonic frequencies, the simple design rules used for low frequency transformer winding design are no longer valid.

Winding resistance and thus winding loss are increased through eddy-current effects — the proximity effect. At power line frequencies these effects can be ignored.

The design methods and aids presented here aim at finding the optimum winding design: that is, the winding geometry that yields lowest loss.

In drafting these design aids, the number of decisions made for the designer has been restricted to a minimum. He thus obtains a maximum of freedom of choice.

The essential background information will be given after presenting practical design procedures.

A certain amount of background information is required to use that freedom properly.

DEFINITION OF THE PROBLEM: BOUNDARY CONDITIONS

Given Boundary Conditions

The following boundary conditions are set once a core is selected:

- Frequency
- Primary and secondary RMS currents
- Primary and secondary turns numbers
- Winding breadth
- Available winding height
- Permissible winding loss

Coil former and winding dimensions are defined in Figure 1 and the List of Symbols which is on the following page.

These parameters can only marginally — if at all — be varied in winding design, therefore, they are termed given boundary conditions.

Winding breadth b_W follows from coil former breadth B_{CF} and the required creepage allowance c as set by the insulation standard. Available winding height is the height of the winding window H_{CF} in the coil former less the height occupied by the screens with the insulation, and the auxiliary windings (control windings not taking part in power transfer.) This available height should accommodate the power-transfer windings. It is not possible to determine beforehand the maximum height of individual windings.

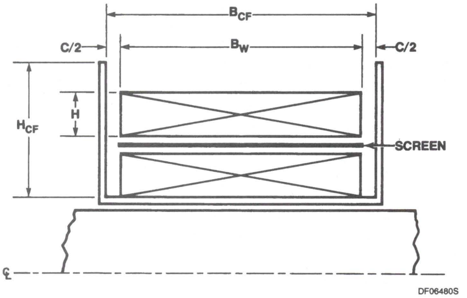

Figure 1. Definitions of Coil Former and Winding Dimensions

Chosen Boundary Conditions

In the winding design process the designer can make his own choice of

- Winding configuration
- Conductor form (wire, strip, bunched wire, etc.)

At the moment of choice, it is not always clear which choice is best. When an inexpensive design has an acceptable loss it may be preferable to a more costly design with even lower loss. It may therefore be desirable to work out more than one design by making preliminary choices for these boundary conditions.

The Design Problem

The actual winding design is now to determine the most suitable winding geometry.

Solving this problem requires (preferably convenient) means and methods to determine

— for strip windings (strip width equal to winding breadth)
  - strip thickness

— for wire windings
  - number of layers
  - wire size.

Having chosen the interleaving thicknesses, all further desired parameters can be calculated. Such means and methods are presented in this paper. For the prevailing set of (given and chosen) boundary conditions they are directed to finding the geometry giving minimum loss.

DESIGN PROCEDURES

The design process is organized in the following five phases.

I Collecting the boundary conditions.

II Determining the ideal power windings.

III Evaluating winding loss and required height. (According to the result, the design process then branches to Phase IV or Phase V, or a new start is required.)

IV Determining the optimum combination of non-ideal designs that will fit into the available height.

V Finalizing the design.

NOTE:
Here, the term "ideal" is used to describe windings designed for minimum loss regardless of the height of coil former required. Non-ideal windings have a height less than that required for ideal windings and the lowest possible loss that this height permits.

PHASE I. COLLECT THE BOUNDARY CONDITIONS

Given Boundary Conditions

Collect the given boundary conditions as set by circuit requirements and the core selected (Parts 1 and 2 of this series for forward and push-pull transformers, Parts 1 and 4 for flyback transformers).

1. Core Related:

- Operating frequency
- Maximum permissible winding loss $P_{W\ MAX}$
- Preliminary primary to secondary turns ratio r′.

For forward and push-pull transformers:

- Number of turns in secondary N_{SEC}
- Full-load RMS secondary current $I_{e\ 2}$.

For flyback transformers:

- Number of turns in primary N_1
- Full-load RMS primary current $I_{e\ 1}$
- Full-load RMS secondary current $I_{e\ 2}$.

2. Circuit Related:

- In the case of power line isolation, creepage distance c
- Data on windings other than power windings, such as demagnetizing and sensor windings
- Single or multiple secondaries.

LIST OF SYMBOLS

SYMBOL	UNIT*	DEFINITION
b	mm	Breadth of (rectangular) conductor
b_W	mm	Actual winding breadth
B	T	Leakage flux density
B_{CF}	mm	Coil former (or winding window) breadth
c	mm	Creepage distance required by the ruling insulation standard
C	–	Winding configuration factor: simple = 1; split/sandwiched = 2
C_N	–	Correction factor for N (strip windings)
C_p	–	Correction factor for p (wire windings)
d	mm	Wire diameter
d_O	mm	Overall wire diameter of enamelled wire
d_∞	mm	Optimum wire diameter for $p > 1$
f	Hz	Operating frequency
f_e	kHz	Effective frequency
F_g	–	Space (copper) factor in the layer breadth
F_R	–	Ratio of AC resistance to DC resistance (at a specified frequency)
h	mm	Conductor height: for solid, round wire $h = d\sqrt{(\pi/4)}$; for strip conductor, strip thickness
H	mm	Height of a winding (portion)
H_A	mm	Available height for power windings or winding portions
H_R	mm	Remaining free winding height: H_A less the combined heights of the power windings
i	mm	Thickness of interleaving
I_E	A	RMS current at full load
ℓ_{AV}	m	Average turn length
n	–	Preliminary number of turns
n_H	–	Winding-height factor for bunched wire
n_S	–	Number of strands in bunched wire
n_t	–	Winding pitch factor for bunched wire
N	–	Rounded number of turns in a winding portion

SYMBOL	UNIT*	DEFINITION
N_ℓ	–	Number of turns per layer
N_{PRIM}	–	Rounded number of primary turns
N_{SEC}	–	Rounded number of secondary turns
p	–	Number of layers
P_M	W	Winding loss margin: $P_{W\,MAX}$ minus total winding loss
P_W	W	Dissipation in transformer windings
$P_{W\,MAX}$	W	Maximum permissible winding dissipation
r	–	Transformer turns ratio
r_{AC}	Ω/m	AC resistance per unit length of conductor (under specified conditions)
r_{DC}	Ω/m	DC resistance per unit length of conductor
R_{AC}	Ω	AC resistance
R_{DC}	Ω	DC resistance
t	mm	Winding pitch
t_{MIN}	mm	Minimum winding pitch required for a given wire size
T	mm	b_W/N, winding breadth-to-turns ratio
z	–	Factor
Δ	mm	Skin thickness
θ	–	Ratio of minimum to maximum leakage flux density over the height of a winding
μ_0	H/m	Permeability of free space: $4\pi \times 10^{-}$ H/m
σ	Ωm	Resistivity
φ	–	Effective conductor height, expressed as a multiple of Δ

SUBSCRIPTS

1	Pertains to a transformer primary or primary winding portion
2	Pertains to a transformer secondary or secondary winding portion
e	An effective value
id	An ideal (optimum) value

SUPERSCRIPT

′	(as in r′) a preliminary (not rounded) value.

* unless otherwise stated.

Chosen Boundary Conditions

1. *Winding configuration:* Choose between the simple configuration (where $C = 1$) or the split/sandwiched configuration (where $C = 2$). In the latter case, decide which winding will be split, and which sandwiched. (It is usual to split the winding with the larger number of turns.) Sketch the complete winding arrangement (not to scale), including any auxiliary or multiple-output windings, as in Figures 4, 18 and 20. Draw also the leakage-flux (or NI) diagram and determine for each of the power windings the value of ϑ, the ratio of minimum to maximum leakage flux density over the height of the winding. Normally $\vartheta = 0$, but in multiple output transformers it occurs that $\vartheta \neq 0$.

   In the case of a flyback transformer, draw the leakage-flux diagram for both the period of primary conduction and the period of secondary conduction.
2. *Conductor form:* Assume single round wire initially. The results thus obtained will guide the final choice of conductor.

Derived Boundary Conditions

1. *Effective frequency:* If the waveform of the current through the windings is known from previous designs, the effective frequency f_e can be obtained by analysis of the current waveform. If the waveform is unknown, assume that f_e is the switching frequency in kHz.
2. *Effective skin thickness* in copper at 100°C is

   $\Delta_e = (5.62/f_e)$ (mm)

   with f_e in kHz.
3. *Number of turns*
   a. Forward and push-pull transformers;
   secondary, $N_2 = N_{SEC}/C$
   primary, $n_1 = N_{SEC}r'$.
   Initially, round n_1 to the next even integer N_{PRIM}. It is essential that N_{PRIM} is even if the winding is to be split, and it avoids a further rounding if there are two layers in a simple winding. Then,

   $N_1 = N_{PRIM}/C$.

   b. Flyback transformers: A flyback transformer may use a split/sandwiched winding configuration to reduce leakage inductance, but this will not, however, reduce winding loss. The design procedures are always those for simple windings. But, of course, the number of turns of the split winding must be rounded to an even number.

   $N_2 = N_1/r'$

   rounded to an integer.

   c. Multiple-output windings
   - Calculate (as described in Part 2 of this series) for the output with the lowest voltage, that is, with the smallest number of turns, and round up to the next integer.
   - To obtain the number of turns for the other outputs divide the required output voltage by the volts-per-turn value for the lowest-voltage winding. Round the numbers of turns of all outputs to the nearest integer.
   - Check whether the various output voltages are within the required limits with these numbers of turns.
   - If not, increase the number of turns of the lowest-voltage winding by one, and repeat the calculations, starting with the volts per turn.
   - When the numbers of turns for the correct output voltages have been established, correct the number of primary turns using the volts-per-turn value last found.
4. *Winding window*
   a. Winding breadth $b_W = B_{CF} - c$, see Figure 1.
   b. Available height: the height available for the *complete* power windings is H_{CF} less
   - An allowance for imperfect contact between layers, interleavings and screens;
   - The height of screens and their insulation (C times);
   - The height of auxiliary windings handling little or no power, such as:
     - A sensor winding on the primary side of the screen that may also supply a little power for the control circuitry,
     - A demagnetizing winding.

Such windings are not designed for minimum loss. To save height, single layers are assumed of winding pitch

$t = b_W/(N + 1)$.

Choose a wire size such that $t_{MIN} \leqslant t$ and $d \leqslant \Delta_e$. Then with an interleaving of thickness i suitable for the winding pitch, the required height is

$H = d_O + i$.

The height that remains after all deductions divided by C is H_A, the height available for one primary and one secondary winding portion.

PHASE II: DETERMINE THE IDEAL POWER WINDINGS

Not yet knowing the value of p, multilayer windings are assumed initially. If, during the design procedure, this assumption proves incorrect, the design procedure switches to that for single-layer windings.

Follow the procedure below for all power windings.

Ideal Multilayer Windings of Solid, Round Wire

1. Calculate $d_\infty = \left(\dfrac{17.1 b_W}{N f_e}\right)^{1/3}$
2. If $\vartheta = 0$, read C_p from the table below. If p is not known, take $p = 1.5$ for a sandwiched winding or $p = 2$ in other cases.

p	1.5	2	2.5	3 to 4.5	> 4.5	if p > 3 check for errors
C_p	1.06	1.03	1.02	1.01	1	

   If $\vartheta \neq 0$, calculate

   $$C_p = \sqrt{\frac{1-\vartheta}{(1-\vartheta^3)^{1/3}}}$$

   Then calculate $d_{ID} = d_\infty C_P$.
3. Select the nearest standard wire size from a wire table and note d, d_O, t_{MIN} and r_{DC}.
4. *Number of layers:*
   a. $p_{ID} = \dfrac{N}{b_W/t_{MIN} - 1}$

   NOTE:
   This expression is valid only for t_{MIN} from Step 3.

   — If $p_{ID} \leqslant 1.5$ a strip or foil alternative may be preferable.

   — If $\vartheta = 0$ and $p_{ID} \leqslant 1$, the expression for d_∞ in Step 1 is not valid. Go to the single-layer winding procedure.

   b. Find p by rounding up p_{ID} to the next suitable value: to a multiple of 0.5 for a sandwiched winding, and to an integer in other cases.

   c. Calculate $N\ell = N/p$. If that value is not an integer, consider an adaptation of N to facilitate manufacture. Start again with the new value of N.

   d. If $\vartheta = 0$, check that the value of p used equals that assumed in Step 1. If not, repeat from Step 2 using the correct value of p.
5. Determine the winding pitch $t = b_W/(N\ell + 1) = pb_W/(N + p)$. $N\ell$ may not be the

High-Frequency Ferrite Power Transformer and Choke Design

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same in all layers (Step 3c); this will result in different values of t. Remember that all layers should occupy the full breadth b_W. Do not allow a difference greater than one turn in $N\ell$.

6. Select a suitable interleaving, thickness i, for the winding pitch and calculate the required height $H_{ID} = p(d_O + i)$.
7. Resistance factor $F_R = 1 + \frac{1}{2}(d/d_{ID})^6$ when $d/d_{ID} < 1.25$. But when $p = 1.5$ this expression holds only for $d/d_{ID} < 1.15$.
8. AC resistance per meter length of wire $r_{AC} = F_R\ r_{DC}$.
9. Winding loss of a complete winding (of C portions) $P_W = CI_e^2N\ell_{AV}r_{AC}$, taking for the average turn length ℓ_{AV} the value for a fully wound coil former in m.

Having found the ideal designs for all power windings using this procedure, proceed to Phase III.

Single- and Half-Layer Windings of Solid Round Wire

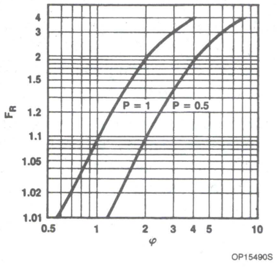
This procedure applies only when $\vartheta = 0$.

Arriving from Step 4a of the previous procedure, take $p = 1$.

1. Winding pitch $t = pb_W/(N + p)$.
2. Select from a wire table the thickest standard wire for which $t_{MIN} \leqslant t$ and note d, d_O and r_{DC}. Also choose a suitable interleaving, thickness i.
3. $H = p(d_O + i)$.
4. $\varphi = \sqrt{(0.124f_ed^3/t)}$, ($f_e$ in kHz, d and t in mm).

NOTE:
If f_e differs from the switching frequency, use the lower value of frequency.

5. Read F_R from Figure 2. Beyond the chart, $F_R = p\varphi$.
6. $r_{AC} = F_Rr_{DC}$.
7. $P_W = CI_e^2N\ell_{AV}r_{AC}$, where ℓ_{AV} in m.



NOTE:
Above $F_R = 4$, take $F_R = p\varphi$.

Figure 2. F_R vs φ for Single- and Half-Layer Windings

In the case of a sandwiched winding, consider a strip or foil winding. If a wire winding is preferred, and if φ from Step 4 is about 4 or greater, a half-layer winding will probably have about equal r_{AC}, about half the wire size and about one quarter of the copper content; follow the above procedure using $p = 0.5$.

Having found the ideal designs for all power windings, go to Phase III.

Ideal Strip or Foil Windings

1. If $\vartheta = 0$, read C_N from the table below.

N	0.5	1	1.5	2	2.5	3 to 4.5	⩾5
C_N	1.69	1.19	1.06	1.03	1.02	1.01	1

If $\vartheta \neq 0$, calculate $C_N = \{\frac{(1-\vartheta)^3}{1-\vartheta^3}\}^{1/4}$

Then determine f_e (kHz).

$h_{ID} = C_N\sqrt{\frac{9.74}{Nf_e}}$ mm, using f_e in kHz.

2. Select the nearest available strip or foil thickness, h.
3. $F_R = 1 + (1/3)(h/h_{ID})^4$ when $h/h_{ID} < 1.4$.
4. $r_{AC} = F_R/(45b_Wh)\Omega/m$ (b_W and h in mm).
5. $P_W = CI_e^2N\ell_{AV}r_{AC}$.
6. Select a suitable interleaving, thickness i, then $H_{ID} = N(h + i)$.

NOTE:
This procedure is for copper at 100°C, resistivity $1/45\Omega mm^2/m$. It can be adapted to aluminium conductor (62% higher resistivity at 100°C). In the expression for h_{ID} (Step 1) replace 9.74 by 15.8; in Step 4, replace 45 by 28.

Compare P_W from Step 5 with that of the wire version of the winding, (Step 9 or Step 7) and choose the ideal solution for lowest r_{AC}. Having found the ideal designs for all power windings, go to Phase III.

PHASE III: EVALUATE THE DESIGN WITH RESPECT TO WINDING LOSS AND HEIGHT

The success of a design attempt is judged on the basis of winding-loss margin P_M and remaining free height H_R.

The winding-loss margin is calculated from $P_{W\ MAX}$ and the total loss of the power windings. The remaining free height is calculated from H_A and the heights of the power windings.

There are four possible results of the evaluation:

- *P_M and H_R both positive:* design attempt successful, proceed to Phase V.
- *P_M and H_R both negative:* boundary conditions do not permit a successful design. Make a fresh start with a higher operating frequency or a larger core, for example
- *P_M positive and H_R negative:* a frequent occurrence, especially at lower frequencies. Try non-ideal winding designs requiring less height as in Phase IV.
- P_M negative and H_R positive: reconsider the chosen boundary conditions and start again. Some basic considerations are:
  - Split/sandwiched designs offer lower loss than simple ones, especially at higher frequencies.
  - Strip or foil windings tend to have lower losses than (single-layer) wire windings.
  - If H_R is large, try replacing a single-wire winding by a multiple-wire or bunched-wire winding. Design procedures are given in the next section. A Litz-wire winding may also be possible if H_r is particularly large. Evaluate the result again.

If adoption of one of these measures results in both H_R and P_M being positive, the design is successful; if not, try a higher operating frequency or a larger core in a new design.

ALTERNATIVE DESIGNS: MULTIPLE, BUNCHED AND LITZ-WIRE WINDINGS

Ideal Multiple-Wire Windings

1. Choose the number of parallel strands n_S: usually 2 or 3.
2. Follow the design procedure for ideal multilayer windings of solid, round wire, as if the winding had n_SN turns. If Step 4a results in $p_{ID} \leqslant 1$, follow the single-layer design procedure, again replacing N by n_SN.
3. Divide the value of r_{AC} by n_S to find the AC resistance of the n_S parallel strands.

Ideal Bunched-Wire Windings

Bunched wire consists of a few strands of insulated wire twisted together to form a bunch. The strand diameter is not so small that eddy-current loss is negligible.

The minimum winding pitch of a bunched wire of n_S strands is $n_T\ t_{MIN}$, and the layer height without interleaving is n_Ht_{MIN}, where t_{min} is the minimum winding pitch given in the wire tables for a single strand. Values of n_t and n_h for crude experimental bunches are given for guidance in the table below.

n_S	4	5	6	7	8	9	10
n_T	2.45	2.94	2.98	3.11	3.61	3.89	4.34
n_H	2.31	2.69	2.93	2.93	3.16	3.16	3.26

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Multilayer Bunched-Wire Winding

1. Choose n_S. a bunch of 7 strands gives the best space (copper) factor.
2. If $\vartheta = 0$, read C_p from the table below. If p is not known, take $p = 1.5$ for a sandwiched winding, and $p = 2$ in other cases.

p	1.5	2	2.5	3 to 4.5	> 4.5	if p > 3 check 1 for errors
C_p	1.06	1.03	1.02	1.01		

If $\vartheta \neq 0$, calculate

$$C_p = \sqrt{\frac{1 - \vartheta}{(1 - \vartheta^3)^{1/3}}}$$

Then $d_{ID} = C_p \left(\frac{17.1 b_w}{n_s N f_e} \right)^{1/3}$

3. Select the nearest standard wire size from a wire table, and note d, d_O, t_{MIN} and r_{DC}.
4. Number of layers:

a. $$p_{ID} = \frac{N}{b_W/(n_T t_{MIN}) - 1}$$

NOTE:
The expression holds only for t_{MIN} from the previous steps. If $p_{ID} \leqslant 1$, the expression in Step 2 does not apply.

b. Find p by rounding p_{ID} up to the next suitable value. For sandwiched windings, round to multiples of 0.5; in other cases, round to integers.

c. Calculate $N\ell = N/p$. If this does not yield and integer, consider adapting N to facilitate manufacture. Start again using the new value of N.

d. If $\vartheta = 0$, check that the value of p found is that assumed in Step 2. If not, repeat from Step 2 using the correct value of p.

5. Winding pitch $t = b_W/(N\ell + 1) = pb_W/(N + p)$. $N\ell$ may not be the same in all layers. This will result in different values of t, since all layers should occupy the full winding breadth. Do not permit differences of more than one turn in $N\ell$.
6. Select a suitable interleaving, thickness i, for the winding pitch. The required height $H = p\ (n_H t_{MIN} + i)$ where n_H is given in the table in the section on Ideal Bunched-Wire Windings.
7. Resistance factor $F_R = 1 + ½\ (d/d_{ID})^6$.
8. Resistance per meter length of bunch $r_{AC} = F_R r_{DC}/n_S$ where r_{DC} is the resistance per meter length of strand.
9. $P_W = CI_e^2 N\ell_{AV} r_{AC}$, where ℓ_{AV} in m.

Single-Layer and Half-Layer Bunched-Wire Windings

This procedure applies only if $\vartheta = 0$ and $p = 1$.

1. Winding pitch $t = pb_W/(N + p)$.
2. From a wire table, select the thickest strand for which $t_{MIN} \leqslant t/n_T$ and note d, t_{MIN} and r_{DC}. Also, choose a suitable interleaving, thickness i, for the winding pitch.
3. Required height $H = p\ (n_H t_{MIN} + i)$.
4. $\varphi = \sqrt{(0.124 n_S f_e d^3/t)}$.

NOTE:
If f_e differs from the switching frequency, use the lower of the two values (in kHz).

5. Read F_R from Figure 2. Beyond the range of Figure 2, $F_R = p\varphi$.
6. The AC resistance per meter length of bunch $r_{AC} = F_R r_{DC}/n_S$, where r_{DC} is the DC resistance of a meter length of *strand.*
7. Winding loss $P_W = CI_e^2 N\ell_{AV} r_{AC}$, where ℓ_{AV} is in m.

If φ in Step 4 is greater than or equal to about 4, a half-layer design might be preferable for a sandwiched winding.

Litz-Wire Windings

Litz-wire is here taken to be a kind of bunched wire in which the strands are so thin ($d \ll \Delta_e$) that eddy-current effects can be neglected. Its main drawback is its low space (copper) factor, often only 25% to 30%.

Litz-wire is standardized and commercially available. The standards specify numbers of strands, strand diameter, overall diameter and DC resistance.

Mechanical stress deforms the bunch so that the breadth in the layer and, thus, the minimum winding pitch are greater than the overall diameter of the bunch, but the height of the layer is smaller.

1. Knowing the winding current I_X, select a bunch of strand diameter d and number of strands n_S such that $\pi d^2 n_S \cong I_X$. The resulting current density will be about 4 A/mm².
2. Due to deformation, the winding pitch $t \cong 1$, $2d_O$, where d_O is the overall diameter of the bunch.
3. Provisional number of layers $p' = Nt/(b_W - t)$.
4. If p' is within 10% of the next lower integer, the winding may be feasible with care with this lower value. Otherwise, take for p the next higher integer. Then calculate $n'_S = n_S(p/p')^2$.
5. Select a standard Litz-wire with the same strand diameter, and a number of strands as large as possible, but lower than n'_S.
6. The required height of the winding will be less than $H = p\ (d_O + i)$, where i is the thickness of the interleaving.
7. The DC resistance per meter length is usually given for 20°C, multiply that value by 1.3 to get the resistance at 100°C. Then calculate $P_W = CI_e^2 N\ell_{AV} r_{DC}$, using ℓ_{AV} in m.

NOTE:
If all windings in the transformer are of Litz-wire, the split/sandwiched winding configuration does not lead to lower losses.

If a suitable Litz-wire is not readily available, the above procedure can be adapted to use multiple Litz-wire using similar methods to those for multiple wire.

PHASE IV: DETERMINE THE OPTIMUM COMBINATION OF NON-IDEAL DESIGNS

When ideal designs overflow the winding space, non-ideal designs must be used. First, collect a few non-ideal versions of, if possible, primary and secondary. The accommodation procedure will then show which combinations fit into the available height. The one having the lowest loss can then be used as the final design.

Non-Ideal Design Versions in Solid Round Wire

Non-ideal design versions of wire windings are generated simply by successively reducing the number of layers to reduce winding height.

The procedure given in this Section is not valid when at the start $p = 1$. However, it remains valid if step 2 yields values of $p \leqslant 1$.

1. Note, for the coil former, b_W and ℓ_{AV} (is in m); and for the ideal design, d_{ID} (before rounding), N, I_e, p, t, d, H, r_{AC}, and P_W.

   A table such as that shown below will be found a convenient design route.
2. Reduce p by one step
   - of 0.5 for a sandwiched winding.
   - of 1 in other cases.
3. If $N\ell = N/p$ is not an integer, consider adapting N to obtain an integral number of turns per layer. If possible, let this adaptation cancel a previous one. Calculate the winding pitch.

   $t = pb_W/(N + p)$.
4. Select (from a wire table) the thickest standard wire for which $t_{MIN} \leqslant t$ and note d, d_O, and r_{DC}. Select a suitable interleaving, thickness i.

5. Required height

   $H = p\ (d_O + i)$.

6. Resistance factor

   $F_R = 1 + \frac{1}{2}(d/d_{ID})^6$.

   If $p_{ID} > 1$, this expression holds for $p \leqslant 1$, but this is not the case if $p_{ID} \leqslant 1$.

7. Resistance per meter length of wire

   $r_{AC} = F_R r_{DC}$.

8. Winding loss

   $P_W = C I_e^2 N \ell_{AV} r_{AC}$.

For each design version, repeat this procedure from Step 2.

Example: In this table of design versions, the 3-layer version is the ideal design; the others are derived using the procedure above.

Primary: Split, $C = 2$, $b_W = 13.4mm$, $d_{ID} = 0.437mm$, $I_e = 0.565A$, $\ell_{AV} = 0.053m$.

p	3	2	1
N	57	58	57
t	0.670	0.447	0.231
d	0.450	0.355	0.180
d_O		0.414	0.222
r_{DC}		0.225	0.873
F_R		1.144	1.002
r_{AC}	0.223	0.257	0.875
P_W	0.430	0.505	1.688
i		0.06	0.06
H	1.728	0.948	0.282

Non-Ideal Design Versions of Strip or Foil Windings

Here, the required reduction in height is obtained by using thinner conductor.

1. Note, for the coil former, b_W and ℓ_{AV}, and for the ideal design, N, I_e, h_{ID} (before rounding), h, i, r_{AC}, H, and P_W. Set out a table in the form shown below.
2. For h, take the next available size below that used in the last design, and select a suitable interleaving, thickness i.
3. Resistance factor $F_R = 1 + (1/3)(h/h_{ID})^4$.
4. Resistance per meter length of conductor

   $r_{AC} = F_R/(45 b_W h)$.
5. Winding loss $P_W = C I_e^2 N \ell_{AV} r_{AC}$.
6. Required height $H = N(h + i)$.

For each successive version, repeat from Step 2 onward.

Example of a table of design versions of strip conductor:

Secondary: Sandwiched, $C = 2$, $N = 4$, $b_W = 13mm$, $h_{ID} = 0.222mm$, $I_e = 8.05A$, $\ell_{AV} = 0.053m$.

h	0.2	0.15	0.1	0.073
i	0.1	0.06	0.06	0.04
F_R		1.069	1.014	1.004
r_{AC}	0.0104	0.0122	0.0173	0.0235
P_W	0.286	0.335	0.475	0.646
H	1.20	0.84	0.64	0.452

Alternative Winding Designs With Reduced Height

It is difficult to predict the value of n_S, that is, the best starting point for the following procedure when the loss margin is positive.

— If $p_{ID} > 1$, use the procedure for Non-Ideal Design Versions, but divide t (Step 3) and r_{DC} (Step 4) by n_S.

— For a sandwiched winding, if $p_{ID} \leqslant 1$ and $p = 1$, use the procedure for single- and half-layer winding, again dividing t (Step 1) and r_{DC} (Step 2) by n_S.

Bunched wire: use the procedure for Ideal Multiple Wire Windings as follows:

— If $p_{ID} > 1$, commence with Step 4b and continue with values of $p > P_{ID}$.

— For a sandwiched winding, if $p_{ID} \leqslant 1$ and $p = 1$, use the procedure for Single-Layer and Half-Layer Bunched Wire Bindings with $p = 0.5$.

Litz-wire: use the appropriate procedure with lower values of p.

Having collected several versions of, preferably, all power windings, follow the procedure in the next section.

Accommodation Procedure

This procedure seeks combinations of design versions that fit into the available winding height, together with their total winding loss.

1. Calculate, for all versions of the primary, the maximum permissible secondary height, as shown in the table below.

   $H_{2MAX} = H_A — H_1$.

   Note, also, primary dissipation $P_{W\,1}$ of all versions.
2. Select, for each primary version, the secondary that most nearly fills H_{2MAX} and note its dissipation P_{W2}.
3. Calculate the remaining free height

   $H_R = H_{2MAX} — H_2$

   and total winding loss

   $P_W = P_{W1} + P_{W2}$.
4. Select the combination having the lowest value of P_W.

Table 1 illustrates the accommodation procedure for a transformer with two power windings. The same principles apply for transformers with more power windings, even though the number of combinations is greater. Much labor might be saved if design versions with excessive loss per mm of winding height are not considered.

Since the maximum permissible winding loss is 1.23W, the 2-layer primary combined with the secondary using 0.1mm strip results in a satisfactory design. There is no need to consider the secondary using 0.15mm strip, although the excess height of 0.02mm ($C = 2$) could perhaps, be accommodated by careful manufacture.

NOTE:

The example is for a split/sandwiched winding configuration ($C = 2$), so that winding heights are for one portion of each winding.

PHASE V: FINALIZING THE DESIGN

In order to prepare the transformer design for production, four further steps are necessary.

1. Check that the design route followed was the correct one, and that no errors have crept in. Moreover, ensure that the correct value of winding-configuration factor C was used throughout.
2. Make a dimensioned sketch of a cross-section through the windings in the winding window. Calculate the conductor lengths required for each winding, using the actual average turn lengths. For wire windings, check that $N\ell$ turns of the wire selected will fit into the winding breadth, that is, that $b_W \geqslant (N\ell + 1)t_{MIN}$.
3. Prior to prototype evaluation, make a final estimate of the transformer temperature rise using winding losses recalculated from the actual winding lengths obtained in the previous step.
4. In preparation for manufacture, collect all required information about core and coil former, windings and interleavings, screens and their interleavings, interwinding insulation, and terminations. Specify winding pitches for wire windings: windings are generally not close-packed since all layers should be of equal breadth.

This concludes the practical design procedures. The following sections contain supplementary information only.

BACKGROUND

The essential difference between a designer and a computer is creative thinking. Thus, a true designer will find no lasting satisfaction in following design procedures that resemble

Table 1. Illustrating the Accommodation Procedure for $H_A = 1.778mm$ and $P_{W\ MAX} = 1.23W$

Primary versions (split, single wire)	p_1	3	2		1
	$P_{W\ 1}$ (W)	0.430	0.505		1.688
	H_1(mm).	1.728	0.948		0.282
Height available for secondary	$H_{2\ MAX}$	0.050	0.830		1.496
Secondary versions (sandwiched, strip)	H_2 (mm)		0.84	0.64	1.20
	h (mm)		0.15	0.1	0.20
	$P_{W\ 2}$ (W)		0.335	0.475	0.286
Remaining height	H_R (mm)		−0.01	0.19	0.296
Total winding loss	P_W (W)		0.840	0.980	1.974

computer flow charts: he cannot help asking why the procedures are as they are, and how they can be extended to solve related problems. This section seeks to answer these and other questions with a view, too, to avoiding mistakes due to misinterpretation of the instructions. It is mainly qualitative in nature: mathematics have been reduced to a minimum, and higher-order effects, although included in the formulae behind the design aids, are generally not discussed.

EDDY-CURRENT EFFECTS IN WINDINGS

Transformer Magnetics

The main flux that couples primary and secondary windings is core-bound.

Since primary and secondary ampere turns oppose, the instantaneous value of the mutual flux is determined by the instantaneous difference between them. The magnetizing flux is proportional to the induced mmf per turn. In an ideal transformer (zero core reluctance and zero winding resistance) with a short-circuited secondary, the induced mmf and, thus, the magnetizing flux are both zero.

Flux also crosses the winding space. This flux is not common to all windings, and not even to all turns in the same winding, and is, therefore, known as leakage flux.

Figure 3a shows the leakage flux paths in a simple, ideal, short-circuited transformer (with no main flux). Within the winding space, primary and secondary leakage flux lie in the same direction. Since they mutually repel, they are in parallel with the interface between primary and secondary; that is, in parallel with the layers if the windings are on top of each other. Thus, in order not to jeopardize this parallelism, only complete layers of equal breadth will be considered.

The leakage flux-density is maximum at the interface between primary and secondary, Figure 3b. On both sides of this maximum, the flux-density falls roughly linearly to zero over the height of the winding.

Consider a flux path crossing the winding window at a distance x from the wall of the coil former. Figure 3a. Assuming that the current density over the height of the primary is constant.

$$\oint \frac{B}{\mu_O} ds = NI\frac{x}{H_1}$$

where B is the flux-density, s is the distance along the flux path, and NIx/H_1 is the number of ampere-turns enclosed. The field strength is negligible in the (high-permeability) core, and is assumed constant over the winding breadth, so that the leakage flux-density

$$B = \mu_O \times \frac{N}{b} \times I \times \frac{x}{H_1}$$

where b is the flux-path length outside core material. Figure 3b shows how B varies over the height of the wound area. There is a good case for arguing that, if b_W is smaller than the width of the winding window (perhaps due to creepage allowance), b should be taken equal to b_W. Note that leakage flux is not due to imperfect core material, but is an intrinsic property of a winding.

The leakage flux through the windings gives rise to eddy currents in the conductors.

In a transformer of normal construction, the leakage flux lies parallel to the layers of the winding and roughly normal to the turns.

Note that the leakage flux-density varies from layer to layer. In any given layer (e.g., at height x in Figure 3a) the leakage flux-density is proportional to the sum of the ampere-turns in that layer and the ampere-turns in the layers between that layer and the nearest point of zero flux-density.

The average leakage flux-density and, thus, the eddy-current losses, can be reduced by suitably mixing primary and secondary windings. One result of this process is the split/sandwiched configuration of Figure 4b.

Figure 4a again shows the leakage-flux distribution of a basic transformer winding arrangement. In Figure 4b, the primary winding is split into halves, with the secondary sandwiched between them. This halves the peak flux-density.

To make this construction possible, the split winding must have an even number of turns, and an even total number of layers. The sandwiched winding, although physically one unit, can also be regarded as consisting of two portions; its leakage flux distribution is shown in more detail so that it can be seen that it may have an odd number of layers. Then, each portion contains a 'half' layer: a layer having half the *height* of a normal layer. Similarly, a portion of a sandwiched winding may contain a 'half' turn if the 'half' layer has an odd number of turns.

Due to the symmetry of the split/sandwiched configuration, only one portion of each winding need be considered in calculating the eddy-current effects.

The splitting-and-sandwiching process could, of course, be repeated to further reduce eddy-current loss. However, this quickly becomes unpractical: each interface between primary and secondary portions requires extra insulation, usually including screens to reduce radio frequency interference. Their presence reduces the space (copper) factor attainable in the winding window, eventually to such a degree that any improvement is either lost or not worth the extra complication.

A distinction can thus be made between

- simple windings, as in Figure 4a
- split windings, such as the primary in Figure 4b.
- sandwiched windings, such as the secondary in Figure 4b.

The design process described in this section deals exclusively with winding portions:

- a complete simple winding
- one half of a split winding
- one half of a sandwiched winding.

In the split/sandwiched winding configuration, the number of turns in a winding portion is half that in the complete primary or secondary.

Penetration of an Electromagnetic Wave Into a Conductor

Eddy currents are induced in a conductor exposed to an electromagnetic wave. They oppose the penetration of the wave and, in

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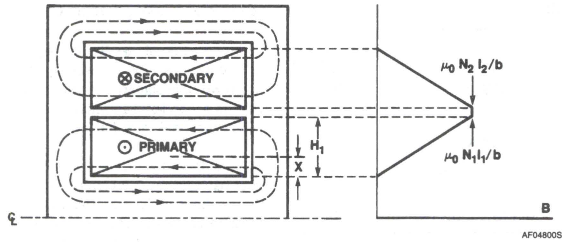
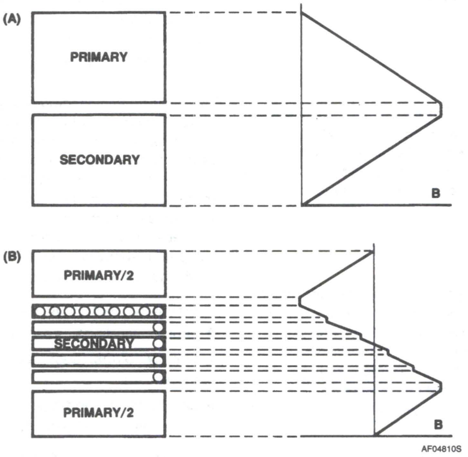


a. Leakage Flux Paths in an Idealized, Short Circuited (to Main Flux) Transformer

b. Flux-Density Distribution

Figure 3



NOTE:
Either side of the secondary is to halve the peak leakage flux and, consequently, the eddy currents.

Figure 4. The Effect of Splitting a Transformer Primary Into Two Portions

resistive conductors, transform electromagnetic energy into heat.

Let plane x = 0 be the surface of a conductor of infinite depth. The electric and magnetic fields of a plane electromagnetic wave propagating in the nonconducting semi-space above the conductor, and incident perpendicularly upon it, are tangential to the surface and mutually perpendicular. If the positive x axis is into the conductor, the penetrating wave can be described by

$$A \exp\left\{-\frac{x}{\Delta} + j\left(\omega t - \frac{x}{\Delta} + \phi\right)\right\}$$

Constants A and ϕ (part of the incident energy is reflected from the surface) are not of interest here. The amplitude of the wave decays within the conductor as $c^{-x/\Delta}$, where Δ depends on the properties of the conductor and the frequency of the wave.

At a depth $x = \Delta$ the amplitude of the wave has decreased to 1/e of its value at the surface and the phase is delayed one radian. At a depth equal to a small multiple of Δ, there is no field in the bulk of the conductor and, consequently, no induced current.

At $x = 2\pi\Delta$, where the phase delay is just 2π radian, the field strengths decay to the negligible value $e^{-2\pi} = 0.0019$. This is at a depth of one wavelength of the penetrating wave.

Skin Effect

A straight, isolated, round wire carrying alternating current generates a concentric, circular magnetic field: both in the wire itself and in the surrounding space.

Isolated in this context means that there are neither other conductors nor magnetic fields in the vicinity of the wire. The low frequency field distribution under these circumstances is shown in Figure 5. The field is tangential to the surface of the wire. This field induces eddy currents that oppose its penetration, enhancing the current flow near the surface and reducing it near the center of the wire as shown in Figure 6.

The net current flow remains the same, but the current density is nonuniform. This effect increases with wire diameter and frequency. The magnetic field within the wire is also redistributed.

As was the case with the penetrating electromagnetic wave, there is a tendency for current to flow only near to the surface of the wire: the skin effect.

Figure 7 shows the current distribution carrying the same alternating current at various frequencies. As frequency increases, Δ decreases and d/Δ increases.

This current redistribution results in the AC resistance of the wire being greater than its DC resistance.

The voltage is constant over any cross-section of the wire normal to its axis since there can be no radial current flow. In general, the voltage across a length of the wire is the sum of resistive and induced voltage drops. With a relatively thick wire ($c/\Delta \gg 1$), the voltage drop near the centre is mainly induced by the eddy currents, whereas, near the surface, where the current density is high, the voltage drop is mainly resistive.

If the wire is replaced by a tube of the same material and diameter, such that the tube has the same DC resistance as the wire of AC, its wall thickness will be equal to Δ, provided that the curvature of the surface is negligible ($d \gg \Delta$). For this reason, Δ is known as the (equivalent) skin thickness.

The term "penetration depth" is often used for Δ, but some authorities prefer this term for the wavelength ($2\pi\Delta$) of the penetrating wave discussed above. The (uniform) current density in the equivalent tube is equal to that at the surface of the wire it replaces. The ratio of AC resistance to DC resistance due to skin effect can be deduced from the relative cross-sectional areas of wire and tube:

$$F_R \cong \frac{d}{4\Delta}, \left(\frac{d}{\Delta} \gg 1, \text{ in practice}\right.$$

$$\left.F_R \cong \tfrac{1}{4}\left(\frac{d}{\Delta} + 1\right) \text{ if } \frac{d}{\Delta} \geqslant 5\right).$$

The AC resistance perimeter length of wire is proportional to d^{-1}, although the DC resistance is proportional to d^{-2}.

Skin thickness Δ depends on conductor material and frequency:

$$\Delta = \sqrt{\frac{\rho}{\pi \mu_O \mu_R f}}$$

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The current redistribution establishes an equilibrium between inductive and resistive voltage drops. Increasing the frequency does not alter the flux-density at the surface because the current remains constant, but does cause an increase in the induced voltage which results in a smaller skin thickness and, thus, a higher current density. This, in turn results in a higher resistive voltage drop which opposes the concentration of current at the surface. A new equilibrium is achieved at a skin thickness proportional to $1/\sqrt{f}$. Similar reasoning can be established for the effect of μ_R and ρ.

The skin thickness itself is independent of the current carried by the wire. Because the wire is is immersed in its own field, there is a fixed relationship between average current density and magnetic flux-density.

Proximity Effect

A different class of eddy currents is found in wire exposed to an external alternating magnetic field normal to the axis of the wire. In that case, eddy-current flow in opposite sides of the wire is in opposite directions, figure 8.

Eddy-current flow is confined to a skin below the conductor surfaces that are tangential to the external field. No net current flow is assumed in the wire. To avoid the complications of a curved surface, a rectangular conductor is shown in Figure 8.

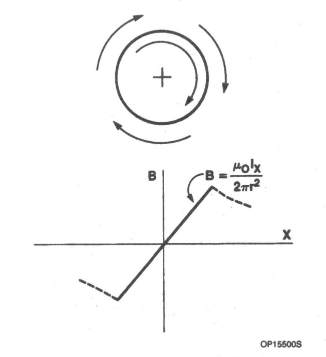
The situation resembles that of a turn in a winding exposed to leakage flux.

The essential difference is that the turn carries an alternating current, and that the leakage flux-density is proportional to this current. The relationship between current and leakage flux is not the same all over the winding, but depends on the position of the layer which contains the turn under consideration.

Because the leakage flux to which the turn is exposed originates from other turns in proximity to it, the eddy-current phenomenon is known as the proximity effect in this case.

Figure 9a represents a section through a few turns in a layer with the concentric magnetic flux paths associated with an isolated wire. Between the turns, however, individual flux lines, which are roughly perpendicular to the layer, oppose and so tend to cancel. The result is the flux pattern of Figure 9b. Such flux patterns from a number of layers result in the flux distribution of Figures 3 and 4. The difference between the two types of eddy-current effect is now evident.

Skin effect: tendency for the current to flow near the conductor surface, no current reversal and thus no increase in current flow. Proximity effect: there are two skin regions below the surfaces tangential to the magnetic field; besides the tendency for the main current to flow in the skin region where the magnetic field is highest, the skin regions carry opposite eddy currents that increase the effective current flow.



NOTE:
X is the distance from the center of the conductor, and r is the conductor radius.

Figure 5. Low-Frequency Distribution of Flux Density B About a Round Current-Carrying Conductor

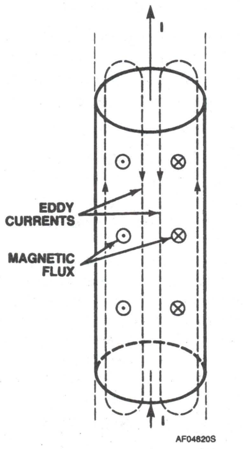


Figure 6. The Magnetic Field Generated by an AC Current in a Wire Induces Currents in the Wire that Oppose its Own Penetration

The leakage flux-density varies from layer to layer, but is constant over the breadth of each layer (Figures 3 and 4). The proximity effect is greatest in the layers at both sides of the interface between primary and secondary, where the leakage flux-density is greatest.

The simplest case is that of a strip or foil winding, where each layer has only one turn. The number of layers (and turns) is thus known at the start of the design process.

Figure 10, which is based on normalized conductor height, shows the relationship between proximity effect and leakage flux-density.

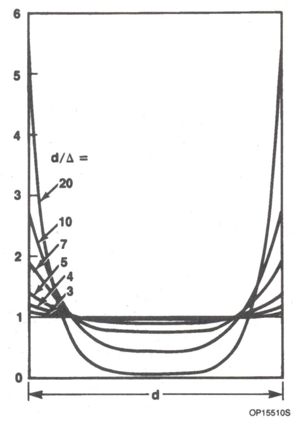


Figure 7. Current Distribution in a Wire Carrying Constant AC at Various Frequencies

The proximity effect in a wire winding depends not only on wire diameter, but also on the layer space (copper) factor.

The main geometrical parameters of a turn in a wire winding are wire diameter d and winding pitch t. Of course, $t \geqslant d_O$.

A useful simplification is to regard a round wire as a square wire of equal cross section and, thus, equal current density, Figure 11. Then, $h = d\sqrt{(\pi/4)} \cong 0.886d$. Extending this model allows a layer to be regarded as a strip of thickness h and layer space (copper) factor $F_\ell = h/t$ carrying a current N_ℓ times greater than that in the wire. The leakage flux is the same as that of the wire-wound layer, but the current density is $1/F_\ell$ times greater.

The equivalent conductor height $\varphi = h/\Delta$ for strip or foil windings, and $\varphi = (h/\Delta)\sqrt{F\ell} = (d/\Delta)\sqrt{(F\ell 4/\pi)} \cong 1.128\,(d/\Delta)\sqrt{F\ell}$ for windings of solid round wire.

Comparison of h/Δ for strip with $(h/\Delta)\sqrt{F\ell}$ for wire indicates that the skin depth in wire seems $1/\sqrt{F\ell}$ times greater than in strip. This can be understood by remembering that Δ is proportional to $\sqrt{\rho}$ and that increasing ρ or increasing the current density has the same effect on the resistive voltage drop on which the equilibrium depends.

RESISTANCE

Resistance Factor F_R

The increase in conductor resistance due to proximity effects can be expressed in terms of resistance factor F_R: the ratio of AC resistance to DC resistance.

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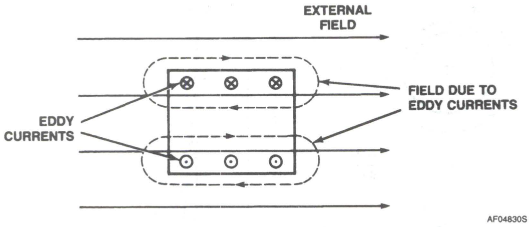
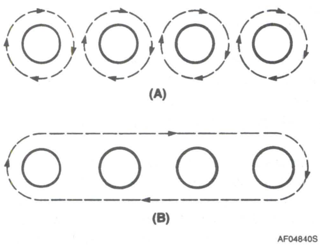


NOTE:
A rectangular conductor is shown for clarity.

Figure 8. Eddy Currents Induced in a Conductor Exposed to an Alternating Magnetic Field Normal to its Length

The chart of Figure 12 gives F_R as a function of equivalent conductor height φ, with the number of layers p as a parameter. Inspection of these curves shows that there is a region where F_R is proportional to φ. In multi-layer windings, this region commences when φ is greater than about 3, but for single layer windings, when $\varphi \geqslant 1$. This is the region of skin conduction, where no current flows in the bulk of the conductor. The situation is similar to that for skin effect when $d/\Delta \gg 1$, where F_R is proportional to d. The curve for $p = 1$ (eddy-current loss negligible when $\varphi \leqslant 1$, skin conduction when $\varphi \geqslant 1$) also represents the behavior of the first layer of a multilayer winding. The curve for $p = 0.5$ shows similar behavior, but at double the values of φ. In all layers of a multilayer winding except the first, eddy-current loss (proportional to $F_R - 1$) increases as φ_4 up to $\varphi \cong 2$, and in proportion to φ above $\varphi \cong 3$. This is most clearly demonstrated by the curve for $p = 10$, but the effect is already evident in the curve for $p = 1.5$. Eddy-current losses in the higher layers evidently dominate the AC losses in the first layer, unless $\varphi \ll 1$.



NOTE:
The concentric flux due to the winding current (a) cancels between turns so that the resultant flux lines are parallel to the layer (b).

Figure 9. Four Turns From a Layer of a Winding

This explains the difference that will become apparent later between single and half-layer windings, and multi-layer windings.

It should be noted that eddy-current loss remains proportional to φ_4 in the lower bend of the curves, below $F_R \cong 2$. The bend is due to DC loss not being negligible compared to eddy-current loss in that region (see also Figure 2, mathematically a plot of $F_R - 1$, scale calibrated for F_R).

Figure 12 is most useful for determining the AC resistance of a winding of known geometry. However, it is not a convenient basis for optimizing winding geometry itself.

AC Resistance Per Meter Conductor Length r_{AC}

The AC resistance per meter conductor length is a useful quantity for comparing various versions of a given winding design.

Winding loss is proportional to winding resistance $R_{AC} = N\ell_{AV}r_{AC}$. In a given design problem, the number of turns and coil former dimensions are known. Conductor length $N\ell_{AV}$ is only slightly influenced by the number of layers or the conductor size. Thus, achievement of the design goal — the winding geometry for minimum loss — can be reduced to the achievement of minimum r_{AC}.

Windings of Strip or Foil Conductor

The geometry of windings of full-width strip or foil conductor is completely established once strip thickness h is known.

Strip breadth is b_W, and the number of layers is equal to the number of turns in the winding portion. These are all set by the boundary conditions, so that the only parameter remaining to be determined is thickness.

Since r_{AC} is proportional to F_R/φ, its value can be derived from Dowell's chart, Figure 12.

$$r_{AC} = r_{DC}F_R = \frac{\rho}{b_W h} F_R = \frac{\rho}{b_W \Delta} \cdot \frac{F_R}{\varphi}$$

(since $\varphi = h/\Delta$)

thus

$$r_{AC}\frac{b_W \Delta}{\rho} = \frac{F_R}{\varphi}$$

Therefore, it is sufficient to plot F_R/φ against φ as in Figure 13. There, the straight, dashed line labelled $F_R = 1$ represents r_{DC}. Since r_{DC} is proportional to φ^{-1}, its slope is -1.

Each curve in Figure 13 has a minimum, marked by a dot. Each minimum occurs at the normalized, ideal* strip thickness h_{ID}/Δ and the lowest possible value of $r_{AC}b_W\Delta/\varphi$ from which the value of $r_{AC\ ID}$ can be calculated.

As, for given Δ, strip thickness increases beyond h_{ID}, eddy-current loss increases more quickly than DC loss decreases. Note that h_{ID} is independent of winding current because leakage flux-density is proportional to current density.

All minima in Figure 13 lie close to the straight line $F_R = 4/3$, although some deviation can be seen at low values of N.

In the practical design procedure, h_{ID} is found assuming this straight line, but a correction factor C_N has been added for the deviation that occurs when $N < 5$. Since, usually, $h \neq h_{ID}$, the approximation $F_R = 1 + (1/3)(h/h_{ID})^4$ is included in the design procedure to give the AC resistance.

Foil or strip conductor is only recommended for sandwiched windings, not for split or even simple windings.

There is no guarantee that current distribution is uniform over the breadth of a strip. In fact, there is a tendency for current density to be higher near the edges of a strip when $\Delta = \ll \sqrt{(b_W h)}$, which is invariably the case. Non-uniform current density cannot occur when the leakage flux is truly parallel to the layers, so advantage should be taken of the repulsive forces between the leakage flux of primary and secondary. Sandwiching a strip winding between two portions of a wire winding, whose current density must be uniform over the layer breadth, ensures that there are strong repulsive forces on both sides of the strip winding, where leakage flux-density is maximum.

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*The term "ideal" is used in preference to "optimum" since the former implies desirability but not neccesarily feasibility. A thickness other than h_{ID} may have to be used due either to conductor or space availability limitations.

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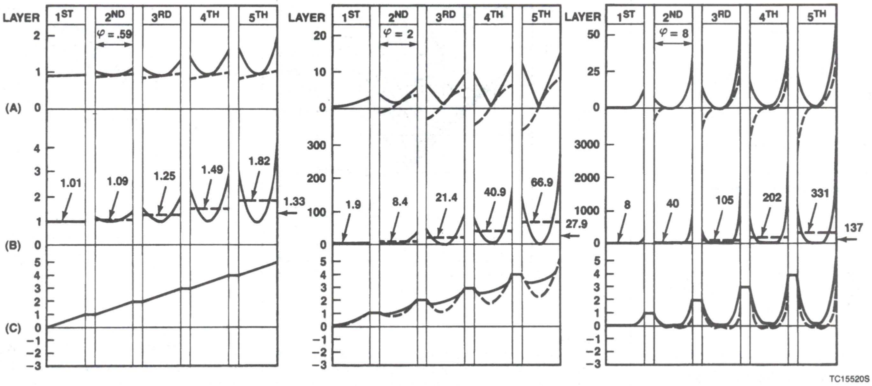

Figure 10. The Proximity Effect in a Winding of 5 Layers. Effective Conductor Heights are $\varphi = 0.59$ (Left), $\varphi = 2$ (Center) and $\varphi = 8$ (Right). Sections Through the Ends of the Layers of the Winding are Shown, Hatched. The Layers are of Strip Conductor, but Could Also be N_ℓ Turns of Rectangular Wire. The Current Density Distribution is Plotted in (a). The Full Line is the Amplitude, the Broken Line the Real Part, and the Dotted Line the Imaginary Part. The Losses are Plotted in (b). The Loss Distribution (Solid Line) is Proportional to the Square of the Current Density Amplitude. The Broken Line Shows the Average Loss in Each Layer, and the Dotted Line the Average Loss in the Complete Winding. Since the Scale Calibration is Multiples of the DC Loss, the Dotted Line Shows the Value of F_R. (c) is the Leakage Flux Diagram, Obtained by Integration of the Current Density. Scale Divisions are Layer Current; Line Types are as in (a)

Wire Windings: Winding Breadth-To-Turns Ratio T

The AC resistance per meter length of wire r_{AC} can be derived from a plot of F_R/φ_2 against φ, Figure 14.

For rectangular wire of breadth b (in the layer) and height h (normal to the layer)

$$\varphi = \frac{h}{\Delta}\sqrt{\frac{b}{t}}$$

and

$$F_R/\varphi^2 = \frac{r_{AC}\Delta^2 t}{r_{DC}h^2 b} = r_{AC}\frac{\Delta^2 t}{\rho h}$$

For round wire of diameter d

$$\varphi = \frac{h}{\Delta}\sqrt{\frac{h}{t}} = \left(\frac{\pi}{4}\right)^{3/4} \times \frac{d}{\Delta}\sqrt{\frac{d}{t}}$$

$$= \frac{1}{\Delta}\left(\frac{d}{t}\sqrt{\frac{\pi}{4}}\right)^{3/2}$$

so that, for a given ratio t/d,

$$F_R/\varphi^2 = r_{AC}\frac{\Delta^2 t}{\rho h} = r_{AC}\frac{\Delta^2 t}{\rho d}\sqrt{\frac{4}{\pi}}$$

is proportional to r_{AC}.
Here, $r_{DC} \propto \varphi^{-2}$ so that the line $F_R = 1$ has a slope of −2. Whereas Figure 13 gave the solution of the design of a strip winding, where the number of layers and conductor breadth were known, the plot of Figure 14 does not contain the solution for wire windings. The number of layers is still not known.

The winding breadth is introduced in the form of the winding breadth-to-turns ratio $T = b_W/N$.

Physically, T is the winding pitch in a single-layer winding containing all N turns. Note that at the interface between primary and secondary, the leakage flux-density $B = \mu_0 I/T$ and also that T is known at the start of the design process.

Since $t = pT$, for a rectangular wire

$$\varphi = \frac{h}{\Delta}\sqrt{\frac{b}{pT}}$$

and for round wire

$$\varphi = \left(\frac{\pi}{4}\right)^{3/4} \times \frac{d}{\Delta}\sqrt{\frac{d}{pT}}.$$

Close-Packed Windings of Round Wire

For close-packed windings, $r_{AC}\Delta^2/\rho$ can be plotted against T/Δ, Figure 15; this gives better access to the design problem.

In close-packed wire windings $t = d_O$, so the layer space (copper) factor depends on the ratio d/d_O for the wire. This ratio is not constant: standard-wire tables show that d/d_O is smallest for fine wire, but the rate of change is rather low. If Figure 14 were replotted to give $r_{AC}\Delta_2/\rho$ against t, the calibration of the axes would, of course, change, but the shape of the curves would hardly be affected because the rate of change of d/t is so low. In order to replace t by T, the values for each of the curves must be divided by p, since $T = t/p$. This shifts every curve horizontally a distance — log p.

The introduction of T is an important step forward: knowing T/Δ, it is possible to read the lowest possible value of $r_{AC}\Delta^2/\rho$, the optimum number of layers, and, finally, from $d_O = t = pT$, the optimum wire size can be determined.

In order to plot Figure 15, values of d/d_O and its variation with wire size were estimated. So, although the plot of Figure 15 is adequate for illustrating the theory, its accuracy is not sufficient for practical design purposes.

Spaced Windings of Round Wire

Windings are also possible with a pitch greater than the overall wire diameter: spaced windings. This introduces an additional degree of freedom that can be exploited to achieve a further reduction in AC resistance. This is illustrated by the plot of Figure 16.

The solid curves in Figure 16 are for close-packed windings ($t = d_O$), as in Figure 15. The dash-dot curves are for windings of two layers, in which $t > d_O$. These show that there is a range of T/Δ where spacing results in lower values of r_{AC}. However, spacing should not be excessive: better performance is always possible if a smaller number of layers can be used.

The straight dashed lines in Figure 16 are a further addition: they show that spacing displaces the curves so that similar points lie on a line of slope $-2/3$. They also show that the curves for $p \leqslant 1$ are so steep that spacing brings no improvement.

In effect, spacing allows designs intermediate between close-packed versions.

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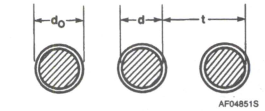
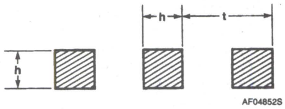


a. Principal Geometrical Parameters Describing a Turn in a Given Layer



b. Replacing a Round Wire With a Square One of Equal Cross Sectional Area Simplifies the Discussion Since Now a Layer

Figure 11

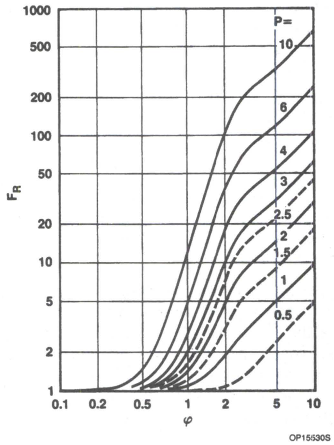
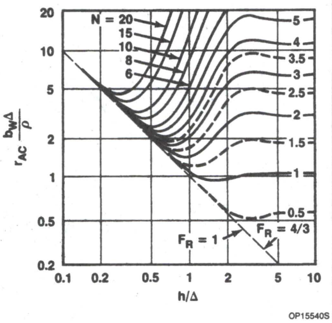


Figure 12. Resistance Factor F_R vs Equivalent Conductor Height φ, With Number of Layers p as a Parameter



NOTE:
This virtually solves the design problem for strip windings. Given the number of turns N, the minimum in the appropriate curves gives the ideal (lowest loss) strip thickness as a multiple of the skin thickness. The resistance per meter length of strip can also be determined.

Figure 13. Plot of F_R/φvsφ

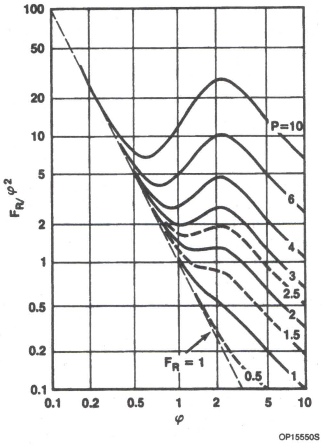


Figure 14. Plot of F_R/φ^2 Versus φ, a First Step Towards the Solution of the Design Problem for Wire Winding

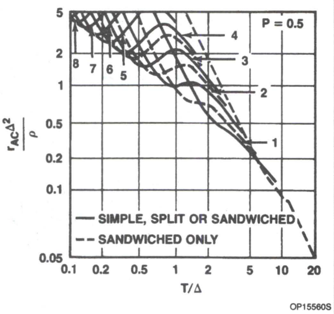


Figure 15. Plot of $r_{AC}\Delta^2/\rho$ Versus T/Δ With P as a Parameter for Close-Packed Wire Windings

The Basic Solution of the Design Problem

Sufficient information is now available to make a plot that effectively solves the design problem. This is given as Figure 17.

Figure 17a differs from Figure 14 in that spaced windings are included where they give lower loss. Furthermore, those parts of the curves for close-packed windings that are not useful for design purposes have been suppressed.

The full lines apply to optimum designs with an integral number of layers. The broken lines apply to optimum designs with a half layer (except in the plot of winding height, these often coincide with the full-line curves). The dotted lines are for non-optimum, close-packed windings.

There it can be seen that, if T/Δ is known, the optimum design is completely determined. Further inspection reveals that:

- for T/Δ greater than about 2, the optimum design is a single-layer winding but, in sandwiched designs, when T/Δ is greater than about 6, the optimum is a half-layer winding
- for T/Δ less than about 2, the optimum design has more than one layer.

Both the full and the broken lines for $p > 1$ show that the resistance minima occur generally for spaced windings so that it is important to include in the manufacturing instructions a specific statement that windings should not be close packed. The curves for $p \leqslant 1$ have a slope of about −1, indicating that $F_R \propto \varphi^{-1}$, so that they belong to the region of skin conduction. Moreover, they are, in principle, close-packed windings. It is clear that multilayer ($p > 1$) windings and those with $p \leqslant 1$ will require different design methods.

Multilayer Windings ($p > 1$)

The full lines in the chart for $r_{AC}\Delta^2/\rho$ and d/Δ, Figure 17, consist of several sections, each for a particular value of p. Together, for $p > 1$, they form nearly straight lines.

The ideal values of d and r_{AC} are, thus, generally independent of p. There is only a slight deviation for the lower values of p: it can be seen that the lines for $p = 1.5$ do not coincide with those for $p = 2$.

The resistance factor for optimum or ideal designs $F_{R\ ID} \cong 1.5$, which means that the eddy current loss is half the frequency-independent resistive loss, also called DC loss.

The slope of the straight lines indicates that $r_{AC\ ID} \propto (T/\Delta)^{-2/3}$ and $d_{ID} \propto (T/\Delta)^{1/3}$. Since $r_{DC} \propto d^{-2}$, $F_R = r_{AC}/r_{DC}$ must be constant.

If the actual wire diameter d deviates from the ideal diameter d_{ID}, the estimated resistance factor becomes

$$F_R = 1 + \tfrac{1}{2}\left(\frac{d}{d_{ID}}\right)^6$$

This approximation, derived from the first two terms of the series expansion of Dowell's expression, is sufficiently accurate for values of $F_R \leqslant 2$. In an ideal winding, where $d = d_{ID}$, $F_R = 1.5$. The expression is not valid in the region of skin conduction.

To find the ideal wire diameter for windings having a large number of layers, the expression $d_\infty/\Delta = 1.45\ (T/\Delta)^{1/3}$ can be used. In a more practical form this expression reads

$$d_\infty = \left(\frac{17.1\text{bw}}{\text{Nf}_e}\right)^{1/3} \quad \text{where } f_e \text{ is in kHz.}$$

The ideal wire diameter for a practical winding, d_{ID}, is then obtained using the correction factor C_p.

This factor corrects for the effect of the small steps between the line sections for practical numbers of layers.

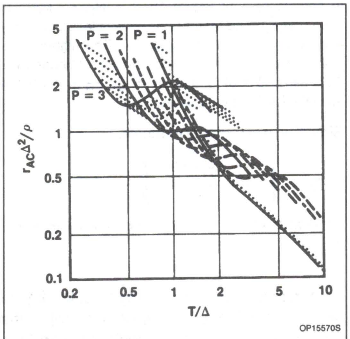
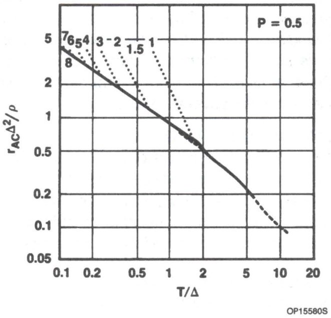
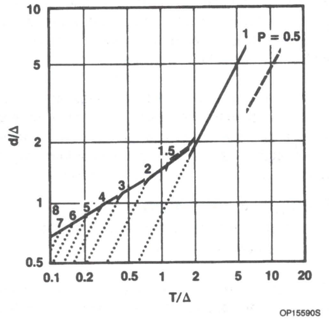


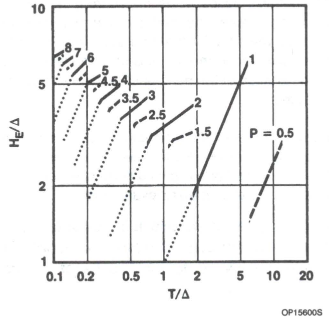
Figure 16. Plot of $r_{AC}\Delta^2/\rho$ vs T/Δ Extended for Spaced Windings



a. $r_{AC}\Delta_2/\rho$



b. d/Δ



c. H_l/Δ vs T/Δ With ρ as a Parameter

NOTE:
H_e is the required height excluding interleaving. Knowing T/Δ, the ideal winding geometry and the resistance per meter length of wire can be determined.

Figure 17. Basic Design Charts for Wire Windings

Using these expressions, ideal designs can be obtained by simple calculation.

Once knowing d_{ID} the winding geometry can be determined. After rounding d_{ID} to the nearest standard wire size, d_O is known. Following the design rules in the practical sections, the number of layers and the required height are easily found. Knowing r_{DC} of the selected wire, r_{AC} can be estimated after calculation of F_R.

Single-Layer and Half-Layer Windings

This is the region where the procedures of the previous section lead to a number of layers $p \leqslant 1$.

This definition is given because the criterion $T/\Delta > 2$ is only an indication.

First it is necessary to decide between strip and wire windings.

Strip or foil windings are often preferable.

For simple and split designs, it is known that $p = 1$. This is also the case in sandwiched designs if T/Δ is below about 6. Since windings should be close packed, geometry is fixed.

The end of the curve for $p = 1$ at $T/\Delta = 6$ is not a theoretical limit; the curve can be extended. But d may be so great that a different form of conductor will probably be chosen.

For sandwiched windings, a half-layer winding may be preferable, provided T/Δ is greater than about 6.

That saves winding height without a loss penalty. In case of doubt ($T/\Delta \cong 6$), a choice can be made after having worked out both alternatives.

The remaining problem is the estimation of r_{AC}. To solve that, calculate

$$\varphi = \left(\frac{\pi}{4}\right)^{3/4} \times \frac{d}{\Delta}\sqrt{\frac{d}{pT}}$$

or, alternatively,

$$\varphi = \sqrt{(0.124 f_e d^3/t)}$$

and read F_R from the plot of F_R versus φ, Figure 2.

Figure 2 gives the F_R plot in a more suitable form than Figure 12. Do not use the expression for F_R given in the previous section: it is not valid in the region of skin conduction.

Winding Height

Ideal Designs

In previous sections, methods were developed for designing minimum-loss windings of both strip and wire conductors. In developing these methods, possible height restrictions have so far been ignored.

By doing this, each winding could be treated separately, the design of a primary was not influenced by the secondary, and vice versa.

Such designs, not affected by a height restriction, are called ideal designs.

Similarly, terms such as ideal windings, ideal number of layers, ideal conductor size, etc., are also used.

It is, of course, necessary to check whether the situation is ideal: that the height of the winding window does not impose a height restriction on the windings.

The height of a winding (portion) is calculated from:
for strip windings, $H = N\ (h + i)$
for wire windings, $H = p\ (d_O + i)$.
For the available winding height (the height available for all power-transferring windings), see the section on "Given Boundary Conditions".

Non-Ideal Design Versions

In strip windings the only way to reduce winding height is to use thinner strip.

Various non-ideal design versions are found by repeatedly stepping to a smaller available strip thickness. The AC resistance is found from the expression for F_R.

In wire windings, a smaller winding height is obtained by reducing p. This leads to reduced pitch ($t = pT$) and thus, also, to reduced wire size ($d_O \leqslant t$), so that $d < d_{ID}$. To reduce the difference between d and d_{ID} as far as possible, a non-ideal wire winding should be close-packed using the thickest possible wire for the number of layers and winding breadth. The AC resistance can be estimated by means of the expression for F_R.

Several non-ideal design versions are found by repeatedly stepping to a lower number of layers.

Thus, non-ideal as well as ideal design versions can be found. Although these non-ideal design versions have smaller winding height than the ideal design, they also have higher loss.

IMPORTANT

There is no justification for using conductor sizes in excess of the ideal size (apart from rounding a calculated ideal size to the available size). Reduction of current density is a false motive. The extra conductor material has only an adverse effect.

Accommodation

Once a few design versions (the ideal design and one or more non-ideal versions) of the primary and secondary have been collected, selection of the most suitable combination is made by an accommodation procedure.

The accommodation procedure is given in detail and comprises the following basic steps:

- List the design versions obtained, the height they require and their losses
- Make combinations of primary and secondary designs having a total height not exceeding the available height, and note the winding loss of each
- Finally, select the lowest-loss combination.

Demagnetizing and control windings are usually designed for minimum height rather than minimum loss, since they do not take part in power transfer. Their height is taken into account in determining the height available for the power windings.

Design Evaluation

A design attempt is successful if the transformer does not run hot.

Final evaluation is, of course, experimental. Unnecessary experimentation can, however, be avoided if the estimated losses are first compared with the estimated permissible loss.

The permissible loss is estimated from the permissible temperature rise and the thermal resistance given in the data for the core selected*. Core loss was estimated in the process of core selection and determination of the number of primary and secondary turns.

Current densities much higher than are usual in low-frequency transformers may well be acceptable. As has been mentioned, conductors in excess of the ideal size make matters even worse.

If a design attempt fails, it is advisable to first review the chosen boundary conditions. This would not invalidate the results of the core selection procedure.

An improvement may be obtained by using split/sandwiched rather than simple windings. These tend to lower r_{AC}, thicker conductors and increased height. A different conductor form might also be considered.

A new start, including the core selection procedure, is required if the given boundary conditions have to be altered.

It may be possible to use same core size if switching frequency is increased. This leads to fewer turns, of thicker conductors and, thus, lower winding loss.

To avoid fruitless effort, the practical design process is so organized that an initial design evaluation is made as soon as suitable ideal designs and their losses have been determined.

Winding height can be reduced with the penalty of increased loss and vice versa (by using bunched wire, for example) but this will not help if the ideal design has neither loss nor height reserve.

Some Notes

Multiple-Output Transformers

Figure 18 shows a possible winding arrangement and leakage flux density distribution for a multiple output transformer.

In both primary and secondary 2, the flux-density varies from zero to a maximum, so these can be designed using the present methods. That is not possible for secondary 1 because its leakage flux distribution does not agree with the assumptions. The ratio of leakage flux-density to number of turns is much higher than has been assumed so far.

The ideal wire diameter for an infinite number of layers d_∞ in the winding exposed to the higher leakage flux is calculated as normal, but the layer correction factor becomes

$$C_p = \sqrt{\frac{1-\vartheta}{(1-\vartheta^3)^{1/3}}}$$

where ϑ is the ratio of minimum to maximum leakage field over the height of the winding.

In secondary 1 of Figure 18, $\vartheta = (N_{SEC\ 2}\ I_{SEC\ 2})/(N_{PRIM} I_{PRIM})$. The factor C_p is always less than unity and decreases with increasing ϑ. The higher leakage field is compensated for by using thinner wire. As is usual ($\vartheta = 0$) for wire windings, $F_{R\ ID} \cong 1.5$: the formula for F_R still applies.

Similarly, for strip conductor,

$$C_N = \left\{ \frac{(1-\vartheta)^3)^{1/4}}{1-\vartheta^3} \right\}$$

As normal ($\vartheta = 0$) for strip windings, $F_{R\ ID} \cong 4/3$.

To obtain lowest total winding loss, the layout of the secondary windings (2 or more) in the winding window must be considered carefully.

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*The thermal resistances in the published data can be reduced by potting the transformers. If this is to be done, it might be possible to eliminate the creepage distance, so increasing winding breadth. The loss in each winding can be estimated as $P_W = I^2 N \ell_{AV} r_{AC}$

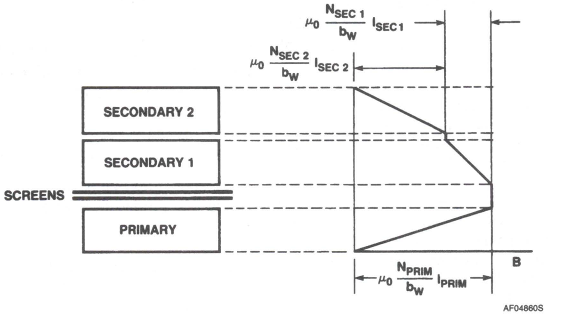
$\mu_0 \frac{N_{SEC\,1}}{b_W} I_{SEC\,1}$
$\mu_0 \frac{N_{SEC\,2}}{b_W} I_{SEC\,2}$
SECONDARY 2
SECONDARY 1
SCREENS
PRIMARY
B
$\mu_0 \frac{N_{PRIM}}{b_W} I_{PRIM}$
AF04860S

Figure 18. An Example of a Multiple-Output Transformer With Corresponding Leakage Flux Diagram

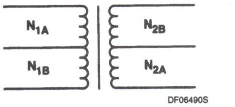

Figure 19. Push-Pull Transformer Windings Divided to Define Conduction Periods

- Secondaries of the same conductor type, either wire or strip: exposing the winding carrying the smallest current, that is, the one using the thinnest conductor, to the highest leakage field will result in lowest loss. Remember that the eddy current loss increases in proportion to φ^4.
- Secondaries of different conductor type (wire or strip): the optimum arrangement is not easy to predict. Work out the possible layouts and select for lowest total loss.

Push-Pull Transformers

In push-pull transformers, Figure 19, not all windings carry current at the same time.

The operation of a push-pull converter is explained in Part 1 of this series of publications. Here it is sufficient to split up one converter operating period into

- Interval a: N_{1A} and N_{2A} are conducting, other windings carry no current. During this interval the current waveforms in N_{1A} and N_{2A} are the same.
- Interval b: N_{1B} and N_{2B} are conducting.
- Interval c, occurring twice per period: N_{1A} and N_{1B} are nonconducting, N_{2A} and N_{2B} carry equal and opposite flywheel currents about half as great as the secondary currents during intervals a and b (magnetizing current neglected). The closer intervals a and b approach a half period (at full load) the shorter this interval will be. Whether or not the flywheel current pulses have an influence on winding design depends on the winding arrangement.

Bifilar windings are often used to achieve close coupling between winding halves.

Figure 20 shows a cross-section through the windings and the leakage flux diagrams during the three intervals.

If wire windings are used the flywheel currents during interval c cancel (higher order effects neglected). That is not quite so if 'bifilar' strip windings are used (two full-breadth strips and interleavings wound simultaneously). The peak flux-density is then about $1/(2N_2)$ times that during intervals a or b. Since the eddy-current loss is proportional to the square of frequency and flux-density, the eddy-current loss in interval c may be negligible if the half-secondaries have at least a few turns. It might not be possible to ignore the contribution of the flywheel currents to the DC loss unless interval c is very short.

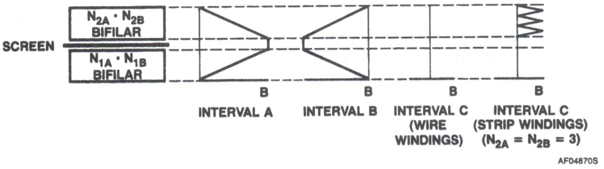
$N_{2A} \cdot N_{2B}$ BIFILAR
SCREEN
$N_{1A} \cdot N_{1B}$ BIFILAR
B
B
B
B
INTERVAL A
INTERVAL B
INTERVAL C (WIRE WINDINGS)
INTERVAL C (STRIP WINDINGS) ($N_{2A} = N_{2B} = 3$)
AF04870S

Figure 20. Cross-Section Through the Windings of a Bifilar-Wound Push-Pull Transformer Together With the Leakage Flux Diagrams for the Conduction Intervals Described in the Text

During intervals a and b, eddy currents are generated in both the conducting and the non-conducting windings.

Both windings of a pair are exposed to the same leakage flux and have about equal eddy-current loss. Only one of these has DC loss at a time.

For minimum loss (ideal designs), the ratio of eddy-current loss to DC loss remains one half for wire windings and one third for strip windings. That requires thinner conductors than in non-bifilar windings having equal numbers of turns, and winding pitch or strip breadth.

For multilayer wire windings, the reduction is $2^{-1/6} = 0.89$ (one step in the wire table), and for strip windings, $2^{-1/4} = 0.84$.

The reader can adapt the design procedures to cope with bifilar windings, as noted in the section "Phase II: Determine the Ideal Power Windings."

Multilayer wire windings:
— in step 1 multiply d_∞ by 0.89
— in step 4 use $2t_{MIN}$ in the expression for p_{ID}
— in step 9 calculate the loss in a winding pair.

Single-layer wire windings:
— in step 2, use $2t_{MIN}$ rather than t_{MIN}
— in step 6, calculate $r_{AC} = (2F_R - 1)r_{DC}$
— in step 7, estimate the loss of a winding pair.

Strip or foil windings:
— in step 1, multiply C_N by 0.84
— in step 5, estimate the loss of a winding pair.

Bifilar windings are not possible if the wire insulation cannot safely withstand at least twice the peak voltage across a winding half.

The transformer of Figure 21 differs from the previous one in that the primary winding halves do not share the same space.

The leakage flux diagrams show an asymmetry. During interval a winding N_{1B}, although not conducting, is subjected to a high leakage flux and has about three times the eddy current loss of the conducting winding N_{1A}, because the average of the RMS flux-density squared in N_{1A} is one third of that in N_{1B}. In interval b, however, N_{1A} has no eddy-current loss. The primary winding halves thus have different AC resistance due to a difference in eddy-current loss by a factor of four. Moreover, the leakage inductance is greater in N_{1A}. The energy stored in the leakage field can be expressed as $\frac{1}{2}LI^2$ or as $\frac{1}{2}VB^2/\mu_O$, where L is the leakage inductance and V the field volume (here proportional to the area of the flux diagram times the average turn length).

By arranging the windings as in Figure 22, only a minor asymmetry due to different turn lengths remains and eddy-current loss in the non-conducting primary is eliminated. In this arrangement the coupling between the primary winding halves will be less close and the stray capacitance across the secondaries, now situated between two screens, will be increased.

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In Figure 23, the secondaries are also divided: non-conducting windings are not exposed to leakage flux. Now eddy-current loss during interval c occurs in the secondaries.

This indicates the effect of different current waveforms in primaries and secondaries, which means that their effective frequencies are different.

For split/sandwiched configurations, similar considerations apply as indicated above for simple configurations.

Here, also, leakage flux diagrams will be of great help in the analysis. The discussion in this Section clearly illustrates the general risk of overlooking important parameters in striving for an optimum in a particular respect.

Flyback Transformers

In a flyback transformer, current conduction in primary and secondary occurs alternately. When the primary conducts, there is no current in the secondary, and vice versa. Two different leakage flux-density diagrams are thus required, as in Figure 24.

The flux diagrams shown do not pretend to be accurate. In drawing the full-line portions, tight coupling to the core and a leakage flux parallel to the layers were assumed. However, since the repulsion between primary and secondary flux does not exist, the latter assumption is an idealization. The broken lines are speculative.
It is therefore recommended that the outer winding has the thinner wire.

The leakage flux generated by the current in the inner winding also induces eddy currents in the outer winding.

As a practical guide, it is recommended that the outer winding be wound with a wire one size smaller than that calculated using the procedures given in this article. The estimated winding loss will then probably prove slightly optimistic.

Although the present design methods are not as accurate for flyback transformers as they are for forward and push-pull types, their use is helpful in preventing excessive eddy-current loss.

Strip or foil windings: Since the leakage flux might not be truly parallel to the layers, we should not be surprised if the losses are higher than calculated. The current density near the edges of the conductor might be considerably higher than near the middle of the breadth. That effect is nearly independent of the conductor thickness. The use of multiple-wire, bunched or Litz-wire might be a better solution for low-voltage windings.

Screens

Eddy-current losses will also occur in the screens between primary and secondary.

Screens are always situated in positions of maximum flux-density.

Screens should not be thicker than necessary; there should be the minimum of overlap of the ends. Copper is not the most suitable material: a (non-magnetic) conductor of higher resistivity is preferable.

Eddy-current loss is directly proportional to conductivity, and proportional to the thickness cubed. Thus, screens should be as thin as possible (UL-1244 specifies a minimum of 0.15mm).

Although its low resistivity makes copper the natural choice for the winding conductor, it is not the first choice for screens. Phosphor bronze CuSn8 has a resistivity 10.9% of that of copper at 20°C and 13.8% at 100°C. The use of such a material reduces losses in proportion.

Additional loss can be caused by the capacitance of the overlap at the ends of the screen, which causes the screen to act as a shorted turn. This overlap should be as small as possible.

CHOSEN BOUNDARY CONDITIONS

Once the given boundary conditions have been established from the choice of core and numbers of primary and secondary turns, the designer can choose winding configuration and conductor type.

Winding Configuration

The designer can choose between:

- Simple windings
- Split/sandwiched windings

The lower losses of split/sandwiched windings arising from the halved peak leakage flux-density will be evaluated further, as will also the required winding height.

In the split/sandwiched configuration, a winding portion has half the number of turns of the complete primary or secondary winding. Hence the value of $T = b_W/N$ is doubled.

Strip or Foil Windings

The use of strip or foil windings is only recommended for sandwiched windings. The following discussion is given for completeness, because the route of a design process cannot always be predicted.

Analysis of the design formula shows that for moderate values of N (where $C_N \cong 1$), halving N increases h_{id} by a factor of about $\sqrt{2}$. Since the total number of turns in the complete winding remains the same, sandwiching increases the height of the ideal winding by 41%.

The influence of the interleaving is neglected. Besides the increase in required height, the extra winding interface with its insulation and screening reduces the available height.

In the extreme case, where N changes from 1 to 0.5, h_{ID} doubles because C_N also increases by a factor of $\sqrt{2}$.

$F_{R\ ID}$ was shown to be about constant for all values of N. So the ideal winding resistance tends to decrease as $1/\sqrt{2}$, a reduction of 29%.

For N = 0.5, $r_{AC\ ID}$ is half that for N = 1.

A smaller improvement can be obtained where the sandwiched version must be non-ideal.

Even if the simple version has to be non-ideal it may occur that its sandwiched counterpart has a lower AC resistance.

Wire Windings

If, for a simple wire winding having at least 2 layers, the ideal design is replaced by an, also ideal, split or sandwiched winding r_{AC} will be improved by about 37%. The penalty is a considerable increase in required height.

The actual increase in height is not readily predictable, since the number of layers may change (the effect of doubling T/Δ is shown in Figure 17). In many cases the split or sandwiched version will be non-ideal, so that the improvement in resistance is smaller than 37%. The improvement of a (non-ideal) split or sandwiched winding replacing a non-ideal simple winding also varies from case to case.

The replacement of an ideal, simple, single-layer winding by an ideal, split or sandwiched winding must be considered separately. Doubling T/Δ (Figure 17) results in halving $r_{AC\ ID}$. If the result is two single-layer portions, wire diameter will be doubled, and required height quadrupled. But, if the result is two half-layer portions, wire diameter and winding height remain the same.

This will not often occur in practice, because strip or foil windings are generally preferable to single-layer windings.

Conductor Form

The designer can choose between solid round wire, strip or foil conductor, multiple-wire, bunched-wire and Litz-wire.

Strip or Foil Versus Solid Round Wire

Strip or foil is only recommended for sandwiched windings. There will seldom be more than 10 turns in a winding portion.

Usually, the total winding may have up to 20 turns with as many interleavings in the (radial) heat-flow path. Depending on current density, internal overheating may occur if the number of turns and interleavings is unduly high.

Strip or foil windings can be considered if $T/\Delta \geqslant 2$, as an alternative for single-layer or half-layer wire windings, for example. If

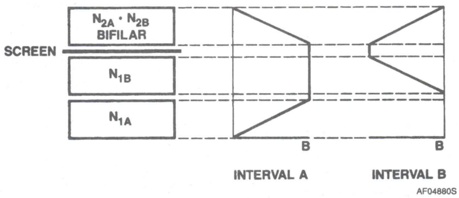


Figure 21. Cross-Section Through the Windings of a Push-Pull Transformer With a Bifilar Secondary, Together With the Leakage Flux Diagrams for Two Conduction Intervals. Note the Asymmetry

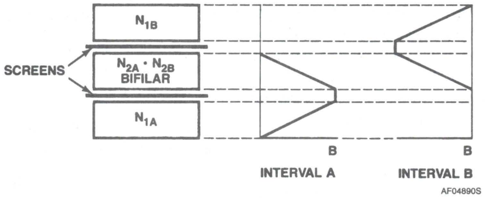


Figure 22. Rearrangement of the Windings of Figure 21 Showing the Reduced Asymmetry

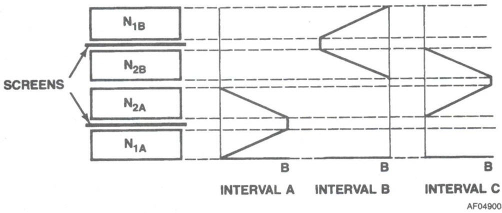


Figure 23. Cross-Section Through the Windings of a Push-Pull Transformer Showing That, With Divided Primary and Secondary Windings, the Non-Conducting Windings are not Exposed to Leakage Flux

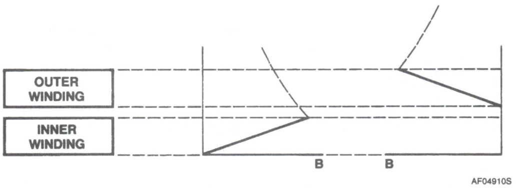


Figure 24. In a Flyback Converter Transformer, Primary and Secondary Conduct Alternately. Thus, Two Leakage Flux Diagrams are Required for Loss Analysis: One for the Inner Winding Conducting (Left) and One for the Outer Winding Conducting (Right)

the winding has only a few turns, they are a must.

In practical transformers, b_W/Δ may be assumed to be > 20. With $N \leqslant 10$, then $T/\Delta \geqslant 2$. The basic design chart for wire windings, Figure 17, shows that that is the region for single-layer or half-layer designs, for which $r_{AC\ ID}\ \Delta^2/\rho \cong 1.1(T/\Delta)^{-1}$

Choosing strip rather than wire reduces the winding resistance by a factor of about $0.9\ \sqrt{N}$ if ideal designs can be used.

If $N > 1$, the expression for the ideal strip thickness can be written as $h_{ID}/\Delta \cong 3^{1/4}N^{-1/2}$. Then, $r_{AC\ ID} = F_{R\ ID}\rho/(b_W h_{ID}) \cong (F_{R\ ID}/1.32)\ \rho N^{1/2}(b_W\Delta)^{-1}$. Since $F_{R\ ID} \cong 1.33$, dividing this result by that for wire windings obtained above yields the factor $0.9/\sqrt{N}$.

With a non-ideal strip design, the improvement over an ideal solid-wire version is, of course, smaller, but the strip version remains preferable as long as the thickness of all turns in the portion together exceeds Δ.

For a non-ideal strip version in which $F_R \cong 1$ (that is, if $h \leqslant 0.5\ h_{ID}$), $r_{AC} \cong r_{DC} = \rho/(b_W h)$. To make this smaller than the $r_{AC\ ID}$ of the wire version, $Nh > \Delta/1.1$ or, as a rule of thumb, $Nh > \Delta$.

Multiple Wire

In a multiple-wire winding, each turn consists of n_S strands lying side-by-side in the layer, Figure 25.

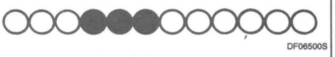
Multiple-wire turns have the height of a single strand, but an area n_S times that of a strand, and a layer space (copper) factor the same as that in a layer wound conventionally with wire of the size of each strand.

The design procedure for solid round wire windings can easily be adapted for multiple-wire.

In the basic design chart of Figure 17, after dividing T/Δ by n_S, read d_{ID}/Δ, p_{ID} and $H_{E\ ID}/\Delta$ as usual. The value of $r_{AC\ ID}\Delta^2/\rho$ for the single strand must be divided by n_S to find the resistance of the multiple wire.

In effect, a single-wire winding is designed with a layer breadth b_W/n_S, or alternatively, the winding geometry is determined as if there were $n_S N$ turns. T/Δ and r_{AC} are thus $1/n_S$ times those for a normal wire winding.

Compared with normal, single-strand, multilayer windings (more than one layer per portion, $T/\Delta < 2$), $r_{AC\ ID}$ and d_{ID} decrease



NOTE:
The strands of one turn are indicated by black dots.

Figure 25. A Multiple-Wire Winding of 4 Turns, Each of 3 Strands

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about as $n_S^{-1/3}$ and H_e increase about as $n_S^{-1/3}$.

With 2 parallel strands, Figure 26, the reduction in $r_{AC\ ID}$ and d_{ID} is about 20%: the height increase is roughly 25%. With 3 parallel strands, the reduction in $r_{AC\ ID}$ and d_{ID} is about 30%: the height increase is roughly 45%.

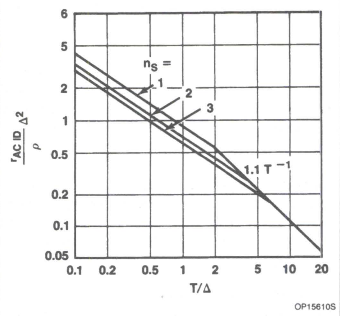
If the increased height does not permit the use of the ideal design of a multiple-wire version, the single-strand winding will often have a lower resistance. More than 3 parallel strands are not often used due to winding difficulty, or inadequate height.

In the region of $T/\Delta > 2$ it is usual to try to use strip or foil conductor. If that is not possible, multiple-wire may be considered.

Strip conductor, although promising lower resistance, cannot always be used because of uneven current distribution over the layer breadth, for example, or due to constructional problems.

If $T/\Delta > 2n_S$ lower resistance cannot be achieved, (Figure 26), but a multiple-wire winding design might be justified by reduced winding height, the use of thinner, more flexible wire, and saving in copper.

The curve for p = 1 in Figure 17 ends at $T/\Delta = 6$ only for practical reasons. There is no theoretical limit: the resistance remains inversely proportional to T/Δ. If p = 1 and $T/\Delta > 2n_S$, or if p = 0.5 and $T/\Delta > 6n_S$ the overall wire diameter and, thus, the winding height, will be found to reduce in inverse proportion to n_S. In order to understand how less copper can have equal resistance, it is necessary to realize that this is in the region of pure skin conduction ($\varphi \gg 1$). The breadth of a turn (either a single wire or n_S strands) and, thus the skin area remains the same. Stranding reduces the amount of useless conductor in the winding.



NOTE:
The improvement quickly vanishes between $T/\Delta = 2$ and $T/\Delta = 2n_S$. But if T/Δ exceeds $2n_s$, winding height and copper content are reduced by the use of thinner wire.

Figure 26. Design Chart for Multiple-Wire Windings Showing the Improvement in $r_{AC\ ID}$ Obtainable for n_s = 1, 2, and 3 Strands

Bunched-Wire

Bunched-wire comprises three or more enamelled wires, twisted around each other to form a bunch.

Here, a distinction is made between bunched-wire and Litz-wire, which latter is discussed in the next section. The difference is in the strand diameter: in bunched-wire it is of the order of magnitude of Δ, whereas in Litz-wire the strands are much finer. In the literature, the term bunched-wire is sometimes used for what is here called Litz-wire

In both bunched- and Litz-wire the strands undulate within the height of the layer. This ensures equal current sharing between the strands, because, on average, the position of each strand is in the middle of the layer height. Bunched-wire windings are designed in much the same way as single-wire windings having Nn_S turns, but adaptations of the procedures are required for the determination of winding pitch and layer height.

Litz-Wire

Litz-wire is a form of bunched-wire in which the strand diameter is small compared to Δ. Eddy-current effects are thus virtually eliminated, and the AC resistance is equal to the DC resistance.

Thus Litz-wire windings require no special design procedures: the design methods for low-frequency windings apply.

Litz-wire is standardized and commercially available.

For instance, IEC Publication 317-11 covers Litz-wire of 3 to 400 strands of 0.025mm to 0.071mm diameter. Standards and manufacturer's catalogs should be consulted for engineering data.

Litz-wire is generally only useful where ample winding space is available.

The main drawback of Litz-wire is its low space (copper) factor. Typically, only one quarter to one third of the winding space will be conductor.

NON-SINUSOIDAL CURRENT, EFFECTIVE FREQUENCY

So far, sinusoidal current waveform of frequency equal to the switching frequency has been assumed.

When considering proximity effect loss compared to DC (i.e., frequency-independent) loss, it was found that the total loss is minimum if the ratio of eddy-current loss to DC loss is 1:3 in strip or foil windings and 1:2 in multi-layer wire windings. In single-layer and half-layer windings there was no such optimum ratio.

The current waveforms associated with SMPS transformers are generally far from sinusoidal.

A non-sinusoidal repetitive waveform can be represented by a DC component, a component at the fundamental frequency (the switching frequency) and several components at harmonic frequencies. The DC component will not, of course, cause eddy-current loss: its current density is uniform over the conductor cross-section. The fundamental component has eddy-current loss as well as DC loss associated with it. This is also the case for the harmonic components, but the ratio of eddy-current to DC loss will be higher than for the fundamental.

Neglecting the non-sinusoidal character of the current waveform introduces an inaccuracy.

The sum of all eddy-current losses should be determined together with the total DC loss to ensure that they have the desired optimum ratio.

One problem is that, when designing the windings, it is not possible to make a reliable estimate of the current waveform.

Sometimes it is possible to make use of experience gained in previous designs.

Many designs have, in fact, been made as if the current were sinusoidal and the results have usually been satisfactory.

The errors due to calculation only at the switching frequency oppose. The component of loss occurring at DC is overestimated, whereas the components due to harmonics are underestimated.

The inaccuracy can be avoided by using an effective frequency in winding design.

The effective frequency is, of course, notional. It should be used only in connection with eddy-current effects.

In so far as eddy-current loss is proportional to φ^4 (that is to f^2), the effective frequency can be found from an analysis of the current waveform:

$$f_e = \frac{1}{2\pi}\,\frac{i}{I}$$

where I is the RMS winding current; i is the RMS value of dI/dt, the first derivative of the current waveform.

This expression does not apply in the region of skin conduction, where the eddy-current loss is proportional to φ or $\sqrt{f}$.

It is apparent that i contains no contribution from the DC component and a more pronounced contribution from the harmonics, since $d(\sin n\omega t)/dt = n\omega \cos n\omega t$. The rise and fall times of the current pulses have a considerable effect on the value of i. Moreover, some (if not all) of the higher harmonics lie in the region of skin conduction.

A simple method of determining f_e has not yet been found: f_e can be expected to be lower than the switching frequency f, but higher than $fI_{E\ AC}/I_E$, where $I_{e\ AC} = \sqrt{(I_e^2 - I_0^2)}$ is the RMS value of the AC component and I_0 is the DC component.

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The use of this effective frequency, despite its not being valid in the region of skin conduction, will yield the optimum winding geometry.

Single-layer windings are chosen if $p_{ID} \leqslant 1$ and since f_e is valid for determining P_{id} the choice between multilayer and single-layer windings is clear. Both single and half-layer windings are close-packed, in principle, so their layer geometry is independent of frequency.

Since the effective frequency for the skin-conduction region is not known, winding loss cannot be accurately estimated, and, consequently, a reliable choice between a single-and a half-layer winding cannot always be made. In most practical cases, however, these problems do not occur because, in any case, strip windings are preferable in this region.

For use in choke design an expression for f_e has been derived and simplified, but due to the large variation in conditions it is impossible to give a typical example for transformer design.

For the waveform of Figure 27, provided that the rise and fall times are between 15% and 85% of the repetition period.

$$f_e \cong \frac{1.3f}{\sqrt{[1 + 3(I_0/I_{AC})^2]}}$$

and the effective current

$$I_e = \sqrt{(I_0^2 + I_{AC}^2/3)}.$$

For a sinusoidal rather than a triangular waveform superimposed on a DC current.

$$f_e = \frac{f}{\sqrt{[1 + 2(I_0/I_{AC})^2]}}$$

and

$$I_e = \sqrt{(I_0^2 + 1_{AC}^2/2)}.$$

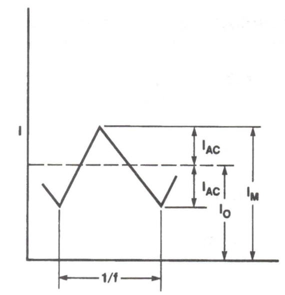

Figure 27. Current Waveform In a Smoothing Choke Idealized for the Calculation of Effective Frequency

APPENDIX: Example of Tables of Standard Wires Sizes

Enamelled Round Copper Winding Wire, IEC-grade 2

NOMINAL DIAMETER d (mm)		MAXIMUM OVERALL DIAMETER d_O (mm)	NOMINAL CROSS-SECT AREA (mm^2)	MINIMUM WINDING PITCH t_{MIN} (mm)	NOMINAL RESISTANCE AT 100°C r_{DC} (Ω/m)
0.040		0.054	0.00126	0.059	17.68
	0.045	0.061	0.00159	0.066	13.97
0.050		0.068	0.00196	0.073	11.32
	0.056	0.076	0.00246	0.082	9.022
0.063		0.085	0.00312	0.091	7.129
	0.071	0.095	0.00396	0.102	5.613
0.080		0.105	0.00503	0.112	4.421
	0.090	0.117	0.00636	0.125	3.493
0.100		0.129	0.00785	0.137	2.829
	0.112	0.143	0.00985	0.152	2.256
0.125		0.159	0.0123	0.169	1.811
	0.140	0.176	0.0154	0.187	1.444
0.160		0.199	0.0201	0.210	1.1052
	0.180	0.222	0.0254	0.234	0.8733
0.200		0.245	0.0314	0.257	0.7074
	0.224	0.272	0.0394	0.284	0.5639
0.250		0.301	0.0491	0.315	0.4527
	0.280	0.334	0.0616	0.348	0.3609
0.315		0.371	0.0779	0.387	0.2852
	0.355	0.414	0.0990	0.431	0.2245
0.400		0.462	0.126	0.481	0.1768
	0.450	0.516	0.159	0.538	0.1397
0.500		0.569	0.196	0.593	0.11318
	0.560	0.632	0.246	0.659	0.09022
0.630		0.706	0.312	0.736	0.07129
	0.710	0.790	0.396	0.823	0.05613
0.800		0.885	0.503	0.922	0.04421
	0.900	0.990	0.636	1.032	0.03493
1.000		1.093	0.785	1.139	0.02829
	1.120	1.217	0.985	1.268	0.02256
1.250		1.351	1.227	1.408	0.01811
	1.400	1.506	1.539	1.569	0.01444
1.600		1.711	2.011	1.783	0.011052
	1.800	1.916	2.545	1.996	0.008733
2.000		2.120	3.142	2.209	0.007074
	2.240	2.366	3.941	2.465	0.005639
2.500		2.631	4.909	2.742	0.004527

NOTE:
Values of t_{MIN} are based on recommendations for mass production of one particular manufacturer. Other manufacturers may use different values.

Medium Enamelled Copper Wires — AWG (B. & S.) (Diameters based on BS1844: 1952 — medium covering)

AWG (B. & S.)	NOMINAL COPPER DIAMETER d		MAXIMUM OVERALL DIAMETER d_O	NOMINAL CROSS-SECT. AREA	NOMINAL RESISTANCE AT 100°Cr_{DC}	MINIMUM WINDING PITCH t_{MIN}
	Inch	mm	(mm)	(mm^2)	(Ω/m)	(mm)
44	0.00198	0.0503	0.06604	0.00199	11.190	0.071
43	0.00222	0.0564	0.07366	0.00250	8.899	0.079
42	0.00249	0.0633	0.08128	0.00314	7.073	0.087
41	0.00280	0.0711	0.09144	0.00397	5.594	0.098
40	0.00314	0.0798	0.1041	0.00500	4.448	0.111
39	0.00353	0.0897	0.1143	0.00631	3.519	0.122
38	0.00397	0.1008	0.1295	0.00799	2.783	0.138
37	0.00445	0.1130	0.1148	0.01003	2.215	0.154
36	0.00500	0.1270	0.1626	0.0127	1.754	0.172
35	0.0056	0.1422	0.1778	0.0159	1.398	0.188
34	0.0063	0.1600	0.1981	0.0201	1.105	0.209
33	0.0071	0.1803	0.2235	0.0255	0.8700	0.236
32	0.0080	0.2032	0.2489	0.0324	0.6853	0.261
31	0.0089	0.2261	0.2743	0.0401	0.5537	0.287
30	0.0100	0.2540	0.3048	0.0507	0.4386	0.319
29	0.0113	0.2870	0.3404	0.0647	0.3435	0.356
28	0.0126	0.3200	0.3759	0.0804	0.2762	0.393
27	0.0142	0.3607	0.4191	0.1022	0.2175	0.438
26	0.0159	0.4039	0.4699	0.128	0.1735	0.491
25	0.0179	0.4547	0.5232	0.162	0.1369	0.547
24	0.0201	0.5105	0.5817	0.205	0.10860	0.608
23	0.0226	0.5740	0.6502	0.259	0.08586	0.679
22	0.0253	0.6426	0.7214	0.324	0.06852	0.754
21	0.0285	0.7239	0.8052	0.412	0.05399	0.841
20	0.0320	0.8128	0.8966	0.519	0.04283	0.937
19	0.0359	0.9119	1.003	0.653	0.03403	1.048
18	0.0403	1.024	1.118	0.823	0.02700	1.168
17	0.0453	1.151	1.247	1.040	0.02137	1.303
16	0.0508	1.290	1.389	1.308	0.01699	1.452
15	0.0571	1.450	1.557	1.652	0.01345	1.627
14	0.0641	1.628	1.737	2.082	0.010670	1.815
13	0.0720	1.829	1.943	2.627	0.008460	2.030
12	0.0808	2.052	2.172	3.308	0.006717	2.270
11	0.0907	2.304	2.431	4.168	0.005331	2.540
10	0.1019	2.588	2.720	5.261	0.004224	2.842

NOTE:
Values of t_{MIN} are based on recommendations for mass production of one particular manufacturer. Other manufacturers may use different values.

High-Frequency Ferrite Power Transformer and Choke Design

AN1261
Part 4

PART 4: IMPROVED METHOD OF POWER CHOKE DESIGN

A power smoothing choke which is to carry a significant direct current component or to have a well-defined inductance is usually wound on a core whose magnetic circuit includes an air gap. The reluctance (magnetic resistance) of this air gap reduces the effective permeability of the core: either to increase the ampere-turns at which saturation occurs, or to reduce the effect of variations in the permeability of the core material on the inductance of the choke.

The traditional route to the design of a choke with a gapped core involves the use of Hanna curves, or some derivative of them. This design route has a number of disadvantages and limitations. Initial core selection is uncertain and designs may have to be made using a number of cores before the optimal solution is found. The design procedure involves considerable calculation and iteration, and the effects of changes in core operating conditions and mechanical tolerances, especially on the airgap, are not readily predicted.

To simplify the design of power chokes using Ferroxcube grade 3C8 cores, we have devised a method based on computer-generated charts. The first step in the design is the selection of a suitable core: this selection usually proves to be final. The published data for each core includes a further chart that replaces the Hanna curve and which is used for graphical design of the choke.

DESIGN METHOD

Ferroxcube 3C8 manganese-zinc ferrite is established as an excellent material for power transformer and choke cores operating at ultrasonic frequencies, especially those in switched-mode power supplies (SMPS). The new core selection and design charts greatly simplify the design of such chokes.

Starting with the peak current I_M that the choke is required to pass without saturating the core, and the minimum inductance required L_{MIN}, the designer obtains directly all the information necessary for the construction of the choke. Core size, spacer thickness, number of turns, and winding geometry are derived by straightforward procedures. Of special interest to those engineers to whom the subject is a black art: the magnetic properties of the core do not enter into the process at all.

The design method allows for ratios of alternating to direct current from small (smoothing chokes) to large (push-pull converter chokes). Parameter spreads due to manufacturing and temperature variations are taken into account in the construction of the design charts. The design procedures allow for spacer tolerances.

DEFINITION OF SYMBOLS

SYMBOL	UNIT	DEFINITION
A_L	H	Induction factor L/N^2
b_W	mm	Winding (layer) breadth
B_M	T	Peak flux density
d	mm	Nominal wire diameter
d_O	mm	Overall wire diameter
f	kHz	Frequency
f_e	kHz	Effective frequency (see text)
F_R	-	AC resistance factor R_{ac}/R_{dc}
h	mm	Thickness of foil conductor
H	mm	Winding height
H_A	mm	Available winding height
i	mm	Thickness of interleaving
I_e	A	RMS current at full load
I_O	A	DC component of current at full load
I_{AC}	A	AC component of current at full load
I_M	A	Peak value of current at full load
L	H	Inductance
N	–	Number of turns in a winding
p	–	Number of layers
P_W	W	Winding loss
R_{AC}	Ω	AC resistance
R_{DC}	Ω	DC resistance
s	mm	Spacer thickness

NOTE:
Subscript ID means "ideal" value.

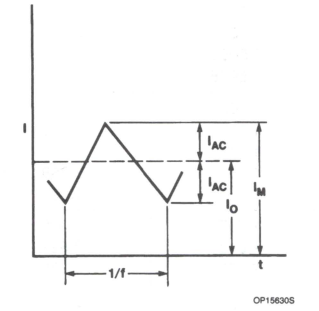

Figure 1. Symbols for Choke Current Used in the Text (See also the Table)

Core Operating Conditions

The selection and design charts are constructed for cores of Ferroxcube 3C8 operating at a hotspot temperature of 100°C. Operation at lower temperatures leads neither to core saturation nor to inductances lower than L_{MIN}. The design peak flux-density B_M is 0.32 T; however, the charts can be used for a lower value by designing for a peak current $0.32 I_M/B_M$. (Symbols used in this article are listed and defined in the table; symbols for currents are illustrated by Figure 1. Note that in the equations the unit of frequency is kHz, *not* Hz; and the unit of length, mm. Some constants in the equations are based on these units.)

APPLICATIONS

For the purposes of the new design method, applications are divided into three classes:

I $I_{AC}/I_O < 0.3$ as in smoothing chokes, and converter chokes for flyback-type SMPS, where the core flux-density remains above zero.

II $I_{AC}/I_O \approx 1$ as in chokes where the operating flux-density returns periodically to zero. This is the case with flyback converters of the ringing-choke type.

III $I_{AC}/I_O > 2$ as in converter chokes for push-pull-type SMPS, and fluorescent-lighting ballast chokes, where excitation is symmetrical.

In class III applications, the limiting factor in a design is core loss rather than core saturation. Operation at a permissible level of core loss usually entails reducing the peak flux density in the core; the amount of the reduction depends on operating frequency. The treatment given to class III designs here generally yields satisfactory results.

CORE SELECTION

The design charts are supplemented by three core selection charts. Each chart covers a group of core types according to shape:

- UU and UI cores (Figure 2), comprising respectively two U cores of a U and an I core, generally give designs with the lowest ferrite cost. However, they are not available complete with coil formers.
- EE cores, a pair of E cores, may be preferable where other considerations dominate, such as the availability of coil formers.
- EC cores, although designed primarily for transformers, might perhaps be chosen because their use for both transformers and chokes in the same equipment simplifies parts stocking.

Figure 2 shows the core selection chart for UU and UI cores, examples of which are shown in Figure 3.

Selection Procedure

The selection curves are used to select a suitable core for the intended application. A full design can then be made using the design chart in the core data sheet with confidence that the result will be useful. The selection charts are used as follows:

- Knowing the value of peak choke current I_M and the minimum inductance required L_{MIN}, calculate the value of $I_M^2L_{MIN}$.
- Choose, at least provisionally, the shape of core (UU/UI, EE, or EC) based on the considerations in the previous paragraph. Draw on the appropriate selection chart a horizontal line $I_M^2L_{MIN}$. For class III designs use a value of $0.1fI_M^2L_{MIN}$, where f is the operating frequency in kHz.
- A core whose curve intersects this horizontal line can be used for the application. The spacer thickness corresponding to the intersection is, however, only an indication of the final value.

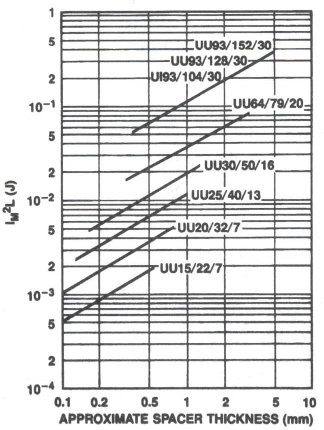

Figure 2. Selection Chart for U Cores

Figure 3. A Selection of Cores in Ferroxcube Grade 3C8 Ferrite

Effect of Core Size

Where, as is usual, more than one core could be used, the final choice may be governed by the consideration that operation near the right-hand end of the curves carries the risk of overheating. Moreover, selection of a larger core will generally result in a more conservative, efficient design than one based on a core that is only marginally large enough.

SPACER THICKNESS AND NUMBER OF TURNS

In the data sheet for the type of core selected, refer to the chart giving $(I_M^2L)_{MAX}$ and A_L as functions of spacer thickness. (Note: A_L for these power cores is the induction factor in Henrys.)

The charts contain a pair of curves of $(I_M^2L)_{MAX}$ and A_L for each of the three application classes. The design chart for the UU64/79/20 is given as Figure 4. In the design procedure, use the pair of curves of the appropriate class of application, as follows:

1. On the chart, draw again the horizontal line $I_M^2L_{MIN}$ (or $0.1fI_M^2L_{MIN}$ for class III applications) as in the selection procedure. The working point of the core must lie above this line and below the $(I_M^2L)_{MAX}$ curve for the core. In Figure 5, that is between lines SQ and SP.
2. Select a suitable spacer, of nominal thickness s. Draw vertical lines s_{MIN} and s_{MAX} on the chart, where $s_{MAX} - s_{MIN}$ is the tolerance field on the thickness of the spacer and the associated adhesive films. (Epoxy adhesive films vary in thickness from about 10μm to about 20μm.) Ensure that the horizontal distance between the intersection and s_{MIN} (a in Figure 5) is greater than the distance from s_{MIN} to s_{MAX} (b in Figure 5).
3. For s_{MIN}, read values of $(I_M^2L)_{MAX1}$ and A_{L1} from the chart. To avoid saturation the maximum number of turns allowed is

$$N_{MAX} = \sqrt{\frac{(I_M^2L)_{MAX1}}{I_M^2A_{L1}}} \tag{1}$$

NOTE:
The upper left-hand corner of the shaded area in Figure 5 is the most critical point regarding number of turns and core saturation.

4. For s_{MAX}, read the value of A_{L2}. The minimum number of turns required to achieve L_{MIN} is then

$$N_{MIN} = \sqrt{\frac{L_{MIN}}{A_{L2}}} \tag{2}$$

   NOTE:
   The lower right-hand corner of the shaded area is the most critical for number of turns and L_{MIN}.

5. Select an integral number of turns N between N_{MIN} and N_{MAX}.

   NOTE:
   If 'a' was taken to be only marginally greater than 'b' (Figure 5), the design attempt might fail since such an integer would not exist. Making a < b makes $N_{MAX} < N_{MIN}$.

6. Establish the winding geometry using the winding design procedure in the next section.

WINDING DESIGN

The losses due to eddy currents in a winding carrying AC increase rapidly with conductor size (as d^4 for wire), but resistive losses in a conductor decrease with increasing size (as d^{-2} for wire). It follows, therefore, that there must be a frequency-dependent 'ideal' conductor size at which losses are minimum. This sets the upper limit to conductor size; there is no reason to increase losses by using a thicker conductor. The use of a thinner conductor is sometimes tolerable (low current density) or necessary (inadequate space).

The procedures that follow allow the ideal number of layers and wire size, or the thickness of strip, to be determined for chokes with an operating current waveform similar to that shown in Figure 1. They also indicate the course of action in the event of the available

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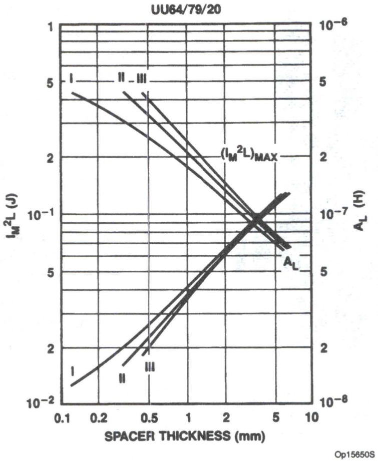

Figure 4. Design Chart for the UU64/79/20

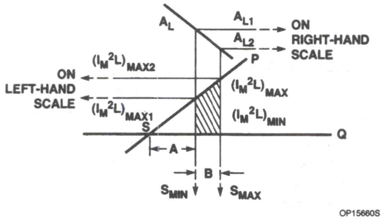

Figure 5. Construction for Graphical Design of Chokes Using the New Design Charts

winding window being insufficient to accommodate the ideal winding.

Copper conductors are assumed here and the operating temperature is taken to be 100°C, so that conductor resistivity is 1/45Ωmm^2/m (30% higher than that at 20°C). Symbols used are defined in the Table and Figure 1.

Effective Frequency and Effective Current

To allow for the effect of waveform on eddy-current losses in the choke windings, it is necessary to convert actual frequencies and currents to effective values. For sinusoidal currents, the effective frequency f_e is equal to the actual frequency f. For small amounts of waveform distortion, and small DC components, f_e can still be taken as equal to f. For the waveform of Figure 1, and provided that the rise and fall times are between 15% and 85% of the repetition period,

$$f_e = \frac{1.3f}{\sqrt{1 + 3(I_0/I_{AC})^2}}$$

In designs for class I applications f_e may be only a few kiloHertz. Eddy-current effects are then negligible so that windings can be designed as if they are to carry DC only. Remember to use the correct value for DC resistivity.

For the waveform of Figure 1, the effective current I_e is given by:

$$I_e^2 = I_0^2 + I_{AC}^2/3$$

For sinusoidal currents with a significant DC component, however,

$$f_e = \frac{f}{\sqrt{1 + 2(I_0/I_{AC})^2}}$$

and

$$I_e^2 = I_0^2 + I_{AC}^2/2$$

where I_{AC} is the amplitude of the AC component.

Multi-Layer Wire Windings of Solid, Round Wire

In the following design procedure, it is assumed that all layers have the same breadth. However, where the number of turns in the winding cannot be divided into the ideal number of layers, a difference of one turn per layer is permissible.

1. The ideal wire diameter is

$$d_{ID} = 2.6\left(\frac{b_W}{Nf_e}\right)^{1/3}$$

2. Select the nearest standard wire size (for d and d_O) from a wire table such as that for IEC grade 1 winding wires.
3. The ideal number of layers is now

$$p_{ID} = \frac{N}{b_W/d_O - 1}$$

NOTE:
This expression is valid only for d_O from Step 2.

- If $p_{ID} \geqslant 1.5$ and the current density in wire d_{ID} is excessive, make a new design using a larger core.
- If $p_{ID} \leqslant 1.5$, also consider a foil or strip winding.
- If $p_{ID} \leqslant 1$, the expression for d_{ID} in step 1 is not valid: go to the single-layer winding procedure.

Find p by rerounding p_{ID} to the next highest integer. This rounding increases the spacing between turns.

4. The required winding height is
$H = p(d_o + i)$
5. If H exceeds the available height H_a, or if current density is low:
   - reduce p by one layer
   - select the thickest wire for which $d_O \leqslant pb_W/(N + p)$,
   - repeat from step 4, even if p = 1.
6. $F_R = 1 + \frac{1}{2}(d/d_{ID})^6$.
Check: if $F_R > 2$ an error has occurred.

NOTE:
$F_R = 1.5$ for $d = d_{ID}$; when $d < 0.7\ d_{ID}$, $F_R \approx 1$.

7. $P_W = I_e^2R_{AC} = I_e^2F_RR_{DC}$.*

NOTE:
*The DC resistance of copper wire is $0.0283/d^2$ Ω/m at 100°C.

Single-Layer Windings of Solid, Round Wire

The design procedure is to be used only when p_{ID} calculated in step 3 of the previous section comes out as equal to or less than unity.

1. Select the thickest wire for which $d_O \leqslant b_W/(N + 1)$.

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2. $F_R = 0.33\, d\, f_e \tfrac{1}{2} N/(N + 1)$, only if $p_{ID} \leqslant 1$ in step 3 of the last section. F_R has no upper limit here.
3. $P_W = I_e^2 R_{AC} = I_e^2 F_R R_{DC}$.*

NOTE:
*The DC resistance of copper wire is $0.0283/d^2$ Ω/m at 100°C.

Bunched-(Litz-) Wire Windings

Eddy-current effects in bunched-conductor (or Litz-wire) windings are negligible and, thus, no special design procedure is required. Conductors of this type are not, however, necessarily the complete solution: their packing factor, and, consequently, winding thermal conductivity are both low. They might be an attractive alternative where the ideal solid-conductor winding fills less than half the available height. The resistance of bunched conductors, like that of solid conductors, is 30% higher at 100°C than at 20°C.

Foil or Strip Windings

Chokes for high current, low voltage SMPS often use windings of strip or foil conductor. The width b_W of the strip is equal to the available winding width.

1. $h_{ID} = \dfrac{3.1}{\sqrt{(Nf_e)}}$
2. $h_{MIN} = 0.8\, \dfrac{h_{ID}}{\sqrt{N}}$
3. $h_{MAX} = \dfrac{H_a}{N} - i$

   Choose a value for i that suits a strip of thickness about H_a/N. If h_{MAX} h_{MIN}, try a wire winding.
4. Select a strip of thickness h such that $h_{MIN} \leqslant h < h_{MAX}$. Aim for $h = h_{ID}$.
5. $F_R = 1 + \dfrac{1}{3}\left(\dfrac{h}{h_{ID}}\right)^4$

   Check that $F_R < 1.8$; if not, reduce h. When $h = h_{ID}$, $F_R = 1.33$; when $h < 0.6\, h_{ID}$, $F_R \simeq 1$.
6. $P_W = I_e^2 R_{AC} = I_e^2 F_R R_{DC}$.

NOTE:
DC resistance of copper strip is $1/(45 b_w h)$Ω/m at 100°C.

DESIGN EXAMPLE

A choke of 30mH minimum inductance is required for a peak current of 1A at 30kHz with a waveform as shown in Figure 1. $I_{AC}/I_0 = 0.1$, so this is a class I design.

Core Selection

Cost is important and quantities justify customized coil formers, so a UU core is selected.

The value of $I_M^2 L_{MIN} = 3 \times 10^{-2}$J. A horizontal line of this value drawn on the UU core selection chart intersects the curve for the UU 64/79/20 core at a spacer thickness of about 0.7mm.

Number of Turns and Spacer Thickness

Another horizontal line for $I_M{}^2 L_{MIN} = 3 \times 10^{-2}$ J drawn on the design chart for the UU64/79/20 core, Figure 4, intersects the $(I_M^2 L)_{MAX}$ curve for class I at a spacer thickness of 0.6mm. A resin-bonded paper sheet of 0.9mm thickness with a tolerance of −0.1mm is available. Adhesive thickness is between 0.01mm and 0.02mm, so the final spacer thickness could be 0.81 to 0.92mm. Vertical lines of these values are drawn on the design chart. The condition given with reference to Figure 5, that a > b, is satisfied.

From Figure 4, $(I_M^2 L)_{MAX1} = 0.036$J and $A_{L1} = 2 \times 10^{-7}$H.

Thus, from Equation 1,

$$N_{MAX} = \sqrt{\frac{0.036}{1 \times 2 \times 10^{-7}}} = 424.26 \text{ turns}$$

$A_{L2} = 1.9 \times 10^{-7}$H, so the minimum number of turns is, from Equation 2,

$$N_{MIN} = \sqrt{\frac{0.03}{1.9 \times 10^{-7}}} = 397.36$$

Since N_{MAX} is, as it should be, greater than N_{MIN}, the design is successful so far and a number of turns can be selected between these limits.

Winding Design

The effective operating frequency for the core is given by Equation 3,

$$f_e = \frac{1.3 \times 30}{\sqrt{1 + 3\ (0.1^{-2})}} \simeq 2.25\text{kHz}$$

At this effective frequency, eddy-current effects can be neglected, and the winding can be designed to fit the space available, allowing for the coil former wall thicknesses.

Signetics

SG3524
SMPS Control Circuit

Product Specification

Linear Products

DESCRIPTION

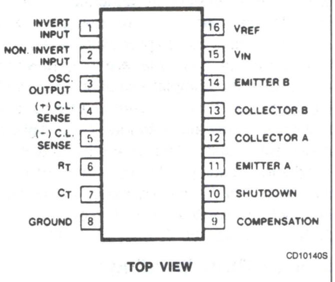
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

D[1], F, N Packages

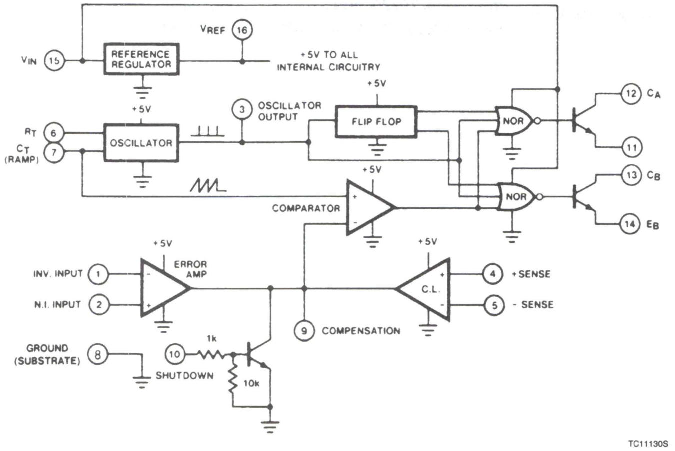

INVERT INPUT 1
NON. INVERT INPUT 2
OSC. OUTPUT 3
(+) C.L. SENSE 4
(−) C.L. SENSE 5
RT 6
CT 7
GROUND 8
16 VREF
15 VIN
14 EMITTER B
13 COLLECTOR B
12 COLLECTOR A
11 EMITTER A
10 SHUTDOWN
9 COMPENSATION
CD10140S
TOP VIEW

NOTE:
1. SOL-Released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	SG3524N
16-Pin Cerdip	0 to +70°C	SG3524F
16-Pin SOL	0 to +70°C	SG3524D

BLOCK DIAGRAM


VREF 16
VIN 15
REFERENCE REGULATOR
+5V TO ALL INTERNAL CIRCUITRY
+5V
3 OSCILLATOR OUTPUT
FLIP FLOP
RT 6
CT (RAMP) 7
OSCILLATOR
NOR
NOR
12 CA
11
13 CB
14 EB
COMPARATOR
+5V
INV. INPUT 1
N.I. INPUT 2
ERROR AMP
C.L.
4 +SENSE
5 - SENSE
9 COMPENSATION
GROUND (SUBSTRATE) 8
10 SHUTDOWN
1k
10k
TC11130S

SMPS Control Circuit SG3524

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Input voltage	40	V
I_{OUT}	Output current (each output)	100	mA
I_{REF}	Reference output current	50	mA
	Oscillator charging current	5	mA
P_D	Power dissipation Package limitation Derate above 25°C	 1000 8	 mW mW/°C
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{IN} = 20V$, and $f = 20kHz$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage		4.6	5.0	5.4	V
	Line regulation	$V_{IN} = 8$ to 40V		10	30	mV
	Load regulation	$I_L = 0$ to 20mA		20	50	mV
	Ripple rejection	$f = 120Hz$, $T_A = 25°C$		66		dB
I_{SC}	Short circuit current limit	$V_{REF} = 0$, $T_A = 25°C$		100		mA
	Temperature stability	Over operating temperature range		0.3	1	%
	Long-term stability	$T_A = 25°C$		20		mV/kHz
Oscillator section						
f_{MAX}	Maximum frequency	$C_T = 0.001$ mF, $R_T = 2k\Omega$		300		kHz
	Initial accuracy	R_T and C_T constant		5		%
	Voltage stability	$V_{IN} = 8$ to 40V, $T_A = 25°C$			1	%
	Temperature stability	Over operating temperature range			2	%
	Output amplitude	Pin 3, $T_A = 25°C$		3.5		V_P
	Output pulse width	$C_T = 0.01$ mF, $T_A = 25°C$		0.5		μs
Error amplifier section						
V_{OS}	Input offset voltage	$V_{CM} = 2.5V$		2	10	mV
I_{BIAS}	Input bias current	$V_{CM} = 2.5V$		2	10	μA
	Open-loop voltage gain		68	80		dB
V_{CM}	Common-mode voltage	$T_A = 25°C$	1.8		3.4	V
CMRR	Common-mode rejection ratio	$T_A = 25°C$		70		dB
BW	Small-signal bandwidth	$A_V = 0dB$, $T_A = 25°C$		3		MHz
V_{OUT}	Output voltage	$T_A = 25°C$	0.5		3.8	V
Comparator section						
	Duty cycle	% each output "ON"	0		45	%
	Input threshold	Zero duty cycle		1		V
	Input threshold	Maximum duty cycle		3.5		V
I_{BIAS}	Input bias current			1		μA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 0°C$ to $+70°C$, $V_{IN} = 20V$, and $f = 20kHz$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Current limiting section						
	Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25°C$	180	200	220	mV
	Sense voltage T.C.			0.2		mV/°C
V_{CM}	Common-mode voltage		−1		+1	V
Output section (each output)						
	Collector-emitter voltage (breakdown)		40			V
	Collector-leakage current	$V_{CE} = 40V$		0.1	50	μA
	Saturation voltage	$I_C = 50mA$		1	2	V
	Emitter output voltage	$V_{IN} = 20V$	17	18		V
t_R	Rise time	$R_C = 2k\Omega$, $T_A = 25°C$		0.2		μs
t_F	Fall time	$R_C = 2k\Omega$, $T_A = 25°C$		0.1		μs
Total standby current						
	(excluding oscillator charging current, error and current limit dividers, and with outputs open)	$V_{IN} = 40V$		8	10	mA

THEORY OF OPERATION

Voltage Reference

An internal series regulator provides a nominal 5V output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5V supply by connecting Pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0V.

This reference regulator may be used as a 5V source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

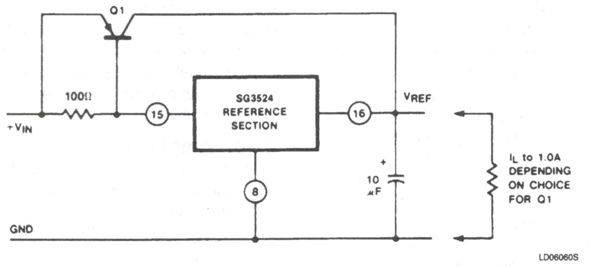
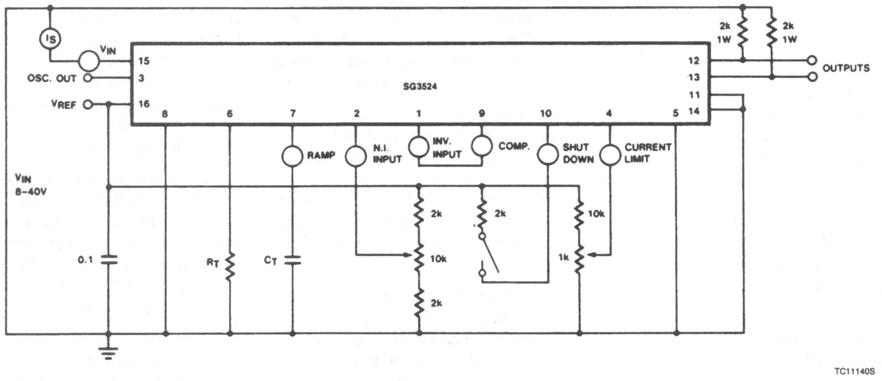

Q1
100Ω
+VIN
15
SG3524 REFERENCE SECTION
16
VREF
+
10 µF
8
IL to 1.0A DEPENDING ON CHOICE FOR Q1
GND
LD06060S

Figure 1. Expanded Reference Current Capability

TEST CIRCUIT


IS
VIN
OSC. OUT
VREF
15
3
16
SG3524
8
6
7
2
1
9
10
4
5
12
13
11
14
2k 1W
2k 1W
OUTPUTS
RAMP
N.I. INPUT
INV. INPUT
COMP.
SHUT DOWN
CURRENT LIMIT
VIN 8-40V
0.1
RT
CT
2k
10k
2k
2k
10k
1k
TC11140S

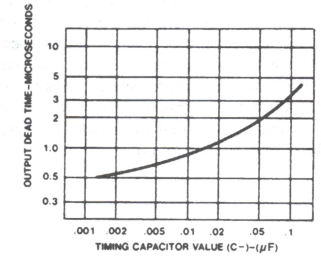


Figure 2. Output Stage Dead Time as a Function of the Timing Capacitor Value

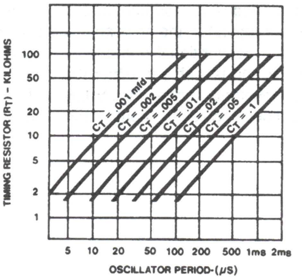


Figure 3. Oscillator Period as a Function of R_T and C_T

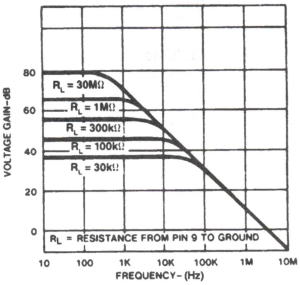


Figure 4. Amplifiers Open-Loop Gain as a Function of Frequency and Loading on Pin 9

Oscillator

The oscillator in the SG3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series-connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V \div R_T$ and should be kept within the approximate range of 30µA to 2mA; i.e., $1.8k < R_T < 100k$.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse-width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5μs may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse-width may still be expanded by adding a shunt capacitance (≈100pF) to ground at the oscillator output. [(Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse-width slightly.)] Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between 0.001 and 0.1 μF.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when $R_T = \Omega$ and $C_T = \mu F$. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0 – 90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 – 45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG3524 to an external clock, a pulse of ≈ + 3V may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse-width apply. The impedance to ground at this point is approximately 2kΩ.

If two or more SG3524s must be synchronized together, one must be designated as master with its $R_T C_T$ set for the correct period. The slaves should each have an $R_T C_T$ set for approximately 10% longer period than the master with the added requirement that C_T(slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse — which occurs first and has a wider pulse width — will reset the slave units.

Error Amplifier

This circuit is a simple differential input transconductance amplifier. The output is the compensation terminal, Pin 9, which is a high-impedance node ($R_L \approx 5M\Omega$). The gain is

$$A_V = g_M R_L = \frac{8\, I_C R_L}{2kT} \cong 0.002\, R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from Pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain crossover at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series RC combination between Pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus 0.001μF.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5V reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open-loop test circuit.

Current Limiting

The current limiting circuitry of the SG3524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R_1:

$$\text{Threshold} = V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2)$$

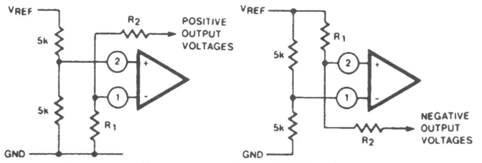
$$= I_1 R_2 \cong 200\text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ± 1V common-mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, Pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and to shorten an output pulse, should transformer saturation occur. Another application is to ground Pin 5 and use Pin 4 as an additional shutdown terminal: i.e., the output will be off with Pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

SMPS Control Circuit SG3524


VREF
5k
R2
POSITIVE OUTPUT VOLTAGES
2
1
+
-
5k
R1
GND
VREF
R1
5k
2
1
+
-
NEGATIVE OUTPUT VOLTAGES
5k
R2
GND

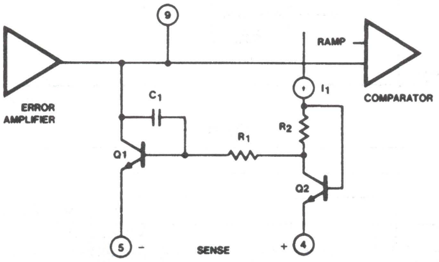
$$V_O = \frac{2.5V (R + R_2)}{R_1}$$

$$\frac{R_1 R_2}{R_2 + R_2} \quad 2.5k\Omega$$

LD06070S

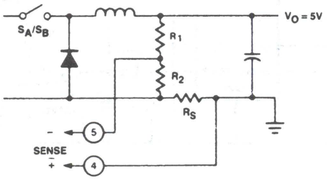
NOTE:
Note change in input connections for opposite polarity outputs.

Figure 5. Error Amplifier Biasing Circuits


9
RAMP
ERROR AMPLIFIER
C1
I1
COMPARATOR
R2
R1
Q1
Q2
5
-
SENSE
+
4

LD06080S

Figure 6. Current Limiting Circuitry of the SG3524


VO = 5V
SA/SB
R1
R2
RS
-
5
SENSE
+
4

$$I_{MAX} = \frac{1}{R_S} \quad V_{TH} + \frac{V_0 R_2}{R_1 + R_2}$$

$$I_{SC} = \frac{V_{TH}}{R_S} \quad \text{WHERE}$$

$$\overline{V_{TH} = 200 \text{ mV}}$$

TC11150S

NOTE:
Foldback current limiting can be used to reduce power dissipation under shorted output conditions.

Figure 7. Foldback Current Limiting

Signetics

AN126
Applications Using the SG3524

Application Note

Linear Products

APPLICATIONS

The capacitor-diode output circuit is used in Figure 1 as a polarity converter to generate a −5V supply from +15V. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current-limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

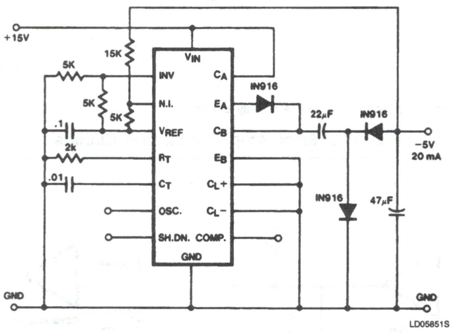
Another low current supply is the flyback converter used in Figure 2 to generate ±15V at 20mA from a +5V regulated line. The reference generator in the SG3524 is unused with the input voltage providing the reference. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft start circuit.

In the conventional single-ended regulator circuit shown in Figure 3, the two outputs of the SG3524 are connected in parallel for effective 0.0 – 90% duty cycle modulation. The use of an output inductor requires an RC phase compensation network for loop stability.

Push-pull outputs are used in this transformer-coupled DC – DC regulating converter shown in Figure 4. Note that the oscillator must be set at twice the desired output frequency, as the SG3524's internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

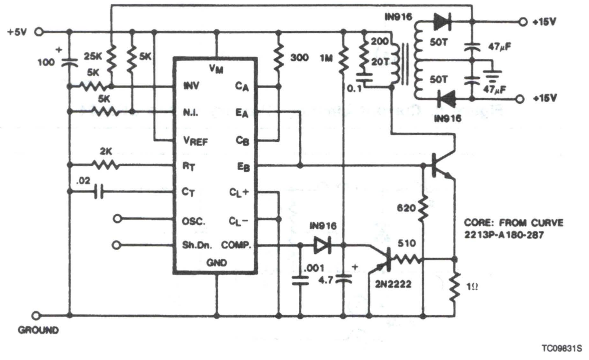
SG3524 PUSH-PULL ±50V, 100W Converter (Off-Line)

A simple solution to off-line converter design for power audio amplifier circuits is shown in Figure 5. The SG3524 emitter outputs are used to drive directly a pair of BUZ41A Power FETs in the primary side of the step-down transformer at a 50kHz rate. (The main oscillator operates at 100kHz.) The transformer consists of 120T of #24 wire centertapped at 60T. This is sandwiched between two 50-turn center-tapped secondary windings of #20 wire. Diodes are fast recovery BYW30s; the output chokes, 500μH wound on EC35 (3C8) pair Ferroxcube cores, provide adequate filtering in conjunction with the 1000μF and 0.01μF ceramic capacitors across the output.



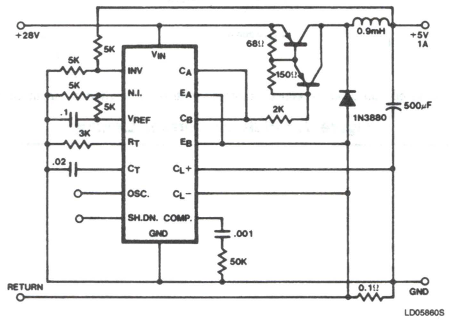
+15V
15K
5K
5K
5K
.1
2k
.01
VIN
INV
N.I.
VREF
RT
CT
OSC.
SH.DN.
CA
EA
CB
EB
CL+
CL−
COMP.
GND
IN916
22μF
IN916
IN916
47μF
−5V
20 mA
GND
GND
LD05851S

Figure 1



+5V
100
25K
5K
5K
5K
2K
.02
VM
INV
N.I.
VREF
RT
CT
OSC.
Sh.Dn.
CA
EA
CB
EB
CL+
CL−
COMP.
GND
300
1M
200
20T
0.1
IN916
50T
47μF
50T
47μF
IN916
+15V
+15V
620
IN916
510
.001
4.7
2N2222
1Ω
CORE: FROM CURVE
2213P-A180-287
GROUND
TC09631S

Figure 2



+28V
5K
5K
5K
5K
.1
3K
.02
VIN
INV
N.I.
VREF
RT
CT
OSC.
SH.DN.
CA
EA
CB
EB
CL+
CL−
COMP.
GND
68Ω
150Ω
2K
1N3880
0.9mH
+5V
1A
500μF
.001
50K
RETURN
0.1Ω
GND
LD05860S

Figure 3

Applications Using the SG3524 AN126

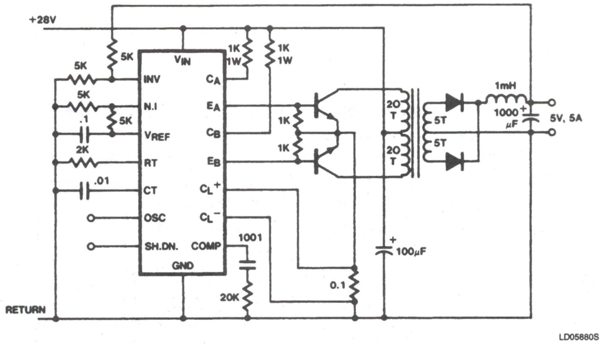

+28V
5K
5K
5K
.1
5K
2K
.01
VIN
INV
N.I
VREF
RT
CT
OSC
SH.DN.
COMP
GND
CA
EA
CB
EB
CL+
CL−
1K 1W
1K 1W
1K
1K
20 T
20 T
5T
5T
1mH
1000 μF
5V, 5A
1001
20K
0.1
+ 100μF
RETURN
LD05880S

Figure 4

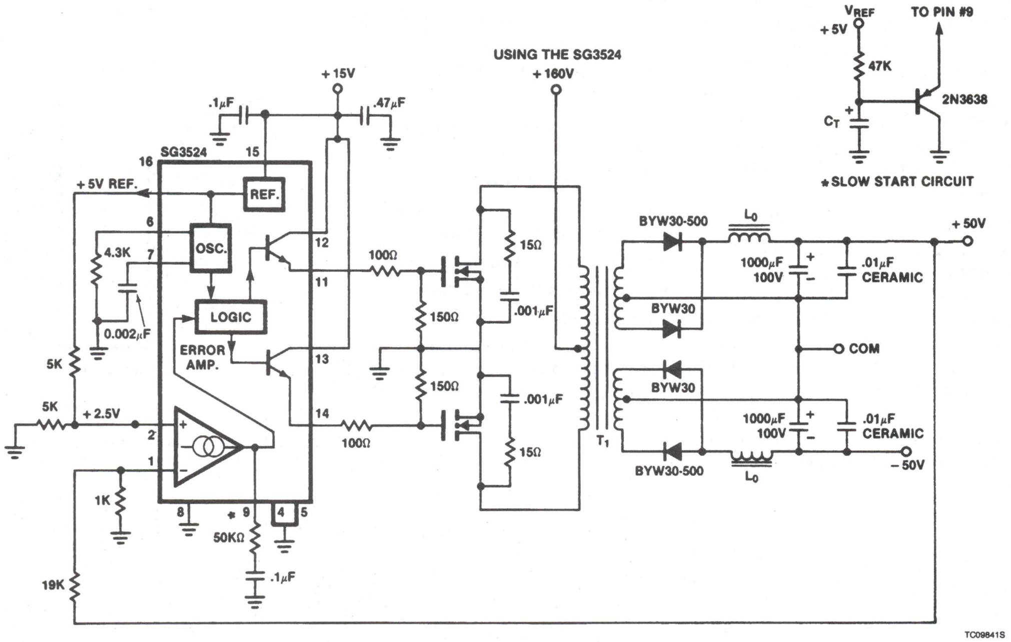

USING THE SG3524
+160V
+15V
.1μF
.47μF
SG3524
16
15
REF.
+5V REF.
6
OSC.
4.3K
7
0.002μF
LOGIC
ERROR AMP.
12
11
13
14
100Ω
100Ω
150Ω
150Ω
15Ω
15Ω
.001μF
.001μF
T1
5K
5K
+2.5V
2
1
1K
8
* 9
4
5
50KΩ
.1μF
19K
BYW30-500
BYW30
BYW30
BYW30-500
L0
L0
1000μF 100V
1000μF 100V
.01μF CERAMIC
.01μF CERAMIC
+50V
COM
−50V
VREF
+5V
47K
CT
TO PIN #9
2N3638
*SLOW START CIRCUIT
TC09841S

Figure 5. ±50V Push-Pull Switched-Mode Converter

Signetics

Linear Products

SG3526
Switched-Mode Power Supply Control Circuit

Preliminary Specification

DESCRIPTION

Specifically designed for use in fixed-frequency switching regulators and other power control applications, this Switched-Mode Power Supply Control Circuit can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer-coupled.

Included in this monolithic integrated circuit is a temperature-compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two 200mA source/sink power drivers. Also included are housekeeping functions such as soft-start and low supply voltage lockout, digital current limiting, double-pulse inhibit, a data latch for single-pulse metering, adjustable dead time, and provision for symmetry correction inputs.

The output circtuit has been redesigned to eliminate the current spiking problem associated with source/sink drivers. The output stage has been designed so that in the transition from source-to-sink, or sink-to-source, the conducting device is shut off one transistor delay before the other device is turned on. This output correction allows the designer to utilize the speed of the other features of this controller at system frequencies up to 400kHz.

For ease of interface, all digital inputs are TTL and CMOS compatible. Active LOW logic allows wired-OR connections for maximum flexibility.

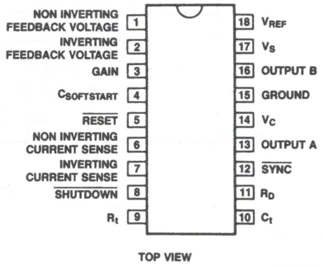
The low-cost SG3526 is rated for continuous operation over the junction temperature range of 0°C to +125°C. It is furnished in either the Cerdip package or a dual in-line plastic package with copper alloy lead frame for improved heat dissipation.

FEATURES

- **7.4 to 35V operation**
- **Dual 200mA source/sink outputs**
- **Cycle-by-cycle operation of all features up to 400kHz**
- **No current spikes on V_C line at source-to-sink or sink-to-source transitions**
- **Stabilized power supply**
- **Current limiting**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Low supply voltage protection**
- **External synchronization**
- **Double-pulse suppression**
- **Programmable dead time**
- **Programmable soft start**
- **18-pin dual in-line plastic package, 18-pin Cerdip hermetic package, or 20-pin plastic SO**

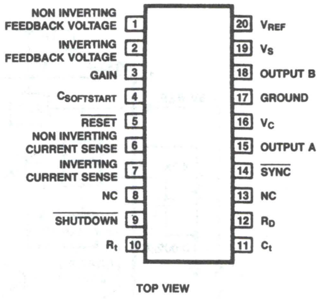
PIN CONFIGURATIONS

F, N Packages


NON INVERTING FEEDBACK VOLTAGE 1
INVERTING FEEDBACK VOLTAGE 2
GAIN 3
$C_{SOFTSTART}$ 4
$\overline{RESET}$ 5
NON INVERTING CURRENT SENSE 6
INVERTING CURRENT SENSE 7
$\overline{SHUTDOWN}$ 8
R_t 9
10 C_t
11 R_D
12 $\overline{SYNC}$
13 OUTPUT A
14 V_C
15 GROUND
16 OUTPUT B
17 V_S
18 V_{REF}
TOP VIEW

CD09600S

D Package[1]


NON INVERTING FEEDBACK VOLTAGE 1
INVERTING FEEDBACK VOLTAGE 2
GAIN 3
$C_{SOFTSTART}$ 4
$\overline{RESET}$ 5
NON INVERTING CURRENT SENSE 6
INVERTING CURRENT SENSE 7
NC 8
$\overline{SHUTDOWN}$ 9
R_t 10
11 C_t
12 R_D
13 NC
14 $\overline{SYNC}$
15 OUTPUT A
16 V_C
17 GROUND
18 OUTPUT B
19 V_S
20 V_{REF}
TOP VIEW

CD09590S

NOTE:
1. SOL and non-standard pinout.

ORDERING CODE

DESCRIPTION	AMBIENT TEMPERATURE	ORDER CODE
20-pin Plastic SOL DIP	0 to +70°C	SG3526D
18-pin Cerdip	0 to +70°C	SG3526F
18-pin Plastic DIP	0 to +70°C	SG3526N

Switched-Mode Power Supply Control Circuit SG3526

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	40	V
V_C	Collector supply voltage	40	V
V_{IN}	Logic input voltage range, Pins 5, 8, 12	−0.3 to +5.5	V
V_{IN}	Analog input voltage range, Pins 1, 2, 6, 7	−0.3V to V_S	V
I_O	Output current	±250	mA
I_{REF}	Reference load current	50	mA
I_{IN}	Logic sink current	15	mA
P_D	Package power dissipation (Plastic DIP)^2 (SO), (Cerdip)^2	1.9 1.4	W^1 W^1
T_S	Storage temperature range	−65 to +150	°C

NOTES:

1. Maximum junction temperature, $T_{JMAX} = 150°C$. Rating is for $T_A = 25°C$.
2. Plastic $\theta_{JA} = 66°C/W$; Cerdip $\theta_{JA} = 88°C/W$; SO $\theta_{JA} = 85°C/W$.

BLOCK DIAGRAM

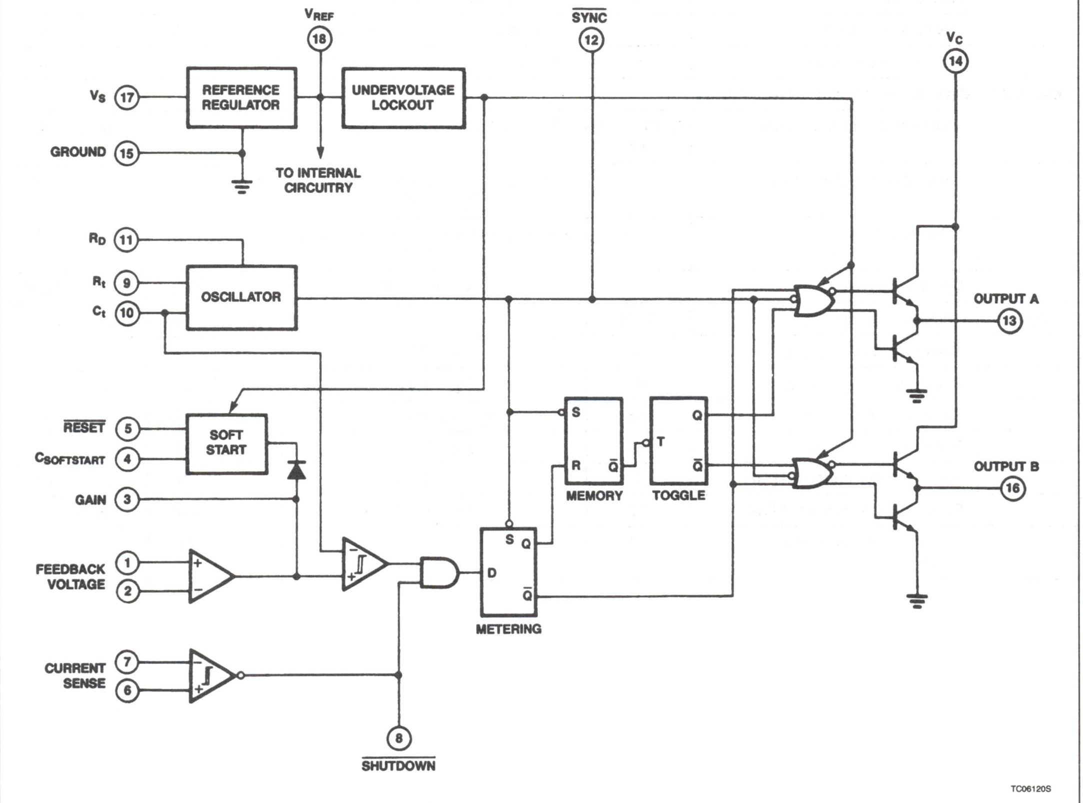

VREF
18
SYNC
12
VC
14
VS
17
REFERENCE REGULATOR
UNDERVOLTAGE LOCKOUT
GROUND
15
TO INTERNAL CIRCUITRY
RD
11
Rt
9
Ct
10
OSCILLATOR
OUTPUT A
13
RESET
5
CSOFTSTART
4
SOFT START
GAIN
3
S
Q
R
Q̄
MEMORY
T
Q
Q̄
TOGGLE
OUTPUT B
16
FEEDBACK VOLTAGE
1
2
S
Q
D
Q̄
METERING
CURRENT SENSE
7
6
8
SHUTDOWN
TC06120S

Figure 1

DC ELECTRICAL CHARACTERISTICS All specs over operating junction temperature range, $V_S = 15V$, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Reference, Pin 18							
V_{REF}	Reference voltage	18	$T_J = +25°C$		5.00		V
	Temperature stability	18			0.2	0.4	mV/°C
	Total output variation	18	$7.4V < V_S < 35V$, $0 < I_L < 10mA$	4.85	5.00	5.15	V
	Line regulation	18	$7.4V < V_S < 35V$, $I_L = 0mA$		0.6	2	mV/V
	Load regulation	18	$0mA < I_L < 10mA$		0.4	2.5	mV/mA
	Maximum output current	18		−25	−50	−100	mA
	Output noise voltage	18	$10Hz \leqslant f \leqslant 80kHz$		100		μV_{RMS}
Low supply shutdown, Internal and Pin 5							
	Comparator threshold voltage			3.8	4.2	4.8	V
	Hysteresis				0.2		V
	Reset voltage out	5	When shutdown for LOW V_S		0.2	0.4	V
	Reset voltage out	5	When not shutdown	2.4	4.8		V
	Reset sink current	5	When shutdown, $V_{IL} = 0.4V$		−190	−360	μA
	Reset source current	5	When not shutdown, $V_{IH} = 2.4V$		−110	−200	μA
Oscillator, Pins 9, 10, 11 and SYNC, Pin 12[1]							
	Minimum frequency range	9, 10, 11 & 12	$R_T = 150k$, $C_T = 20\mu F$, $R_D = 0\Omega$			1.0	Hz
	Maximum frequency range		$R_T = 2k$, $C_T = 300pF$, $R_D = 0\Omega$, $T_J = 125°C$	400			kHz
	Initial accuracy	9, 10	$R_T = 4.12k$, $C_T = 0.01\mu F$, $R_D = 0\Omega$, $T_J = 25°C$	36	38	40	kHz
V_{COSC}	Voltage stability	9, 10	$7.4V < V_S < 35V$		0.02	0.04	%/V
T_{COSC}	Temperature stability	9, 10			0.04	0.06	%/°C
	Sawtooth peak voltage	10	$V_S = 35V$	2.0	3.0	3.5	V
	Sawtooth valley voltage	10	$V_S = 7.4V$	0.5	1.0	1.5	V
	Sync. in HIGH level	12	$I_{SOURCE} = 40\mu A$	2.4	4.0		V
	Sync. in LOW level	12	$I_{SINK} = 3.6mA$		0.2	0.4	V
	Sync. in bias current, HIGH	12	$V_{IH} = 2.4V$		−105	−200	μA
	Sync. in bias current, LOW	12	$V_{IL} = 0.4V$		−180	−360	μA
	Min sync. in pulse width to trigger	12		200	150		ns

Switched-Mode Power Supply Control Circuit SG3526

DC ELECTRICAL CHARACTERISTICS (Continued) All specs over operating junction temperature range, $V_S = 15V$, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Error amp, Pins 1, 2 and 3							
V_{OS}	Input offset voltage	1, 2			2.0	10	mV
I_B	Input bias current	1, 2			210	1000	nA
I_{OS}	Input offset current	1, 2			5	200	nA
A_{VOL}	DC open-loop gain	1, 2, 3		60	68		dB
V_{OH}	High output voltage	3	$I_{SOURCE} = 100\mu A$	3.6	4.2		V
V_{OL}	Low output voltage	3	$I_{SINK} = 100\mu A$		0.11	0.4	V
CMRR	Common-mode rejection ratio	1, 2, 3	$R_S = 2k$	70	110		dB
PSRR	Power supply rejection ratio	1, 2, 3	$V_S = 10V$ to 20 V	90	110		dB
	Small-signal bandwidth	1, 2, 3			1.0		MHz
	Feedback resistor range	2, 3		50		1000	kΩ
	Output sink current	3		70	100		μA
	Output source current	3		70	100		μA
PWM comparator, Internal and Pin 3[1]							
	Minimum duty cycle		$V_{COMP} = 0.4V$			0	%
	Maximum duty cycle		$V_{COMP} = 3.6V$	45	49		%
	Dead time accuracy		$R_T = 4.12k$, $C_T = 0.01\mu F$, $R_D = 0\Omega$		1.5		μs
	Prop. delay, PWM comp to output				250		ns
	Bias current, duty cycle control	3			1		μA
Soft-start, Pins 4 and 5							
	Soft-start trip voltage	4	$V_{RESET} = 0.4V$		22	50	mV
	Soft-start charge current	4	$V_{RESET} = 2.4V$	−180	−120	−85	μA
V_{LOW}	Reset voltage, OFF	5	$I_{SINK} = 3.6mA$		0.2	0.4	V
V_{HIGH}	Reset voltage, ON	5	$I_{SOURCE} = 40\mu A$	2.4	4.0		V
	Reset bias current, HIGH	5	$V_{IN} = 2.4V$		−110	−200	μA
	Reset bias current, LOW	5	$V_{IN} = 0.4V$		−200	−360	μA
Remote ON/OFF (shutdown), Pin 8							
	Off (LOW)	8	$I_{SINK} = 3.6mA$		0.2	0.4	V
	On (HIGH)	8	$I_{SOURCE} = 40\mu A$	2.4	4.0		V
	Input current, shutdown HIGH	8	$V_{IN} = 2.4V$		−100	−200	μA
	Input current, shutdown LOW	8	$V_{IN} = 0.4V$		−190	−360	μA
	Delay to output(s)	8			400		ns
Current limit comparator, Pins 6 and 7							
	Common-mode range	6, 7	$V_S = 18V$	0		15	V
	Sense voltage for Min duty cycle	6, 7		70	100	140	mV
	Input bias current	6, 7	$V_{CM} = 0V$ to 15V		−3	−20	μA
	Voltage gain	6, 7			68		dB
	Delay to outputs	6, 7	100mV overdrive		700		ns

DC ELECTRICAL CHARACTERISTICS (Continued)

All specs over operating junction temperature range, $V_S = 15V$, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Output stage, Pins 13, 14 and 16							
V_{OH}	High output voltage	13, 14, 16	$I_{SOURCE} = 20mA$, $V_C = 15V$	12.8	13.5		V
			$I_{SOURCE} = 100mA$, $V_C = 15V$	12.5	13.3		V
			$I_{SOURCE} = 200mA$, $V_C = 15V$	12.0	13.2		V
V_{OL}	Low output voltage	13, 14, 16	$I_{SINK} = 20mA$, $V_C = 15V$		0.15	0.3	V
			$I_{SINK} = 100mA$, $V_C = 15V$		1.25	1.8	V
			$I_{SINK} = 200mA$, $V_C = 15V$		2.20	3.00	V
	Output leakage	13, 14, 16	$V_C = 40V$		45	100	μA
	I_{SINK} Max	13, 14, 16	$V_C = 15V$	200	250		mA
	I_{SOURCE} Max	13, 14, 16	$V_C = 15V$	200	250		mA
t_R	Rise time	13, 14, 16	$C_L = 1000pF$, $V_C = 15V$		300		ns
			$C_L = 0pF$, $V_C = 15V$		50		ns
t_F	Fall time	13, 14, 16	$C_L = 1000pF$, $V_C = 15V$		200		ns
			$C_L = 0pF$, $V_C = 15V$		50		ns
Supply current							
I_{CC}	Shutdown LOW	17	$7.4V < V_S < 35V$, $f_{OSC} = 40kHz$		18	30	mA
Operating frequency for cycle-by-cycle operation of all protect features							
	Maximum frequency			400	500		kHz

NOTE:

1. $f_{OSC} = 40kHz$ ($R_T = 4.12k$, $C_T = 0.01\mu F$, $R_D = 0\Omega$) unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_S	Logic supply voltage	7.4	35	V
V_C	Collector voltage	4.5	35	V
I_O	Output load current	0	±200	mA
I_L	Reference load current	0	10	mA
f_{OSC}	Oscillator frequency	1Hz	400	kHz
R_t	Oscillator timing resistance	2	150	kΩ
C_t	Oscillator timing capacitance	150pF	20	μF
DT	Programmed dead time	3	50	%
T_A	Ambient temperature range	0	+70	°C
T_J	Junction temperature range	0	+125	°C

Switched-Mode Power Supply Control Circuit SG3526

THEORY OF OPERATION

Internal Reference

The internal reference is capable of maintaining 1% accuracy over the specified operating temperature range. The reference voltage is 5.00V at Pin 18. Short-circuit current is typically 50mA. The reference output remains stable within 30mV over an input range of 8 to 35V. Complete regulation characteristics versus line and load (see Figure 1) are listed in the Electrical Characteristics section of the data sheet. The maximum recommended load on the reference supply is 20mA.

THE RAMP OSCILLATOR

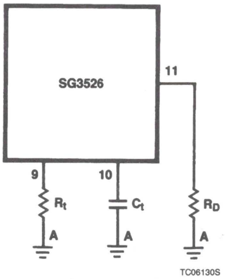
The ramp oscillitor is a self-sustained, fixed-frequency circuit with programmability provided by selecting the value of an external resistor and capacitor as shown in Figure 2. An internal current source is set by the resistor R_t to a certain value of charging current sufficient to generate a stable ramp over a range of 1Hz to 400kHz.

THE ERROR AMPLIFIER

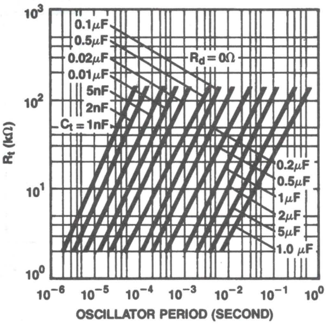
The error amplifier is a transconductance-type with open-loop unity gain bandwidth of 1MHz. Typical source/sink current is 100μA. Open-loop DC gain is 68dB with a single dominant pole at 500Hz. (See Figure 3 for detailed response.) Compensation is achieved by simple 'C' (100pF) or RC network for lag-lead compensation. This network is placed in shunt to ground from Pin 3 (refer to Figure 4). Common-mode voltage is 5V for a standard positive supply and ground for negative supply.

The Pulse Width Modulator

The pulse width modulator consists of a high-speed comparator with non-inverting input tied to the ramp generator and inverting input driven by the error amplifier output. (See Figure 5.) The resultant output forms a gated input to the metering flip-flop of which the '$\overline{Q}$' output feeds the 'R' input on the memory latch, and 'Q' output enables the main output gates (G2, G3). Alternate half-cycles are then enabled at the output (Pins 13 and 16) by the action of the toggle flip-flop. Initiation of the beginning of each half of the duty cycle is triggered by the start of the ramp, and termination occurs at the point in time where error output meets ramp voltage. It is with this sequence of control events that glitch-free output is guaranteed.



a. Ramp Oscillator Frequency Determining Components and Dead Time Programming



b. Oscillator Period vs R_+ and C_+

Figure 2

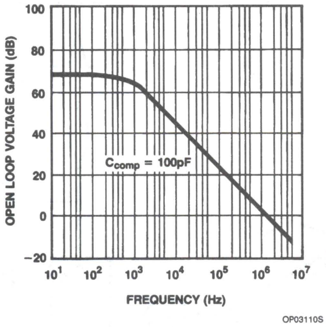


Figure 3. Error Amplifier Open-Loop Gain vs Frequency

Pulse delay times in the PWM loop are specified in the data sheet. Maximum operating frequency must take such delay times into account in order to guarantee reliable functioning of the controller under a closed-loop condition. The Signetics SG3526 is rated at a typical maximum frequency of 500kHz.

PWM GAIN

The DC gain of the pulse width modulator is determined by the ratio of input voltage to the primary power switching circuit to the active ramp voltage differential. This is given as 3.6V and 0.4V with a differential of 3.2V.

Example:

The DC supply voltage to the power converter is 48V.

$$\text{Therefore, PWM Gain} = \frac{48}{3.2} = 15$$

(For further information on loop response calculations, please refer to references 1, 2.)

THE OUTPUT DRIVER STAGE

The output driver circuit has been carefully designed to prevent cross-conduction current spikes by eliminating any overlap conduction within the totem-pole structure. The source and sink capacity is rated at 200mA. In addition, supply voltage on the driver transistors is rated at 35V with no risk of destroying the IC due to excessive power dissipation. Note the output waveform in Figure 6 shows a full 10V drive level at the rated 200mA load current. This capability means that a Power MOS gate capacity of 4000pF can be driven with a voltage rise time of 0.2μs for a 10V output.

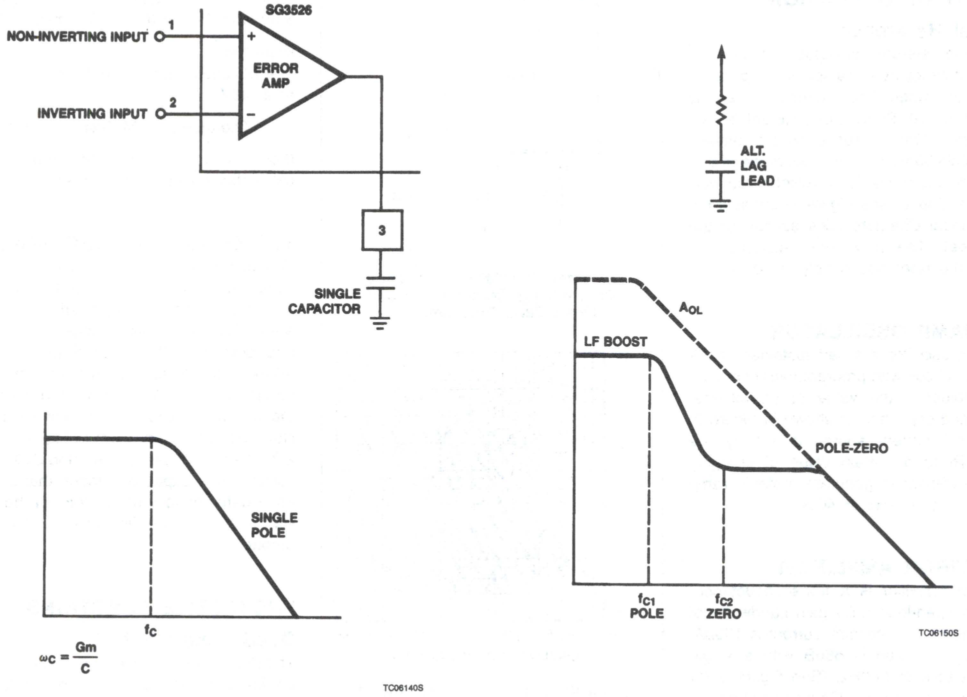
PROTECTIVE FUNCTIONS

Dead Time Control

The dead time control circuit, incorporated as an integral part of the ramp oscillator, is provided to allow the designer the ability to control the minimum off time between alternate half-cycles. (See Figures 7 and 8.) The value of R_D, as shown in the graph, allows the programming of this delay time from a minimum (Pin 11 grounded) of 1.5μs to a maximum of 9.7μs for a resistance of 22Ω tied from Pin 11 to ground (Figure 8b). Obviously, dead time in the oscillator must conform to the limitations imposed by the operating frequency.

Overcurrent Limit

The overcurrent limit function is an integral part of the PWM circuit and, as such, inputs on Pins 6 and 7 will control the cycle-by-cycle operation of the output stage on both halves of the duty cycle. The overcurrent comparator is specifically designed to propagate a high-speed shutdown signal to turn off the output metering flip-flop in the event of an overcurrent of predetermined magnitude. The overcurrent sense inputs must be treated with care in respect to lead length and shunt capacity in order to obtain the maximum speed of response. Some typical circuit configurations are shown in Figure 9a. Note that either Pin 6 or 7 may be used as threshold reference voltage anywhere within the common-mode voltage range of the comparator. As shown, a simple technique is to ground Pin 6 and to program Pin 7 high ($\geqslant$100mV) for shutdown. Very little noise immunity is allow-


SG3526
NON-INVERTING INPUT
1
+
ERROR
AMP
INVERTING INPUT
2
−
3
SINGLE
CAPACITOR
ALT.
LAG
LEAD
SINGLE
POLE
f_C
$\omega_C = \frac{Gm}{C}$
TC06140S
A_{OL}
LF BOOST
POLE-ZERO
f_{C1}
POLE
f_{C2}
ZERO
TC06150S

a. b.

Figure 4. Loop Compensation

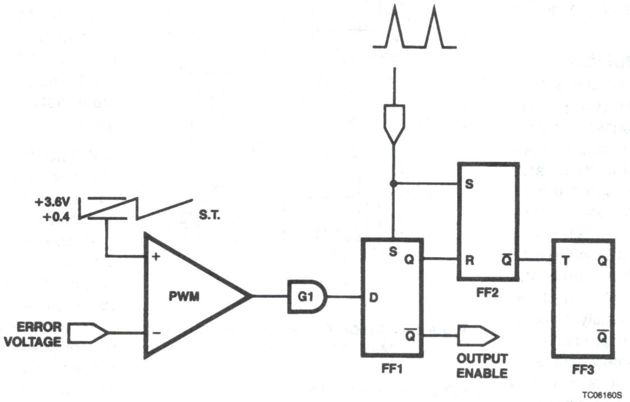

+3.6V
+0.4
S.T.
+
PWM
−
ERROR
VOLTAGE
G1
S
Q
D
$\overline{Q}$
FF1
S
R
$\overline{Q}$
FF2
OUTPUT
ENABLE
T
Q
$\overline{Q}$
FF3
TC06160S

Figure 5. PWM

ed in this case. An improved method is to set Pin 6 at some positive voltage level (such as +2.5V) and thus provide an average noise threshold of 2.5V +100mV as shown in Figure 9b. This particular circuit provides a considerable improvement in noise immunity. Note that care must be taken in providing a low impedance reference at Pin 6. The overcurrent sense comparator provides a typical hysteresis of 20mV with a threshold of 100mV (Figure 9c). The typical delay time to deactivate the output drive is 700ns at $T_J = 25°C$ rising to 1200ns at $T_J = 125°C$.

Soft-Start

This circuit provides a programmed ramp-up of the duty cycle at power-on, after remote shutdown (reset Pin 5) or low supply sense. A capacitor from Pin 4 to ground is charged towards the turn-on threshold by a 100μA source. Time constants for various values of capacitance are plotted for the designer's convenience as shown in Figure 10. The soft-start function is inititated by holding the reset below 0.2V which causes C to discharge. The Reset function, when low, also holds the error amplifier output low, initiating a minimum duty cycle at the output drivers. Low voltage shutdown occurs when V_S (Pin 17) drops below 4.0V.

External Synchronization

An external sync pulse may be injected into Pin 12 in order to provide synchronous operation of a switched-mode controller as shown in Figure 11. The required voltage level is active LOW with a threshold of 0.4V typical and a minimum pulse width of 150ns. A periodic signal at a rate approximately 10% higher than the free-running frequency of the ramp oscillator is required.

THERMAL CONSIDERATIONS

The power dissipation of the SG3526 must be considered in the design procedure in order to insure operation within the allowable device limits, particularly when maximum operating frequency is desired. The graph provided in Figure 12 will serve as a guide to staying within the device thermal limits in any design. Device dissipation is determined by summing all of the various current-voltage products, both pulsed and DC, noting the package type and the ambient operating temperature, then plotting this total device power on the respective derating graph.

UNDERVOLTAGE LOCKOUT

Should supply voltage in Pin 17 drop low enough to affect the internal reference regulator, an output inhibit circuit is activated. In addition, the voltage on Pin 5 (Reset) will be brought to a low state in order to signal remote sensing indicators. This characteristic is shown graphically in Figures 13a and b.

SYMMETRY CORRECTION

Should an external symmetry monitoring and correction circuit be required where drive unbalance may be critical, Pin 8, the shutdown function, is available to program either half of the output cycle off. This is accomplished by applying a TTL low signal with a pulse synchronized to the clock frequency. Keep in mind that the typical delay from Pin 8 is either output before shutdown is 400ns.

DOUBLE PULSE PROTECTION

The memory flip-flop must be reset by the PWM signal. This set-reset sequence provides insurance that alternate sync pulses initiate alternate A-B output cycle, preventing double pulses at the output.

CAUTION: Supply Decoupling —
Pin 17, the supply input to the internal regulator, should be decoupled from Pin 14 in order to prevent pulsed switching currents from interacting with outputs.

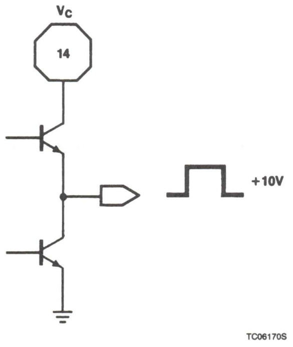


Figure 6. Output Stage

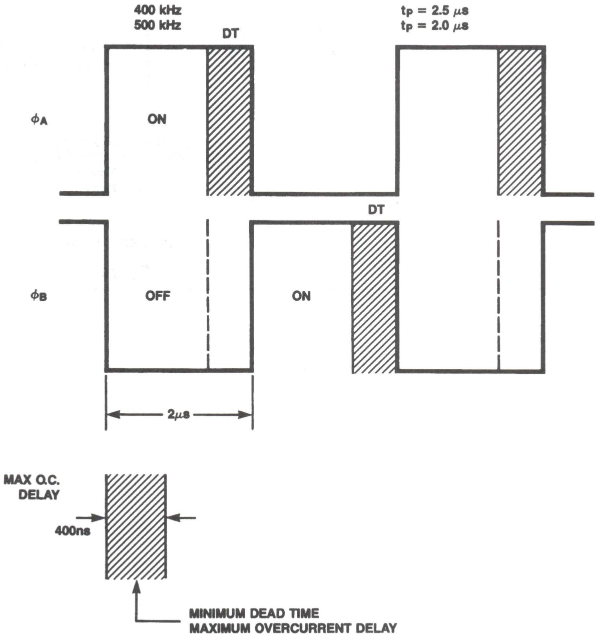
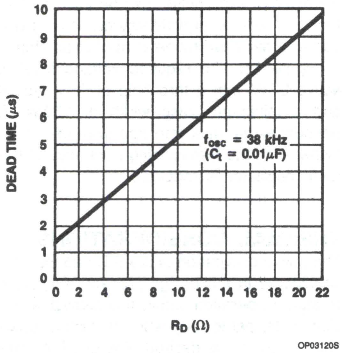
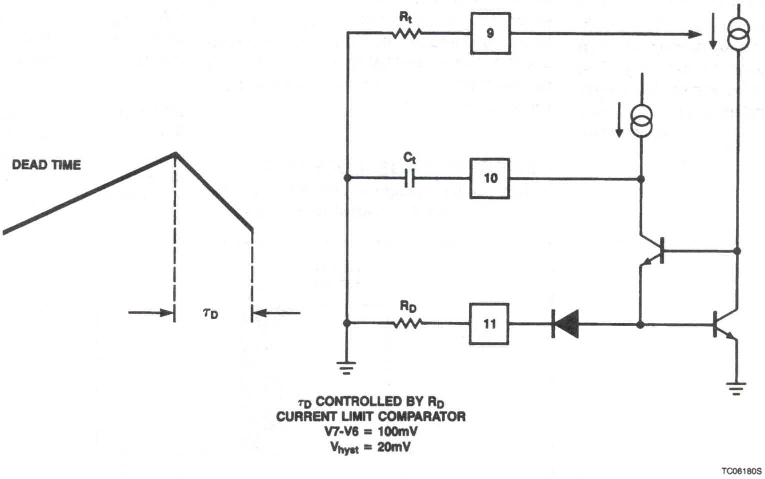


Figure 7



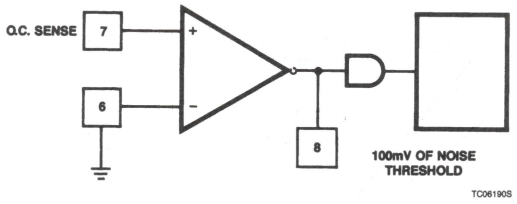
a. Output Driver Dead Time vs R_D Value


DEAD TIME
τ_D
R_t
9
C_t
10
R_D
11
TC06180S

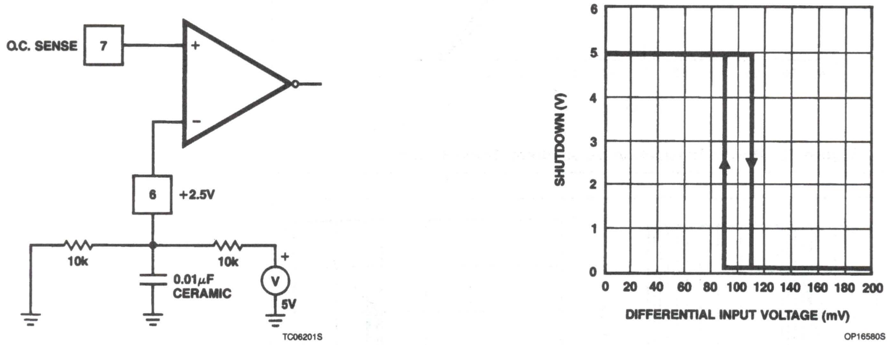
τ_D CONTROLLED BY R_D
CURRENT LIMIT COMPARATOR
V7-V6 = 100mV
V_{hyst} = 20mV

b. Dead Time

Figure 8


Q.C. SENSE
7
6
+
−
8
100mV OF NOISE THRESHOLD
TC06190S

a. OC Threshold



b. OC Threshold

c. Current Limit Transfer Function

Figure 9

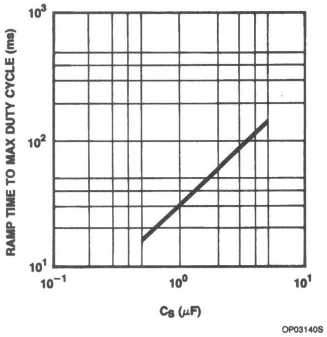


Figure 10. Soft-Start Time Constant vs C_S

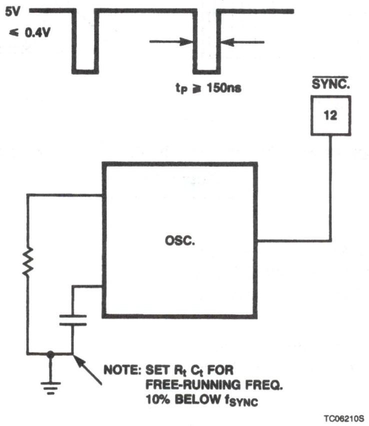

5V
≤ 0.4V
t_P ≥ 150ns
$\overline{\text{SYNC.}}$
12
OSC.
NOTE: SET R_t C_t FOR FREE-RUNNING FREQ. 10% BELOW f_{SYNC}
TC06210S

Figure 11

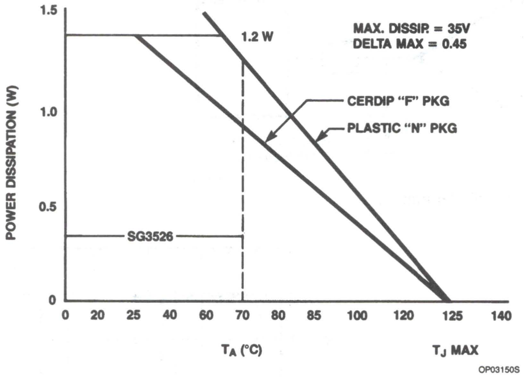
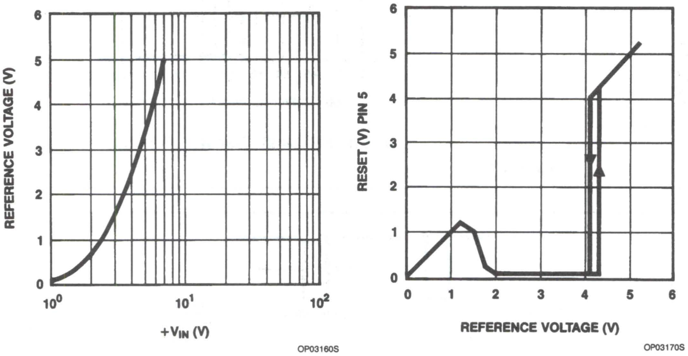


Figure 12. Power Dissipation vs Ambient Temperature



a. Reference Voltage vs Supply Voltage b. Undervoltage Lockout Characteristic

Figure 13

REFERENCES:

1. *Advances in Switched-Mode Power Conversion*, Volumes I and II, R.D.Middlebrook and Slobodan Cuk; Telsa Co., Pasadena, CA, 1983.

2. *Stability Analysis Made Simple*, H. Dean Venable; Venable Industries, Rancho Palos Verdes, CA, 1981.

Signetics

TEA1039

Control Circuit for Switched-Mode Power Supply

Product Specification

Linear Products

DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g., a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

FEATURES

- **Wide frequency range**
- **Adjustable input sensitivity**
- **Adjustable minimum frequency or maximum duty factor limit**
- **Adjustable overcurrent protection limit**
- **Supply voltage out-of-range protection**
- **Slow-start facility**

APPLICATIONS

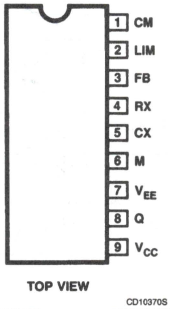
- **Home appliances**
- **Frequency regulation**
- **Flyback converters**
- **Forward converters**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP	−25°C to +125°C	TEA1039U

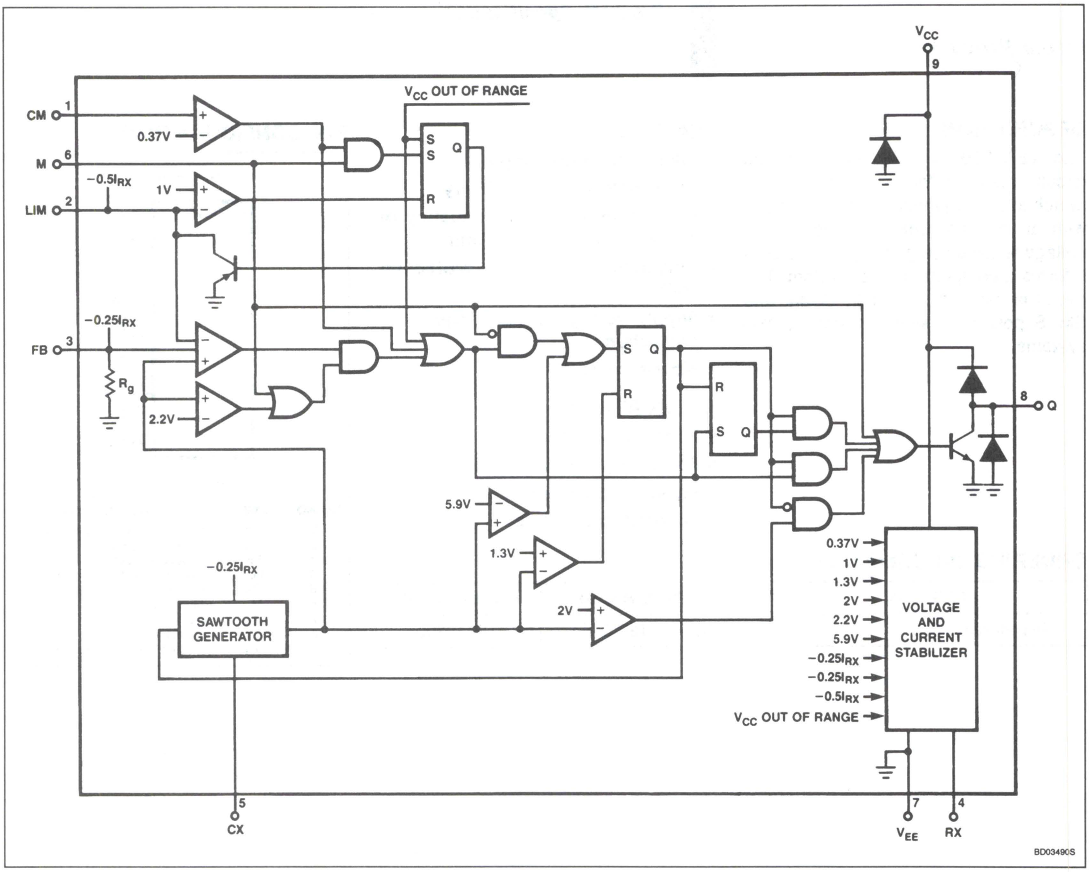
PIN CONFIGURATION

U Package



PIN NO.	SYMBOL	DESCRIPTION
1	CM	Overcurrent protection input
2	LIM	Limit setting input
3	FB	Feedback input
4	RX	External resistor connection
5	CX	External capacitor connection
6	M	Mode input
7	V_{EE}	Common
8	Q	Output
9	V_{CC}	Positive supply connection

BLOCK DIAGRAM


VCC
9
V CC OUT OF RANGE
CM 1
0.37V
M 6
S
S
Q
R
−0.5I RX
1V
LIM 2
−0.25I RX
FB 3
Rg
2.2V
S Q
R
R
S Q
8
Q
5.9V
1.3V
2V
−0.25I RX
SAWTOOTH GENERATOR
0.37V
1V
1.3V
2V
2.2V
5.9V
−0.25I RX
−0.25I RX
−0.5I RX
V CC OUT OF RANGE
VOLTAGE AND CURRENT STABILIZER
5
CX
7
V EE
4
RX
BD03490S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range, voltage source	−0.3 to +20	V
I_{CC}	Supply current range, current source	−30 to +30	mA
V_I	Input voltage range, all inputs	−0.3 to +6	V
I_I	Input current range, all inputs	−5 to +5	mA
V_{8-7}	Output voltage range	−0.3 to +20	V
	Output current range		
I_8	output transistor ON	0 to 1	A
I_8	output transistor OFF	−100 to +50	mA
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range (see Figure 1)	−25 to +125	°C
F_D	Power dissipation (see Figure 1)	max. 2	W

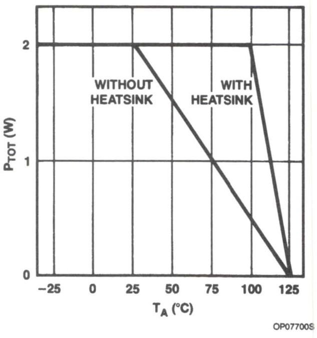


Figure 1. Power Derating Curve

DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = 14$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Supply V_{CC} (Pin 9)					
V_{CC}	Supply voltage, operating	11	14	20	V
	Supply current				
I_{CC}	at $V_{CC} = 11V$		7.5	11	mA
I_{CC}	at $V_{CC} = 20V$		9	12	mA
$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	variation with temperature		−0.3		%/°C
	Supply voltage, internally limited				
V_{CC}	at $I_{CC} = 30mA$	23.5		28.5	V
$\Delta V_{CC}/\Delta T$	variation with temperature		18		mV/°C
V_{CCmin}	Low supply threshold voltage	9	10	11	V
$\Delta V_{CC}/\Delta T$	variation with temperature		−5		mV/°C
V_{CCmax}	High supply threshold voltage	21	23	24.6	V
$\Delta V_{CC}/\Delta T$	variation with temperature		10		mV/°C
Feedback input FB (Pin 3)					
$V_{3\ 7}$	Input voltage for duty factor = 0; M input open	0		0.3	V
$-I_{FB}$	Internal reference current		0.5 I_{RX}		mA
R_g	Internal resistor R_g		130		kΩ
Limit setting input LIM (Pin 2)					
$V_{2\ 7}$	Threshold voltage		1		V
$-I_{LIM}$	Internal reference current		0.25 I_{RX}		mA
Overcurrent protection input CM (Pin 1)					
$V_{1\ 7}$	Threshold voltage	300	370	420	mV
$\Delta V_{1\ 7}/\Delta T$	variation with temperature		0.2		mV/°C
t_{PHL}	Propagation delay, CM input to output		500		ns
Oscillator connections RX and CX (Pins 4 and 5)					
	Voltage at RX connection				
$V_{4\ 7}$	at $-I_4 = 0.15$ to 1mA	6.2	7.2	8.1	V
$\Delta V_{4\ 7}/\Delta T$	variation with temperature		2.1		mV/°C
V_{LS}	Lower sawtooth level		1.3		V
V_{FT}	Threshold voltage for output H to L transition in F mode		2		V
V_{FM}	Threshold voltage for maximum frequency in F mode		2.2		V
V_{HS}	Higher sawtooth level		5.9		V
$-I_{CX}$	Internal capacitor charging current, CX connection		0.25 I_{RX}		mA
f_{OSC}	Oscillator frequency (output pulse repetition frequency)	1		10^5	Hz
	Minimum frequency in F mode,				
$\Delta f/f$	initial deviation	−10		10	%
$\frac{\Delta f/f}{\Delta T}$	variation with temperature		0.034		%/°C
	Maximum frequency in F mode,				
$\Delta f/f$	initial deviation	−15		15	%
$\frac{\Delta f/f}{\Delta T}$	variation with temperature		−0.16		%/°C

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 14, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	Output LOW time in F mode,				
$\Delta t/t$	initial deviation	−15		15	%
$\frac{\Delta t/t}{\Delta T}$	variation with temperature		0.2		%/°C
	Pulse repetition frequency in D mode,				
$\Delta f/f$	initial deviation	−10		10	%
$\frac{\Delta f/f}{\Delta T}$	variation with temperature		0.034		%/°C
	Minimum output LOW time in D mode				
t_{OLmin}	at C_5 = 3.6nF		1		µs
$\frac{\Delta t/t}{\Delta T}$	variation with temperature		0.2		%/°C
Output Q (Pin 8)					
$V_{8\ 7}$	Output voltage LOW at I_8 = 100mA		0.8	1.2	V
$\Delta V_{8\ 7}/\Delta T$	variation with temperature		1.5		mV/°C
$V_{8\ 7}$	Output voltage LOW at I_8 = 1A		1.7	2.1	V
$\Delta V_{8\ 7}/\Delta T$	variation with temperature		−1.4		mV/°C

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e., when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (Pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary DC voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode Input M (Pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, Pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

Oscillator Resistor and Capacitor Connections RX and CX (Pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (Pin 5) and ground (V_{EE}, Pin 7), and an external resistor R4 connected between the RX connection (Pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Figure 2). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2.2V. As soon as the capacitor voltage reaches 5.9V the capacitor is discharged rapidly to 1.3V and a new cycle is initiated (see Figures 3 and 4).

For voltages on the FB and LIM inputs lower than 2.2V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1.3V to 5.9V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figures 5 and 6). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback Input FB (Pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit Setting Input LIM (Pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (Pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{MAX} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent Protection Input CM (Pin 1)

A voltage on the CM input exceeding 0.37V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (Pin 8)

The output is an open-collector NPN transistor, only capable of sinking current. It requires an external resistor to drive an NPN transistor in the SMPS (see Figures 7 and 8).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Figure 1).

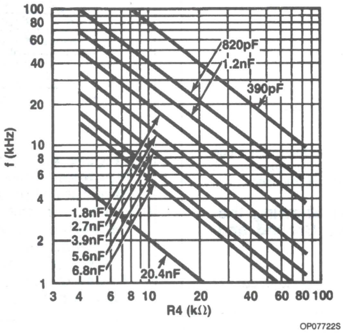
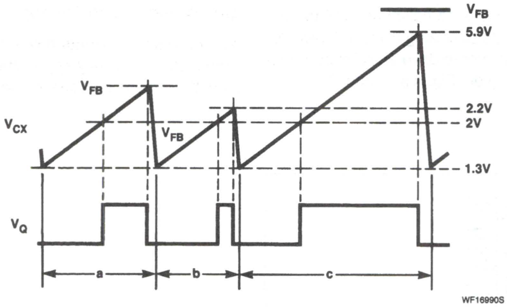


Figure 2. Minimum Pulse Repetition Frequency in the Frequency Regulation Mode, and Working Pulse Repetition Frequency in the Duty Factor Regulation Mode, as a Function of External Resistor R4 Connected Between RX and Ground with External Capacitor C5 Connected Between CX and Ground as a Parameter

Control Circuit for Switched-Mode Power Supply TEA1039



NOTES:
a. The voltages on inputs FB or LIM are between 2.2V and 5.9V. The circuit is in its normal regulation mode.
b. The voltage on input FB or input LIM is lower than 2.2V. The circuit works at its maximum frequency.
c. The voltages on inputs FB and LIM are higher than 5.9V. The circuit works at its minimum frequency.

Figure 3. Timing Diagram for the Frequency Regulation Mode Showing the Voltage on External Capacitor C5 Connected between CX and Ground and the Output Voltage as a Function of Time for Three Combinations of Input Signals

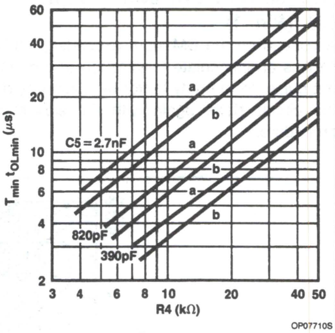
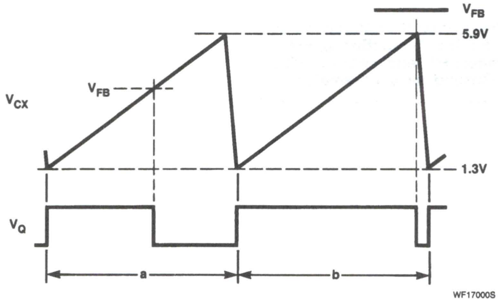


Figure 4. Minimum Output Pulse Repetition Time t_{MIN} (Curves a) and Minimum Output LOW Time t_{OLmin} (Curves b) in the Frequency Regulation Mode as a Function of External Resistor R4 Connected Between RX and Ground with External Capacitor C5 Connected Between CX and Ground as a Parameter



NOTES:
a. The voltages on inputs FB or LIM are below 5.9V. The circuit is in its normal regulation range.
b. The voltages on inputs FB and LIM are higher than 5.9V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

Figure 5. Timing Diagram for the Duty Factor Regulation Mode Showing the Voltage on External Capacitor C5 Connected Between CX and Ground and the Output Voltage as a Function of Time for Two Combinations of Input Signals

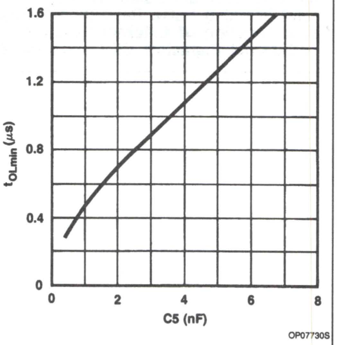
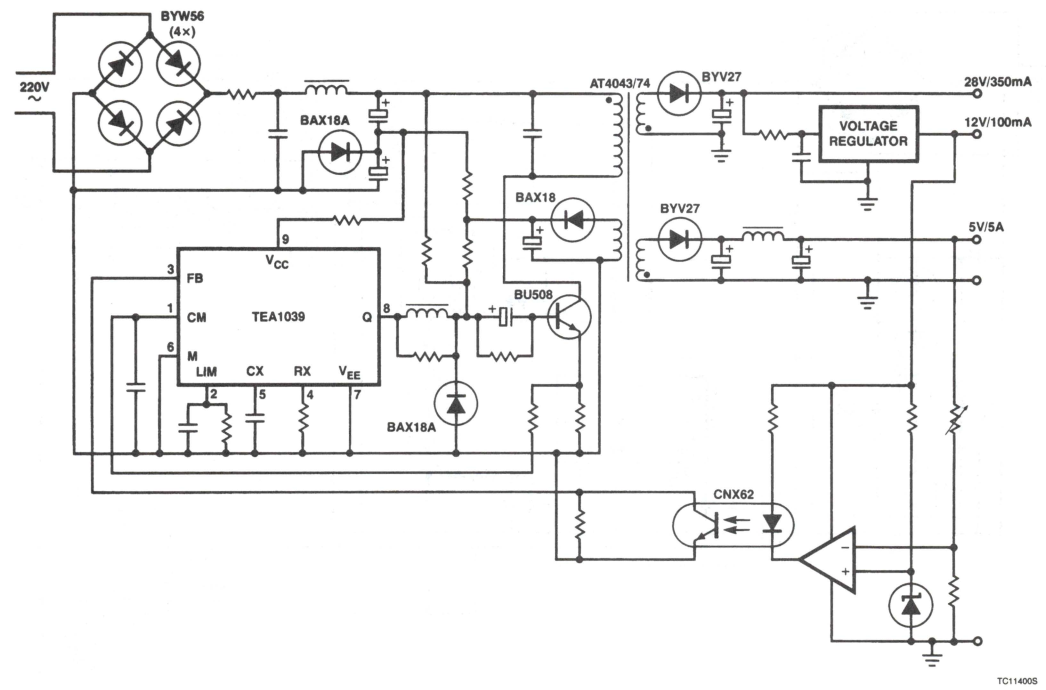


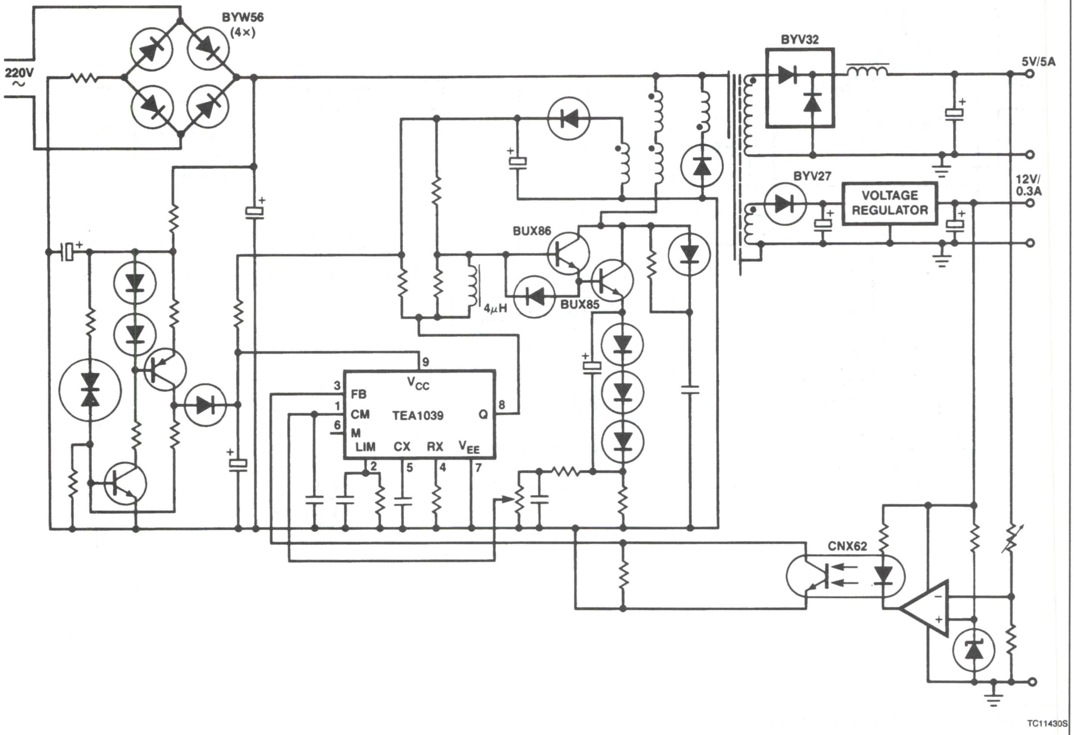
Figure 6. Minimum Output LOW Time t_{OLmin} in the Duty Factor Regulation Mode as a Function of External Capacitor C5 Connected Between CX and Ground. In This Mode the Minimum Output LOW Time is Independent of R4 for Values of R4 Between 4kΩ and 80kΩ

Control Circuit for Switched-Mode Power Supply TEA1039


BYW56
(4×)
220V
~
BAX18A
AT4043/74
BYV27
28V/350mA
VOLTAGE REGULATOR
12V/100mA
BAX18
BYV27
5V/5A
9
VCC
3 FB
1 CM
TEA1039
Q 8
6 M
LIM
CX
RX
VEE
2
5
4
7
BU508
BAX18A
CNX62
TC11400S

NOTE:
An Optocoupler CNX62 is Used for Voltage Separation.

Figure 7. Typical Application of the TEA1039 in a Variable-Frequency Flyback Converter Switched-Mode Power Supply


BYW56
(4×)
220V
~
BYV32
5V/5A
BYV27
VOLTAGE
REGULATOR
12V/
0.3A
BUX86
BUX85
4μH
9
3
FB
V_{CC}
1
CM
TEA1039
Q
8
6
M
LIM
CX
RX
V_{EE}
2
5
4
7
CNX62
TC11430S

NOTE:
An Optocoupler CNX62 is Used for Voltage Separation.

Figure 8. Typical Application of the TEA21039 in a Fixed-Frequency Variable Duty Factor Forward Converter Switched-Mode Power Supply

Signetics

μA723/723C/SA723C
Precision Voltage Regulator

Product Specification

Linear Products

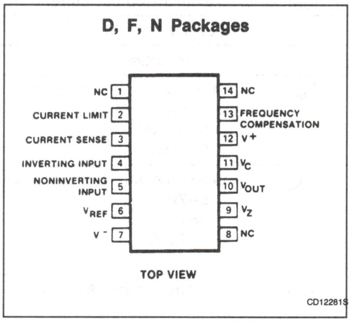
DESCRIPTION

The μA723/SA723C is a monolithic precision voltage regulator capable of operation in positive or negative supplies as a series, shunt, switching, or floating regulator. The 723 contains a temperature-compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

- **Positive or negative supply operation**
- **Series, shunt, switching, or floating operation**
- **0.01% line and load regulation**
- **Output voltage adjustable from 2V to 37V**
- **Output current to 150mA without external pass transistor**
- **μA723 MIL-STD-883A, B, C available**

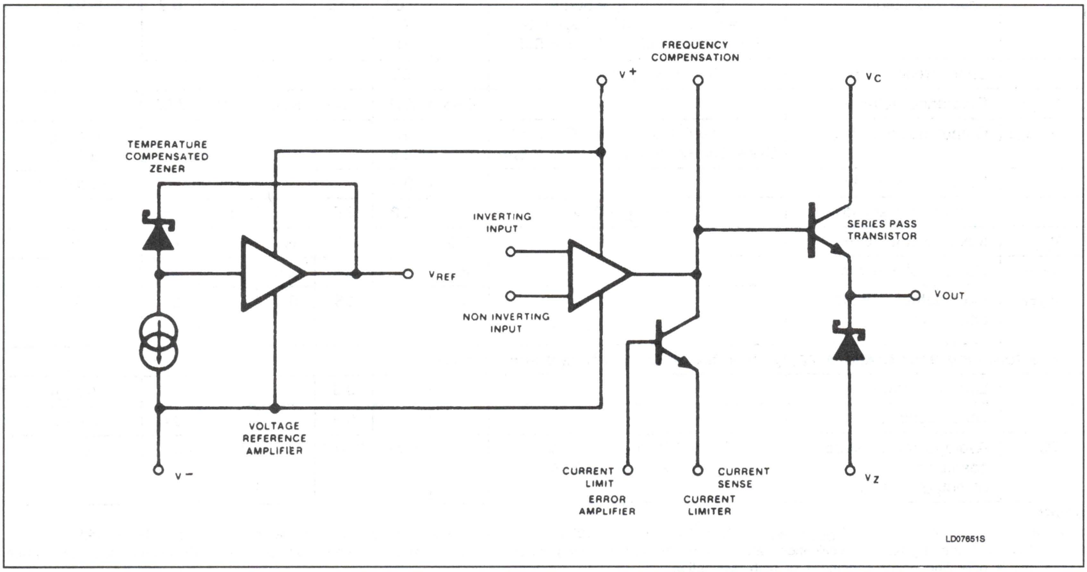
PIN CONFIGURATION


D, F, N Packages
NC 1
CURRENT LIMIT 2
CURRENT SENSE 3
INVERTING INPUT 4
NONINVERTING INPUT 5
VREF 6
V− 7
14 NC
13 FREQUENCY COMPENSATION
12 V+
11 VC
10 VOUT
9 VZ
8 NC
TOP VIEW
CD12281S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Ceramic DIP	−55°C to +125°C	μA723F
14-Pin Plastic DIP	−55°C to +125°C	μA723N
14-Pin Plastic DIP	−40°C to +85°C	SA723CN
14-Pin Ceramic DIP	0 to 70°C	μA723CF
14-Pin Plastic DIP	0 to 70°C	μA723CN
14-Pin Plastic SO	0 to 70°C	μA723CD

EQUIVALENT CIRCUIT


FREQUENCY COMPENSATION
V+
VC
TEMPERATURE COMPENSATED ZENER
INVERTING INPUT
SERIES PASS TRANSISTOR
VREF
VOUT
NON INVERTING INPUT
VOLTAGE REFERENCE AMPLIFIER
V−
CURRENT LIMIT
CURRENT SENSE
VZ
ERROR AMPLIFIER
CURRENT LIMITER
LD07651S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Pulse voltage from V+ to V– (50ms)	50	V
	Continuous voltage from V+ to V–	40	V
	Input-output voltage differential	40	V
I_{OUT}	Maximum output current	150	mA
	Current from V_{REF}	15	mA
	Current from V_Z	25	mA
P_{MAX}	Maximum power dissipation $T_A = 25°C$ (still-air)[1] F package N package D package	 1190 1420 1040	 mW mW mW
T_A	Operating ambient temperature range µA723 µA723C SA723C	 –55 to +125 0 to 70 –40 to +85	 °C °C °C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.[1]

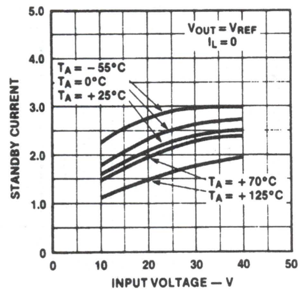
SYMBOL	PARAMETER	TEST CONDITIONS	µA723			µA723C/SA723C			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Line regulation[2]	$V_{IN} = 12V$ to $V_{IN} = 15V$ $V_{IN} = 12V$ to $V_{IN} = 40V$		0.01 0.02	0.1 0.2		0.01 0.1	0.1 0.5	$\%V_{OUT}$ $\%V_{OUT}$
	Load regulation[2]	$I_L = 1mA$ to $I_L = 50mA$ $f = 50Hz$ to $10kHz$, $C_{REF} = 0$ $f = 50Hz$ to $10kHz$, $C_{REF} = 5\mu F$		0.03 74 86	0.15		0.03 74 86	0.2	$\%V_{OUT}$ dB dB
	Short-circuit current limit	$R_{SC} = 10\Omega$, $V_{OUT} = 0$		65			65		mA
V_{REF}	Reference voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
V_{NOISE}	Output noise voltage	$BW = 100Hz$ to $10kHz$, $C_{REF} = 0$ $BW = 100Hz$ to $10kHz$, $C_{REF} = 5\mu F$		20 2.5			20 2.5		μV_{RMS} μV_{RMS}
	Long-term stability			0.1			0.1		%/1000 hrs.
	Standby current drain	$I_L = 0$, $V_{IN} = 30V$		2.3	3.5		2.3	4.0	mA
V_{IN}	Input voltage range		9.5		40	9.5		40	V
V_{OUT}	Output voltage range		2.0		37	2.0		37	V
V_{DIFF}	Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges.									
	Line regulation				0.3			0.3	$\%V_{OUT}$
	Load regulation				0.6			0.6	$\%V_{OUT}$
TC	Average temperature coefficient of output voltage	$V_{IN} = 12V$ to $V_{IN} = 15V$ $I_L = 1mA$ to $I_L = 50mA$		0.002	0.015		0.003	0.015	%/°C

NOTES:

1. $V_{IN} = V+ = V_C = 12V$, $V- = 0V$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leqslant 10k\Omega$.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

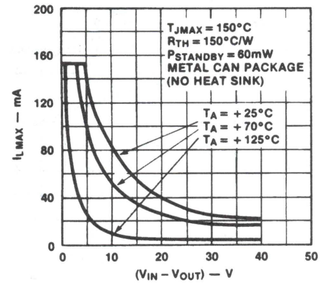
TYPICAL PERFORMANCE CHARACTERISTICS

Standby Current Drain as a Function of Input Voltage



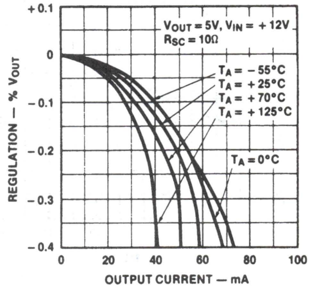
OP16420S

Maximum Load Current as a Function of Input-Output Voltage Differential



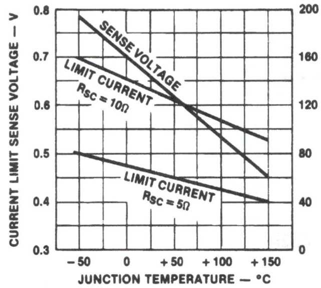
OP16430S

Load Regulation Characteristics with Current Limiting



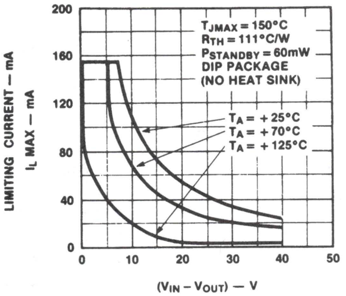
OP16440S

Current Limiting Characteristics as a Function of Junction Temperature



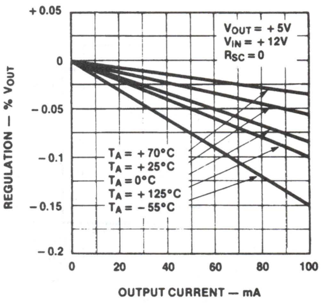
OP16451S

Maximum Load Current as a Function of Input-Output Voltage Differential



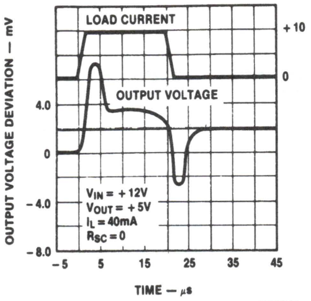
OP16460S

Load Regulation Characteristics Without Current Limiting



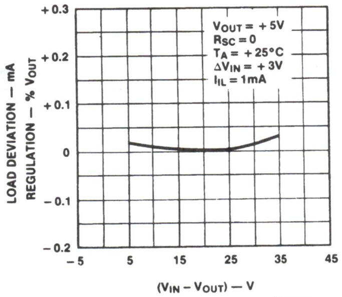
OP16470S

Load Transient Response



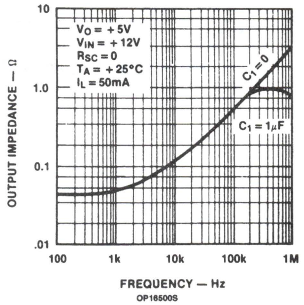
OP16480S

Line Regulation as a Function of Input-Output Voltage Differential



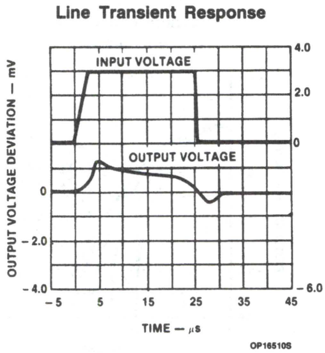
OP16490S

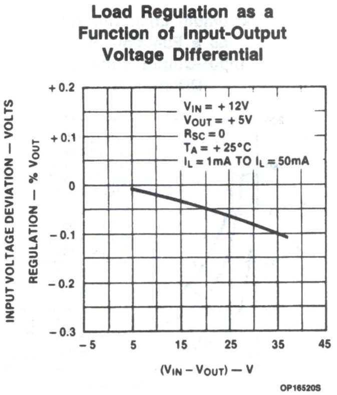
Output Impedance as a Function of Frequency

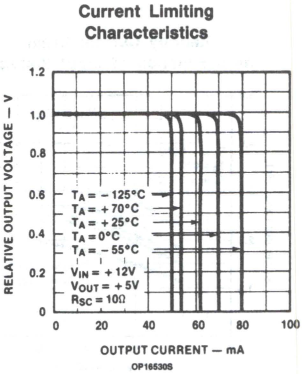


OP16500S

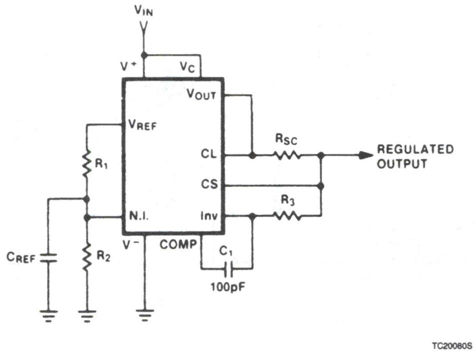
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)







TYPICAL APPLICATIONS

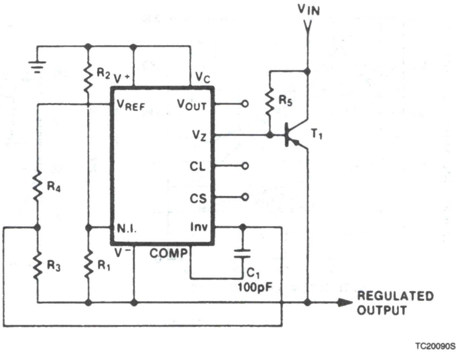

V_IN
V+
V_C
V_OUT
V_REF
R_SC
CL
REGULATED OUTPUT
CS
R_1
R_3
N.I.
Inv
V−
COMP
C_1
C_REF
R_2
100pF
TC20080S

NOTES:

$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

Low Voltage Regulator ($V_{OUT} = 2$ to 7V)

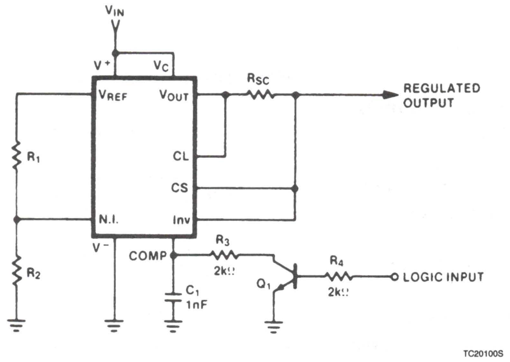

V_IN
R_2
V+
V_C
V_REF
V_OUT
R_5
V_Z
T_1
CL
R_4
CS
N.I.
Inv
V−
COMP
R_3
R_1
C_1
100pF
REGULATED OUTPUT
TC20090S

NOTE:

$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right]; \ R_3 = R_4$

Negative Voltage Regulator

TYPICAL APPLICATIONS (Continued)

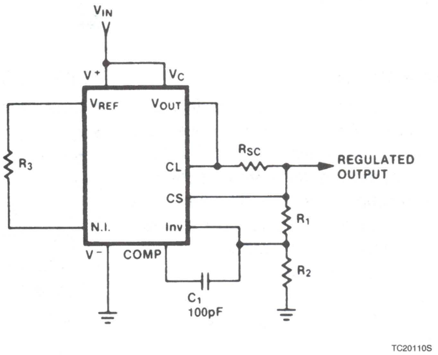

VIN
V+
VC
VREF
VOUT
RSC
REGULATED OUTPUT
R1
CL
CS
N.I.
Inv
V−
COMP
R3
2kΩ
R4
2kΩ
Q1
LOGIC INPUT
R2
C1
1nF

TC20100S

NOTE:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

Remote Shutdown Regulator With Current Limiting (V_{OUT} = 2 to 7V)


VIN
V+
VC
VREF
VOUT
R3
RSC
CL
REGULATED OUTPUT
CS
R1
N.I.
Inv
V−
COMP
R2
C1
100pF

TC20110S

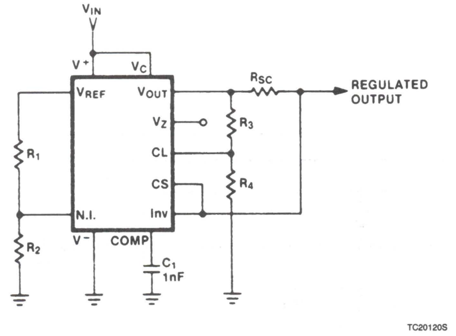
NOTES:

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right];\ R_3 = R_4$$

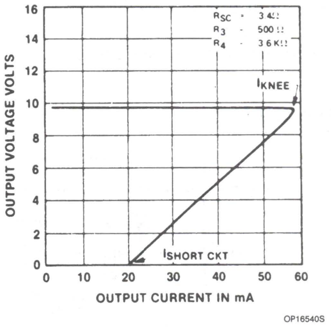
$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

R_3 may be eliminated for minimum component count

High Voltage Regulator (V_{OUT} = 7 to 37V)


VIN
V+
VC
VREF
VOUT
RSC
REGULATED OUTPUT
VZ
R3
R1
CL
CS
R4
N.I.
Inv
R2
V−
COMP
C1
1nF

TC20120S



OP16540S

NOTES:

$$I_{KNEE} = \left[\frac{V_{OUT}R_3}{R_{SC}\ R_4} + \frac{V_{SENSE}\ (R_3 + R_4)}{R_{SC}R_4}\right]$$

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}\right]$$

NOTES:

$$\frac{R_4}{R_3} = \frac{V_{OUT}\ I_{SC}}{V_{SENSE}(I_{KNEE} - I_{SHORT\ CKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

Foldback Current Limiting Regulator (V_{OUT} = 2 to 7V)

UC1842/2842/3842
Current-Mode PWM Controller

Preliminary Specification

Linear Products

DESCRIPTION

The UC1842 family of control ICs provides in an 8-Pin mini-DIP the necessary features to implement off-line, fixed-frequency current-mode control schemes with a minimal external parts count. This technique results in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting.

Protection circuitry includes built-in undervoltage lock-out and current limiting. Other features include fully-latched operation, a 1% trimmed bandgap reference, and start-up current less than 1mA.

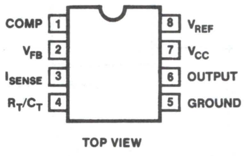
These devices feature a totem-pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N-channel power devices, the output is low in the OFF state.

FEATURES

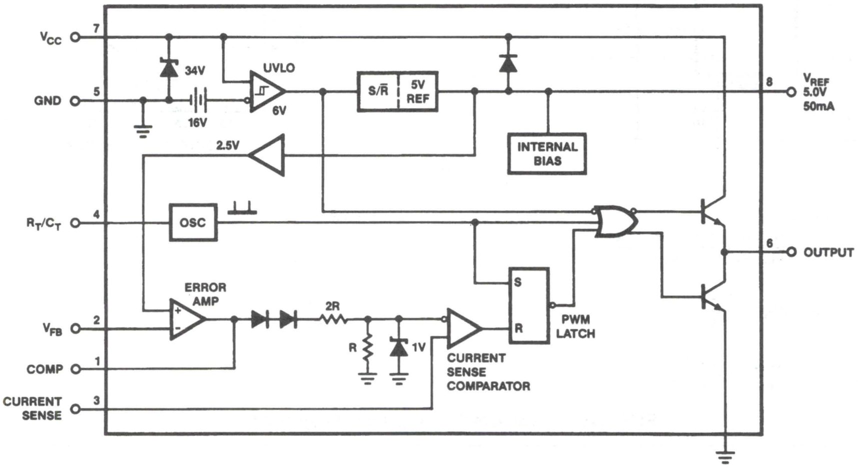
- **Low start-up current (≤ 1mA)**
- **Automatic feed-forward compensation**
- **Pulse-by-pulse current limiting**
- **Enhanced load response characteristics**
- **Undervoltage lock-out with 6V hysteresis**
- **Double pulse suppression**
- **High current totem-pole output**
- **Internally-trimmed bandgap reference**
- **500kHz operation**

PIN CONFIGURATION

N, FE, D Packages


COMP 1
V_{FB} 2
I_{SENSE} 3
R_T/C_T 4
8 V_{REF}
7 V_{CC}
6 OUTPUT
5 GROUND
TOP VIEW
CD10470S

BLOCK DIAGRAM


V_{CC} 7
GND 5
R_T/C_T 4
V_{FB} 2
COMP 1
CURRENT SENSE 3
34V
16V
UVLO
6V
S/R̄
5V REF
2.5V
INTERNAL BIAS
OSC
ERROR AMP
2R
R
1V
CURRENT SENSE COMPARATOR
S
R
PWM LATCH
8 V_{REF} 5.0V 50mA
6 OUTPUT
BD03500S

Current-Mode PWM Controller UC1842/2842/3842

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	UC3842N
8-Pin Ceramic DIP	0 to +70°C	UC3842FE
8-Pin Plastic SO	0 to +70°C	UC3842D
8-Pin Plastic DIP	−40 to +85°C	UC2842N
8-Pin Ceramic DIP	−40 to +85°C	UC2842FE
8-Pin Plastic SO	−40 to +85°C	UC2842D
8-Pin Ceramic DIP	−55 to +125°C	UC1842FE
8-Pin Plastic DIP	−55 to +125°C	UC1842N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage ($I_{CC} < 30mA$)		Self-Limiting
V_{CC}	Supply voltage (low impedance source)	30	V
I_{OUT}	Output current	±1	A
	Output energy (capacitive load)	5	μJ
	Analog inputs (Pin 2, Pin 3)	-0.3V to V_{CC}	
	Error amp output sink current	10	mA
P_D	Power dissipation at $T_A \leqslant 70°C$ (derate 12.5mW/°C for $T_A > 70°C$)	1	W
T_{STG}	Storage temperature range	-65°C to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec max)	300	°C

NOTE:
1. All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.

DC AND AC ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for $-55 \leqslant T_A \leqslant 125°C$ for UC1842; $-25 \leqslant T_A \leqslant 85°C$ for UC2842; $0 \leqslant T_A \leqslant 70°C$ for UC3842; $V_{CC} = 15^4$; $R_T = 10k\Omega$; $C_T = 3.3nF$.)

SYMBOL	PARAMETER	TEST CONDITIONS	UC1842 UC2842			UC3842			UNIT
			Min	Typ	Max	Min	Typ	Max	
Reference section									
V_{OUT}	Output voltage	$T_J = 25°C$, $I_O = 1mA$	4.95	5.00	5.05	4.90	5.00	5.10	V
	Line regulation	$12 \leqslant V_{IN} \leqslant 25V$		6	20		6	20	mV
	Load regulation	$1 \leqslant I_O \leqslant 20mA$		6	25		67	25	mV
	Temp. stability[1]			0.2	0.4		0.2	0.4	mV/°C
	Total output variation	Line, load, temp.[1]	4.90		5.10	4.82		5.18	V
V_{NOISE}	Output noise voltage	$10Hz \leqslant f \leqslant 10kHz$, $T_J = 25°C$[1]		50			50		μV
	Long-term stability	$T_A = 125°C$, 1000 Hrs.[1]		5	25		5	25	mV
	Output short-circuit	$T_A = 25°C$		−100	−130		−100	−130	mA
Oscillator section									
	Initial accuracy	$T_J = 25°C$	47	52	57	47	52	57	kHz
	Voltage stability	$12 \leqslant V_{CC} \leqslant 25V$		0.2	1		0.2	1	%
	Temp. stability	$T_{MIN} \leqslant T_A \leqslant T_{MAX}$[1]		5			5		%
	Amplitude	$V_{PIN\ 4}$ peak-to-peak		1.7			1.7		V
Discharge current									
	Discharge current	$T_1 = 25°C$, $T_{MIN} \leqslant T_a \leqslant T_{MAX}$	7.8 7.5	8.3	8.8 9.0	7.8 7.6	8.3	8.8 9.0	mA
I_{BIAS}	Input bias current			−0.3	−1		−0.3	−2	μA
A_{VOL}		$2 \leqslant V_O \leqslant 4V$	65	90		65	90		dB
	Unity gain bandwidth[1]		0.7	1		0.7	1		MHz
PSRR	Power supply rejection ratio	$12 \leqslant V_{CC} \leqslant 25V$	60	70		60	70		dB
I_{SINK}	Output sink current	$V_{PIN\ 2} = 2.7V$, $V_{PIN\ 1} = 1.1V$	2	6		2	6		mA
I_{SOURCE}	Output source current	$V_{PIN\ 2} = 2.3V$, $V_{PIN\ 1} = 5V$	−0.5	−0.8		−0.5	−0.8		mA
	V_{OUT} High	$V_{PIN\ 2} = 2.3V$, $R_L = 15k$ to ground	5	6		5	6		V
	V_{OUT} Low	$V_{PIN\ 2} = 2.7V$, $R_L = 15k$ to Pin 8		0.7	1.1		0.7	1.1	V
Current sense section									
	Gain[2,3]		2.85	3	3.15	2.85	3	3.15	V/V
	Maximum input signal	$V_{PIN\ 1} = 5V$[2]	0.9	1	1.1	0.9	1	1.1	V
PSRR	Power supply rejection ratio	$12 \leqslant V_{CC} \leqslant 25V$[2]		70			70		dB
I_{BIAS}	Input bias current			−2	−10		−2	−10	μA
	Delay to output	$T_J = 25°C$[1]		200	400		200	400	ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

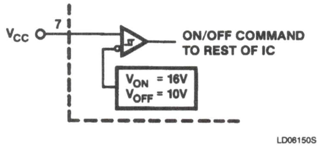
(Unless otherwise stated, these specifications apply for $-55 \leqslant T_A \leqslant 125°C$ for UC1842; $-25 \leqslant T_A \leqslant 85°C$ for UC2842; $0 \leqslant T_A \leqslant 70°C$ for UC3842; $V_{CC} = 15V^4$; $R_T = 10k\Omega$; $C_T = 3.3nF$.)

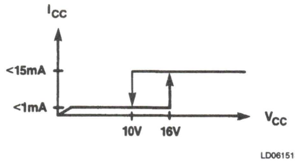
SYMBOL	PARAMETER	TEST CONDITIONS	UC1842 UC2842			UC3842			UNIT
			Min	Typ	Max	Min	Typ	Max	
Output section									
I_{OL}	Output Low-Level	$I_{SINK} = 20mA$		0.1	0.4		0.1	0.4	V
		$I_{SINK} = 200mA$		1.5	2.2		1.5	2.2	V
I_{OH}	Output High-Level	$I_{SOURCE} = 20mA$	13	13.5		13	13.5		V
		$I_{SOURCE} = 200mA$	12	13.5		12	13.5		V
t_R	Rise time	$T_J = 25°C$, $C_L = 1nF^1$		50	150		50	150	ns
t_F	Fall time	$T_J = 25°C$, $C_L = 1nF^1$		50	150		50	150	ns
Undervoltage lockout section									
	Start threshold		15	16	17	14.5	16	17.5	V
	Min. operating voltage	After turn on	9	10	11	8.5	10	11.5	V
Total standby current									
	Start-up current			0.5	1		0.5	1	mA
I_{CC}	Operating supply current	$V_{PIN\ 2} = V_{PIN\ 3} = 0V$		11	15		11	15	mA
	V_{CC} zener voltage	$I_{CC} = 25mA$		34			34		V

NOTES:

1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{PIN\ 2} = 0$.
3. Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$; $0 \leqslant V_{PIN\ 3} \leqslant 0.8V$.
4. Adjust V_{CC} above the start threshold before setting at 15V.

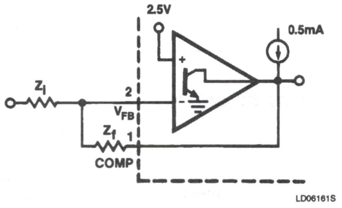
UNDERVOLTAGE LOCKOUT





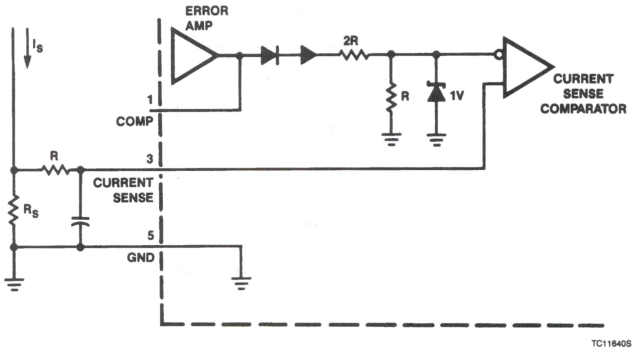
NOTE:
During Undervoltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

ERROR AMP CONFIGURATION


2.5V
0.5mA
+
–
Z_I
2
V_{FB}
Z_f
1
COMP
LD06161S

NOTE:
Error AMP can source or sink up to 0.5mA.

CURRENT SENSE CIRCUIT

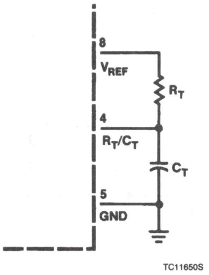

ERROR
AMP
I_S
2R
R
1V
CURRENT
SENSE
COMPARATOR
1
COMP
R
3
CURRENT
SENSE
R_S
5
GND
TC11640S

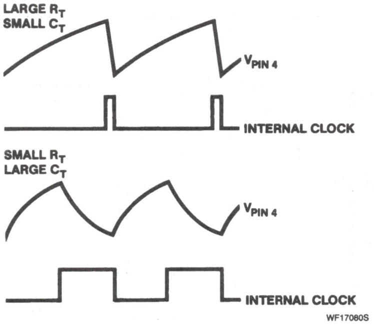
NOTE:
Peak current (I_S) is determined by the formula:

$$I_S\ MAX = \frac{1.0V}{R_S}.$$

A small RC filter may be reqiured to suppress switch transients.

OSCILLATOR WAVEFORMS AND MAXIMUM DUTY CYCLE


8
V_{REF}
R_T
4
R_T/C_T
C_T
5
GND
TC11650S


LARGE R_T
SMALL C_T
$V_{PIN\ 4}$
INTERNAL CLOCK
SMALL R_T
LARGE C_T
$V_{PIN\ 4}$
INTERNAL CLOCK
WF17080S

NOTES:

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:

$$t_C \simeq 0.55\, R_T C_T$$

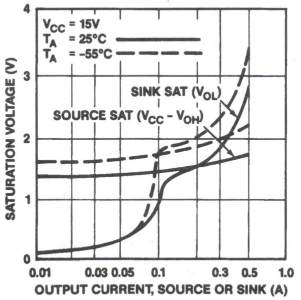
$$t_D \simeq R_T C_T \ln\left(\frac{0.0063\, R_T - 2.7}{0.0063\, R_T - 4}\right)$$

Frequency, then, is: $f = (t_C + t_D)^{-1}$

For $R_T > 5k$ $\quad f \simeq \frac{1.8}{R_T C_T}$

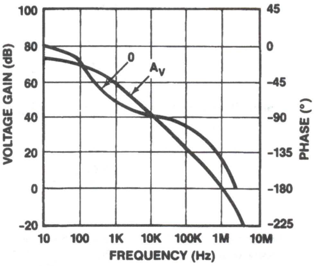
TYPICAL PERFORMANCE CHARACTERISTICS

Output Saturation Characteristics



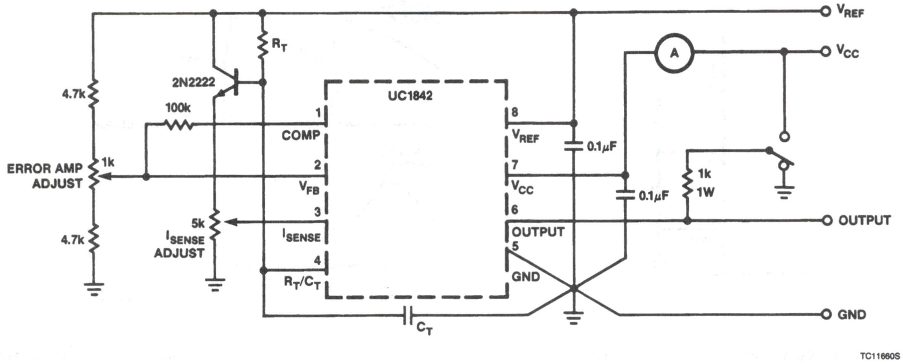
OP07790S

Error Amplifier Open-Loop Frequency Response



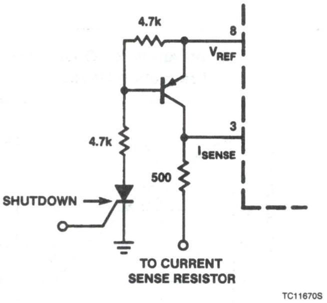
OP07800S

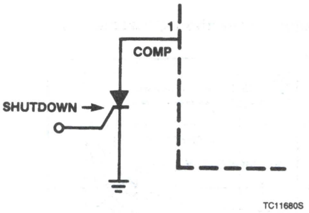
OPEN-LOOP LABORATORY TEST FIXTURE


UC1842
2N2222
R_T
4.7k
100k
ERROR AMP ADJUST
1k
4.7k
5k
I_{SENSE} ADJUST
1 COMP
2 V_{FB}
3 I_{SENSE}
4 R_T/C_T
8 V_{REF}
7 V_{CC}
6 OUTPUT
5 GND
0.1µF
0.1µF
1k 1W
A
V_{REF}
V_{CC}
OUTPUT
GND
C_T
TC11660S

NOTE:
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

SHUTDOWN TECHNIQUES

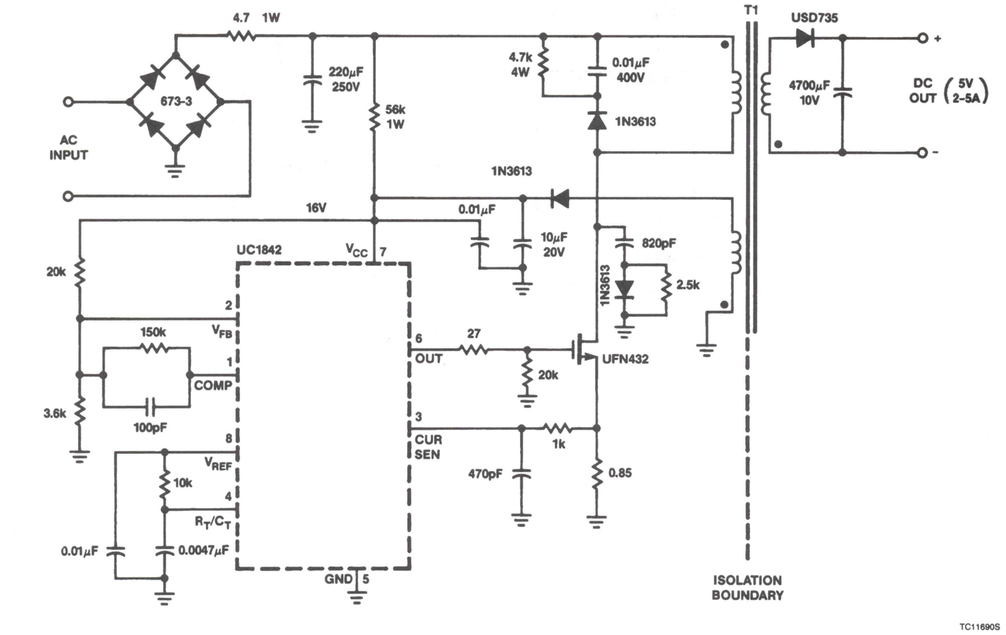

4.7k
8 V_{REF}
3 I_{SENSE}
4.7k
500
SHUTDOWN
TO CURRENT SENSE RESISTOR
TC11670S


1 COMP
SHUTDOWN
TC11680S

NOTE:
Shutdown of the UC1842 can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to Block Diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In the examples shown, an externally-latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

Current-Mode PWM Controller UC1842/2842/3842

OFF-LINE FLYBACK REGULATOR



4.7 1W
673-3
AC INPUT
220µF 250V
56k 1W
4.7k 4W
0.01µF 400V
1N3613
T1
USD735
4700µF 10V
DC OUT (5V 2-5A)
+
-
1N3613
16V
0.01µF
10µF 20V
820pF
1N3613
2.5k
UC1842
VCC 7
20k
2 VFB
150k
1 COMP
100pF
3.6k
8 VREF
10k
4 RT/CT
0.01µF
0.0047µF
GND 5
6 OUT
27
20k
UFN432
3 CUR SEN
1k
470pF
0.85
ISOLATION BOUNDARY
TC11690S

NOTES:

T1: Coilcraft E-4140-B
Primary - 97 turns
single AWG 24
Secondary - 4 turns
4 parallel AWG 22
Control - 9 turns
3 parallel AWG 28

SPECIFICATIONS

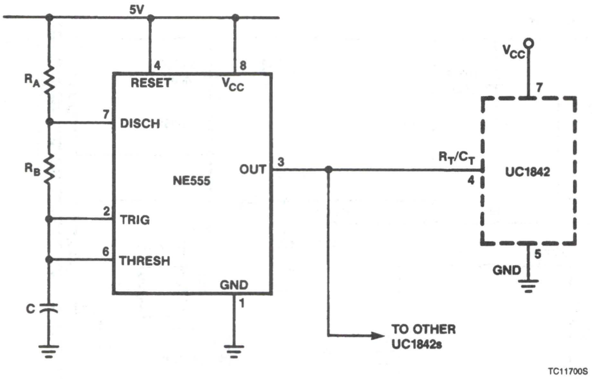
Input line voltage:	$90V_{AC}$ to $130V_{AC}$
Input frequency:	50 or 60Hz
Switching frequency:	40kHz± 10%
Output power:	25W maximum
Output voltage:	5V± 5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*

Efficiency @ 25 W,	
$V_{IN} = 90V_{AC}$:	70%
$V_{IN} = 130V_{AC}$:	65%
Output short-circuit current:	2.5A average

NOTE:

*This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the UC1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance. For applications requiring better load regulation, a UC1901 Isolated Feedback Generator can be used to directly sense the output voltage.

SYNCHRONIZATION AND MAXIMUM DUTY CYCLE CLAMP


5V
R_A
R_B
C
4
RESET
8
V_{CC}
7
DISCH
NE555
OUT
3
2
TRIG
6
THRESH
GND
1
TO OTHER
UC1842s
V_{CC}
7
R_T/C_T
4
UC1842
5
GND
TC11700S

NOTES:

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$D_{MAX} = \frac{R_B}{R_A + 2R_B}$$

Signetics

Linear Products

AN125
Progress in SMPS Magnetic Component Optimization

Application Note

Author: L. P. M. Bracke
N. V. Philips

The last ten years have seen considerable progress in the development of the switched-mode power supply. Both design methods and associated hardware have been refined by experience and intensive development. These improvements, especially in the understanding of the influence of magnetic material and winding-conductor properties on SMPS operation, are reflected in the more straightforward and complete design routines now available. The better understanding that made for the improved design routines has also resulted in improved core designs: the ETD range of ferrite cores. Furthermore, lessons learned from experience in wound-component production have been applied to the design of the associated hardware, especially the coil former. The improved core and coil former, together with specially-developed assembly hardware, form the ETD system.

IMPROVED DESIGN ROUTINES

AN1261 presents complete design routines for the magnetic components of all common versions of SMPS. Part 1 covers most aspects of SMPS design, with emphasis on the interaction between the electronic and magnetic aspects. The basic electrical relationships are given for forward, push-pull and flyback converters. Practical formulae are given for inductance and effective-current values. Auxiliary outputs and other special features are included in the coverage, as are related control aspects. All treatments are related to the magnetic design.

The data derived from Part 1 are used in Part 2 to select a suitable ferrite core for the transformer. Here, the magnetic and thermal properties of ferrite cores are considered as they affect their suitability for a given application. Initial selection of a suitable core is by means of charts showing the limits of performance to be expected at various frequencies. The optimum working conditions for cores in various transformer types are discussed, and a further chart enables this optimum to be determined. Wound transformer thermal characteristics are discussed, and formulae given for the losses in the core itself.

SELECTING THE CORRECT CORE

Most SMPS requirements can be satisfied by the range of cores currently available. The preferred grade of material for such high-frequency power applications is Ferroxcube 3C8.

Core Selection Charts

Due to the wide variation in application conditions, the selection charts have been designed to indicate the range of operation of the cores. This is done by using areas of throughput power as a function of frequency as shown in Figure 1. These are effectively areas of good design, since both boundaries represent the performance of a well-designed transformer.

The upper boundary of each area corresponds to a transformer design operating at optimum flux density sweep, with maximum use of the winding window, and Litz-wire windings, for minimum AC resistance. The lower boundary corresponds to a transformer design that also operates at optimum flux density, but has optimized solid-wire windings incorporating 8mm creepage distance for IEC 435 mains isolation, and with a demagnetising winding occupying one-third of the winding space.

Selection charts are given for push-pull, forward and flyback converter SMPS. However, the flyback converter charts are mainly intended as a cross-check on the design obtained by the method given in Reference 4 for chokes.

Operating Conditions

Converter type has the largest influence on throughput power obtainable, but other factors also influence performance, principally

- flux-density sweep
- winding configuration (simple or split, for example) and
- the presence of sensor or demagnetizing windings
- the type of conductor used in the windings
- the number of output windings required
- mains insulation requirements.

Generally, the selection charts assume worst-case conditions. Operation at ambient temperatures lower than the 60°C assumed, the use of feed-forward to ease the restriction on peak flux-density ($\frac{1}{1.72}$ of saturation to allow for transient conditions), or heatsinking or potting to reduce thermal resistance, will all increase transformer power capacity.

Flyback Transformers and Chokes

Flyback converter transformers and output chokes are magnetically much the same: the main design requirement is stored energy, $\frac{1}{2}I^2L$. This is the basis of a separate design routine that includes winding design. This routine, using specially-developed design

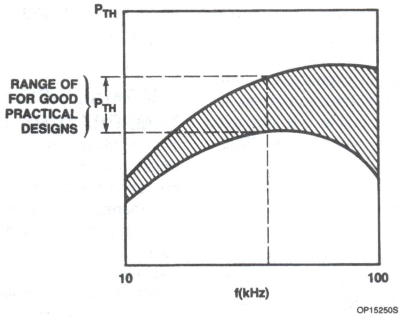
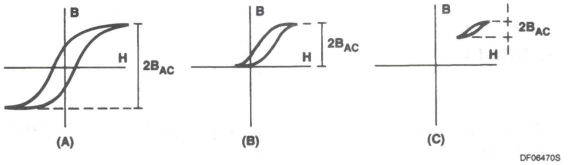


Figure 1. In the Core Selection Charts Given in AN1261, the Power-Handling Capabilities of Each Core are Plotted as a Shaded Area Extending From 10kHz to 100kHz. The Vertical Boundaries of This Area are the Upper and Lower Limits of Throughput Power Capacity Achievable by Good Design but Depending on Conductor Type and Insulation Requirements.

Progress in SMPS Magnetic Component Optimization AN125

charts, leads directly to spacer thickness and number of turns.



a. Push-Pull

b. Forward Converter Transformers (With Slow-Rise Capacitor) or Ringing Choke

c. Flyback Converter Chokes

Figure 2. Flux-Density Excursions and Corresponding Flux-Density Sweeps

OPERATING FLUX DENSITY

For chokes and flyback-converter transformers (which operate as chokes), stored energy is the basis of the design (subject to the core not being driven into saturation). With forward and push-pull converter transformers, the operating flux-density (both AC and DC components) is set at the beginning of the design process.

Forward and Push-Pull Converters

The operating flux density in forward and push-pull converter transformers strongly influences the overall volume of the transformer. Thus, it is set at the beginning of the design process to as high a level as is practical. For forward converter transformers, this level is determined by transient protection requirements or permissible core loss only. With push-pull converters, however, considerations of symmetry may dominate the choice.

Both forward and push-pull converter transformers must be designed to accommodate rapid changes of load. This is done by introducing a transient factor, usual symbol α, related to the range of input voltage for which the power supply is designed. A common value of α is 1.72. This is suitable for mains-fed supplies (215V to 370V or 200V to 340V), telephone supplies (40V to 70V), and mobile supplies (9V to 15.5V).

Considerations of symmetry usually result in the value of α being multiplied by a further factor ϵ for push-pull converter transformers. Asymmetry leads to core saturation, which in turn results in destruction of power switches. Principal causes of asymmetry are unbalanced flux linkage in windings and unequal conduction times in switches. Where care has been taken to achieve balanced transformer windings, and protection circuitry is incorporated to ensure equal conduction times, the value of ϵ may be 1.15; that is, α is increased from 1.72 to 2 for a typical core. Where unbalance is accepted, however, the value of ϵ should be 2. (A list of the symbols used in this article, together with their definitions, is given as Table 1.)

The use of feed-forward can considerably reduce the value of α required but at the expense of reduced transient response.

In forward-converter transformers, core remanence should also be taken into consideration. (Remanence is the induction remaining in a magnetized substance when the magnetizing force has become zero.) However, the introduction of a small air gap in the core, and the use of a slow-rise capacitor allow the whole first quadrant of the core hysteresis loop to be used.

Figure 2 shows the maximum transformer flux-density sweeps for various converter types, and Table 2 gives the value of transient factors α and ϵ under various conditions.

Optimum Flux-Density Sweeps

Manipulation of the expression for the throughput power of an SMPS transformer shows that power reaches a maximum at a combination of operating frequency and flux density such that core loss is 44% of total loss. That is, when

$$0.44 \frac{\Delta T}{R_{th}} = 16.7\ f^{1.3}\ B_{ac\ em}^{2.5}\ V_e$$

Here, the right-hand part of the expression is the typical hysteresis loss of Ferroxcube 3C8 ferrite. Since eddy current loss is neglected, this expression applies only up to about 100kHz.

Using this expression, curves of $B_{ac\ em}$, the peak flux-density sweep, have been derived for all Philips' SMPS transformer cores (See Figure 3).

THERMAL RESISTANCE AND TEMPERATURE RISE

The maximum permissible dissipation of a transformer or choke is set by its maximum operating temperature; ambient temperature and thermal resistance depend on core size, mounting method and attitude, the type of conductor in the winding and the amount of insulation incorporated. Due to the insulating effect of the interleaving where 8mm creepage distance is allowed for in the windings, two values are quoted for thermal resistance in AN1261 with and without creepage allowance.

Results confirm that transformer temperature rise can be accurately calculated from the product of total transformer dissipation and thermal resistance for any ratio of core to winding loss.

THE EFFECT OF OPERATING FREQUENCY

Winding Properties

Depending on frequency, the windings of an SMPS transformer fall into one of three categories. At low frequencies, the available winding-window height will be insufficient to accommodate minimum-loss (ideal) windings. At some higher frequency, f_L, the height of minimum-loss windings becomes less than that of the winding window. Finally, at some higher frequency, f_1, the number of turns required for the lowest-voltage winding becomes unity.

Where the winding height is insufficient for minimum-loss windings, winding loss is inversely proportional to the squares of both flux-density sweep and operating frequency. At frequencies above f_L winding loss becomes inversely proportional to operating frequency.

Flux-Density Sweep

From the considerations given earlier, it is apparent that at lower frequencies, operating flux density is limited by core saturation rather than loss. Above some frequency f_T, the optimum operating flux-density (for maximum power) becomes less than the saturation-related maximum, and the flux-density sweep is limited by the requirement that (for Ferroxcube 3C8) core loss $P_C = 0.44\ P_{TOT}$, where P_{TOT} is the total permissible dissipation.

Throughput Power

These various effects of operating frequency are combined to explain the observed variation of SMPS transformer throughput power with operating frequency for Ferroxcube 3C8 cores. Figure 4a shows the division between core and winding loss for an SMPS transformer as a function of operating frequency. Frequencies f_L, f_T and f_1, are marked. (Note

Table 1. List of Symbols

SYMBOL	DEFINITION	UNIT
B_{ac}	Flux-density sweep; half the peak-to-peak flux density excursion	T
B_{CF}	Coil former breadth	mm
f	Operating frequency	Hz
f_1	The frequency at which the number of turns on the lowest-voltage transformer winding becomes unity	Hz
f_L	The lowest frequency at which the coil former height is sufficient to accommodate ideal (minimum-loss) windings	Hz
f_T	The frequency above which no useful increase in the throughputpower capacity of a transformer can be obtained	Hz
H_{CF}	Coil former height	mm
L	Choke inductance	H
φ_{av}	Average turn length	mm
P_c	Total transformer core loss	W
θ_C	Transformer or choke thermal resistance with winding creepage distance incorporated	°C/W
θ_N	Transformer or choke thermal resistance for a winding without creepage distance	°C/W
V_e	Effective volume of a core	m^3
a	Ratio of core saturation flux to working flux allowed: for transient response without saturation	–
ΔT	Temperature rise above ambient	°C
ϵ	Unbalance factor	–

NOTES:
subscripts
e Effective value
cp Pertains to center pole

Table 2. Maximum Values of Flux-Density Sweep for Various Converter Types and Control Circuits

BOUNDARY CONDITIONS	FLUX-DENSITY SWEEP $B_{ac\ cp}$ (T)	
	Forward	Push-Pull
Maximum sweep for FXC 3C8 (100°C)	0.16	0.32
At transient factor a	$\frac{0.32}{2a}$	$\frac{0.32}{a}$
With unbalance factor ϵ*	–	$\frac{0.32}{\epsilon a}$
With x% feed-forward	$\frac{0.32}{2\ (1 + x/100)}$	$\frac{0.32}{(1 + x/100)}$
With unbalance factor ϵ and x% feed-forward	–	$\frac{0.32}{\epsilon\ (1 + x/100)}$

NOTE:
* ϵ is the ratio of peak flux-density in a balanced converter to the peak flux-density in an unbalanced converter.

that f_L may, in fact, be higher than f_T for some cores. This does not alter the main argument.) In Region I, operating flux-density is limited by saturation considerations only, so that throughput power is roughly proportional to frequency. Operation remains saturation limited into Region II, but here power increases roughly as the root of the frequency. (This relationship is complicated by the fact that average turn length decreases as ideal winding height decreases.) Region III begins at f_T, where core operating flux-density becomes limited by core loss to the optimum value for that frequency. The shape of the throughput power curve in the region depends on core material characteristics: the Steinmetz coefficient and its associated flux-density and frequency exponents. For Ferroxcube 3C8, flux-density is inversely proportional to the root of frequency. Then, winding resistance decreases slightly with frequency so that, since winding loss is constant, throughput power is also about constant.

Region IV begins where frequency increases to the point where the number of turns required on the lowest voltage winding falls to unity. (Contours of number of turns N as a function of frequency for various voltages are indicated in Figure 4a). When this happens, flux-density must then decrease with frequency. The rate of this decrease is greater than that required for optimum core loss, so that throughput power decreases. The effect is accentuated by the increasing contribution of eddy current losses at high frequencies.

In practice, other factors, such as eddy currents, parasitic capacitance and rounding of numbers of turns, cause the transitions from one region to another to become blurred so that, as Figure 4c shows, the throughput power characteristic is more rounded. Calculated values for real cores, Figure 5, shows that the general characteristics remain; however, there is always a frequency, close to the core transition frequency, above which no useful increase in throughput power can be obtained.

EFFECT OF CORE DESIGN

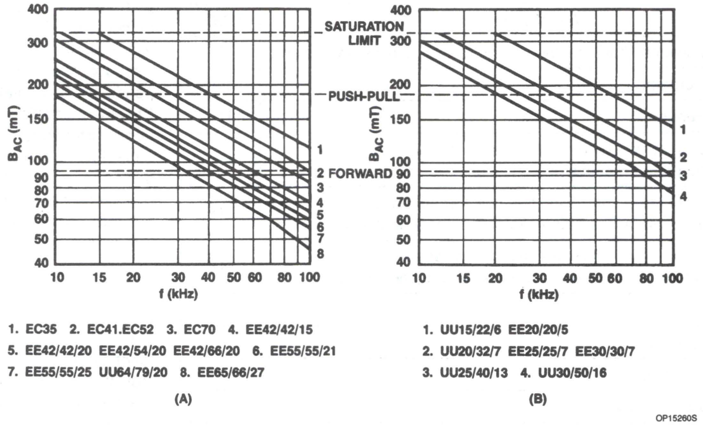
The more complete understanding of the factors that influence throughput power obtainable has made it possible to examine established core designs with a view to improving the designs available. Electrical, magnetic and mechanical considerations can now be combined so that the core can be made as effective as possible.

Existing Core Designs

Analysis of existing core designs shows that performance agrees well with values of f_T. The performance of the smaller cores is found to be relatively poor at 50kHz due to lack of sufficient winding window height for ideal windings.

The effectiveness of the use of core materials is another important consideration, since it directly affects the weight of an SMPS. Constant cross-section E cores generally have the best power-to-weight ratios.

Mechanical design is of great importance since this influences manufacturing cost and transformer production cost. The core should



NOTE:
Horizontal lines indicate the limits for various converter types ($\propto = 1.72$). The curves were calculated for a peak temperature rise of 40k.

Figure 3. Optimum, Peak, Center-Pole Flux-Density Sweeps $B_{AC\ CP}$ for a Variety of Cores for SMPS Applications

be cheap to manufacture. Enclosed cores, such as pot cores and their variants (RM, PQ, PM cores) are more expensive to make than E cores for a given power capacity. However, round center legs make for easier winding, with less leakage inductance — especially for strip. For all but the smallest transformers, E cores result in more compact design than U cores. Finally, due to their symmetry, E cores require some 20% less core material for a given power capacity than U cores, with a consequent reduction in eddy current losses. This last point is of special importance at higher operating frequencies.

Core Design Requirements

The requirements for a new core design are clear. The range of cores should be optimized for frequencies appropriate to their power handling capacity: 50kHz for 300W, 100kHz for 100W, for example. This requires proper choice of f_L and f_T. Optimization should be aimed at forward converter applications (the cores will then also be suitable for unbalanced push-pull converters).

The design of the associated coil formers is also critically important. They should be suitable for automatic handling. A large number of pins is required, both for flexibility of layout and to accommodate multiple secondaries.

The core and wound coil former should be quick and easy to assemble. The combination should be designed for horizontal mounting on PC boards to minimize height and make termination of strip windings easier.

THE ETD SYSTEM

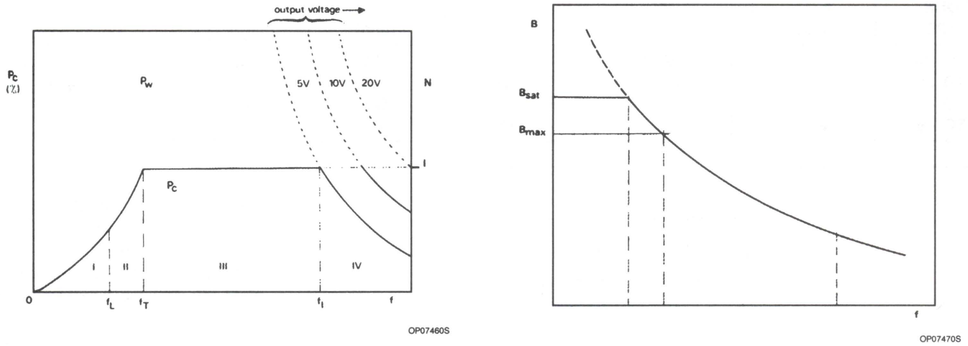
The Cores

These criteria have been adopted in the design of the ETD cores. They are constant cross-section E cores in Ferroxcube 3C8 ferrite with round center legs, photo and Figure 6, and are designed for

- Minimum throughput powers in the range 100W to 300W
- Economical manufacture
- Minimum weight of ferrite
- Operating frequencies in the range 50kHz to 150kHz
- High throughput power density
- Mains isolation
- Minimum transformer volume and PC board areas.

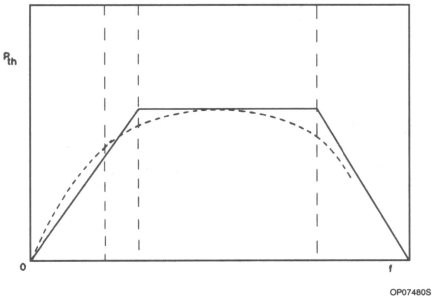
Magnetic properties are given in Table 3.

The ETD cores are compared with existing core designs for power per unit weight in Figure 7. Throughput power areas as a function of frequency for ETD cores are given in Figure 8, and the optimum flux-density sweep in Figure 9.



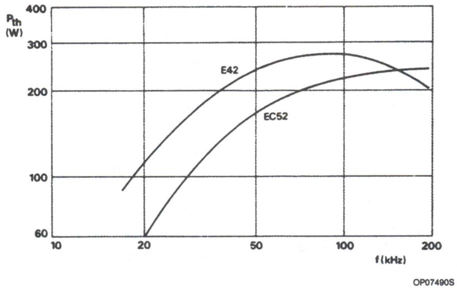
a. Division of Transformer Loss Between Core Loss and Winding Loss as a Function of Frequency Showing the Various Boundary Frequencies

b. Relation Between Flux Density and Frequency for Maximum Throughput Power



c. The Corresponding Throughput Power Characteristic

Figure 4



NOTE:
There is a frequency (from Figure 3) above which no useful increase in throughput power can be obtained. For the EC52 core this is 100kHz, for the E42 core it is 52kHz.

Figure 5. Calculated Throughput Powers (5V Forward Converters) With Frequency for EC52 and E42/21/20 Core Show the Same General Characteristics

The Coil Former and Assembly Hardware

Simple, rapid winding and assembly of ETD system-based transformers and chokes is made possible by the coil former of Figure 10, together with the associated snap-on stainless-steel assembly clips.

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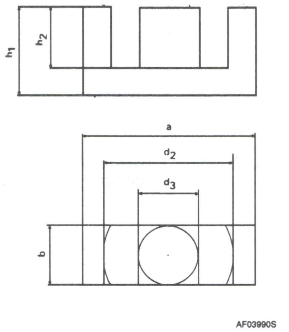
Table 3. Magnetic Dimensions of ETD System Cores

CORE TYPE	$A_{CP\ min}$ (mm^2)	A_e (mm^2)	V_e (mm^3)	φ_e (mm)
ETD 34	87	97.1	7640	78.6
ETD 39	117	125	11500	92.2
ETD 44	167	173	17800	103
ETD 49	204	211	24000	114



CORE TYPE	MID-LIMIT DIMENSIONS (mm) a	d_2	d_3	h_1	h_2	b	MASS (g) (CORE HALF)
ETD 34	34.2	26.3	10.8	17.3	12.1	10.8	20
ETD 39	39.1	30.1	12.5	19.8	14.6	12.5	30
ETD 44	44.0	33.3	14.9	22.3	16.5	14.9	47
ETD 49	48.7	37.0	16.4	24.7	18.1	16.4	62

Figure 6. Outline Drawing and Dimensions of the New ETD Core Range

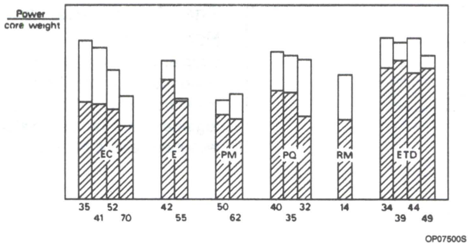


Figure 7. The Thoughput Power per Unit Weight of Core Material for ETD Cores Compared With That of Other Popular Core Types at two Operating Frequencies: 50kHz (Shaded Areas) and 100kHz (Open Areas). Forward-Converter Operation Is Assumed

Principal features of the design are indicated in Figure 10:

- The length and number of slots gives a wide choice of lead-out position
- There is at least 8mm creepage distance from the pins to the ferrite core
- The pegs between the slots allow wire to be run from any one slot or pin to any other
- The four support legs provide 8mm creepage distance between the windings and the PC board
- The hood over the pins provides 8mm creepage distance between leadouts and assembly clips
- A separate grounding clip for the core is to be available.

The coil former itself is moulded in polybutylene terephthalate, a high-grade, flame retardant (UL94-VO), thermoplastic. Windings dimensions are given in Table 4.

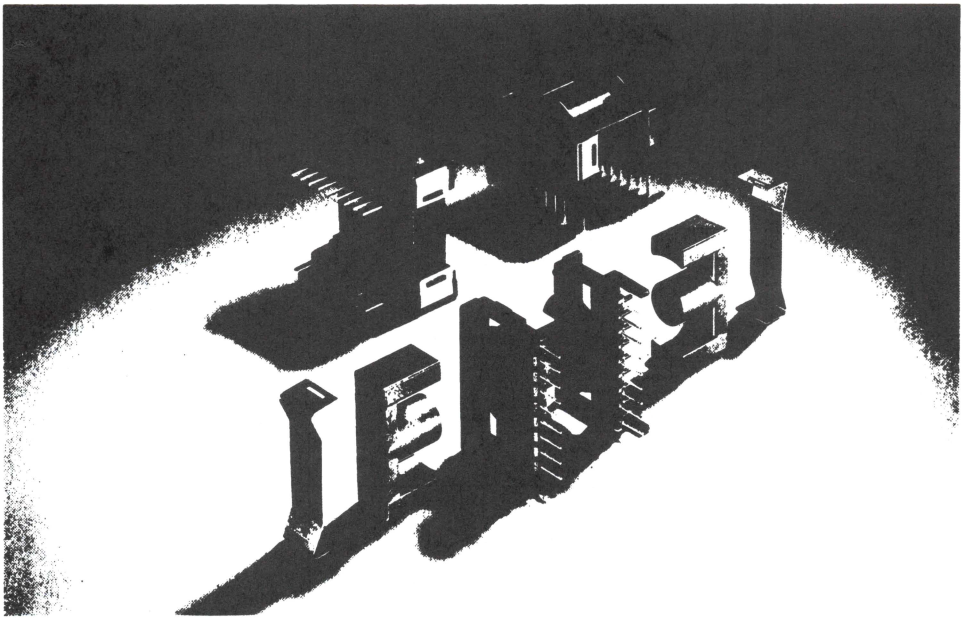
ETD system components provide OEMs with the most efficient electrical, magnetic and mechanical route to full, economical, automated production of SMPS transformers.

SWITCHED-MODE POWER SUPPLIES

The essential difference between switched-mode and conventional (mains) power supplies is operating frequency. Whereas conventional power supplies operate at mains frequencies, 50Hz or 60Hz, switched-mode power supplies (SMPS) operate at frequencies on the order of 50kHz. The complications associated with operation at these high frequencies are more than compensated for by the savings in weight and volume, especially of transformers and smoothing components.

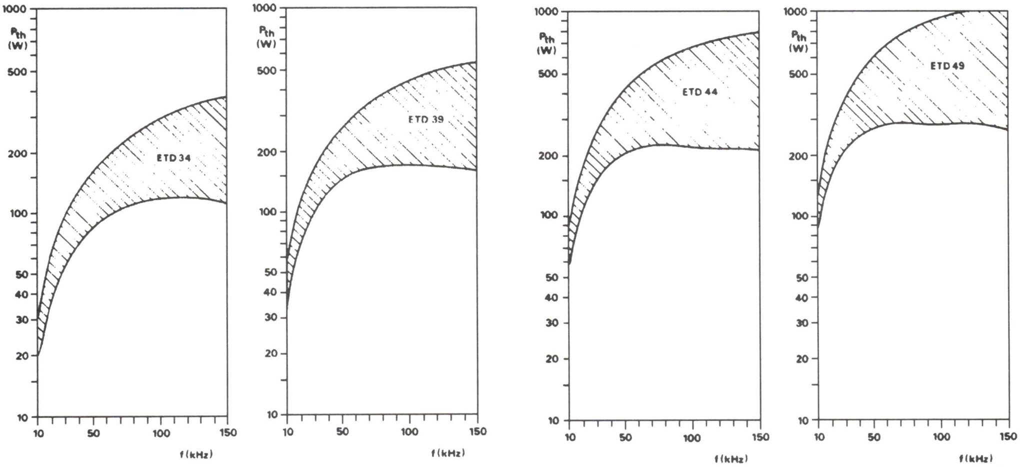
Voltage conversion and control in SMPS is achieved by chopping the incoming supply voltage with a high-speed switch such as a transistor. The chopped voltage is applied to a transformer which performs voltage conversion and provides isolation. This transformer is generally wound on a ferrite core, and is much smaller and lighter than a 50Hz unit of comparable power capacity. Fine control of output voltage is obtained by varying the duty cycle of the switch.

Most SMPS converters require a DC input and provide a DC output. For operation from the mains, therefore, a rectifier and smoothing circuit generally precedes the converter itself (Figure 11).



DF07600S

These ETD System Components Provide OEMs With the Most Efficient and Economical Route to SMPS Transformers



OP07510S

OP07520S

Figure 8. Throughput Power as a Function of Frequency for ETD Cores in Forward-Converter Transformers

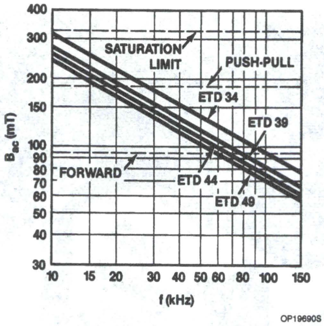


Figure 9. Optimum Flux-Density Sweeps for ETD Cores

Table 4. Winding Dimensions of ETD System Coil Formers

TYPE	B_{CF} (mm)	H_{CF} (mm)	φ_{av} (mm)
ETD 34	20.9	5.9	61
ETD 39	25.7	6.9	69
ETD 44	29.5	7.3	78
ETD 49	32.7	8.4	86

SMPS Converters

There are three basic SMPS converter arrangements; they and their variants are discussed in detail in AN1261.

In the forward converter, Figure 12, power is transferred directly to the load while the switch is closed; the energy stored in the inductor is transferred to the load while the switch is open. The switch may be transformer-coupled to the inductor for input/output isolation.

In the flyback converter, Figure 13, power is stored in the inductor while the switch is closed and transferred to the load while the switch is open. The functions of transformer and inductor may be combined where voltage transformation is required.

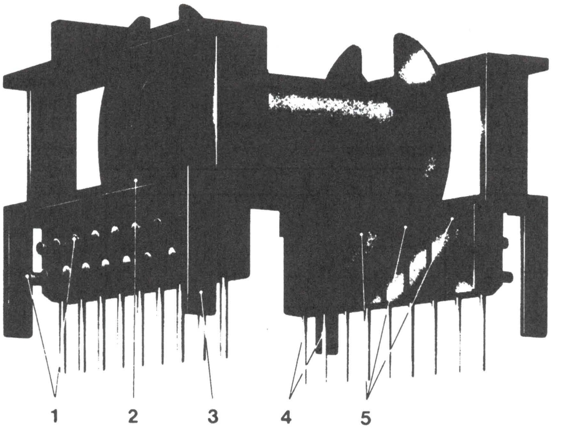
The push-pull converter is, effectively, a forward converter in which the output choke is driven by any push-pull arrangement of power transistors, including a full bridge (see Figure 14). Operation after the transformer is similar to that of a forward converter, but with twice the effective switching frequency.

Transformer and Choke Requirements

There are two main boundary conditions for the power transformer: it must not saturate (otherwise the power transistors will be damaged) and it must not overheat. In addition to these boundary conditions, the output choke should be capable of storing sufficient energy to deliver one output cycle so that ripple will be low and regulation good.

Saturation is prevented by designing for worst probable combinations of load change and input voltage fluctuation. In forward converters, provision must be made for removing energy stored in the transformer at the end of the ON period of the switch. In push-pull converters, the degree of symmetry achievable in both power switches and transformer windings determines the unbalance allowance.

Overheating of the transformer and choke is prevented by calculation of total power dissipation: core hysteresis and eddy current losses, and winding losses.



NOTES:
Pegs allow wires to be taken from most appropriate slot to chosen pin.
These plates give 8mm creepage distance between wires and assembly clips.
Legs give 8mm creepage distance from windings and PC board.
8mm creepage from pins to core.
Multiple slots for maximum freedom of lead-out position.

Figure 10. Coil Former Design for the ETD System, Intended for Automatic Winding

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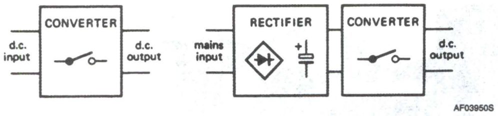
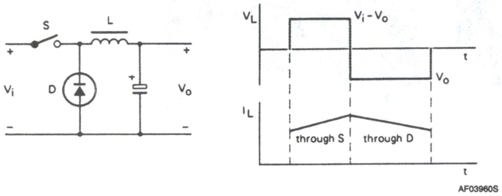

CONVERTER
d.c. input
d.c. output
mains input
RECTIFIER
CONVERTER
d.c. output
AF03950S

Figure 11. SMPS Converter


S
L
+
+
Vi
D
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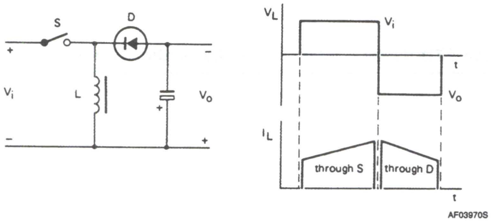
AF03960S

Figure 12. Forward Converter


S
D
+
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L
+
Vo
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+
VL
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t
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IL
through S
through D
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AF03970S

Figure 13. Flyback Converter

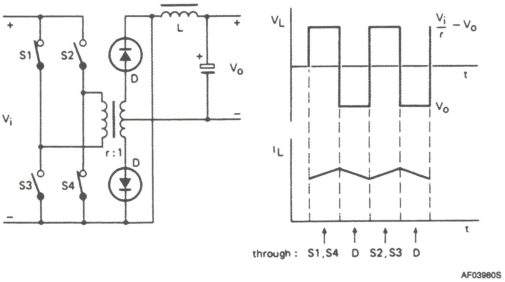
+
S1
S2
D
L
+
+
Vo
−
Vi
r:1
D
S3
S4
−
VL
Vi/r − Vo
t
Vo
IL
t
through: S1,S4 D S2,S3 D
AF03980S

Figure 14. Push-Pull Converter

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Signetics

Linear Products

AN128
Introduction to the Series-Resonant Power Supply

Application Note

Authors: E. B. G. Nijhof and H. W. Evers

There has long been a need for a smaller and more efficient alternative to the transformer/rectifier/series stabilizer circuit for deriving a constant, easily-isolated DC supply from the mains. The development of high voltage switching transistors has allowed the construction of SMPS circuits which go a long way toward meeting this need but are still far from providing the ideal answer to the problem. The main drawbacks of the SMPS, when it is supplied from the AC line, is limited efficiency due to switching losses and dissipation in dV/dt limiting RC networks, RFI due to the generation of near-rectangular current waveforms, difficult transformer design, and the need for a complex control circuit to ensure continued operation with an open-circuit or short-circuit load. A circuit that overcomes these drawbacks is the series-resonant power supply (SRPS) which incorporates an inverter in which a semiconductor switch maintains sinusoidal oscillation in a series-resonant LC network. Although the high-frequency sinusoidal currents generated in an SRPS allow it to be made compact and efficient, with far less RFI than the SMPS, its use has so far been restricted to low voltage power supplies due to the lack of a suitable low-loss, high voltage semiconductor switch.

Recently introduced GTOs (gate turn-off Thyristors described in References 1, 2 and 3) with their high VA ratings, fast switching and simple, transistor-like drive, now allow the construction of SRPS circuits which can operate from a rectified AC input and will undoubtedly replace the SMPS for controlled mains power conversion in applications such as television sets, industrial drives, fluorescent lighting systems, microwave and inductive cookers. The SRPS is also suitable for controlling the speed of DC series-wound motors in domestic appliances, and for reducing harmonic distortion in the AC supply by acting as a buffer between the AC line and a DC power supply. The main advantages of the SRPS are:

- It is a more than 90% efficient power converter.
- It causes minimal EMI/RFI because the AC input current can be made sinusoidally in phase with the AC line voltage.
- It can be built with a single, easily-designed, inductive element (transformer) which also provides line isolation.
- It continues to operate with the output short-circuit. It also continues to supply a well-stabilized output when it is not connected to a load.
- It can be made self-starting and, therefore, does not need a small transformer to supply the control circuit for the GTO.

Survey of GTOs for SRPS

TYPE NUMBER	V_{DRM} (V)	I_{TCRM} (A)	$I_{T(AV)}$ (A)	CASE
BT157	1500	10	2.2	TO-220
	1300	10	2.2	TO-220
BTW58	1500	25	6.5	TO-220
	1300	25	6.5	TO-220
	1000	25	6.5	TO-220
BTW59*	1500	50	12	TO-238
	1300	50	12	TO-238

NOTE:
* With isolated base.

PRINCIPLES OF SRPS OPERATION

Figure 1 is the basic circuit of an SRPS, the operating principle of which depends on sinusoidal alternating current generation in the $L_1C_1C_O$ circuit. For guaranteed self-oscillation, there are two conditions regarding the values of the components. The inductance of L_S must be at least ten times that of L_1, and the value of C_O must be at least twice that of C_1. The operation of the circuit will first be described without a load connected to V_O and with a very brief conduction period for the GTO. This will be followed by a description of the circuit operation under similar conditions but with a longer conduction period for the GTO. Since the behavior of the SRPS is complex (it sometimes functions as a fourth-order network), a complete analysis of the circuit is only possible with the aid of a computer. These theoretical descriptions are therefore only intended to give a basic understanding of the circuit operation and are followed by plots of the current and voltage waveforms derived by computer analysis of the basic circuit. The application note concludes with a description of ten methods of connecting a load to the SRPS.

Unloaded Circuit With Brief GTO Conduction Period

The waveforms for this mode of operation are given in Figure 2. Since $L_S \gg L_1$, and I_O is very small, the influence of L_S and I_O on the circuit behavior can be disregarded for this simplified description.

In the steady state, with the GTO turned off, C_1 is charged to V_S. Assume that the GTO is turned on for the very short time necessary to just discharge C_1. Further assume that current I_1 is negligible during this brief on-time of the GTO. When the GTO is switched off, current I_1 oscillates sinusoidally about zero at the resonant frequency of the circuit, comprising L_1 together with C_O and C_1 in series:

$$\omega = \frac{1}{\sqrt{(L_1\ C_{TOT})}}$$

where

$$C_{TOT} = \frac{C_1C_O}{C_1 + C_O}$$

The peak oscillatory current is the supply voltage divided by the impedance of the resonant circuit (Z_1),

$$\hat{I}_1 = \frac{V_S}{Z_1} = V_S\sqrt{\frac{C_{TOT}}{L_1}} \qquad (1)$$

which has an instantaneous value

$$I_1 = \frac{V_S}{Z_1}\sin\omega t$$

For stable self-oscillation of the circuit, the minimum level of V_1 must just reach zero during each cycle. The instantaneous value of V_1 is therefore given by

$$V_1 = V_S(1 - \cos\omega t)$$

$$\hat{V}_1 = 2V_S \qquad (2)$$

the AC component of which is

$$\hat{V}_{1\ AC} = V_1 - V_S = V_S$$

This voltage therefore oscillates sinusoidally between 0V and $2V_S$ and has an average value equal to the supply voltage (V_S). Since the average value of the oscillatory current I_1 must therefore be zero, it is apparent that, as is to be expected, power is not drawn from the supply when the output from the circuit is unloaded.

The ratio V_O/V_1 is determined by the ratio of the values of C_1 and C_O. The peak value of V_O is

$$\hat{V}_O = V_S + \frac{\hat{V}_1C_1}{2C_O} = V_S\frac{C_1 + C_O}{C_O}$$

the AC component of which is

$$\hat{V}_{O\ AC} = \hat{V}_O - V_S = V_S\frac{C_1}{C_O} \qquad (3)$$

Unloaded Circuit With Longer GTO Conduction Period

The waveforms for this mode of operation are given in Figure 3. If the conduction period of the GTO is made longer than that necessary to just discharge C_1, considerable current due

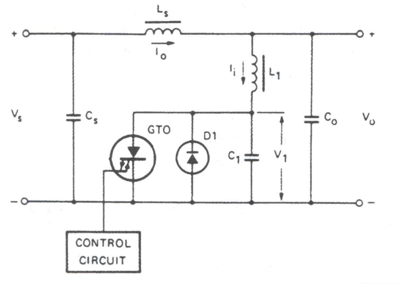


Figure 1. Basic SRPS Circuit

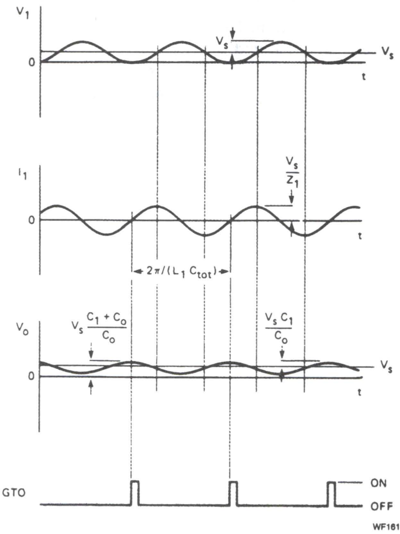


Figure 2. Waveforms of the Basic SRPS for the Shortest Possible Conduction Time for the GTO

to I_O and the discharge of C_O is flowing in L_1 at the turn-off instant. This value of I_1 will be denoted I_{OFF}. The peak oscillatory current V_S/Z_1 from equation (1) will now increase, in proportion to the ratio I_{OFF} to V_S/Z_1, by a factor

$$M = \sqrt{\left[\left(\frac{I_{OFF}Z_I}{V_S}\right)^2 + 1\right]}$$

The peak current through L_1 will therefore be

$$\hat{I}_1 = \frac{MV_S}{Z_1} \qquad (4)$$

The peak voltage across C_1 in Equation 2 was V_S above its average value V_S. The rise of V_1 above V_S will now increase by the multiplying factor M, which gives

$$\hat{V}_1 = V_S + MV_S = V_S(M + 1) \qquad (5)$$

the AC component of which is

$$\hat{V}_{1\ AC} = MV_S$$

Solving Equation 5 for the maximum multiplying factor in terms of the supply voltage and the maximum allowable peak voltage across the GTO gives

$$M_{MAX} = \frac{\hat{V}_1}{V_S} - 1 \qquad (6)$$

The AC component of the output voltage is $\hat{V}_{1\ AC}$ multiplied by the ratio C_1/C_O, which gives

$$\hat{V}_{O\ AC} = \frac{\hat{V}_{1\ AC}\ C_1}{C_O} = \frac{MV_S\ C_1}{C_O} \qquad (7)$$

Voltage Control Range of the Basic SRPS

Assuming that V_S is the rectified line voltage (300V) and that the maximum peak voltage permitted across the GTO (V_1) is 1200V, then from Equation 6 the maximum multiplying factor is 3 and, from Equation 4, the maximum peak current through L_1 is

$$\hat{I}_1 = \frac{3V_S}{Z_1} \qquad (8)$$

Comparing Equations 1 and 8 shows that the peak current through L_1 increases threefold when the conduction period of the GTO is increased to the maximum allowed by the permitted peak voltage across the GTO (V_1). Comparing Equations 2 and 5 shows that, with M = 3, the peak voltage across the GTO increases from $2V_S = 600V$ to $4V_S = 1200V$ when the conduction period of the GTO is changed from minimum to maximum. Comparing Equations 3 and 7 shows that, with $C_1/C_O = 0.5$, the control range for the AC component of V_O is

$$V_{O\ AC}\ \text{min} = 0.5\ V_S = 150\ V$$

$$V_{O\ AC}\ \text{max} = 1.5\ V_S = 450\ V$$

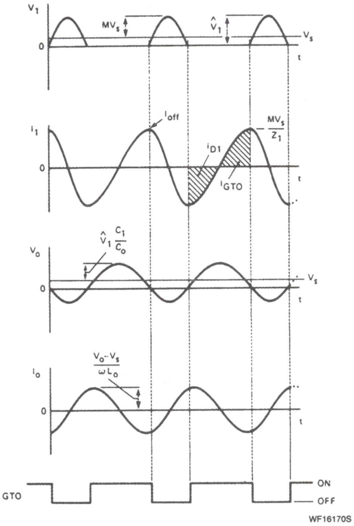


Figure 3. Waveforms for the Longest Possible Conduction Time for the GTO and V_1 = 1200V max, V_S = 300V, C_1 = 10nF, C_O = 22nF, L_O = 10mH, L_1 = 1mH, M = 3

The circuit can therefore be used as a power converter with its output voltage controllable over a 3:1 range by varying the conduction period of the GTO.

Alternatively, for a lower supply voltage such as $V_S = 100V$, and the same maximum peak voltage $V_1 = 1200V$, the maximum multiplying factor from Equation 6 is 11. Solving Equation 2 and 5 for V_S shows that the variation of supply voltage (V_S) that can be compensated by variation of the conduction period of the GTO is:

$$V_{S\ min} = \frac{\hat{V}_1}{M + 1} = 100V$$

$$V_{S\ max} = \frac{\hat{V}_1}{2} = 600V$$

The SRPS output voltage can therefore be stabilized against a 6:1 DC supply voltage variation by varying the conduction period of the GTO.

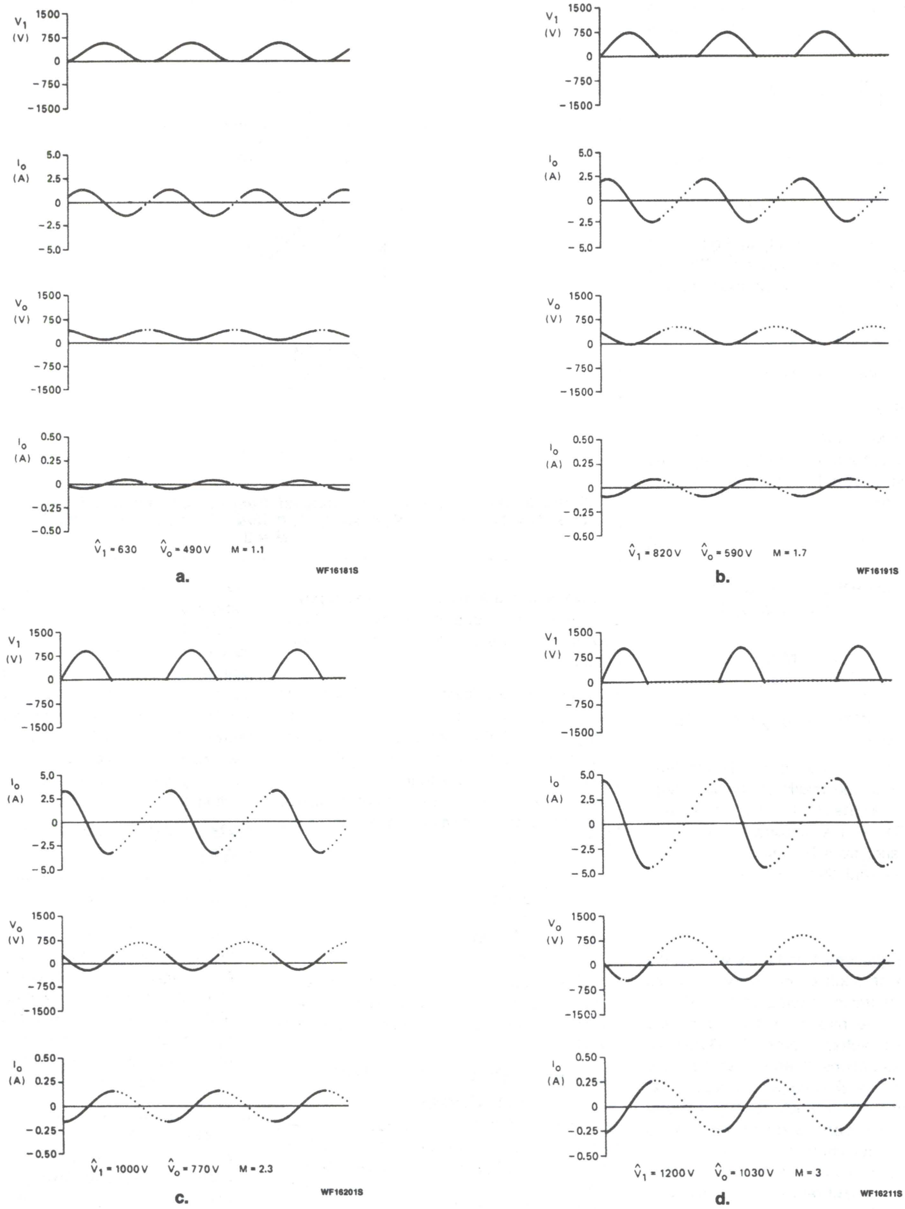
Computer Plot of the SRPS Voltage and Currents

As shown in Figure 4, a computer program has been used to plot the exact time functions for I_O, I_1, V_O and V_1 with $V_S = 300V_{DC}$ and components values $L_S = 10mH$, $L_1 = 1mH$, $C_O = 20nF$ and $C_1 = 10nF$. The computer plots have been made for peak values of V_O of 490V, 590V, 770V and 1030V. Subtracting $V_S = 300V$ from these figures gives the AC component of V_O, which is about 190V, 290V, 470V and 720V, respectively. This shows that the available output voltage control range for $V_S = 300V$ and V_1 max. = 1200V is at least 3.8:1 instead of 3:1 as calculated in Equations 3 and 7. This is due to the fact that the voltages across the capacitors in the oscillatory circuit are almost 180° out of phase so that the voltage division between them is not directly proportional to their values. The plots also indicate that the operating frequency decreases as the conducting time of the GTO is increased.

Extracting Power From the SRPS

There are three basic methods of extracting power from the SRPS. They are:

1. From capacitor C_O, via a diode, to an output electrolytic capacitor. Since the output voltage $V_{O\ AC}$ is superimposed on the input DC level V_S, the voltage across the electrolytic capacitor will always exceed V_S. The circuit is therefore an up-converter and its main use is as a buffer between the AC line and a DC power supply unit.
2. From capacitor C_O via a capacitor which blocks the DC component of V_O so that pure AC is available at the output. This circuit is suitable for driving resistive loads and fluorescent lighting tubes. If the output from the blocking capacitor is rectified in a voltage doubler circuit, this type of SRPS is suitable for controlling the speed of a series-wound DC motor.



a. b. c. d.

NOTE:
The dotted sections are the conduction period of the GTO, which is the maximum allowed by the V_1 specification.

Figure 4. Computer Plots of the Waveforms in the Circuit of Figure 1 With $V_S = 300V_{DC}$, $L_O = 10mH$, $L_1 = 1mH$, $C_O = 20nF$, $C_1 = 10nF$

Introduction to the Series-Resonant Power Supply AN128

3. By replacing inductor L_S with a transformer. This arrangement gives the best performance because it gives very good line isolation and the load can be correctly matched to the SRPS by adjustment of the turns ratio of the transformer. This type of circuit can drive resistive or rectifier loads and can also be used as a supply for fluorescent tubes. For rectifier loads, however, the leakage inductance of the transformer must be made very low; for example, by using sandwiched windings. The final part of this application note shows how inductor L_1 can be integrated with the transformer to overcome this problem and create an SRPS with a single inductive component.

PRACTICAL SRPS CIRCUITS WITHOUT POWER LINE ISOLATION

Direct-Coupled SRPS Up-Converter

The circuit of this type of SRPS is given in Figure 5. Diode D_O half-wave rectifies V_O and feeds the resultant half-sinewaves to output electrolytic C_O. Since the average value of V_O is V_S, the rectified half-sinewaves at the output are superimposed on the DC input voltage and the DC output voltage must necessarily exceed this level. The circuit is therefore an up-converter. The percentage of the total output power which has to be converted by the series-resonant circuit is $(V_O-V_S)/V_O$. For $V_S = 200V$ (average voltage of full-wave rectified 220V mains) and $V_{O\ AC} = 500V$, this amounts to only 60% of the total output power. This, together with the inherent high efficiency of the SRPS (about 95% at $V_S = 200V_{DC}$), allows the circuit to feed some current to the load, even when the input voltage is as low as 10% of the output voltage. For $V_{O\ AC} = 500V$ to 600V, the full-wave rectified AC input need not therefore be smoothed and can be obtained directly from a bridge rectifier followed by a low value decoupling capacitor (a few μF). This arrangement results in an SRPS up-converter with a well-stabilized DC output with a low level of superimposed 100Hz ripple. Since the AC current flowing via the bridge rectifier without a high value smoothing capacitor is sinusoidal, the circuit can convert unlimited power without exceeding the limits of power line harmonic generation specified for domestic equipment in CENELEC specification EN 50 006.

The foregoing considerations indicate that the main use for this type of SRPS is for reducing power line distortion by acting as a buffer between the AC supply and a 500V to 600V DC power supply of more than 500W.

Capacitively-Coupled SRPS Circuits

In capacitively-coupled SRPS circuits, the DC component of voltage V_O is blocked by a capacitor between C_O and the output rectifier. The circuit is given in Figure 6 which shows three methods of rectifying the AC component V_O.

Circuit 1. In Circuit 1 of Figure 6, the AC component of V_O is rectified in a voltage doubler circuit that applies a positive DC voltage to the load. Like the previously described up-converter, this circuit works best with a DC output of more than 500V, but has the added advantage of being immune to output short-circuits. The main use of Circuit 1 is speed control of a series DC motor connected as shown in Figure 7. Since inductor L_S has now been replaced by the series-connected armature and field windings of the motor, the SRPS has an effective input voltage of V_S minus the back EMF. Since the back EMF is proportional to the current through the motor at a given speed, it is not necessary to use a high value capacitor to smooth the rectified mains input. The current flowing in the 50Hz mains can therefore be made sinusoidal so that mains pollution is minimal. The range of back EMF must not exceed about 75% of supply voltage V_S so that the SRPS can still supply a reasonable amount of current when the motor is running at full speed.

Circuit 2. Circuit 2 of Figure 6 is similar to Circuit 1 except that the output rectifier/voltage doubler is connected to provide a negative DC output voltage. The possible uses for this circuit are few.

Circuit 3. Circuit 3 of Figure 6 is again similar to Circuits 1 and 2 except that the output is bridge-rectified. Since the bridge rectifier provides half the average output voltage of a voltage doubler rectifier, the minimum peak value for the DC output can be reduced to about 250V. A disadvantage of the circuit, however, is that the output is floating with respect to the return line of the input voltage.

SRPS CIRCUITS WITH POWER LINE ISOLATION

Since capacitor C_{IN} has a much higher value than C_O, C_O is effectively in parallel with L_S so that V_O appears across this inductor. If line isolation is required, L_S can therefore be replaced by a transformer with output rectifier connected to the secondary winding (Figure 8). The manner in which the rectifier and transformer are connected then determines the mode of operation; i.e., power transferred to the load

- when the current in the primary winding of the transformer is positive (forward mode, Circuit 1)
- when the current in the primary is negative (flyback mode, Circuit 2)
- when the current in the primary is positive and when it is negative (forward flyback mode, Circuit 3).

In Circuit 3, a bridge rectifier can also be used with an untapped secondary winding.

In addition to driving rectifier loads via a transformer with low leakage inductance, these circuits with transformer-coupled output are also suitable for driving a resistive load or a load that behaves like a voltage source, for example, a fluorescent lamp or a magnetron in a microwave cooker. The best performance is obtained with a DC output of about 300V.

SRPS With a Single Inductive Component (Transformer)

In the circuits shown in Figure 8, inductor L_1 is rather bulky because, at operating frequencies of about 50kHz, the flux swing in the core is quite large. It is therefore necessary to use a large core to prevent saturation and consequent overheating due to hysteresis losses. The core heating problem can be completely overcome by constructing the output transformer in such a manner that L_S is formed by

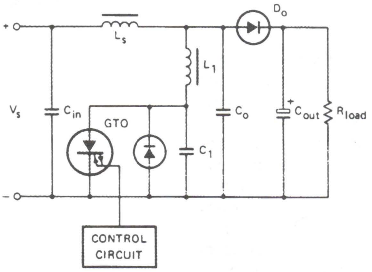


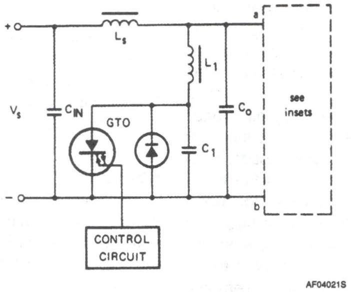
Figure 5. SRPS Up-Converter

the primary self-inductance and magnetizing inductance of the transformer, and L_1 is formed by the primary and secondary leakage inductances. The flux swing of the transformer core is then quite small and the hysteresis losses are low.

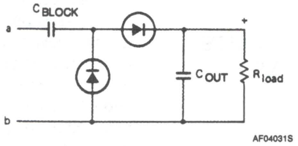
Figure 9 shows how inductor L_1 can be integrated with the output transformer. First, since C_{IN} is a much higher value than C_O, C_O is effectively in parallel with the primary winding of the transformer and can therefore be connected in this position. Second, if the value of C_O is multiplied by the square of the turns-ratio of the transformer, it can be connected in parallel with the secondary winding. Finally, since there is now no connection to the junction of L_S and L_1, L_1 can be integrated with the output transformer. This final step is clarified by the equivalent T-circuit of the transformer given in Figure 10. Since a requirement for guaranteed self-oscillation of the SRPS is that the value of L_S is at least ten times that of L_1, the minimum coefficient of coupling for the transformer is $\geqslant 0.8$. A transformer with sufficient leakage inductance can easily be constructed on a pair of ferroxcube U-cores with the primary wound round one pole and the secondary wound round the other. If the external magnetic field with this type of construction is too great (for example, in a television receiver), the primary and secondary windings can be stacked on the gapped center pole of a pair of E-cores. Experiments have shown that when this type of transformer is installed in a working SRPS and positioned within 4cm of the deflection coils of a 26-inch CTV set with a 30AX deflection system, there is no perceptible distortion of the raster. If the transformer is positioned within 4cm of the most sensitive part of the tube (cathode, grid 1 and 2 area), the maximum distortion of the raster is 1mm.

An important advantage of the SRPS with a single inductive element is that it is inherently immune to a short-circuited output. It is therefore self-starting, even with 0V across the output capacitor, so it is not necessary to use a separate transformer to provide a supply for the GTO control circuit.

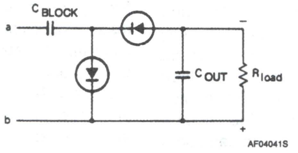
The single-transformer SRPS can be used in any of the modes of operation illustrated in Figure 8 and can provide controlled power for all the previously mentioned types of load. Because the design of SRPS circuits is complex, we have calculated the time functions for the variables V_O, V_I, I_O and I_I and used them in a closed-loop computer program to calculate the steady-state conditions for any set of input conditions. The computer program has also been used to construct a set of five universally-applicable graphs as a design aid for SRPS circuits.



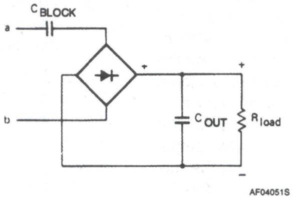
a. General Circuit



b. Circuit 1



c. Circuit 2



d. Circuit 3

Figure 6. SRPS Circuits With Capacitively-Coupled Output

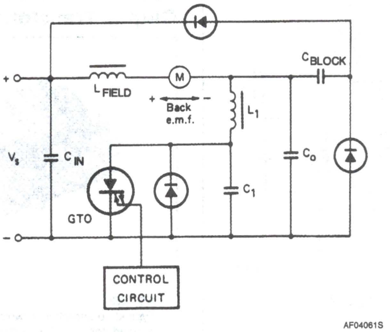
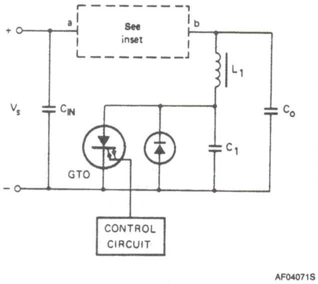
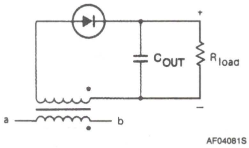

+
−
V_s
C_{IN}
GTO
L_{FIELD}
M
+ Back e.m.f. −
L_1
C_1
C_{BLOCK}
C_o
CONTROL CIRCUIT
AF04061S

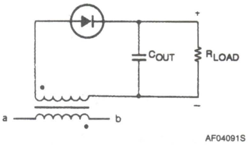
Figure 7. SRPS With Capacitively-Coupled Output Controlling the Speed of a DC Series-Wound Motor


+
−
a
b
See inset
V_s
C_{IN}
GTO
L_1
C_1
C_o
CONTROL CIRCUIT
AF04071S

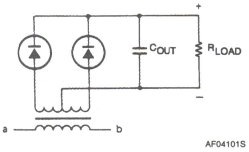
a. General Circuit


+
−
C_{OUT}
R_{load}
a
b
AF04081S

b. Circuit 1 — Forward

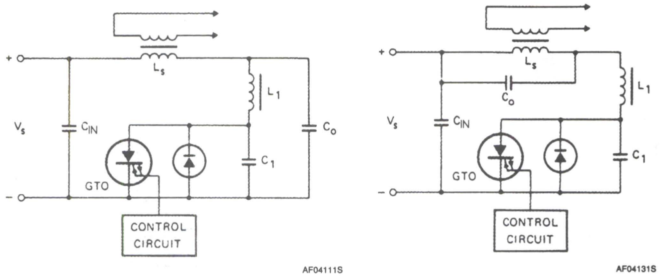

+
−
C_{OUT}
R_{LOAD}
a
b
AF04091S

c. Circuit 2 — I^2 Flyback


+
−
C_{OUT}
R_{LOAD}
a
b
AF04101S

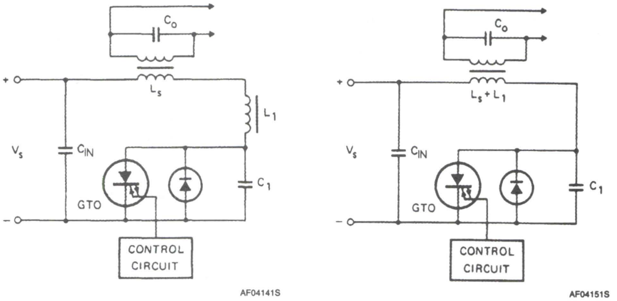
d. Circuit 3 — Forward/Flyback

Figure 8. SRPS Circuits With Transformer-Coupled Output


+
−
V_s
C_{IN}
GTO
L_s
L_1
C_o
C_1
CONTROL CIRCUIT
AF04111S
AF04131S

a. Original Circuit

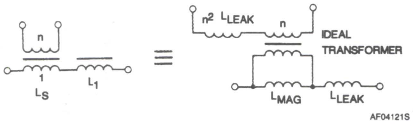
b. Stage 1


+
−
V_s
C_{IN}
GTO
L_s
L_1
$L_s + L_1$
C_o
C_1
CONTROL CIRCUIT
AF04141S
AF04151S

c. Stage 2

d. Stage 3

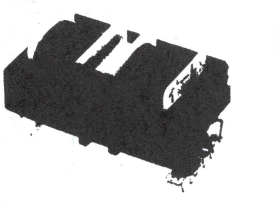
Figure 9. The Three Stages of Integrating Inductor L_1 With the Output Transformer of an SRPS


n
1
L_S
L_1
≡
$n^2 L_{LEAK}$
n
IDEAL TRANSFORMER
L_{MAG}
L_{LEAK}
AF04121S

NOTES:
Approximate Relations in the Equivalent Circuit ($L_S \geq 10L_1$)
$L_1 = 2L_{leak}$
$L_S = L_{mag}$

Figure 10. Transformer Equivalent T-Circuit With Ideal Transformation

Power Line Isolated SRPS Output Transformer



NOTES:
Typical construction in which the leakage inductance is used for L_S. This transformer is for a 150W to 200W power supply operating at a frequency of 30–40kHz

REFERENCES

1. Burgum, F. J., Nijhof, E. B. G. and Woodworth, A., *"Gate turn-off switch," Electronic Components and Applications*, Vol. 2, No. 4, August 1980.
2. Woodworth, A., *"Understanding GTO data as an aid to circuit design," Electronic Components and Applications*, Vol. 3, No. 3, May 1981.
3. Burgum, F. J., *"Basic GTO drive circuits," Electronic Components and Applications*, Vol. 3, No. 4, August 1981.

Signetics

TDA1023
Time-Proportional Triac Trigger

Product Specification

Linear Products

DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in the time-proportional or burst firing mode. It permits very precise temperature control of heating equipment and is especially suited to the control of panel heaters. The circuit generates positive-going trigger pulses and complies with the regulations on radio interference and mains distortion.

FEATURES

- **Adjustable proportional range width**
- **Adjustable hysteresis**
- **Adjustable trigger pulse width**
- **Adjustable firing burst repetition time**
- **Control range translation facility**
- **Failsafe operation**
- **Supplied from the mains**
- **Provides supply for external temperature bridge**

APPLICATIONS

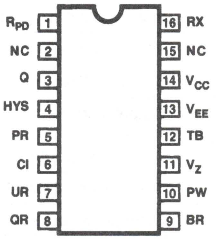
- **Triac control**
- **Temperature control**
- **Panel heater control**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−20°C to +75°C	TDA1023N

PIN CONFIGURATION

N Package



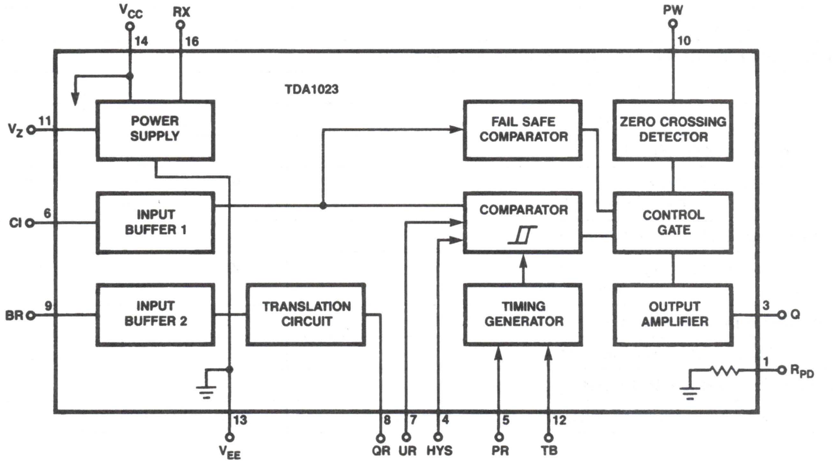
R_{PD} 1
NC 2
Q 3
HYS 4
PR 5
CI 6
UR 7
QR 8
16 RX
15 NC
14 V_{CC}
13 V_{EE}
12 TB
11 V_Z
10 PW
9 BR

TOP VIEW

CD10811S

PIN NO.	SYMBOL	DESCRIPTION
1	R_{PD}	Internal pull-down resistor connection
2	NC	Not connected
3	O	Output
4	HYS	Hysteresis control input
5	PR	Proportional range control input
6	CI	Control input
7	UR	Unbuffered reference input
8	OR	Output of reference buffer
9	BR	Buffered reference input
10	PW	Pulse width control input
11	V_Z	Reference supply output
12	TB	Firing burst repetition time control input
13	V_{EE}	Ground connection
14	V_{CC}	Positive supply connection
15	NC	Not connected
16	RX	External resistor connection

BLOCK DIAGRAM



V_{CC}
RX
14
16
PW
10
TDA1023
V_Z 11
POWER SUPPLY
FAIL SAFE COMPARATOR
ZERO CROSSING DETECTOR
CI 6
INPUT BUFFER 1
COMPARATOR
CONTROL GATE
BR 9
INPUT BUFFER 2
TRANSLATION CIRCUIT
TIMING GENERATOR
OUTPUT AMPLIFIER
3 Q
1 R_{PD}
13
V_{EE}
8 QR
7 UR
4 HYS
5 PR
12 TB

BD07390S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage, DC	16	V
 $I_{16(AV)}$ $I_{16(RM)}$ $I_{16(SM)}$	Supply current average repetitive peak non-repetitive peak	 30 100 2	 mA mA A
V_I	Input voltage, all inputs	16	V
$I_{6;\,7;\,9;\,10}$	Input current, CI, UR, BR, PW input	10	mA
V	Voltage on R_{PD} connection (Pin 1)	16	V
$V_{3;\,8;\,11}$	Output voltage, Q, QR, V_Z output	16	V
 $-I_{OH(AV)}$ $-I_{OH(M)}$	Output current average peak, max. 300 μs	 30 700	 mA mA
P_{TOT}	Total power dissipation	500	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +75	°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 11$ to 16V; $T_A = -20°C$ to $+75°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply: V_{CC} and RX (Pins 14 and 16)					
 V_{CC} $\Delta V_{CC}/\Delta I_{16}$	Internally stabilized supply voltage at $I_{16} = 10mA$ Variation with I_{16}	 12	 13.7 30	 15	 V mV/mA
  I_{16} I_{16}	Supply current at $V_{16-13} = 11$ to 16V; $I_{10} = 1mA$; f = 50Hz; Pin 11 open; $V_{6-13} > V_{7-13}$; Pins 4 and 5 open Pins 4 and 5 grounded			 6 7.1	 mA mA
Reference supply output V_Z for external temperature bridge 0(Pin 11)					
V_{11-13}	Output voltage		8		V
$-I_{11}$	Output current			1	mA
Control and reference inputs CI, BR, and UR (Pins 6, 9, and 7)					
V_{6-13}	Input voltage to inhibit the output		7.6		V
$I_{6;\,7;\,9}$	Input current at $V_I = 4V$			2	μA
Hysteresis control input HYS (Pin 4)					
ΔV_6 ΔV_6	Hysteresis, Pin 4 open Pin 4 grounded	9	20 320	40	mV mV
Proportional range control input PR (Pin 5)					
ΔV_6 ΔV_6	Proportional range, Pin 5 open Pin 5 grounded	50	80 400	130	mV mV
Pulse width control input PW (Pin 10)					
t_W	Pulse width at $I_{10(RMS)} = 1mA$; f = 50Hz	100	200	300	μs
Firing burst repetition time control input t_B (Pin 12)					
t_B/C_T	Firing burst repetition time, ratio to capacitor C_T	320	600	960	ms/μF

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 11$ to 16V; $T_A = -20°C$ to $+75°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Output of reference buffer QR (Pin 8)					
	Output voltage				
V_{8-13}	at input voltage $V_{9-13} = 1.6V$		3.2		V
V_{8-13}	$V_{9-13} = 4.8V$		4.8		V
V_{8-13}	$V_{9-13} = 8V$		6.4		V
Output Q (Pin 3)					
V_{OH}	Output voltage HIGH at $-I_{OH} = 150mA$	10			V
$-I_{OH}$	Output current HIGH			150	mA
Internal pull-down resistor R_{PD} (Pin 1)					
R_{PD}	Resistance to V_{EE}	1	1.5	3	kΩ

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes RF interference and transients on the mains supply. The trigger pulses come in bursts, with the net effect that the load is periodically switched on and off. This further minimizes mains pollution. The average power in the load is varied by varying the duration of the trigger pulse burst in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power Supply: V_{CC}, RX and V_Z (Pins 14, 16, and 11)

The TDA1023 is supplied from the AC mains via resistor R_D to the RX connection (Pin 16), while the V_{EE} connection (Pin 13) is connected to the neutral line (see Figure 5). A smoothing capacitor C_S has to be connected between the V_{CC} and V_{EE} connections.

The circuit contains a string of stabilizer diodes between the RX and V_{EE} connections that limit the DC supply voltage and a rectifier diode between the RX and V_{CC} connections (see Figure 1).

At Pin 11 the device provides a stabilized reference voltage V_Z for an external temperature sensing bridge.

The operation of the supply arrangement is as follows. During the positive half of the mains cycles the current through external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX reaches the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1023 itself plus the average output current $I_{3(AV)}$ plus the current required from the V_Z connection for an external temperature bridge, and recharge the smoothing capacitor C_S (see Figures 7 to 10). Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles, external smoothing capacitor C_S has to supply the sum of the currents mentioned above. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

Dissipation in resistor R_D is halved by connecting a diode in series (see Figures 2 and 7 to 10).

A further reduction of dissipation is possible by using a high-quality voltage dropping capacitor C_D in series with a resistor R_{SD} (see Figures 2 and 12). A suitable VDR connected across the mains provides protection of the TDA1023 and of the triac against mains-borne transients.

Control and Reference Inputs CI, BR and UR (Pins 6, 9, and 7)

For room temperature control (5°C to 30°C) the best performance is obtained by using the translation circuit. The buffered reference input BR (Pin 9) is used as a reference input, and the output of the reference buffer QR (Pin 8) is connected to the unbuffered reference input UR (Pin 7). In this arrangement, the translation circuit ensures that most of the potentiometer rotation can be used to cover the room temperature range. This provides an accurate temperature setting and a linear temperature scale.

If the translation circuit is not required, the unbuffered reference input UR (Pin 7) is used as a reference input. The buffered reference input BR (Pin 9) must be connected to the reference supply output V_Z (Pin 11).

For proportional power control the unbuffered reference input UR (Pin 7) must be connected to the firing burst repetition time control input TB (Pin 12), and the buffered reference input BR (Pin 9), which is inactive now, must be connected to the reference supply output V_Z (Pin 11).

In all arrangements, the train of output pulses becomes longer when the voltage at the control input CI (Pin 6) becomes lower.

Proportional Range Control Input PR (Pin 5)

With the proportional range control input PR open, the output duty factor changes from 0% to 100% by a variation of 80mV at the control input CI (Pin 6). For temperature control, this corresponds with a temperature difference of only 1k.

This range may be increased to 400mV, i.e., 5k, by connecting the proportional range control input PR (Pin 5) to ground. Intermediate values are obtained by connecting the PR input to ground via a resistor R5 (see Table 1).

Hysteresis Control Input HYS (Pin 4)

With the hysteresis control input HYS (Pin 4) open, the device has a built-in hysteresis of 20mV. For temperature control this corresponds with 0.25k.

Hysteresis is increased to 320mV, corresponding with 4k, by grounding HYS (Pin 4). Intermediate values are obtained by connecting Pin 4 to ground via a resistor R4. See Table 1 for a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger Pulse Width Control Input PW (Pin 10)

The trigger pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the trigger pulse width control input PW (Pin 10) and the AC mains.

The pulse width is inversely proportional to the input current (see Figure 11).

Output Q (Pin 3)

Since the circuit has an open-emitter output, it is capable of sourcing current; i.e., supplying a current out of the output. Therefore, it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 150mA and the output pulses are stabilized at 10V for output currents up to that value.

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figures 3 to 6). This minimizes the total supply current and the power dissipation.

Pull-Down Resistor R_{PD} (Pin 1)

The TDA1023 includes a 1.5kΩ pull-down resistor R_{PD} between Pins 1 and 13 (V_{EE}, ground connection), intended for use with sensitive triacs.

Table 1. Adjustment of Proportional Range and Hysteresis. Combinations of Resistor Values Giving Hysteresis > 1/4 Proportional Range

PROPORTIONAL RANGE (mV)	PROPORTIONAL RANGE RESISTOR R5 (kΩ)	MINIMUM HYSTERESIS (mV)	MAXIMUM HYSTERESIS RESISTOR R4 (kΩ)
80	Open	20	Open
160	3.3	40	9.1
240	1.1	60	4.3
320	0.43	80	2.7
400	0	100	1.8

Table 2. Timing Capacitor C_T Values (Electrolytic Capacitors)

EFFECTIVE DC VALUE (μF)	MARKED AC SPECIFICATION	
	μF	V
68	47	25
47	33	40
33	22	25
22	15	40
15	10	25
10	6.8	40

Time-Proportional Triac Trigger TDA1023

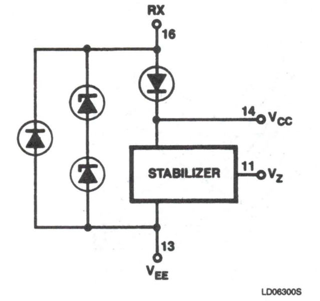

RX
16
14
VCC
STABILIZER
11
VZ
13
VEE
LD06300S

Figure 1. Internal Supply Connections

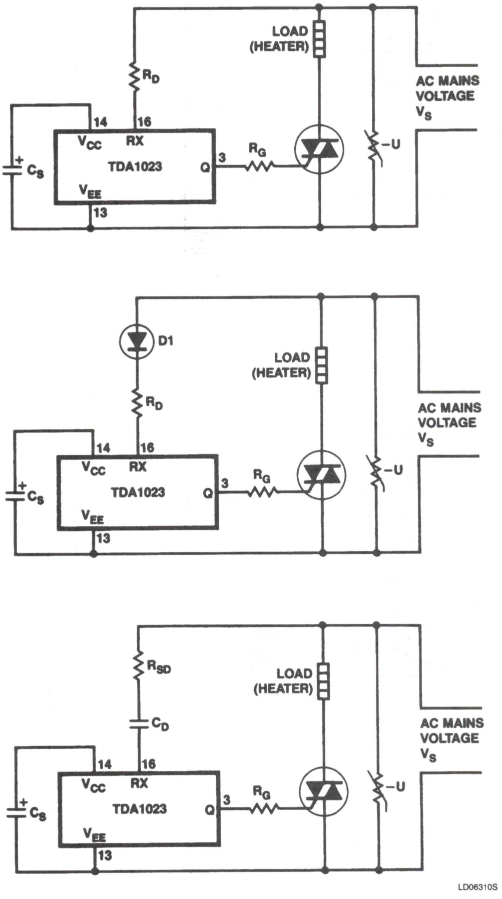

LOAD (HEATER)
RD
D1
RSD
CD
AC MAINS VOLTAGE VS
14
16
VCC
RX
TDA1023
Q
3
RG
VEE
13
CS
–U
LD06310S

Figure 2. Alternative Supply Arrangements

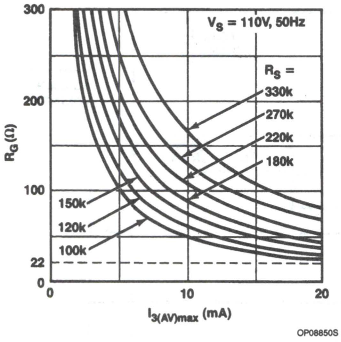


Figure 3

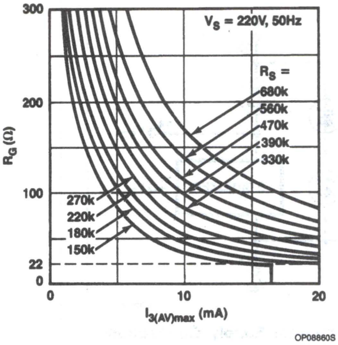


Figure 4

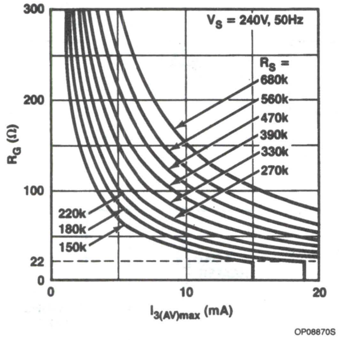


Figure 5

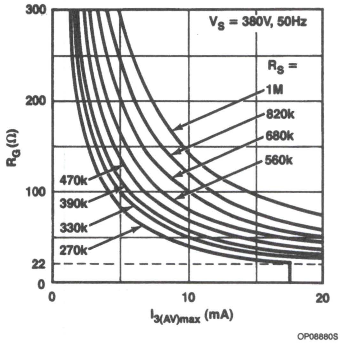


Figure 6

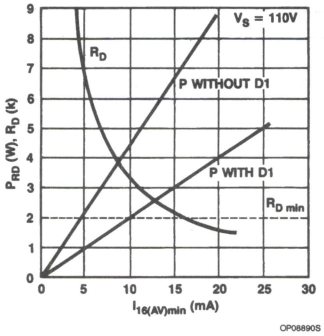


Figure 7

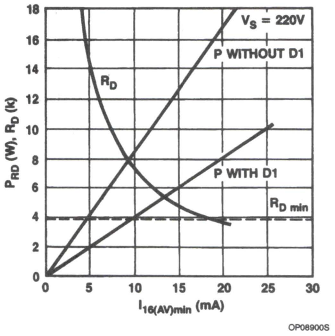


Figure 8

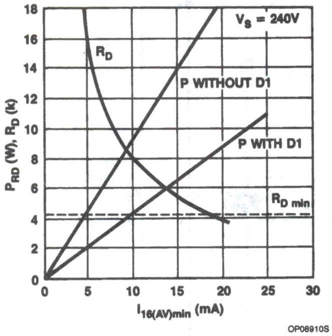


Figure 9

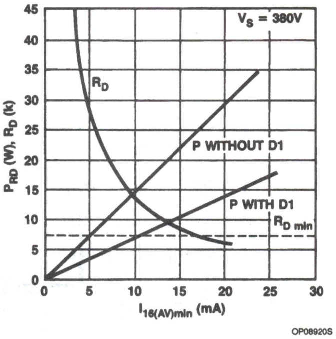


Figure 10

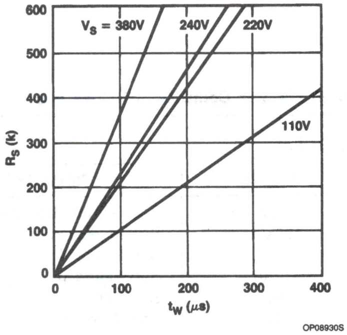


Figure 11

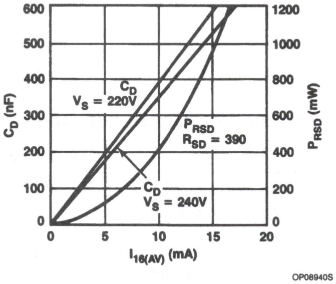
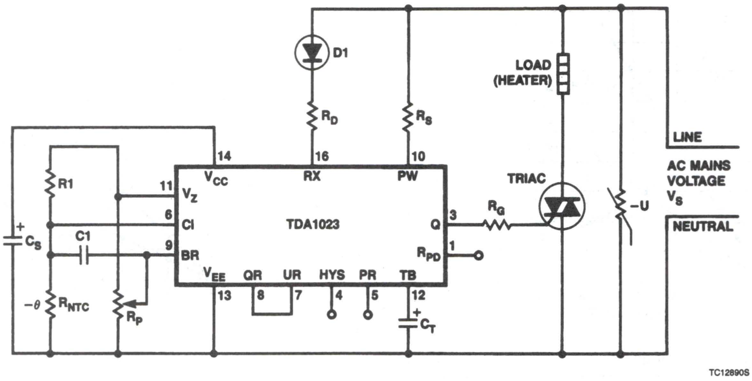


Figure 12. Nominal Value of Voltage Dropping Capacitor C_D and Power P_{RSD} Dissipated in Voltage Dropping Resistor R_{SD} as a Function of the Average Supply Current $I_{16(AV)}$ with the Mains Supply Voltage V_S as a Parameter


D1
R_D
R_S
LOAD (HEATER)
LINE
AC MAINS VOLTAGE V_S
NEUTRAL
TRIAC
R_G
−U
14
16
10
V_{CC}
RX
PW
11
V_Z
6
CI
9
BR
TDA1023
3
Q
1
R_{PD}
V_{EE}
QR
UR
HYS
PR
TB
13
8
7
4
5
12
R1
+
C_S
C1
−θ
R_{NTC}
R_P
+
C_T
TC12890S

NOTE:
Mains supply: $V_S = 220V$
Temperature range = 5 to 30°C

BT139 data: $V_{GT} < 1.5V$, $I_{GT} > 70mA$, $I_L < 60mA$ } at $T_J = 25°C$

Figure 13. The TDA1023 Used in a 1200 to 2000W Heater With Triac BT139. For Component Values see Table 3

Table 3. Temperature Controller Component Values (see Figure 13)

SYMBOL	PARAMETER	VALUE	REMARKS
t_W	Trigger pulse width	75μs	See BT139 data sheet
R_S	Synchronization resistor	180kΩ	See Figure 11
R_G	Gate resistor	110Ω	See Figure 4
$I_{3(AV)}$	Maximum average gate current	4.1mA	See Figure 6
R4	Hysteresis resistor	NC	See Table 1
R5	Proportional band resistor	NC	See Table 1
$I_{16(AV)}$	Minimum required supply current	11.1mA	
R_D	Mains dropping resistor	6.2kΩ	See Figure 8
P_{RD}	Power dissipated in R_D	4.6W	See Figure 8
C_T	Timing capacitor (eff. value)	68μF	See Table 2
VDR	Voltage-dependent resistor	$250V_{AC}$	Cat. no. 2322 593 62512
D1	Rectifier diode	BYW56	
R1	Resistor to Pin 11	18.7kΩ	1% tolerance
R_{NTC}	NTC thermistor (at 25°C)	22kΩ	B = 4200k Cat. no. 2322 642 12223
R_P	Potentiometer	22kΩ	
C1	Capacitor between Pins 6 and 9	47nF	
C_S	Smoothing capacitor	220μF; 16V	
If R_D and D1 are replaced by C_D and R_{SD}			
C_D	Mains dropping capacitor	470nF	
R_{SD}	Series dropping resistor	390Ω	
P_{RSD}	Power dissipated in R_{SD}	0.6W	
VDR	Voltage-dependent resistor	$250V_{AC}$	Cat. no. 2322 594 62512

Signetics

Linear Products

AN1291
Design of Time-Proportional Temperature Controls Using the TDA1023

Application Note

Author: D.C. deRuiter

Electronic temperature control is no longer new; phase and on/off controls for room heaters have been widely used to replace mechanical switches. However, both phase and on/off control have disadvantages. Phase control produces RF interference and transients on the mains supply, while the hysteresis required to prevent oscillation of the output for on/off control systems prevents accurate control of the temperature.

Time-proportional control, with zero-crossing switching, eliminates these disadvantages, giving accurate temperature control and no RF interference or supply transients. The TDA1023 has been designed to provide time-proportional control using a minimum number of external components. It incorporates additional features to provide fail-safe operation and fine control of the temperature in the range 5°C to 35°C.

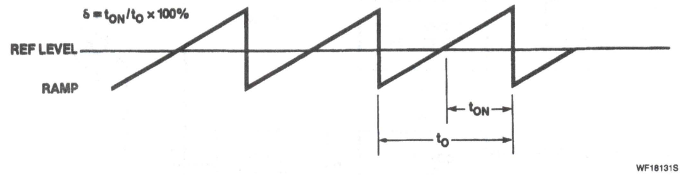
The design of the TDA1023 is such that it may also be usefully employed as a time-proportional power regulator for heating elements in electric cookers.

THE PRINCIPLE OF TIME-PROPORTIONAL CONTROL

Conventional phase control allows fully-proportional control of the power dissipated in the load, but the high rates of change of current and voltage cause RF interference. Because of this effect, phase control is not allowed to be used for domestic heaters. Simple on/off control with zero-voltage switching avoids generation of RFI but does not possess the required accuracy when stabilized with a small amount of hysteresis.

Time-proportional control combines the zero-voltage switching of on/off control with the accuracy of proportional control. Figures 1 and 2 illustrate the principle: the load is switched on once and off once in a fixed repetition period, the ratio of the on and off periods providing the proportional control. This method of control can cause mains flicker; the mains voltage will change slightly each time the load is switched on or off.

CENELEC, the European Committee for Electro-technical Standardization, has published rules which limit the rate at which domestic heating apparatus may be switched on and off. Table 1 gives the minimum repetition period for a range of load powers and common mains voltages from CENELEC publication EN50.006.



NOTE:
A change in the reference level will cause a change in t_{ON} and the load power.

Figure 1. Load Power is Proportional to the Duty Factor

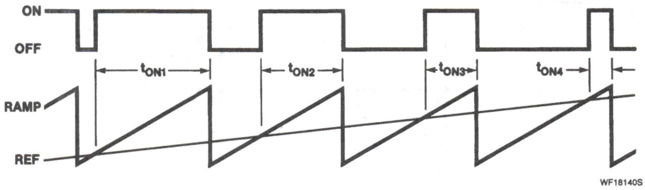


Figure 2. An Increase in Temperature Raises the Reference Voltage, Causing a Decrease in the Duty Factor and Average Load Power

There are three states of operation when using time-proportional control:

- load switched fully off
- load power proportional to the difference between actual and desired temperatures, while within the proportional range
- load switched fully on.

Clearly, this system of control will regulate the load power such that there will be no overshoot or undershoot of the desired temperature as is the case with normal on/off systems (see Figure 2). The minimum range over which there is proportional control is about 1°C, corresponding to about 80mV at the input to the comparator. This allows extremely accurate control of the temperature.

DESCRIPTION OF THE TDA1023

The TDA1023 is a 16-pin dual in-line integrated circuit designed to provide time-proportional power control of electrical heating elements, particularly panel heaters. Its time-proportional control system allows accurate temperature stabilization with the minimum of external components. Apart from panel heaters, the TDA1023 is ideally suited for the control of:

- Cooker elements
- Electric irons
- Water heaters
- Industrial temperature control, e.g., oil baths, air conditioners, etc.

It incorporates the following functions:

- A stabilized power supply. The TDA1023 may be connected directly to the AC mains using either a dropping resistor or capacitor. It provides a stabilized reference voltage for the temperature-sensing network.
- A zero-crossing detector to synchronize the output trigger pulses to the zero-crossings of the mains supply. The detector produces a pulse, the duration of which is determined by an external resistor, centered on the zero-crossing of the mains voltage.
- A comparator with adjustable hysteresis, preventing spurious triggering of the output. This compares a thermistor voltage, a function of the room

Design of Time-Proportional Temperature Controls Using the TDA1023

Table 1. Minimum Repetition Periods for Domestic Heater Applications

APPLIANCE POWER (W)	REPETITION PERIOD t_O (s)		
	220V	240V	380V (AC)
600	0.2	0.2	
800	0.8	0.3	0.1
1000	2.0	1.0	0.2
1200	4.6	2.0	0.2
1400	7.0	4.3	0.2
1600	10	6.3	0.3
1800	16	8.9	0.5
2000	24	13	0.9
2200	32	17	1.3
2400	40	24	1.9
2600		31	2.6
2800			3.6

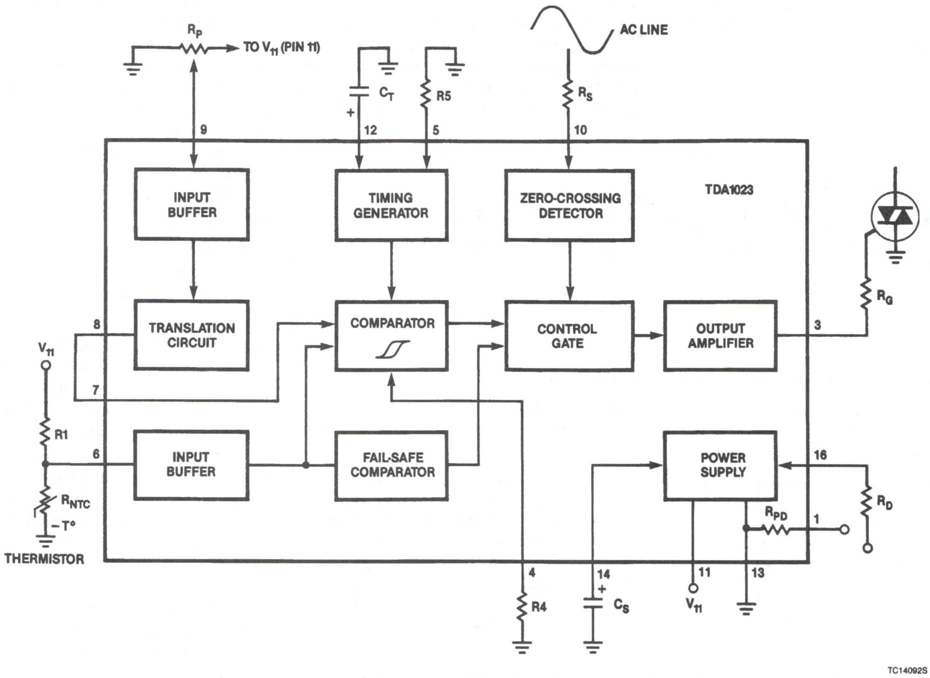
temperature, with the voltage from the temperature selection dial.

- A voltage translation circuit for the potentiometer input. Normally, the relatively small temperature variation in a room (5°C to 30°C) corresponds to a narrow angle of rotation of the potentiometer shaft. Use of this circuit doubles the angle of rotation of the potentiometer shaft for the same temperature range.
- A sensor fail-safe circuit to prevent triggering if the thermistor input becomes open or short-circuited.
- A timing generator with an adjustable proportional band. This allows a full 100% control of the load current over a temperature range of only 1°C. It can be adjusted to work over a range of 5°C. The repetition period of the timing generator may be set by an external capacitor to conform to the CENELEC specifications for mains load switching.
- An output amplifier with a current-limited output. The amplifier has an output current capability of at least 200mA and is stabilized to 10V while the current limit is not exceeded.
- Two input buffers, to isolate the voltage translation circuit and comparator from external influences.
- A control gate circuit to activate the output if there is a mains zero-crossing, the comparator is ON and the fail-safe comparator is OFF.

Although designed specifically for time-proportional control, the TDA1023 is also suitable for applications requiring on/off control if the timing generator is not used. In that case, Pin 12 must be connected to ground to inhibit the timing waveform.

SELECTION OF EXTERNAL COMPONENTS

The external components required by the TDA1023 determine the operating characteristics of the device. The following paragraphs describe the selection of these components to ensure reliable operation under worst-case conditions.



R_P
TO V_{11} (PIN 11)
9
C_T
+
12
R5
5
AC LINE
R_S
10
INPUT BUFFER
TIMING GENERATOR
ZERO-CROSSING DETECTOR
TDA1023
TRANSLATION CIRCUIT
COMPARATOR
CONTROL GATE
OUTPUT AMPLIFIER
8
7
V_{11}
3
R_G
R1
6
INPUT BUFFER
FAIL-SAFE COMPARATOR
POWER SUPPLY
16
R_D
R_{NTC}
-T°
THERMISTOR
R_{PD}
1
4
R4
14
+
C_S
11
V_{11}
13
TC14092S

Figure 3. Block Diagram of the TDA1023 and the Required External Components

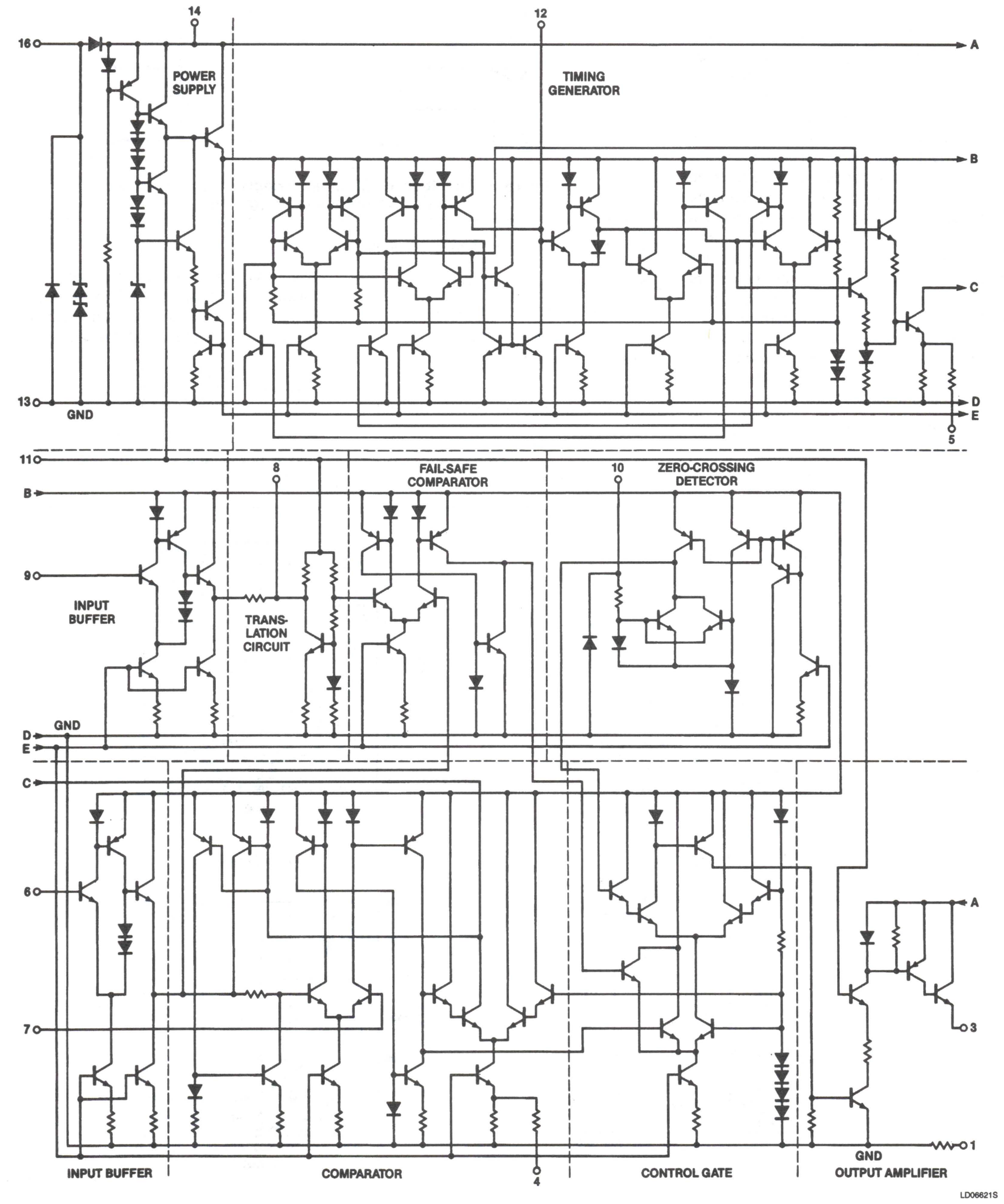

14
12
16
A
POWER SUPPLY
TIMING GENERATOR
B
C
13
GND
D
E
5
11
8
FAIL-SAFE COMPARATOR
10
ZERO-CROSSING DETECTOR
B
9
INPUT BUFFER
TRANS-LATION CIRCUIT
D
E
GND
C
6
A
7
3
1
GND
INPUT BUFFER
COMPARATOR
4
CONTROL GATE
OUTPUT AMPLIFIER
LD06621S

Figure 4. Circuit Diagram of the TDA1023

Design of Time-Proportional Temperature Controls Using the TDA1023

Required Duration of Triac Trigger Pulse

The main advantage of triggering at the instant when the applied voltage passes through zero is that this mode of operation renders the use of RF suppression components unnecessary. For time-proportional control, continuous conduction of the triac may be required for many cycles of the mains supply. To maintain conduction while the load current is approaching the zero-crossing, the trigger pulse must last from the time when the load current falls to the value of the triac holding current (I_H), until the time when the load current reaches the triac latching current (I_L). In general, the latching current of a triac is 20% higher than the holding current, so the minimum trigger pulse duration may be taken as twice the time for the load current in the triac (I_T) to rise from zero to the triac's latching current (see Figure 5).

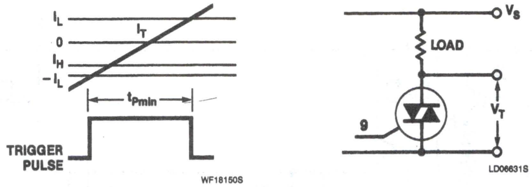


Figure 5. Definition of Minimum Trigger Pulse Width for Mains Zero-Voltage Triggering

The current passed by the triac is a function of its on-state voltage, the load resistance, and the applied AC voltage. The required trigger pulse width (t_P) is therefore a function of:

- The triac latching current (I_L)
- The applied AC voltage ($v = V \sin\omega t$)
- The load resistance (R)
- The on-state voltage of the triac (V_T) at I_L.

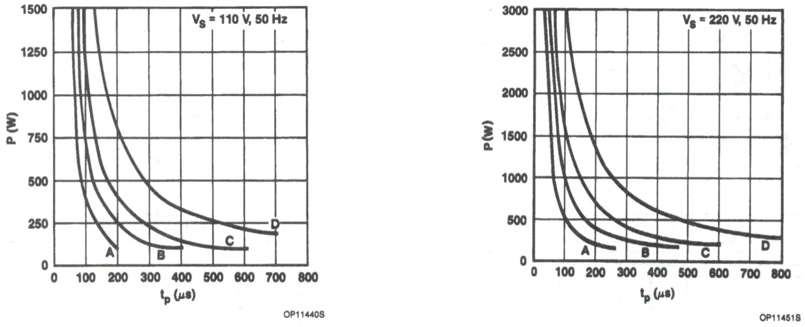
The following equation can be derived:

$$t_P = \frac{2(I_L R + V_T)}{dv/dt} \text{ at } t = 0.$$

Assuming that the load resistance has a tolerance of 5% and the AC voltage variation is 10%, the minimum required width of the trigger pulse in the worst case is:

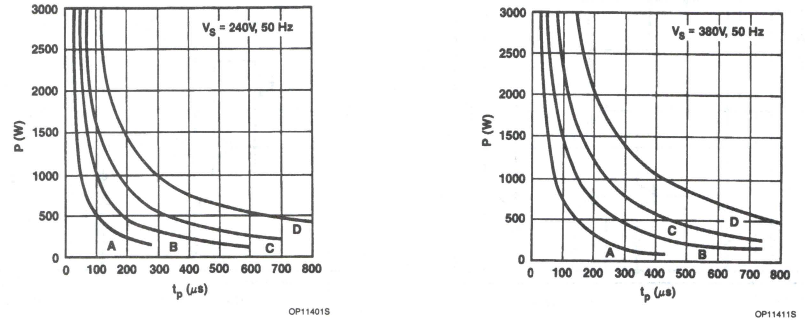
$$t_{P\ MIN} = \frac{2(1.05 R I_L + V_T)}{0.9\omega\sqrt{2V_S}}$$

in which $R = \frac{V_S{}^2}{P}$, where P is the nominal heater power and V_S is the nominal supply voltage.



a. I_L = 30mA

b. I_L = 60mA



c. I_L = 100mA

d. I_L = 200mA

Figure 6. Minimum Pulse Width as a Function of Switched Power for Four Supply Voltages, With Latching Current as a Parameter

Using this equation, with values of 30mA, 60mA, 100mA, and 200mA for the triac latching current I_L, and a maximum on-state voltage of 1.2V at I_L, the graphs of Figure 6 were computed. These show $t_{P\ MIN}$ as a function of P, with I_L as a parameter, for four common mains voltages.

Synchronization Resistor

the zero-crossing detector used to provide trigger pulse synchronization is a current comparator. It compares the current through the synchronization resistor (R_S) with a fixed internal reference current. As the supply voltage passes through zero, the current in the synchronization resistor becomes less than the reference current and a trigger pulse is given until the current in R_S increases above the reference current.

Thus, the duration of the trigger pulse depends upon the rate of change of current in R_S at the supply voltage zero-crossing point. This rate of change is affected by:

- the AC supply voltage
- the supply frequency
- the value of the synchronization resistor.

The general expression for the width of the trigger pulse is:

$$t_P = t_P^* \times \frac{1\text{mA}}{I_{10}}$$

where I_{10} is the RMS current flowing into Pin 10 in mA, at 50Hz, and t_P^* is the specified trigger pulse at $I_{10} = 1\text{mA}$.

When the frequency of the supply is not 50Hz, the value of t_P may be found by multiplying the right-hand side of the equation by the factor:

$$\frac{50}{f_{SUPPLY}}$$

The minimum width of the trigger pulse available from Pin 3 of the TDA1023 is specified in the published data as 100µs with a synchronization current into Pin 10 of 1mA at 50Hz.

Assuming a tolerance of 10% for the mains supply voltage and 5% for the synchronization resistor, the worst-case minimum trigger pulse duration for the TDA1023 appears to be:

$$t_{P\ MIN} = 0.1\,\frac{0.95R_S}{1.1V_S}\ \mu s.$$

This, however, is not realistic because the longest trigger pulse is required when the rate of change of the triac current is slowest, i.e., when the applied voltage is minimum (see Figure 5). The true worst-case therefore occurs when the applied voltage is minimum and the pulse due to R_S is minimum. This is given by:

$$t_{P\ MIN} = 0.1\,\frac{0.95R_S}{0.9V_S}\ \mu s.$$

Figure 7 shows the value of R_S as a function of the required trigger pulse width with the AC supply voltage as a parameter.

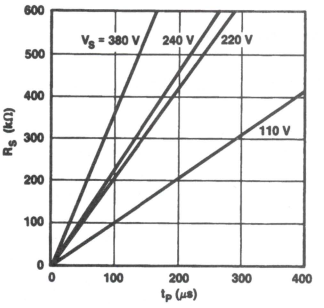


Figure 7. Synchronization Resistor Values as a Function of Required Trigger Pulse Width With Applied AC Voltage as a Parameter

Gate Resistor Value

The guaranteed minimum amplitude of the output trigger pulse at Pin 3 of the TDA1023 is specified as 10V at an output current of 200mA. The output voltage is at least 10V for all values of output current less than 200mA. The output stage is protected against damage due to short-circuits by current-limiting action when the current rises above 200mA.

Although the output is current-limited, it is still advantageous to include a gate series resistor in the circuit. Inclusion of a gate resistor to limit the gate current to the minimum value required reduces the overall current consumption and the power dissipation in the mains dropping resistor. Furthermore, the point at which current limiting occurs is subject to considerable variation between samples of the TDA1023: a gate resistor will reduce the effect of this in production circuits.

The rectangular output V/I characteristic of the TDA1023 is shown in Figure 8. Load lines for various values of gate resistor (with a worst-case tolerance of +5%) have been plotted on this diagram so that the maximum value of gate resistor can be selected by plotting horizontal and vertical lines to represent the required minimum gate current and voltage. The following example illustrates the use of Figure 8.

The triac to be triggered is a type BT139. The trigger pulse requirements for reliable triggering of all devices at 0°C are:

$I_{GT\ MIN} = 72\text{mA};$

$V_{GT\ MIN} = 1.6\text{V}.$

The lines representing $V_{GT} = 1.6\text{V}$ and $I_3 = 72\text{mA}$ cross between the load lines for gate resistor values of 100Ω and 120Ω. The maximum value of gate resistor is thus 100Ω for this example.

If gate resistor values are to be calculated more accurately, Figure 9 shows that:

$$R_{G\ MAX} = \frac{V_3 - V_{GT\ MIN}}{1.05I_3}$$

where V_3 is stabilized to 10V and the resistor tolerance is 5%.

Gate Termination Resistor R_{PD}

The TDA1023 has a resistor of approximately 1.5kΩ between Pin 1 and Pin 13. This is intended for use as a pull-down resistor when sensitive triacs are being used.

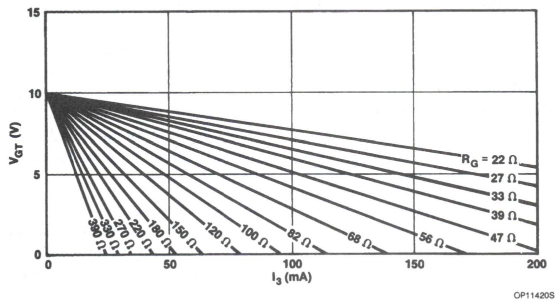


Figure 8. Gate Voltage as a Function of Output Current With Gate Resistor Load Lines

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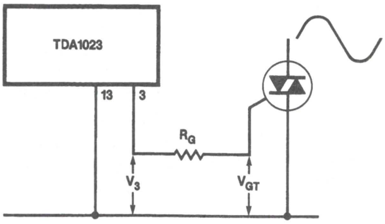


Figure 9. Inclusion of a Gate Series Resistor to Limit Trigger Current

Hysteresis Resistor R_4

The comparator of the TDA1023 is designed with built-in hysteresis to eliminate instability and oscillation of the output which would cause spurious triggering of the triac. Apart from providing a stable two-state output, the hysteresis gives the comparator increased noise immunity and prevents half-waving.

Figure 10 shows the application of hysteresis to the comparator and the transfer characteristic obtained. The comparator switches when the voltage at point A becomes equal to the reference voltage, V_7. The current source I_H is switched on when the voltage at Pin 6 is Low. As the voltage at Pin 6 rises, corresponding to a drop in temperature, the voltage at point A also rises, but, because of the current I_H being drawn through R_H, V_A is $I_H R_H$ less than V_6. For the comparator to switch, V_6 must increase to a value of $V_7 + I_H R_H$, corresponding to V_A equal to V_7. At this point the circuit switches and the current I_H is turned off, resulting in an increase of $I_H R_H$ volts at point A. For the circuit to switch back to its original state, the voltage V_6 must decrease by $I_H R_H$ volts.

The built-in hysteresis is 20mV; this may be increased by adding a resistor (R_4) from Pin 4 to ground which increases the current I_H. Pin 4 shorted to ground gives a maximum of 320mV. Table 2 gives the value of R_4 for a range of hysteresis settings.

Table 2. Choice of Hysteresis According to Proportional Band Setting

PROP. BAND (mV)	R_5 (kΩ)	MIN HYST (mV)	MAX R_4 (kΩ)
80		20	
160	3.3	40	9.1
240	1.1	60	4.3
320	0.43	80	2.7
400	0	100	1.8

The Proportional Band Resistor R_5

The proportional band is the voltage range at Pin 6 that provides control from 0% to 100% of the load power. The TDA1023 has a built-in proportional band of 80mV (corresponding to about 1°C) which can be increased by the addition of resistor R_5 between Pin 5 and ground. The maximum proportional band of 400mV is obtained by shorting Pin 5 to ground. The proportional band is derived from the triangular timing waveform, Figures 11 and 12.

When the proportional band (V_{pb}) is increased, it may be necessary to increase the hysteresis voltage (V_h) according to the requirement:

$$V_h \geqslant \frac{V_{pb}}{4}.$$

In accordance with this requirement, Table 2 gives a range of proportional band settings, the values of R_5 required for these, the corresponding minimum hysteresis voltage and the maximum value of hysteresis resistor R_4.

Timing Capacitor C_T

The minimum repetition period required for a particular application can be found in Table 1. This timing is selected using the external capacitor C_T connected between Pin 12 and ground. Typical electrolytic capacitors have wide tolerances: +50% to −10%. Moreover, the effective DC capacitance is different from the marked (AC) value, usually 20% greater. Thus, the use of standard capacitors may lead to repetition periods far in excess of those required.

Special capacitors

A special range of electrolytic capacitors has been developed for use with the TDA1023. These have the following advantages:

- Effective DC capacitance is known for each marked AC value
- Tolerance for the DC capacitance is ±20%
- Very low leakage current (< 1μA)
- Long lifetime (> 100,000 hours at 40°C).

Table 3 gives details of these capacitors. In all further references to C_T, the use of the special capacitors is assumed.

The timing circuit

The TDA1023 employs a triangular waveform for timing purposes. This gives two advantages over the conventional sawtooth waveform:

- For a given capacitor value, the triangular waveform provides twice the repetition period that the sawtooth gives, allowing the use of smaller capacitors.
- The effects of the capacitor leakage current are minimized, reducing the spread in repetition periods.

Figure 11 shows the generation of the triangular waveform using two current sources.

The published data for the TDA1023 specifies the repetition period as 0.6 ±0.2s/μF. The special capacitors have ±20% tolerances. The value of a capacitor required for a particular minimum repetition period is given by:

$$0.8C_T = \frac{t_{O\ MIN}}{0.4},$$

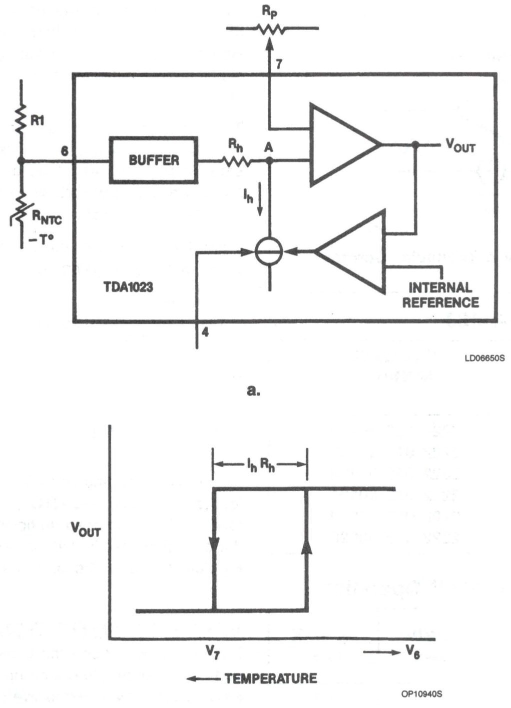
where C_T is in μF and t_O in seconds.

The maximum value, $t_{O\ MAX}$, resulting from the use of the capacitor to achieve the required $t_{O\ MIN}$ may be derived from the equation:

$$t_{O\ MAX} = 1.2C_T \times 0.8$$

where C_T is in μF and t_O in seconds.

Figure 13 shows the repetition period as a function of the timing capacitor for nominal and worst-case conditions. Table 4 is derived from Figure 13 and shows the minimum preferred value of C_T (DC value) to provide the required minimum repetition time for a range of appliance powers operating at 220V AC. The resulting nominal, minimum, and maximum repetition times are also given. In the case of 1.8 and 2kW appliances, the minimum time is slightly less than that required. However, this situation is unlikely to occur in practice; if larger capacitors are used, the nominal repetition times become very long.



a.

b.

Figure 10. Hysteresis Is Included in the Circuit of (a) Giving the Transfer Characteristic in (b)

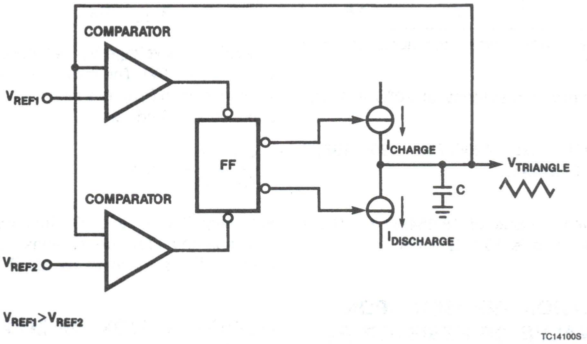


Figure 11. Generation of the Triangular Timing Waveform Using Internal Reference Voltages V_{REF1} and V_{REF2}

INFLUENCE OF THE INPUT VOLTAGE TRANSLATION CIRCUIT ON THE DESIGN OF THE TEMPERATURE SENSING BRIDGE

Many arrangements of temperature sensing networks are possible; the circuit of Figure 14 requires a minimum of components and possesses the advantage of eliminating performance spreads due to potentiometer tolerances. When room heaters are to be controlled, the voltage variation at the NTC thermistor will be very much less than the available voltage variation at the potentiometer. This will result in the required temperature range being controlled by a very small angle of rotation of the potentiometer shaft. The voltage translation circuit incorporated in the TDA1023 allows the use of 80% of the potentiometer rotation for the normal range of room temperatures, allowing far more accurate control of the temperature. If the voltage translation circuit is not used, Pins 9 and 11 must be shorted together to disable the circuit.

The transfer characteristic of the translation circuit is shown in Figure 15. Because only 80% of the potentiometer is used, the midpoint of the slider voltage range is at 60% of V_{11}, which must correspond to the thermistor voltage at 20°C. From Figure 14:

$$\frac{V_6}{V_{11}} = \frac{R_{20}}{R_{20} + R_1} = 0.6$$

giving:

$$R_1 = \frac{2R_{20}}{3}$$

where R_{20} is the thermistor resistance at 20°C.

The resistance of an NTC thermistor at a given temperature is determined by the equation:

$$R_{NTC} = A \exp (B/T) \ \Omega$$

where $A = R_{25}/\{\exp(B/298)\}$, B is a constant for the device type, and T is the temperature in degrees Kelvin.

The characteristics of a suitable NTC thermistor (catalog number 2322 642 12223) are:

$R_{25} = 22\text{k}\Omega \pm 10\%$;

$B = 4200 \pm 5\%$.

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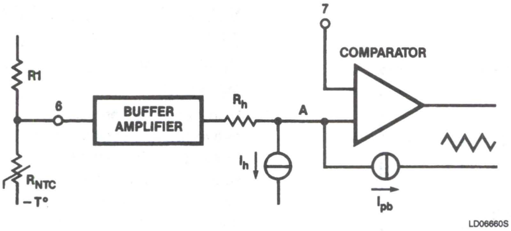

Figure 12. The Proportional Band Is Produced by a Triangular Current Waveform I_{pb}

Table 3. Special Capacitors for use With TDA1023

MARKED AC SPECIFICATION (µF)	(V)	EFFECTIVE DC VALUE (µF)	CATALOG NUMBER
47	25	68	2222 016 90129
33	40	47	2222 016 90131
22	25	33	2222 015 90102
15	40	22	2222 015 90101
10	25	15	2222 015 90099
6.8	40	10	2222 015 90098

Table 4. Repetition Time Capacitor Values for 220V Operation

APPLIANCE POWER (W)	t_O (CENELEC) (sec)	C_T (DC) (µF)	t_O NOM (sec)	t_O MIN (sec)	t_O MAX (sec)
2000	24	68	41	22	65
1800	16	47	28	15	45
1600	10	33	20	11	32
1400	7	22	13	7	21
1200	4.6	15	9	4.8	14
1000	2	10	6	3.2	9.6
800	0.8	10	6	3.2	9.6
600	0.3	10	6	3.2	9.6

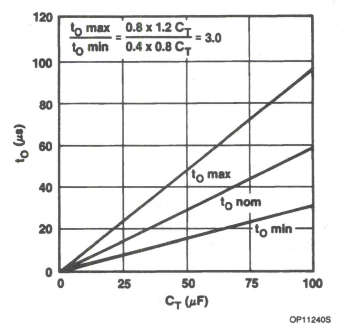

Figure 13. Repetition Period t_O as a Function of the Timing Capacitor for Nominal and Worst-Case Values

A thermistor with these values is chosen to provide a compromise between low current consumption and noise sensitivity: high impedance reduces current but increases noise sensitivity.

The thermistor resistance at 20°C is thus:

$$R_{20} = R_{25}\ \exp\ (4200/293 - 4200/298)\Omega$$
$$= 27.982k\Omega.$$

This gives a value of 18.654kΩ for R_1; a practical value is 18.7kΩ ±1%.

LIMITATION IMPOSED UPON THE VALUE OF RESISTOR R_1 DUE TO THE FAIL-SAFE CIRCUIT

The TDA1023 is fail-safe for both short-circuit and open-circuit conditions. Either of these conditions will prevent production of trigger pulses for the triac.

Short-circuit sensing is automatically obtained from the normal temperature sensing circuit. When the thermistor input voltage is zero, the triac will never be triggered because the potentiometer slider voltage will be higher. Normally the use of the voltage translation circuit gives a minimum slider voltage of 20% of V_{11}.

To sense the open-circuit thermistor condition, an extra comparator is used. This fail-safe comparator will inhibit output pulses if the thermistor input voltage rises above 0.95 V_{11} (see Figure 16).

From Figure 16 the maximum permissible value of R_{NTC} is given by:

$$V_{11} \frac{R_{NTC}}{R_{NTC} + R_1} < 0.95V_{11}$$

which gives,

$$R_{NTC\ MAX} < 19R_1.$$

For normal operating conditions, even at very low temperatures, the NTC thermistor resistance will not increase sufficiently to violate the condition specified above for the value of R_1 determined in the previous section.

VALUE OF POTENTIOMETER R_P

It is desirable to keep the current consumption of the temperature sensing bridge as low as possible to avoid excessive power dissipation in the mains dropping circuit components. A reasonable limit to the bridge current is 1mA. The current in the bridge, I_{BR}, is given by:

$$I_{BR} \approx \frac{V_{11}}{R_1 + R_{NTC}} + \frac{V_{11}}{R_P}.$$

The reference voltage V_{11} will never exceed 9V (nominally 8V). The maximum value of I_{BR} will occur when R_{NTC} is a minimum, giving the approximate condition:

$$\frac{V_{11}}{R_1} + \frac{V_{11}}{R_P} < 1mA.$$

Assuming the value of R_1 that was determined in the previous sections, a suitable value of R_P is found to be 22kΩ.

DETERMINATION OF MAXIMUM AVERAGE OUTPUT CURRENT

Before any calculations concerning the required supply current can be made, the maximum average output current of the TDA1023 must be determined. For the worst-case conditions, a 5% tolerance for R_S and R_G and a 10% variation of the mains is assumed. The maximum value of the trigger pulse, $t_{P\ MAX}$, is specified in the published data as 300µs at

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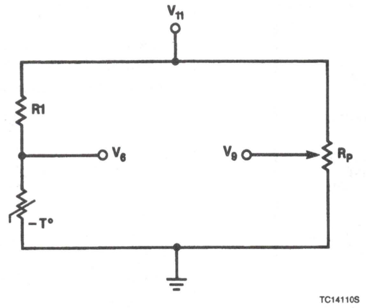
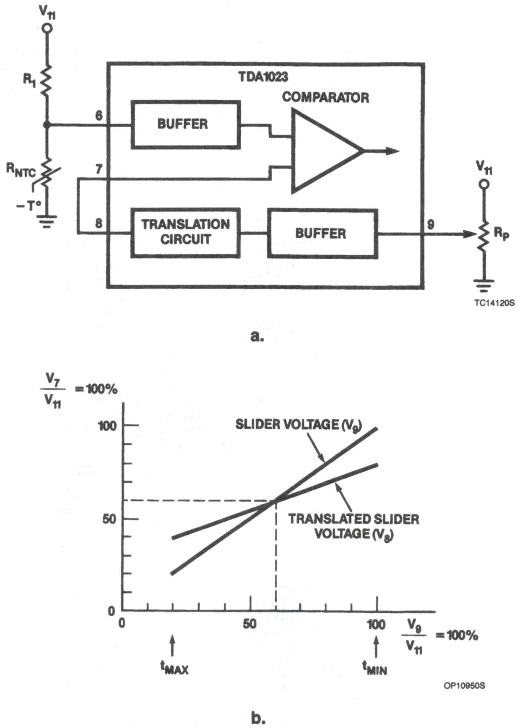


Figure 14. Temperature-Sensing Bridge Circuit



a.

b.

Figure 15. Voltage Translation Circuit (a) and Its Transfer Characteristics (b)

I_{10} = 1mA$_{RMS}$ at a frequency of 50Hz; $V_{3\ MAX}$ is specified as 15V.

The maximum average output current, $I_{3(AVG)\ MAX}$, can be determined from the equation:

$$I_{3(AVG)\ MAX} = I_{3\ MAX}\ t_{P\ MAX}\ N$$

where $t_{P\ MAX}$ is expressed in seconds and N is the number of pulses/second.

Under the worst-case conditions, assuming that V_{GTmin} for the triac is zero, the maximum trigger current is:

$$I_{3\ MAX} = \frac{V_{3\ MAX}}{0.95R_G}$$

and the maximum pulse length at 50Hz is:

$$t_{P\ MAX} = 0.3\frac{1.05\ R_S}{0.9V_S}10^{-6}s.$$

The final equation for $I_{3(AVG)\ MAX}$ is:

$$I_{3(AVG)\ MAX} = 5.53\frac{R_S}{V_S R_G}10^{-4}\ A.$$

Figure 17 shows graphs of $I_{3(AVG)\ MAX}$ as a function of R_G with R_S as a parameter, for four 50Hz supply voltages. When the curves reach the value of 22Ω for R_G, there is no further increase in I_3 if R_G is decreased as the output current is limited to 700mA.

MINIMUM REQUIRED SUPPLY CURRENT I_{16}

The minimum supply current required at Pin 16 of the TDA1023 is the sum of the following currents:

- the maximum average output current
- the current drawn by the external temperature-sensing circuit
- the current required by the integrated circuit.

The maximum average output current has been determined in the previous section. The current drawn by the temperature-sensing circuit must not be greater than 1mA.

The current consumption of the internal circuits of the TDA1023 depends upon the hysteresis and proportional band settings and whether the circuit is in the ON or OFF state. The circuit draws more current in the ON state to provide the output current pulse. With Pins 4 and 5 open-circuit (hysteresis and proportional band at minimum) the maximum current consumption is 6mA. When Pins 4 and 5 are connected to ground, the current consumption increases by 1.1mA. Figure 18 shows the minimum required supply current as a function of the maximum average output current for maxima and minima of hysteresis and proportional band settings.

DETERMINATION OF THE VALUE OF THE MAINS DROPPING RESISTOR R_D

The value of the mains dropping resistor must be chosen such that the average supply current to Pin 16 of the TDA1023 is at least equal to the required minimum.

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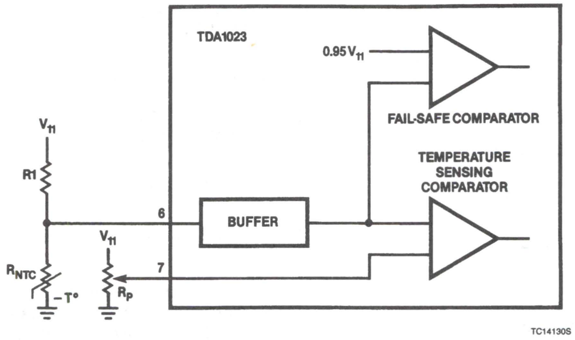

NOTE:
An extra comparator is included to provide fail-safe action should the thermistor input become open-circuit.

Figure 16

Figure 19 shows the supply circuit and the mains voltage waveform. The shaded area denotes a positive voltage across the dropping resistor providing supply current.

During the positive half-cycle of the mains voltage, the current supplied through R_D is given by:

$$I_{16(AVG)} = \frac{1}{2\pi}\int_{\alpha 1}^{\alpha 2} \frac{\sqrt{2}V_S \sin \alpha - V_{16}}{R_D}\, d\alpha.$$

Assuming 10% mains voltage variation, 10% tolerance for R_D and a maximum of 16V at Pin 16, the worst-case condition is given by:

$$I_{16(AVG)\ MIN} = \frac{1}{2\pi}\int_{\alpha 1}^{\alpha 2} \frac{0.9\sqrt{2}V_S \sin \alpha - 16}{1.1R_D}\, d\alpha.$$

in which $\alpha_1 = \pi - \alpha_2 = \arcsin 16/(0.9\sqrt{2}V_S) = \arcsin 12.58/V_S$. Using this equation, graphs of $I_{16(AVG)\ MIN}$ as a function of R_D have been drawn for four supply voltages and are shown in Figure 20.

MINIMUM PERMISSIBLE VALUE FOR R_D

The maximum value of the resistor R_D is defined by the maximum current that can flow into Pin 16, the maximum peak mains voltage, and the minimum voltage at Pin 16. The published data for the TDA1023 specifies the absolute limit for I_{16} as:

$I_{16(AVG)\ MAX} = 30\text{mA}$
and $I_{16M\ MAX} = 100\text{mA}$.

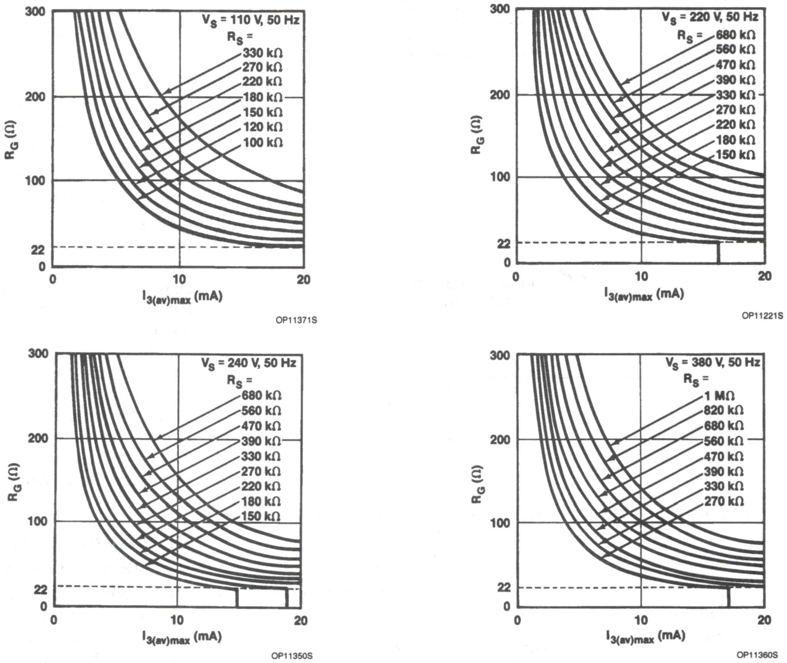

Figure 17. $I_{3(AVG)\ MAX}$ as a Function of Resistor R_G With Synchronization Resistor R_S and Mains Voltage as Parameters

The peak current flowing into Pin 16 is given by:

$$I_{16\ MAX} = \frac{\sqrt{2V_S - V_{16\ MIN}}}{R_D}$$

For a sinusoidal supply voltage, the relationship between the peak and average current into Pin 16 is:

$$\frac{I_{16\ MAX}}{I_{16(AVG)}} = \pi.$$

Because the ratio of the specified limits for the peak and average supply current, 100/30, is greater than π, the minimum value of R_D is defined by $I_{16(AVG)\ MAX}$:

$$R_{D\ MIN} = \frac{\sqrt{2V_{S\ MAX} - V_{16\ MIN}}}{\pi I_{16(AVG)\ MAX}}$$

Assuming a 10% variation in the supply voltage and R_D, the minimum value for the dropping resistor is:

$$0.9R_{D\ MIN} = \frac{1.1V_S\sqrt{2 - 12.5}}{0.03\pi}$$

Table 5 shows practical values for $R_{D\ MIN}$ for four common mains supply voltages.

Table 5. Practical Mains Dropping Resistor Values

SUPPLY VOLTAGE V_S (V)	$R_{D\ MIN}$ (Ω)	PRACTICAL VALUE OF $R_{D\ MIN}$ (kΩ)
110	1870	2.0
220	3887	3.9
240	4254	4.3
380	6821	7.5

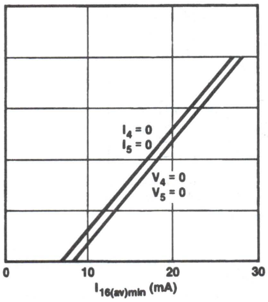

Figure 18. Minimum Required Supply Current as a Function of Average Trigger Current, With Hysteresis and Proportional Band Settings as Parameters

DETERMINATION OF POWER DISSIPATED IN MAINS DROPPING RESISTOR R_D

The general expression for the power dissipated by resistor R_D in Figure 19 is:

$$P = \frac{V^2_{RMS}}{R_D}$$

in which,

$$V^2_{\ RMS} = \frac{1}{2\pi}\int_{\alpha 1}^{\alpha 2}(\sqrt{2V_S \sin\alpha - V_{16}})^2 d\alpha + \frac{1}{2\pi}\int_{\pi}^{2\pi}(\sqrt{2V_S \sin\alpha})^2\, d\alpha.$$

If supply voltage variations of 10% and a tolerance of 10% for R_D are assumed, the maximum power dissipated by R_D is given by:

$$P_{MAX} = \frac{1}{2\pi} \times \frac{1}{0.9R_D}\int_{\alpha 1}^{\alpha 2}(1.1\sqrt{2V_S \sin\alpha - 12.5})^2 d\alpha + \frac{1}{2\pi} \times \frac{1}{0.9R_D}\int_{\pi}^{2\pi}(1.1\sqrt{2V_S \sin\alpha})^2\, d\alpha.$$

Values of P_{MAX} have been computed for four mains voltages as a function of R_D and the results plotted on the graphs of Figure 20.

The power dissipated in R_D may be considerably reduced by the addition of a series diode as in Figure 23. In this case there is no conduction through R_D during the negative half-cycle of the supply voltage, giving a reduction of more than 50% of the power dissipated in R_D. For worst-case conditions, the power dissipation when a series diode is included in the mains dropping circuit is given by:

$$P_{MAX} = \frac{1}{2\pi} \times \frac{1}{0.9R_D}\int_{\alpha 1}^{\alpha 2}(1.1\sqrt{2V_S \sin\alpha - 12.5})^2 d\alpha.$$

Values of P_{MAX} as a function of R_D, with the series diode present, have also been calculated and plotted in Figure 20 to allow easy comparison with the values obtained without the series diode.

USE OF A CAPACITOR TO REDUCE POWER DISSIPATION

It is possible to replace the mains dropping resistor and series diode with a capacitor (Figure 21), and thereby reduce the power dissipation in the voltage reduction components still further. However, for mains voltages below 220V, the power dissipated by the dropping resistor is comparatively small and the use of a capacitor is not considered to be necessary. For mains voltages above 240V, the additional cost of the required high-voltage capacitor is not justified. For these reasons, it is recommended that capacitive voltage reduction is only used with mains supplies of $200V_{RMS}$ or $240V_{RMS}$.

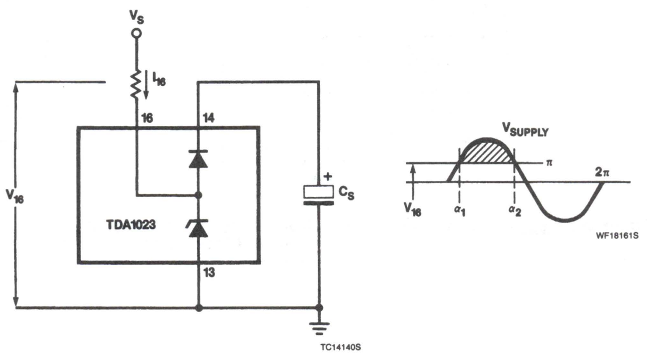

Figure 19. Mains Supply Circuit and Voltage Waveform

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When selecting a capacitor for mains voltage reduction, the following points must be considered:

- The specified maximum AC voltage for the capacitor must be compatible with the mains supply voltage;
- Inrush current must be limited to less than 2A by a series resistor (R_{SD});
- Mains-borne transients must be suppressed to limit the maximum current to Pin 16 to less than 2A;
- The value of the capacitor must be calculated as a function of the required average current at Pin 16 of the TDA1023, using the mains voltage as a parameter. The maximum permissible value of the capacitor must be calculated to ensure that, under worst-case conditions, the maximum permissible current into Pin 16 is not exceeded.

Suppression of mains-borne transients

A voltage-dependent resistor must be connected across the mains input to limit mains-borne transients to:

$$V_{TRANS} = I_{16SM} \times 0.95R_{SD}$$

where I_{16SM} is the maximum permitted non-repetitive peak current at Pin 16 (2A).

For $R_{SD} = 390\Omega$, this yields a maximum transient voltage of about 740V. For 220V operation, a VDR (catalog number 2322 594 13512) will limit the supply voltage to the required level during current transients of up to about 200A. For 240V operation, a VDR (catalog number 2322 594 13912) will limit the supply voltage to the required level during current transients of up to about 80A.

Limit of Inrush Current

Resistor R_{SD} must also limit the peak value of the inrush current to less than 2A under worst-case operating conditions. With a $240V_{RMS}$ supply, the value of 390Ω will limit the worst-case peak value of the in rush current to:

$$\frac{240 \times 1.1}{0.95 \times 390}\sqrt{2} = 1.01\ \text{A}.$$

Dropping Capacitor Value

The average current supplied to Pin 16 of the TDA1023 via capacitor C_D is given approximately by:

$$I_{16(AVG)} = \frac{1}{\pi}\,\frac{\sqrt{2V_S - V_{16}}}{\sqrt{\left(R^2{}_{SD} + \frac{1}{\omega^2 C^2{}_D}\right)}}$$

When worst-case tolerances are taken into account, the minimum average current through the capacitor is given by:

$$I_{16(AVG)\,MIN} = \frac{1}{\pi}\,\frac{0.9\sqrt{2V_S - V_{16\,MAX}}}{\sqrt{\left\{1.1R^2{}_{SD} + \left(\frac{1}{0.9\omega C_D}\right)^2\right\}}}$$

where $V_{16\ MAX} = 16V$ and $R_{SD} = 390\Omega$.

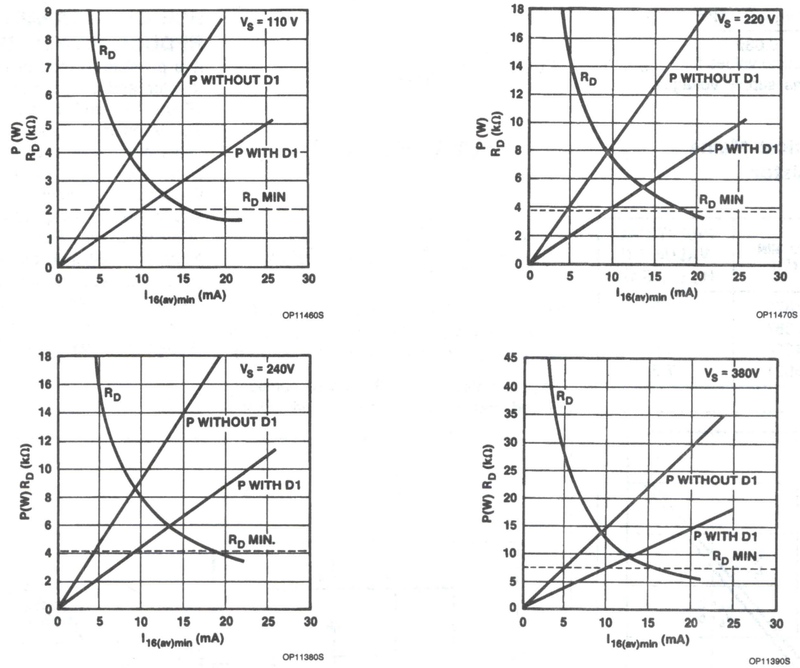


Figure 20. $I_{16(AVG)\ MIN}$ as a Function of Mains Dropping Resistor R_D, and the Power Dissipation in that Resistor, With and Without a Series Diode, With Supply Voltage as a Parameter

Using this equation, values of C_D have been computed as a function of the minimum required average current into Pin 16 for mains voltages of $220V_{RMS}$ and $240V_{RMS}$. The results have been plotted in the graphs of Figure 21, allowing simple selection of the capacitor value once the minimum required average current is known.

Maximum Permissible Value for the Capacitor C_D

The capacitor C_D must not be chosen so large that the current into Pin 16 of the TDA1023 violates the absolute maximum specified in the published data. Assuming a 10% tolerance for C_D and a 10% variation in the mains voltage, the maximum value of C_D that may be used is given by:

$$1.1C_{D\ MAX} = \frac{\pi I16\ AV_{MAX}}{1.1\omega V_S\sqrt{2}}$$

where the effect of R_{SD} on the calculation of $C_{D\ MAX}$ is so small that it may be ignored. The values of $C_{D\ MAX}$ obtained from this equation are given in Table 6.

Power Dissipated by the Series Resistor R_{SD}

The power dissipated by the 390Ω resistor R_{SD} is given by:

$$P = I^2_{16\ RMS}\ R_{SD}$$

where $I_{16\ RMS}$ may be approximated to:

$$I_{16\ RMS} = \omega C_D V_S.$$

Assuming tolerances of 10% for R_{SD} and C_D and a mains variation of 10%, the worst-case maximum power dissipation in resistor R_{SD} is given by:

$$P_{MAX} = 1.1R_{SD}\,(1.21\omega C_D V_S)^2.$$

The power dissipated in R_{SD} has been plotted as a function of the supply current $I_{16(AVG)}$ and is shown in Figure 21.

SMOOTHING CAPACITOR C_S

The smoothing capacitor is required to provide the supply current to the TDA1023 during the negative half-cycles of the mains voltage waveform. As the TDA1023 possesses an internal voltage stabilization circuit, a high ripple voltage can be tolerated at Pin 14.

The value of the smoothing capacitor is given by:

$$C_S > \frac{It}{V_R}$$

where:
I = the maximum average current consumption during the half-cycle. This is never more than 20mA.
t = the time for which the current must be supplied; 10ms for 50Hz mains supplies.
V_R = the maximum acceptable ripple voltage at Pin 14; 1V.

Using these figures, the required value for C_S is 200μF. A practical preferred value is 220μF, 16V.

TRIAC PROTECTION

If the mains dropping circuit consists of capacitor C_D and resistor R_{SD}, a VDR must be included in the circuit as described in the section dealing with the use of a dropping capacitor. This VDR will also protect the triac against current surges in the mains supply.

However, if the mains dropping circuit consists of resistor R_D and diode D_1, the VDR may be connected directly across the triac, giving improved protection due to the series resistance of the heater. Current surges in the supply will not harm the TDA1023 as the dropping resistor will limit the current to a safe level.

EFFECT OF BRIDGE COMPONENT TOLERANCES ON THE ACCURACY OF TEMPERATURE CONTROL

The general expression for the voltage across the thermistor at a temperature of T°C is:

$$V_T = \frac{R_{25}\ \exp\ \{B/(273 + T) - B/298\}}{R_1 + R_{25}\ \exp\ \{B/(273 + T) - B/298\}}\,V_{11}.$$

In order to calculate the maximum and minimum values of V_T, tolerances of 10% for R_{25}, 5% for B and 1% for R_1 have been assumed. Table 7 shows the combination of tolerances used to calculate the worst-case values of V_T for temperatures above and below 25°C.

The ratios V_6/V_{11} and V_9/V_{11}, as functions of temperature, are plotted in Figure 22 for nominal and worst-case values of V_T.

If it is assumed that the potentiometer has a linear temperature scale, represented by the broken line in Figure 22, then the maximum deviation of the actual temperature from the selected temperature is found by drawing a horizontal line intersecting the broken line at the given temperature. The intersection points with the worst-case curves then give the maximum temperature deviation. Table 8 shows the possible worst-case temperature errors for a series of temperatures in the range of application.

REDUCTION OF TEMPERATURE ERROR BY SCALE CALIBRATION

The error of a temperature control unit built on the described principles can be considered mainly as an offset, which can be corrected by shifting the temperature scale on the potentiometer. Scale calibration can best be accomplished by maintaining the thermistor at a constant, known temperature and adjusting the potentiometer until trigger pulses just occur. The scale is then fixed so that the control pointer indicates the known temperature of the thermistor. To minimize errors, the calibration should be performed with the thermistor at 20°C (mid-point of the range) and the timing generator inhibited (Pin 12 connected to 0V).

Use of this scale calibration technique results in a temperature control accuracy of +0.2 to −0.1°C over the range 10°C to 30°C as shown in Table 9.

SENSITIVITY OF THE TEMPERATURE-SENSING BRIDGE

To determine the choice of hysteresis and proportional band, the sensitivity of the temperature-sensing network must be known. As the thermistor is not a linear device, the sensitivity will vary according to the temperature. The sensing network is shown in Figure 14. The voltage at Pin 6 is given by:

$$V_6 = \frac{A\ \exp\ (B/T)}{R_1 + A\ \exp\ (B/T)}\,V_{11}.$$

From which the sensitivity is:

$$\frac{dV_6}{dT} = \frac{-BR_1A\ \exp\ (B/T)}{T^2\{R_1 + A\ \exp\ (B/T)\}^2}\,V_{11}.$$

Table 10 is based on this equation and shows the effect of sensitivity on the hysteresis and proportional band for the temperature range 10°C to 30°C.

APPLICATION EXAMPLES

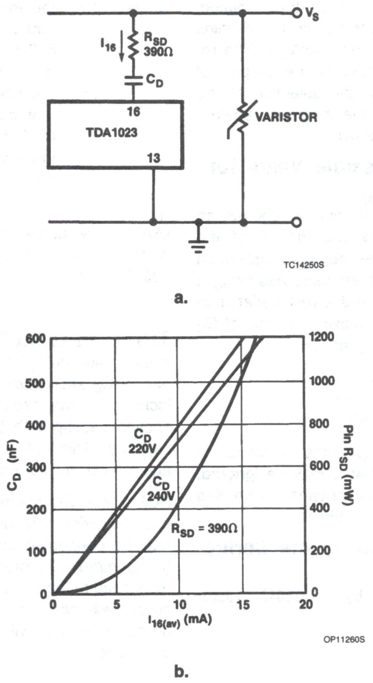
The TDA1023 is intended primarily for room temperature control using electric panel heaters. The controllable heater power range is from 400W to 2000W, although the upper limit may be increased by suitable choice of triacs and/or heatsinks. The TDA1023 may also be used as a time-proportional switch for cooker elements and similar devices, giving 100% control of the power dissipation.

Design of Time-Proportional Temperature Controls Using the TDA1023

AN1291

A Design For Temperature Control Of Domestic Panel Heaters

Figure 23 shows the design for a time-proportional heater control using the TDA1023. Because of the economies that may be gained by the use of smaller or lower power components, two versions are described. Version A, for heaters from 400W to 1200W, uses triac BT138 and a 15μF timing capacitor; version B, for heaters from 1200W to 2000W, uses triac BT139 and a 68μF timing capacitor.



V_S
I_{16}
R_{SD} 390Ω
C_D
16
TDA1023
13
VARISTOR
TC14250S
600
500
400
300
200
100
0
C_D (nF)
1200
1000
800
600
400
200
0
Pin R_{SD} (mW)
C_D 220V
C_D 240V
R_{SD} = 390Ω
0
5
10
15
20
$I_{16(av)}$ (mA)
OP11260S

a.

b.

NOTE:
The circuit is shown in (a) and the power dissipated by the dropping resistor and the capacitor value as functions of the current into Pin 16, with the mains supply voltage as a parameter is shown in (b).

Figure 21. Using a Capacitor for Mains Voltage Dropping

Table 6. Practical Dropping Capacitor Values

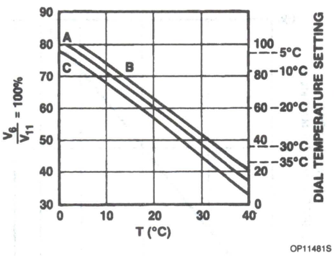
SUPPLY VOLTAGE V_S (V)	$C_{D\ MAX}$ (nF)	PRACTICAL VALUE OF $C_{D\ MAX}$ (nF)
220	797	680
240	730	680

Table 7. Tolerance Combinations for Thermistor Voltage Calculations

TEMPERATURE	FOR $V_{T\ MAX}$	FOR $V_{T\ MIN}$
T < 25°C	R_{25} + 10% B + 5% R_1 – 1%	R_{25} – 10% B – 5% R_1 + 1%
t > 25°C	R_{25} + 10% b – 5% R_1 – 1%	R_{25} – 10% b+5% R_1 + 1%

Design of Time-Proportional Temperature Controls Using the TDA1023

AN1291



NOTES:
A = Nominal Curve, B = Maximum Curve,
C = Minimum Curve.
The broken line represents the ideal linear function.

Figure 22. Nominal and Worst-Case Values of V_6 as a Function of Temperature

Table 8. Maximum Deviation From Selected Temperature

SELECTED TEMP. (°C)	DEVIATION	
	Upper (°C)	Lower (°C)
5	+2.3	-3.6
10	+2.6	-2.8
14	+2.6	-2.7
20	+2.4	-2.7
26	+2.3	-2.6
30	+2.6	-2.6
35	+3.0	-3.0

Table 11 gives the necessary component values for each of these versions for use with mains supplies of 220V, 50Hz. All figures in Table 11 have been calculated using the equations given in the previous sections, allowing for worst-case conditions. Because each version is designed to control a range of heater powers, it follows that each may not be ideal for all load powers in the range. If the ideal circuit is required, then this must be calculated as shown in the earlier sections.

The capacitor C_1 has been included in the circuit of Figure 23 to minimize the effects of any interference picked up in the sensor lines. This is only necessary when the sensor is remote from the control circuit. The built-in hysteresis and proportional band have been designed to provide optimum performance for panel heaters, so Pins 4 and 5 are not connected.

Design Of Temperature Control For 220V, 50Hz Operation With 2kW Load

For a load power of 2kW the triac BT139 must be used. The relevant data for this triac (also applicable to move the BT138) are given in Table 9.

Table 9. Maximum Deviation From Selected Temperature Scale Calibrated at 20°C

SELECTED TEMP. (°C)	DEVIATION	
	Upper (°C)	Lower (°C)
5	−0.1	−0.9
10	+0.2	−0.1
14	+0.1	0
20	0	0
26	−0.1	+0.1
30	+0.2	+0.1
35	+0.6	+0.3

- I_{GT} to trigger, all devices = 72mA; ⎫
- V_{GT} to trigger all devices = 1.6V; ⎬ at 0°C
- I_L = 60mA ⎭

The circuit used will be that of Figure 23. Pins 4 and 5 are not connected as the built-in hysteresis and proportional band will give the optimum performance.

Value of R_S

The required trigger pulse width can be found from Figure 6 as a function of the load power, latch current, and supply voltage (2000W, 60mA, and 220V, 50Hz, respectively): $t_{P\ MIN} = 64\mu s$.

From Figure 6, the value of R_S to provide a trigger pulse of the required duration is then: $R_S = 135k\Omega$. The next preferred value above this is 150kΩ, providing a $t_{P\ MIN}$ of approximately 70μs.

Value of R_G

The maximum value of R_G that may be used is determined by the minimum voltage and current to reliably trigger all samples of the triac. In Figure 8 it can be seen that the operation point of 1.6V and 72mA lies between the load lines for 100Ω and 120Ω. The lesser of these two values, $R_G = 100\Omega$, must be chosen. By calculation, it is found that this resistor may be 110Ω.

Value of C_T

For a load of 2kW, the repetition period must be at least 24 seconds (from Table 1). From Table 3 the minimum preferred value of C_T to provide this period is 68μF. However, due to the different performance under AC and DC conditions, the actual capacitor used should be a 47μF, 25V, catalog number 2222 016 90129 (see Table 2).

Value of R_1 and R_P

For control over the range 5°C to 35°C and thermistor characteristics of B = 4200 and $R_{25} = 22k\Omega$, the value of R_1 has previously been shown to be 18.7kΩ ±1%. A suitable value for R_P is 22kΩ.

Value of R_D

First, the maximum average output current must be found. Figure 17 gives $I_{3(AVG)\ MAX}$ as a function of the values of resistors R_S and R_G. For this circuit $I_{3(AVG)\ MAX} = 3.5mA$.

Once the maximum average output current is known, the minimum required supply current can be found from Figure 18. With minimum hysteresis and proportional band, the average value of the supply current is 10.5mA.

Using this value of $I_{16(AVG)}$, the required value of R_D can be found from Figure 20: $R_D = 6.8k\Omega$. The power dissipation in the resistor, when diode D_1 is present in the circuit, is then 4.3W.

Final component list

Table 12 gives a summary of the component values for the 2kW, 220V, 50Hz temperature controller.

Time-Proportional Power Control

The TDA1023 may be used to provide proportional control of devices such as electric cooker elements. The temperature-sensing bridge is replaced by a potentiometer, the power in the load being proportional to the potentiometer setting (see Figure 24).

The inputs to the comparator are:

- Pin 7: the triangular waveform at the timing capacitor
- Pin 6: the potentiometer voltage.

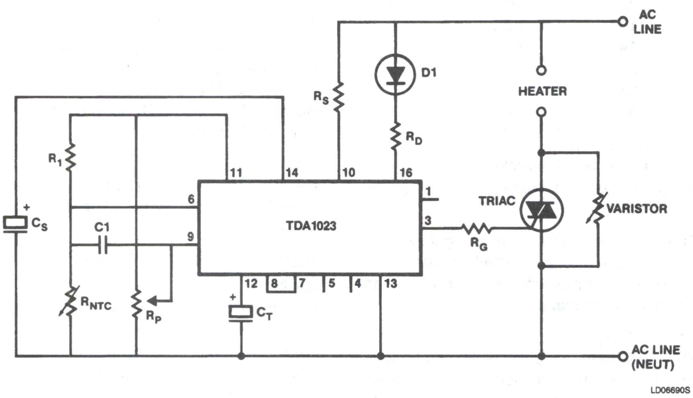
Proportional power control is thus obtained while the potentiometer voltage lies between the upper and lower limits of the triangular waveform. As the timing capacitor is charged and discharged by current sources, the voltage across it will never reach zero, so that load power will be zero before the potentiometer reaches its minimum setting. Similarly, maximum load power is reached before the maximum setting of the potentiometer. This effect can be reduced by the addition of resistors R_1 and R_2. To ensure that 0% and 100% load power can be selected by the potentiometer setting, the values of R_1 and R_2 should each be limited to 10% of the value of R_P.

All the circuit components are calculated in the same way as for the temperature controller, including the timing capacitor C_T. An example circuit, with components suitable for the control of loads from 1 to 2kW from 220V, 50Hz supplies, is shown in Figure 25. Pins 9 and 11 are shorted together as the voltage translation circuit is not used.

Design of Time-Proportional Temperature Controls Using the TDA1023

Table 10. Sensitivity of Temperature-Sensing Network NTC Thermistor: Catalog Number 2322 642 12223 Resistor: 18.7kΩ

TEMP (°C)	SENS (mV/°C)	HYSTERESIS (°C/20mV)	PROP BAND (°C/80mV)
10	86	0.23	0.93
15	91	0.22	0.88
20	94	0.21	0.85
25	94	0.21	0.85
30	91	0.22	0.88


AC LINE
D1
R_S
R_D
HEATER
R_1
11
14
10
16
1
3
6
9
TDA1023
TRIAC
VARISTOR
C_S
C1
R_G
12
8
7
5
4
13
R_{NTC}
R_P
C_T
AC LINE (NEUT)
LD06690S

NOTE:
Refer to Table 11 for component values for use with 220V, 50Hz supplies.

Figure 23. Circuit Diagram of Time-Proportional Heater Control Using the TDA1023

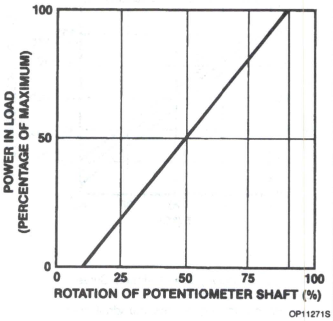


Figure 24. Typical Load Power as a Function of Potentiometer Shaft Rotation for a Time-Proportional Power Regulator

Design of Time-Proportional Temperature Controls Using the TDA1023

Table 11. Temperature Controller Component Values Mains supply: 220V, 50Hz
Version A: Heater Powers 400 – 1200W Version B: Heater Powers 1200 – 2000W

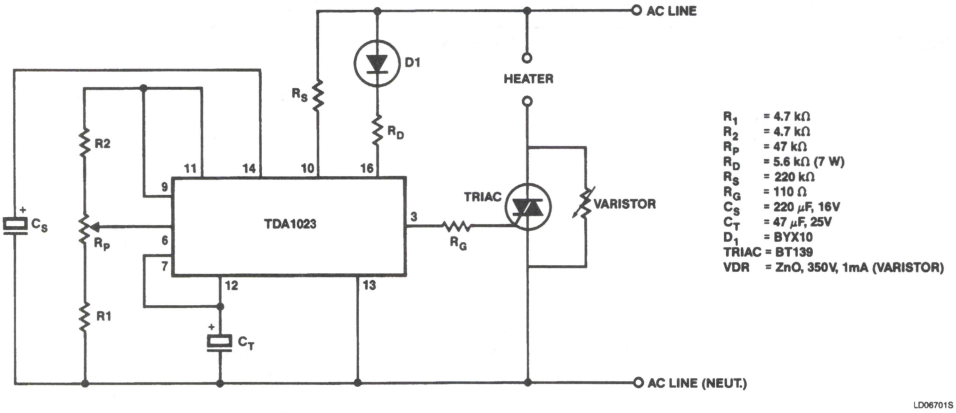
COMPONENT	VERSION A	VERSION B	REMARKS
Triac	BT138	BT139	
VDR	350V, 1mA	350V, 1mA	Cat. No. 2322 594 13512 (Varistor)
D_1	BYX10	BYX10	
R_1	18.7kΩ	18.7kΩ	1% tolerance
R_{NTC}	R_{25} = 22kΩ B = 4200k	R_{25} = 22kΩ B = 4200k	Cat. No. 2322 642 12223 (Thermistor)
R_P	22kΩ	22kΩ	Potentiometer
R_D	4.3kΩ	6.2kΩ	Power in R_D: A = 6.8W B = 4.8W
R_G	110Ω	110Ω	
R_S	430kΩ	180kΩ	
C_1	47nF	47nF	
C_S	220μF, 16V	220μF, 16V	
C_T	15μF (DC)	68μF (DC)	See Table 3
C_D*	680nF	470nF	
R_{SD}*	390Ω	390Ω	Power in R_{SD}: A = 1.2W B = 0.6W

NOTE:
*C_D and R_{SD} only required if used in place of D_1 and R_D.

Table 12. Temperature Controller Component Value
Mains Supply: 220V, 50Hz Heater Power: 2000W

COMPONENT	TYPE/VALUE	REMARKS
Triac	BT139	
VDR	350V, 1mA	Cat. No. 2322 594 13912 (Varistor)
D_1	BYX10	
R_1	18.7kΩ	1% tolerance
R_{NTC}	R_{25} = 22kΩ B = 4200k	Cat. No. 2322 642 12223 (Thermistor)
R_P	22kΩ	Potentiometer
R_D	6.8kΩ	Power in R_D = 4.3W
R_G	110Ω	
R_S	150kΩ	
C_1	47nF	
C_S	220μF, 16V	
C_T	47μF	Cat No. 2222 016 90129

Design of Time-Proportional Temperature Controls Using the TDA1023


AC LINE
D1
HEATER
R_S
R_D
R2
11
14
10
16
9
TDA1023
3
TRIAC
VARISTOR
C_S
R_P
6
7
R_G
12
13
R1
C_T
AC LINE (NEUT.)
LD06701S

R_1 = 4.7 kΩ
R_2 = 4.7 kΩ
R_P = 47 kΩ
R_D = 5.6 kΩ (7 W)
R_S = 220 kΩ
R_G = 110 Ω
C_S = 220 μF, 16V
C_T = 47 μF, 25V
D_1 = BYX10
TRIAC = BT139
VDR = ZnO, 350V, 1mA (VARISTOR)

NOTE:
Component values are for a load power of 2kW from 220V, 50Hz supplies.

Figure 25. Circuit Using the TDA1023 for Time-Proportional Power Regulation

NOTE:
Previously published as Technical Information 025, March 1, 1977, ELCOMA, the Netherlands.

Section 9
Packaging Information

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Signetics

Substrate Design Guidelines for Surface-Mounted Devices

Linear Products

INTRODUCTION

SMD technology embodies a totally new automated circuit assembly process using a new generation of electronic components: surface-mounted devices (SMDs). Smaller than conventional components, SMDs are placed onto the surface of the substrate, not through it like leaded components. And from this, the fundamental difference between SMD assembly and conventional through-hole component assembly arises; SMD component positioning is relative, not absolute.

When a through-hole (leaded) component is inserted into a PCB, either the leads go through the holes, or they don't. An SMD, however, is placed onto the substrate surface, its position only relative to the solderlands, and placement accuracy is therefore influenced by variations in the substrate track pattern, component size, and placement machine accuracy.

Other factors influence the layout of SMD substrates. For example, will the board be a mixed-print (a combination of through-hole components and SMDs) or an all-SMD design? Will SMDs be on one side of the substrate or both? And there are process considerations, such as: what type of machine will place the components and how will they be soldered?

Using our expertise in the world of SMD technology, this section draws upon applied research in the area of substrate design and manufacture, and presents the basic guidelines to assist the designer in making the transition from conventional through-hole PCB assembly to SMD substrate manufacture.

Designing With SMD

SMD technology is penetrating rapidly into all areas of modern electronic equipment manufacture — in professional, industrial, and consumer applications. Boards are made with conventional print-and-etch PCBs, multilayer boards with thick film ceramic substrates, and with a host of new materials specially developed for SMD assembly.

However, before substrate layout can be attempted, footprints for all components must be defined. Such a footprint will include the combination of patterns for the copper solderlands, the solder resist, and, possibly, the solder paste. So the design of a substrate breaks down into two distinct areas: the SMD footprint definition, and the layout and track routing for SMDs on the substrate. Each of these areas is treated individually; first, the general aspects of SMD technology, including substrate configurations, placement machines, and soldering techniques, are discussed.

Substrate Configurations

SMD substrate assembly configurations are classified as:

Type I — Total surface mount (all-SMD); substrates with no through-hole components at all. SMDs of all types (SM integrated circuits, discrete semiconductors, and passive devices) can be mounted either on one side, or both sides, of the substrate. See Figure 1a.

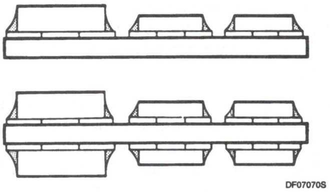
Type IIA — Double-sided mixed-print; substrates with both through-hole components and SMDs of all types on the top, and smaller SMDs (transistors and passives) on the bottom. See Figure 1b.

Type IIB — Underside attachment mixed-print; the top of the substrate is dedicated exclusively to through-hole components, with smaller SMDs (transistor and passives) on the bottom. See Figure 1c.

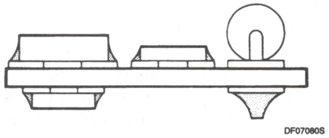
Although the all-SMD substrate will ultimately be the cheapest and smallest variation as there are no through-hole components, it's the mixed-print substrate that many manufacturers will be looking to in the immediate future, for this technique enjoys most of the advantages of SMD assembly and overcomes the problem of non-availability of some components in surface-mounted form.

The underside attachment variation of the mixed-print (type IIB — which can be thought of as a conventional through-hole assembly with SMDs on the solder side) has the added advantages of only requiring a single-sided, print-and-etch PCB and of using the established wave soldering technique. The all-SMD and mixed-print assembly with SMDs on both sides require reflow or combination wave/reflow soldering, and, in most cases, a double-sided or multilayer substrate.

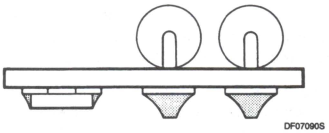
The relatively small size of most SMD assemblies compared with equivalent through-hole designs means that circuits can often be repeated several times on a single substrate. This multiple-circuit substrate technique (shown in Figure 2) further increases production efficiency.



a. Type I — Total Surface-Mount (all-SMD) Substrates



b. Type IIA — Mixed-Print (Double-Sided) Substrate



c. Type IIB — Mixed-Print (Underside Attachment) Substrate

Figure 1

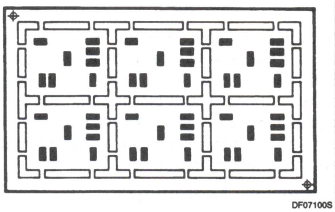


Figure 2. Multiple-Circuit Substrate

Mixed Prints

The possibility of using a partitioned design should be investigated when considering the mixed-print substrate option. For this, part of the circuit would be an all-SMD substrate, and the remainder a conventional through-hole

PCB or mixed-print substrate. This allows the circuit to be broken down into, for example, high and low power sections, or high and low frequency sections.

Automated SMD Placement Machines

The selection of automated SMD placement machines for manufacturing requirements is an issue reaching far beyond the scope of this section. However, as a guide, the four main placement techniques are outlined. They are:

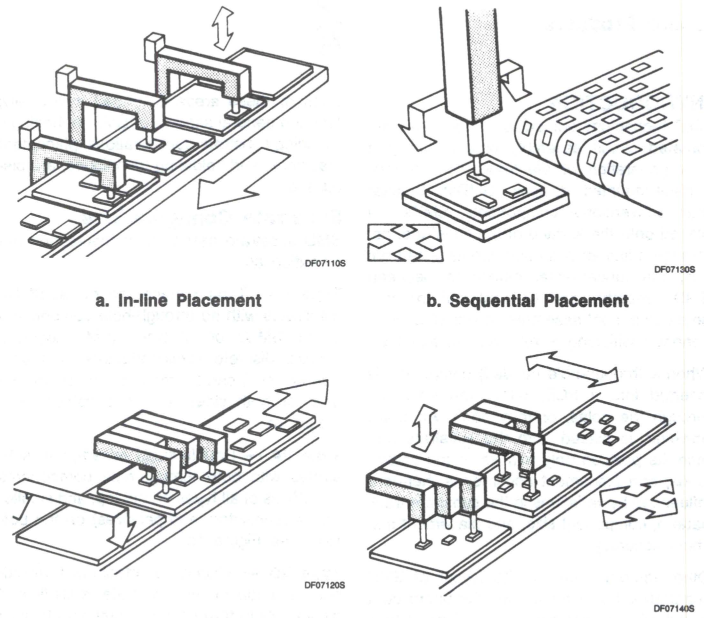
In-Line Placement — a system with a series of dedicated pick-and-place units, each placing a single SMD in a preset position on the substrate. Generally used for small circuits with few components. See Figure 3a.

Sequential Placement — a single pick-and-place unit sequentially places SMDs onto the substrate. The substrate is positioned below the pick-and-place unit using a computer-controlled X-Y moving table (a "software programmable" machine). See Figure 3b.

Simultaneous Placement — places all SMDs in a single operation. A placement module (or station), with a number of pick-and-place units, takes an array of SMDs from the packaging medium and simultaneously places them on the substrate. The pick and place units are guided to their substrate location by a program plate (a "hardware programmable" machine), or by software-controlled X-Y movement of substrate and/or pick-and-place units. See Figure 3c.

Sequential/Simultaneous Placement — a complete array of SMDs is transferred in a single operation, but the pick-and-place units within each placement module can place all devices simultaneously, or individually (sequentially). Positioning of the SMDs is software-controlled by moving the substrate on an X-Y moving table, by X-Y movement of the pick-and-place units, or by a combination of both. See Figure 3d.

All four techniques, although differing in detail, use the same two basic steps: picking the SMD from the packaging medium (tape, magazine, or hopper) and placing it on the substrate. In all cases, the exact location of each SMD must be programmed into the automated placement machine.



a. In-line Placement

b. Sequential Placement

c. Simultaneous Placement

d. Sequential/Simultaneous Placement

Figure 3

Soldering Techniques

The SMD-populated substrate is soldered by conventional wave soldering, reflow soldering, or a combination of both wave and reflow soldering. These techniques are covered at length in another publication entitled *SMD Soldering Techniques*, but, briefly, they can be described as follows:

Wave Soldering — the conventional method of soldering through-hole component assemblies where the substrate passes over a wave (or more often, two waves) of molten solder. This technique is favored for mixed-print assemblies with through-hole components on the top of the substrate, and SMDs on the bottom.

Reflow Soldering — a technique originally developed for thick-film hybrid circuits using a solder paste or cream (a suspension of fine solder particles in a sticky resin-flux base) applied to the substrate which, after component placement, is heated and causes the solder to melt and coalesce. This method is predominantly used for Type I (all-SMD) assemblies.

Combination Wave/Reflow Soldering — a sequential process using both the foregoing techniques to overcome the problems of soldering a double-sided mixed-print substrate with SMDs and through-hole components on the top, and SMDs only on the bottom. (Type IIB).

Footprint Definition

An SMD footprint, as shown in Figure 4, consists of:

- A pattern for the (copper) solderlands
- A pattern for the solder resist
- If applicable, a pattern for the solder cream.

The design for the footprint can be represented as a set of nominal coordinates and dimensions. In practice, the actual coordinates of each pattern will be distributed around these nominal values due to positioning and processing tolerances. Therefore, the coordinates are stochastic; the actual values form a probability distribution, with a mean value (the nominal value) and a standard deviation.

The coordinates of the SMD are also stochastic. This is due to the tolerances of the actual component dimensions and the positional errors of the automated placement machine.

The relative positions of solderland, solder resist pattern, and SMD, are not arbitrary. A number of requirements may be formulated concerning clearances and overlaps. These include:

- Limiting factors in the production of the patterns (for example, the spacing between solderlands or tracks has a minimum value)

Substrate Design Guidelines for Surface-Mounted Devices

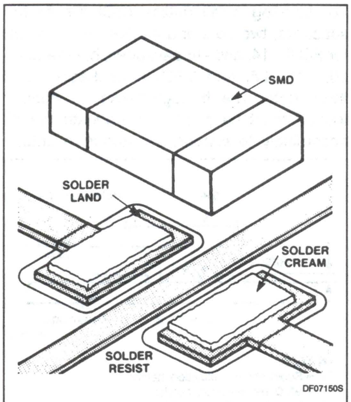


Figure 4. Component Lead, Solder Land, Solder Resist, and Solder Cream "Footprint"

- Requirements concerning the soldering process (for example, the solderlands must be free of solder resist)
- Requirements concerning the quality of the solder joint (for example, the solderland must protrude from the SMD metallization to allow an appropriate solder meniscus)

Mathematical elaboration of these requirements and substitution of values for all tolerances and other parameters lead to a set of inequalities that have to be solved simultaneously. To do this manually using worst-case design is not considered realistic. A better approach is to use a statistical analysis; although this requires a complex computer program, it can be done.

Such an approach may deliver more than one solution, and, if this is so, then the optimal solution must be determined. Optimization is achieved by setting the following objective — find the solution that:

- Minimizes the area occupied by the footprint
- Maximizes the number of tracks between adjacent solderlands.

The final SMD footprint design also depends on the soldering process to be used. The requirements for a wave-soldered substrate differ from those for a reflow-soldered substrate, so each is discussed individually.

Footprints for Wave Soldering

To determine the footprint of an SMD for a wave-soldered substrate, consider four main interactive factors:

- The component dimensions plus tolerances — determined by the component manufacturer
- The substrate metallization — positional tolerance of the solderland with respect to a reference point on the substrate
- The solder resist — positional tolerance of the solder resist pattern with respect to the same reference point
- The placement tolerance — the ability of an automated placement machine to accurately position the SMD on the substrate.

The coordinates of patterns and SMDs have to meet a number of requirements. Some of these have a general validity (the minimum overlap of SMD metallization and solderland) and available space for solder meniscus. Others are specifically required to allow successful wave soldering. One has to take into account factors like the "shadow effect" (missing of joints due to high component bodies), the risk of solder bridging, and the available space for a dot of adhesive.

The "Shadow Effect"

In wave soldering, the way in which the substrate addresses the wave is important. Unlike wave soldering of conventional printed boards where there are no component bodies to restrict the wave's freedom to traverse across the whole surface, wave soldering of SMD substrates is inhibited by the presence of SMDs on the solder-side of the board. The solder is forced around and over the SMDs as shown in Figure 5a, and the surface tension of the molten solder prevents its reaching the far end of the component, resulting in a dry-joint downstream of the solder flow. This is known as the "shadow effect."

The shadow effect becomes critical with high component bodies. However, wetting of the solderlands during wave soldering can be improved by enlarging each land as shown in Figure 5b. The extended substrate metallization makes contact with the solder and allows it to flow back and around the component metallization to form the joint.

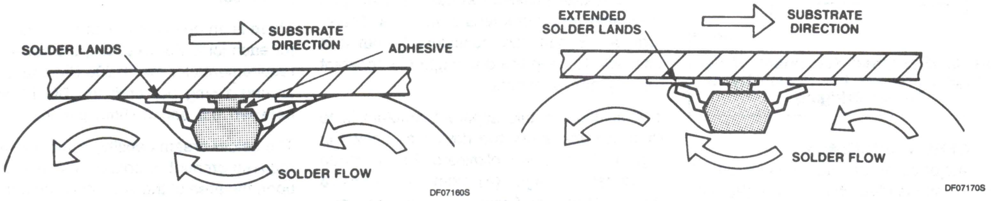
The use of the dual-wave soldering technique also partially alleviates this problem because the first, turbulent wave has sufficient upward pressure to force solder onto the component metallization, and the second, smooth wave "washes" the substrate to form good fillets of solder. Similarly, oil on the surface of the solder wave lowers the surface tension, (which lessens the shadow effect), but this technique introduces problems of contaminants in the solder when the oil decomposes.

Footprint Orientation

The orientation of SO (small outline) and VSO (very small outline) ICs is critical on wave-soldered substrates for the prevention of solder bridge formation. Optimum solder penetration is achieved when the central axis of the IC is parallel to the flow of solder as shown in Figure 6a. The SO package may also be transversely oriented, as shown in Figure 6b, but this is totally unacceptable for the VSO package.

Solder Thieves

Even with parallel mounted SO and VSO packages, solder bridges have a tendency to form on the leads downstream of the solder flow. The use of solder thieves (small squares of substrate metallization), shown in Figure 7 for a 40-pin VSO, further reduces the likelihood of solder-bridge formation.

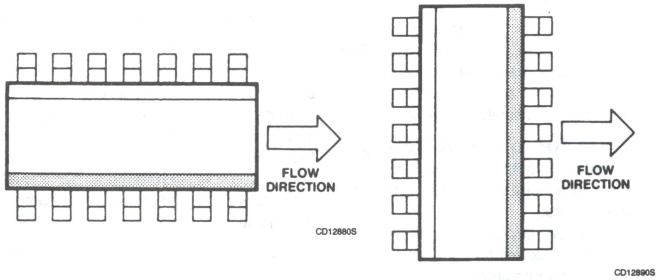


a. Surface Tension Can Prevent the Molten Solder From Reaching the Downstream End of the SMD, Known as the "Shadow Effect"

b. Extending the Solder Lands to Overcome the Shadow Effect

Figure 5

Substrate Design Guidelines for Surface-Mounted Devices



a. Parallel Orientation for SO and VSO Packages

b. Transverse Orientation for SO Packages Only

Figure 6

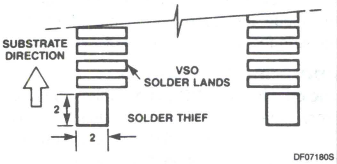


Figure 7. Example of Solder Thieves for VSO-40 Footprints (Dims in mm)

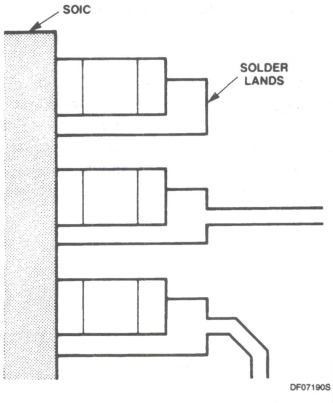


Figure 8. Misaligned Placement of SO Package Increases the Possibility of Solder Bridging

Placement Inaccuracy

Another major cause of solder bridges on SO ICs and plastic leaded chip carriers (PLCCs) is a slight misalignment as shown in Figure 8. The close spacing of the leads on these devices means that any inaccuracy in placement drastically reduces the space between adjacent pins and solderlands, thus increasing the chance of solder bridges forming.

Dummy Tracks for Adhesive Application

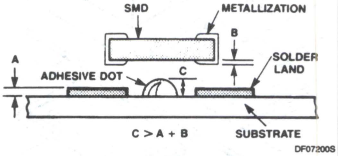
For wave soldering, an adhesive to affix components to the substrate is required. This is necessary to hold the SMDs in place between the placement operation and the soldering process (this technique is covered at length in another publication entitled *Adhesive Application and Curing*).

The amount of adhesive applied is critical for two reasons: first, the adhesive dot must be high enough to reach the SMD, and, second, there mustn't be too much adhesive which could foul the solderland and prevent the formation of a solder joint. The three parameters governing the height of the adhesive dot are shown in Figure 9. Although this diagram illustrates that the minimum requirement is $C > A + B$, in practice, $C > 2(A + B)$ is more realistic for the formation of a good strong bond.

Taking these parameters in turn, the substrate metallization height (A) can range from about 35μm for a normal print-and-etch PCB to 135μm for a plated through-hole board. And the component metallization height (B) (on 1206-size passive devices, for example) may differ by several tens of microns. Therefore, $A + B$ can vary considerably, but it is desirable to keep the dot height (C) constant for any one substrate.

The solution to this apparent problem is to route a track under the device as shown in Figure 10. This will eliminate the substrate metallization height (A) from the adhesive dot-height criteria. Quite often, the high component density of SMD substrates necessitates the routing of tracks between solderlands, and, where it does not, a short dummy track should be introduced.

For bonding small outline (SO) ICs to the substrate, two dots of adhesive are sufficient for SO-8, -14, and -16 packages, but the SOL-20, -24, -28, and VSO-40 packages need three dots. The through-tracks (or dummy tracks) must be positioned beneath the IC accordingly to support the adhesive dots.



NOTES:
A = Substrate metallization height
B = SMD metallization height
C = Height of adhesive dot

Figure 9. Adhesive Dot Height Criteria

Footprints for Reflow Soldering

To determine the footprint of an SMD for a reflow-soldered substrate, there are now five interactive factors to consider: the four that affect the wave solder footprints (although the solder resist may be omitted), plus an additional factor relating to the solder cream application (the positional tolerance of the screen-printed solder cream with respect to the solderlands).

Solder Cream Application

In reflow soldering, the solder cream (or paste) is applied by pressure syringe dispensing or by screen printing. For industrial purposes, screen printing is the favored technique because it is much faster than dispensing.

Screen Printing

A stainless steel mesh coated with emulsion (except for the solderland pattern where cream is required) is placed over the substrate. A squeegee passes across the screen and forces solder cream through the uncoated areas of the mesh and onto the solderland. As a result, dots of solder cream of a given height and density (in mg/mm^2) are produced.

There is an optimum amount of solder cream for each joint. For example, the solder cream requirements for the C1206 SM capacitor are around 1.5mg per end; the SO IC requires between 0.5 and 0.75mg per lead.

The solder cream density, combined with the required amount of solder, makes a demand upon the area of the solderland (in mm^2). The footprint dimensions for the solder cream pattern are typically identical to those for the solderlands.

Substrate Design Guidelines for Surface-Mounted Devices

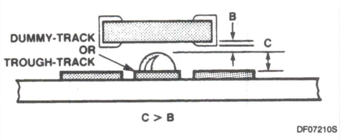


Figure 10. Through-Track or Dummy Track to Modify Dot Height Criteria

Floating

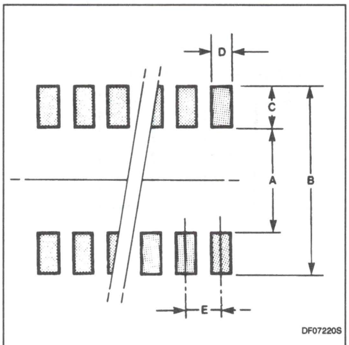
One phenomenon sometimes observed on reflow-soldered substrates is that known as "floating" (or "swimming"). This occurs when the solder paste reflows, and the force exerted by the surface tension of the now molten solder "pulls" the SMD to the center of the solderland.

When the solder reflows at both ends simultaneously, the swimming phenomenon results in the SMD self-centering on the footprint as the forces of surface tension fight for equilibrium. Although this effect can remove minor positional errors, it's not a dependable feature and cannot be relied upon. Components must always be positioned as accurately as possible.

Footprint Dimensions

The following diagrams (Fig. 11 to 19) show footprint dimensions for SO ICs, the VSO-40 package, PLCC packages, and the range of surface-mounted transistors, diodes, resistors, and capacitors. All dimensions given are based on the criteria discussed in these guidelines.

Please note — these footprints are based on our experience with both experimental and actual production substrates and are reproduced for guidance only. Research is constantly going on to cover all SMDs currently available and those planned for in the future, and data will be published when in it becomes available.



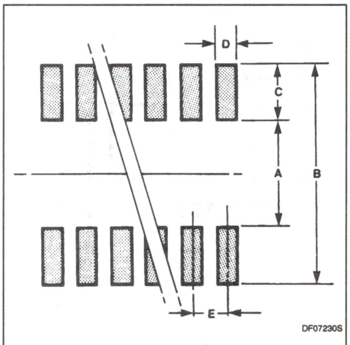
PACKAGE OUTLINE	INCHES A	B	C	D	E
SO-8, 14, 16	.155	.275	.060	.024	.050
SOL-16, 20, 24, 28	.310	.450	.070	.024	.050

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
SO SMALL	4.0	7.0	1.5	.6	1.27
SO LARGE	7.8	11.4	1.8	.6	1.27

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
SOL-8	9.0	13.2	2.1	.6	1.27

PACKAGE OUTLINE	INCHES A	B	C	D	E
SOL-8	.36	.528	.084	.024	.050

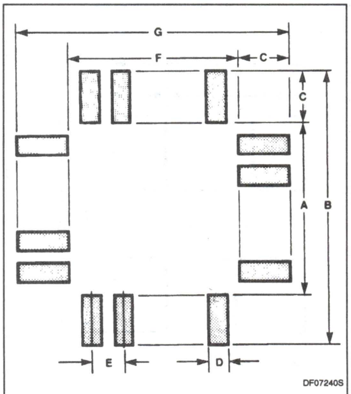
Figure 11. Footprints for SO ICs



PACKAGE OUTLINE	INCHES A	B	C	D	E
VSO-40	.32	.536	.108	.02	.030
VSO-56	.46	.676	.108	.02	.030

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
VSO-40	8.0	13.4	2.7	.5	.762
VSO-56	11.5	16.9	2.7	.5	.75

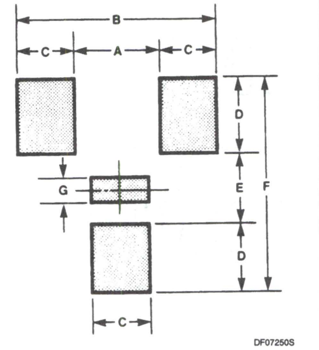
Figure 12. Footprints for VSO ICs



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G
PLCC-20	.260	.440	.090	.024	.050	.260	.440
PLCC-28	.360	.540	.090	.024	.050	.360	.540
PLCC-44	.560	.740	.090	.024	.050	.560	.740
PLCC-52	.660	.840	.090	.024	.050	.660	.840
PLCC-68	.860	1.040	.090	.024	.050	.860	1.040
PLCC-84	1.060	1.240	.090	.024	.050	1.060	1.240
PLCC-32	.360	.540	.090	.024	.050	.460	.640

Figure 13. Footprints for PLCCs

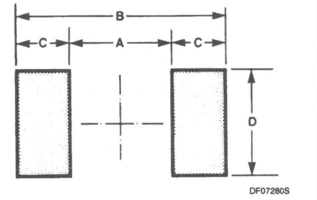
Substrate Design Guidelines for Surface-Mounted Devices



SOT-23	INCHES A	B	C	D	E	F
Reflow	0.048	0.104	0.028	0.044	0.104	—
Wave	0.032	0.136	0.052	0.052	0.048	0.152

SOT-23	METRIC (mm) A	B	C	D	E	F
Reflow	1.2	2.6	0.7	1.1	2.6	—
Wave	0.8	3.4	1.3	1.3	1.2	3.8

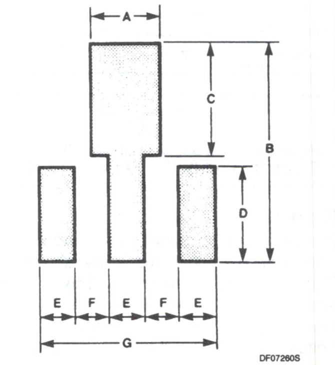
Figure 14. Footprints for SOT-23 Transistors



SOD-80	INCHES A	B	C	D
Reflow	0.096	0.208	0.056	0.056
Wave	0.10	0.2	0.05	0.08

SOD-80	METRIC (mm) A	B	C	D
Reflow	2.4	5.2	1.4	1.4
Wave	2.5	5.0	1.25	2.0

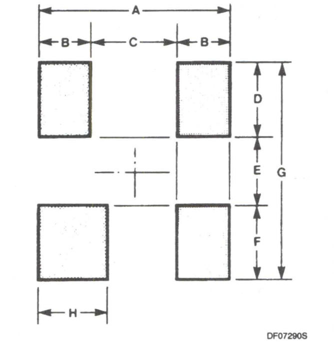
Figure 15. Footprints for SOD-80 Diodes



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G
SOT-89	0.08	0.184	0.104	0.048	0.032	0.028	0.152

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E	F	G
SOT-89	2.0	4.6	2.6	1.2	0.8	0.7	3.8

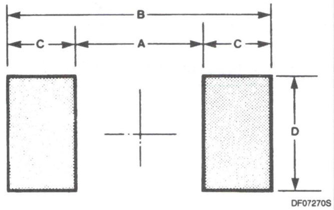
Figure 16. Footprints for Reflow-Soldered SOT-89 Transistors



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G	H
SOT-143	0.104	0.028	0.048	0.036	0.044	0.036	0.116	0.044

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E	F	G	H
SOT-143	2.6	0.7	1.2	0.9	1.1	0.9	2.0	1.1

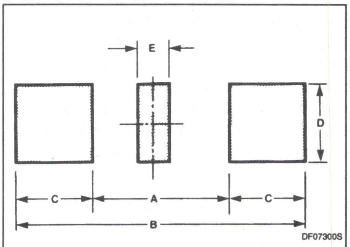
Figure 17. Footprints for Reflow-Soldered SOT-143 Transistors



CODE	SIZE	INCHES A	B	C	D
C0805	0.08 × 0.05	0.032	0.136	0.052	0.056
R/C1206	0.128 × 0.064	0.072	0.184	0.056	0.068
C1210	0.128 × 0.1	0.072	0.184	0.056	0.104
C1808	0.18 × 0.08	0.112	0.248	0.068	0.084
C1812	0.18 × 0.128	0.112	0.248	0.068	0.132
C2220	0.228 × 0.2	0.16	0.296	0.068	0.204

CODE	SIZE	METRIC (mm) A	B	C	D
C0805	2.0 × 1.25	0.8	3.4	1.3	1.4
R/C1206	3.2 × 1.6	1.8	4.6	1.4	1.7
C1210	3.2 × 2.5	1.8	4.6	1.4	2.6
C1808	4.5 × 2.0	2.8	6.2	1.7	2.1
C1812	4.5 × 3.2	2.8	6.2	1.7	3.3
C2220	5.7 × 5.0	4.0	7.4	1.7	5.1

Figure 18. Footprints for Reflow-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors



	SIZE	INCHES A	B	C	D	E
C0805	0.08 × 1.05	0.048	0.144	0.048	0.048	0.016
R/C1206	0.128 × .064	0.08	0.192	0.056	0.056	0.020

CODE	SIZE	METRIC (mm) A	B	C	D	E
C0805	2.0 × 1.25	1.2	3.6	1.2	1.2	0.4
R/C1206	3.2 × .6	2.0	4.8	1.4	1.4	0.5

Figure 19. Footprints for Wave-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors

Substrate Design Guidelines for Surface-Mounted Devices

Layout Considerations

Component orientation plays an important role in obtaining consistent solder-joint quality. The substrate layout shown in Figure 20 will result in significantly better solder joints than a substrate with SMD resistors and capacitors positioned parallel to the solder flow.

Component Pitch

The minimum component pitch is governed by the maximum width of the component and the minimum distance between adjacent components. When defining the maximum component width, the rotational accuracy of the placement machine must also be considered. Figure 21 shows how the effective width of the SMD is increased when the component is rotated with respect to the footprint by angle $\phi°$. (For clarity, the rotation is exaggerated in the illustration.)

The minimum permissible distance between adjacent SMDs is a figure based upon the gap required to avoid solder-bridging during the wave soldering process. Figure 22 shows how this distance and the maximum component width are combined to derive the basic expression for calculating the minimum pitch (F_{MIN}).

As a guide, the recommended minimum pitches for various combinations of two sizes of SMDs, the R/C1206 and C0805 (R or C designating resistor or capacitor respectively; the number referring to the component size), are given in Table 1. These figures are statistically derived under certain assumed boundary conditions as follows:

- Positioning error (Δp)± 0.3mm; (± 0.012")
- Pattern accuracy (Δq)± 0.3mm; (± 0.012")
- Rotational accuracy (ϕ)± 3°
- Component metallization/solderland overlap (M_{MIN}) 0.1mm (0.004") (Note this figure is only valid for wave soldering)
- The figure for the minimum permissible gap between adjacent components (G_{MIN}) is taken to be 0.5mm (0.020").

As these calculations are not based on worst-case conditions, but on a statistical analysis of all boundary conditions, there is a certain flexibility in the given data.

For example, it is possible to position R/C1206 SMDs on a 2.5mm pitch, but the probability of component placements occurring with G_{MIN} smaller than 0.5mm will increase; hence, the likelihood of solder-bridging also increases. Each application must be assessed on individual merit with regard to acceptable levels of rework, and so on.

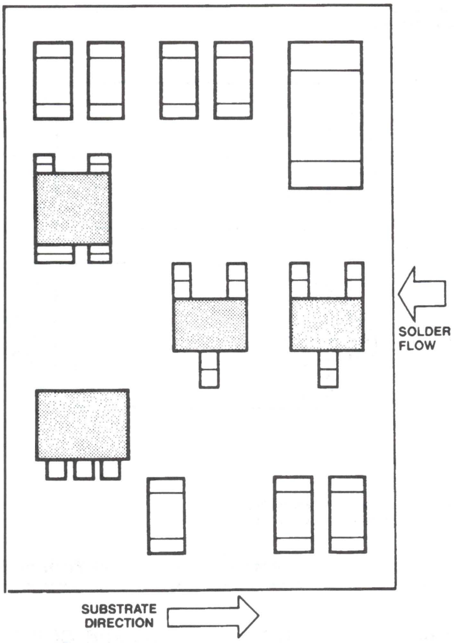
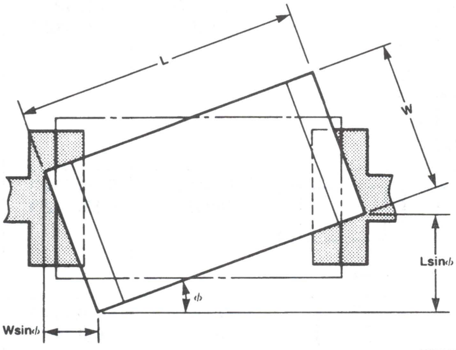


Figure 20. Recommended Component Orientation for Wave-Soldered Substrates



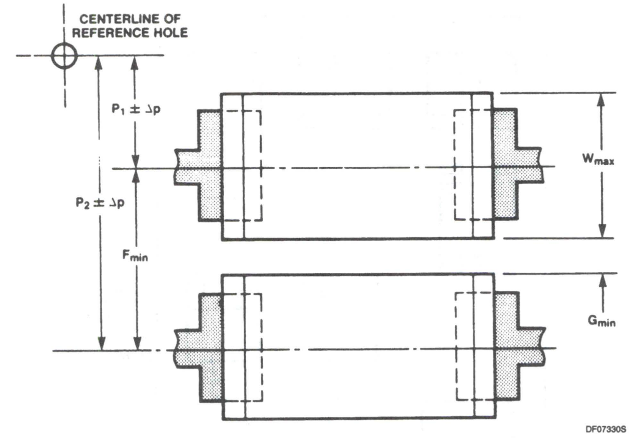
NOTES:
ϕ = Component rotation with respect to footprint
L sin ϕ = Effective increase in width
W sin ϕ = Effective increase in length

Figure 21. The Influence of Rotation of the SMD With Respect to the Footprint

Solderland/Via Hole Relationship

With reflow-soldered multilayer and double-sided, plated through-hole substrates, there must be sufficient separation between the via holes and the solderlands to prevent a solder well from forming. If too close to a solder joint, the via hole may suck the molten solder away from the component by capillary action; this results in insufficient wetting of the joint.

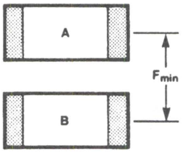
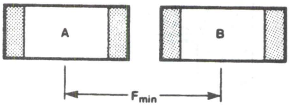
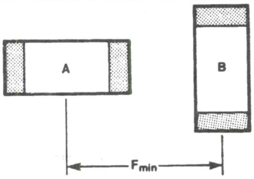
Substrate Design Guidelines for Surface-Mounted Devices



NOTES:
W_{MAX} = Maximum width of component
G_{MIN} = Minimum permissible gap
F_{MIN} = Minimum pitch
P_1 = Nominal position of component 1 (tolerance Δp)
P_2 = Nominal position of component 2 (tolerance Δp)
$F_{MIN} = W_{MAX} + 2\Delta p + G_{MIN}$

Figure 22. Criteria for Determining the Minimum Pitch of SMDs

Table 1. Recommended Pitch For R/C1206 and C0805 SMDs

Combination	Component A	Component B	
		R/C1206	C0805
	R/C1206 C0805	3.0(0.12") 2.8(0.112")	2.8(0.112") 2.6(0.0104")
	R/C1206 C0805	5.8(0.232") 5.3(0.212")	5.3(0.212") 4.8(0.192")
	R/C1206 C0805	4.1(0.164") 3.6(0.144")	3.7(0.148") 3.0(0.12")

Solderland/Component Lead Relationship

Of special consideration for mixed-print substrate layout is the location of leaded components with respect to the SMD footprints and the minimum distance between a protruding clinched lead and a conductor or SMD. Figure 23 shows typical configurations for R/C1206 SMDs mounted on the underside of a substrate with respect to the clinched leads of a leaded component. Minimum distances between the clinched lead ends and the SMDs or substrate conductors are 1mm (0.04") and 0.5 (0.02") respectively.

Placement Machine Restrictions

There are two ways of looking at the distribution of SMDs on the substrate: uniform SMD placement and non-uniform SMD placement. With nonuniform placement, center-to-center dimensions of SMDs are not exact multiples of a predetermined dimension as shown in Figure 24a, so the location of each is difficult to program into the machine.

Uniform placement uses a modular grid system with devices placed on a uniform center-to-center spacing. (For example, 2.5 (0.1") or 5mm (0.2") as shown in Figure 24b.) This placement has the distinct advantage of establishing a standard and enables the use of other automated placement machines for future production requirements without having to redesign boards.

Substrate Population

Population density of SMDs over the total area of the substrate must also be carefully considered, as placement machine limitations can create a "lane" or "zone" that restricts the total number of components which can be placed within that area on the substrate.

For example, on a hardware-programmable simultaneous placement machine (see Figure 3c), each pick-and-place unit within the placement module can only place a component on the substrate in a restricted lane (owing to

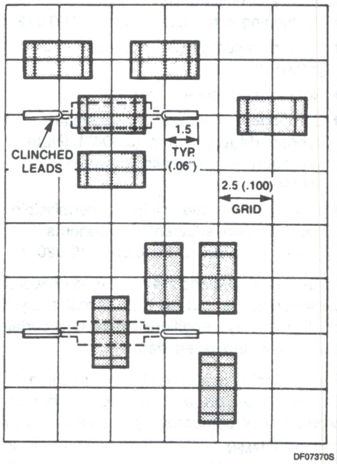
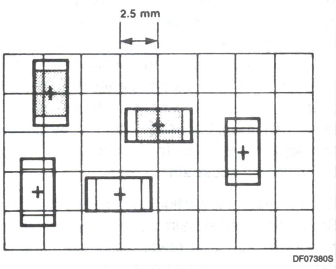
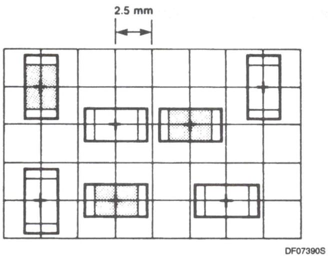


Figure 23. Location of R/C1206 SMDs on the Underside of a Mixed-Print Substrate with Respect to the Clinched Leads of Through-Hole Components (Dimensions in mm)

Substrate Design Guidelines for Surface-Mounted Devices



a. Non-Uniform Component Placement



b. Uniform Component Placement

Figure 24

adjacent pick-and-place units), typically 10 to 12mm (0.4" to 0.48") wide, as shown in Figure 25.

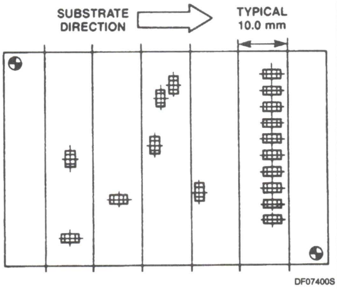


Figure 25. Substrate "Lanes" From Use of a Simultaneous Placement Machine

Placement of the 10 components in the lane on the right of the substrate shown will require a machine with 10 placement modules (or ten passes beneath a single placement module), an inefficient process considering that there are no more than three SMDs in any other lane.

Test Points

Siting of test points for in-circuit testing of SMD substrates presents problems owing to the fewer via holes, higher component densities, and components on both sides of SMD substrates. On conventional double-sided PCBs, the via holes and plated-through component lead-holes mean that most test-points are accessible from one side of the board. However, on SMD substrates, extra provision for test-points may have to be made on both sides of the substrate.

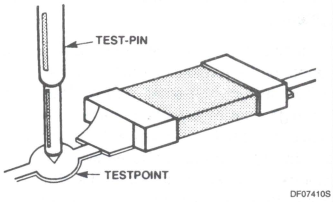
Figure 26a shows the recommended approach for positioning test-points in tracks close to components, and Figure 26b shows an acceptable (though not recommended) alternative where the solderland is extended to accommodate the test pin. This latter method avoids sacrificing too much board space, thus maintaining a high-density layout, but can introduce the problem of components moving ("floating") when reflow-soldered. The approach shown in Figure 26c is totally unacceptable since the pressure applied by the test pin can make an open-circuit soldered joint appear to be good, and, more importantly, the test pin can damage the metallization on the component, particularly with small SMDs.

CAD Systems for SMD Substrate Layout

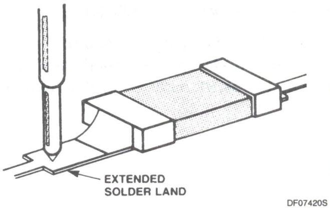
At present, about half of all PCBs are laid out using computer-aided design (CAD) techniques, and this proportion is expected to rise to over 90% by 1988. Of the many current CAD systems available for designing PCB layouts for conventional through-hole components and ICs in DIL packages, few are SMD-compatible, and systems dedicated exclusively to SMD substrate layout are still comparatively rare. There are two main reasons for this: some CAD suppliers are waiting for SMD technology to fully mature before updating their systems to cater to SMD-loaded substrates, and others are holding back until standard package outlines are fully defined.

However, updating CAD systems used for through-hole printed boards is not simply a case of substituting SMD footprints for conventional component footprints, since SMD-populated substrates impose far tougher restraints on PCB layout and require a total rethink of the layout programs. For example, systems must deal with higher component densities, finer track widths, devices on both sides of the substrate (possibly occupying corresponding positions on opposite sides), and even SMDs under conventional DILs on the same side of the substrate.

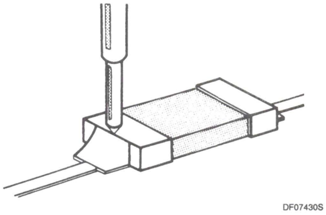
The amount of reworking that a program requires depends on whether it's an interactive (manual) system, or one with fully automatic routing and placement capabilities. For



a. RECOMMENDED Test Point Location Close to an SMD



b. Acceptable Test Point Location



c. UNACCEPTABLE Test Point Location

Figure 26

interactive systems, where the user positions the components and routes the tracks manually on-screen, program modifications will be minimal. Automatic systems, however, must contend with the stricter design rules for SMD substrate layout. For example, many autorouting programs assume that every solderland is a plated through-hole and, therefore, can be used as a via hole. This is not applicable for SMD-populated substrates.

CAD programs base the substrate layout on a regular grid. This method, analogous to drawing the layout on graph paper, must have the grid lines on a pitch that is no larger than the smallest component or feature (track width, pitch, and so on). For conventional DIL boards, this is typically 0.635mm (0.025"), but with the much smaller SMDs, a grid spacing of 0.0254mm (0.001") is required. Consequently, for the same area of substrate, a CAD system based on this finer grid requires a resolution more than 600 times greater than that required for conventional-layout CAD systems.

To handle this, extra memory capacity can be added, or the allowable substrate area can be limited. In fact, the small size of SMDs, and the high-density layouts possible, generally result in a smaller substrate. However, high-density layout gives rise to additional complications not directly related to the SMD substrate design guidelines. Most CAD systems, for instance, cannot always completely route all interconnects, and some traces have to be routed manually. This can be particularly difficult with the fewer via holes and smaller component spacing of SMD boards.

Ideally, the CAD program should have a "tear-up and start again" algorithm that allows it to restart autorouting if a previous attempt reaches a position where no further traces can be routed before an acceptable percentage of interconnects (and this percentage must first be determined) have been made. This minimizes the manual reworking required.

CAE/CAD/CAM Interaction

Computer-aided production of printed boards has evolved from what was initially only a computer-aided manufacturing process (CAM — digitizing a manually-generated layout and using a photoplotter to produce the artwork) to fully-interactive computer-aided engineering, design, and manufacture using a common database. Figure 27 illustrates how this multi-dimensional interaction is particularly well-suited to SMD-populated substrate manufacture in its highly-automated environment of pick-and-place assembly machines and test equipment.

Using a fully-integrated system, linked by local area network to a central database, will make it possible to use the initial computer-aided engineering (CAE — schematic design, logic verification, and fault simulation) in the generation of the final test patterns at the end of the development process. These test patterns can then be used with the automatic test equipment (ATE) for functional testing of the finished substrates.

Such a system is particularly useful for testing SMD-populated substrates, as their high component density and fewer via-holes make in-circuit testing ("bed of nails" approach) difficult. Consequently, manufacturers are turning to functional testing as an alternative. These aspects are covered in another publication entitled *Functional Testing and Repair.*

Substrate Design Guidelines for Surface-Mounted Devices

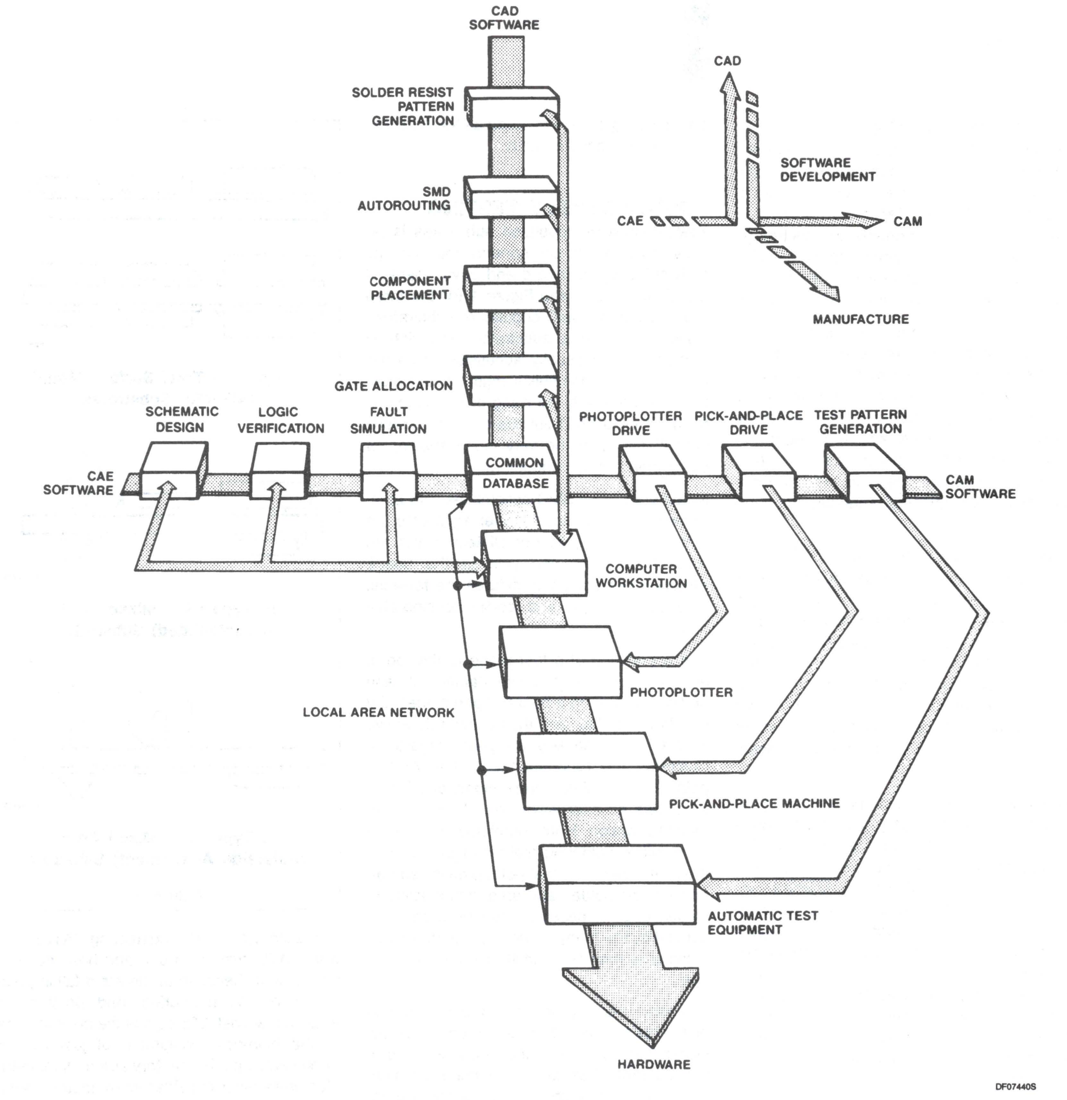

CAD SOFTWARE
SOLDER RESIST PATTERN GENERATION
SMD AUTOROUTING
COMPONENT PLACEMENT
GATE ALLOCATION
CAD
SOFTWARE DEVELOPMENT
CAE
CAM
MANUFACTURE
SCHEMATIC DESIGN
LOGIC VERIFICATION
FAULT SIMULATION
COMMON DATABASE
PHOTOPLOTTER DRIVE
PICK-AND-PLACE DRIVE
TEST PATTERN GENERATION
CAE SOFTWARE
CAM SOFTWARE
COMPUTER WORKSTATION
PHOTOPLOTTER
LOCAL AREA NETWORK
PICK-AND-PLACE MACHINE
AUTOMATIC TEST EQUIPMENT
HARDWARE
DF07440S

Figure 27. The Software-Hardware Interaction for the Computer-Aided Engineering, Design, and Manufacture of SMD Substrates

Signetics

Test and Repair

Linear Products

AN INTRODUCTION

The key questions that must be asked of any electronic circuit are "does it work, and will it continue to do so over a specified period of time?" Until zero-defect soldering is achieved, and all components are guaranteed serviceable by the vendors, manufacturers can only answer these questions by carrying out some form of test on the finished product.

The types of tests, and the depth to which they are carried out, are determined by the complexity of the circuit and the customer's requirements. The amount of rework to be performed on the circuit will depend on the results of these tests and the degree of reliability demanded. The criteria are true of all electronic assemblies, and the test engineer must formulate test schedules accordingly.

Substrates loaded with surface mounted devices (SMDs), however, pose additional problems to the test engineer. The devices are much smaller, and substrate population density is greater, leading to difficulty in accessing all circuit nodes and test points. Also SMD substrate layout designs often have fewer via and component lead holes, so test points may not all be on one side of the substrate and double-sided test fixtures become necessary.

To achieve the high throughput rates made possible by using highly automated SMD placement machines and volume soldering techniques, automatic testing becomes a necessity. Visual inspection of the finished substrate by trained inspectors can normally detect about 90% of defects. With the correct combination of automatic test equipment, the remainder can be eliminated. In this publication, we hope to provide the manufacturer with information to enable him to evaluate and select the best combination of test equipment and the most effective test methods for his product.

BARE-BOARD TESTING

Although SMD substrates will undoubtedly be smaller than conventional through-hole substrates and have less space between conductors, the principles of bare-board testing remain the same. Many of the testers already in use can, with little or no modification, be used for SMD substrates. As this is already a well-established and well-documented practice, it will not be discussed further in this publication, but it is recommended that bare-board testing always be used as the first step in assuring board integrity.

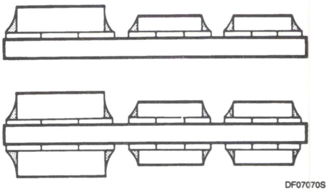
POST-ASSEMBLY TESTING

Testing densely populated substrates is no easy task, as the components may occupy both sides of the board and cover many of the circuit nodes (see Figure 1 for the three main types of SMD-populated substrates). Unlike conventional substrates, on which all test points are usually accessible from the bottom, SMD assemblies must be designed from the start with the siting of test points in mind. Probing SMD substrates is particularly difficult owing to the very close spacing of components and conductors.

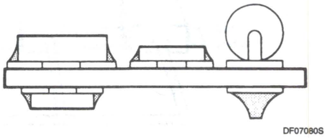
Mixed print or all-SMD assemblies with components on both sides further aggravate the testing problems, as not all test points are present on the same side of the board. Although two-sided test fixtures are feasible, they are expensive and require considerable time to build.

The application of a test probe to the top of an SMD termination could damage it, and probe pressure on a poor or open solder joint can force contact and thus allow a defective joint to be assessed as good. Figure 2a illustrates the recommended siting of test points close to SMD terminations, and Figure 2b shows an alternative, though not recommended, option. Here, problems could arise from reflow soldering (solder migrating from the joint) unless the test point area is separated from the solder land area with a stripe of solder resist. Excessive mechanical pressure caused by too many probes concentrated in a small area may also result in substrate damage.

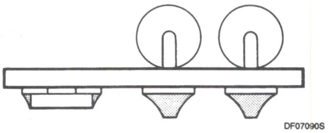
It is good practice for substrates to have test points on a regular grid so that conventional, rather than custom, testers may be used. If the substrate has tall components or heatsinks, the test points must be located far enough away to allow the probes to make good contact. All test points should be solder coated to provide good electrical contact. Via holes may also be used as test points, but the holes must be filled with solder to prevent the probe from sticking.



a. Type I — Total Surface Mount (All-SMD) Substrates



b. Type IIA — Mixed Print (Double-Sided) Substrate



c. Type IIB — Mixed Print (Underside Attachment) Substrate

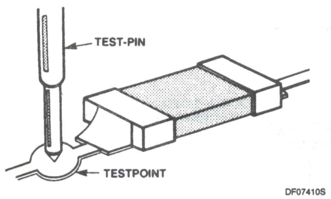
Figure 1

AUTOMATIC TEST EQUIPMENT (ATE)

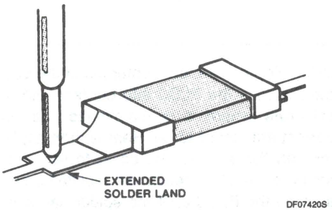
As manufacturers strive to increase production, the question becomes not whether to use automatic test engineering (ATE), but which ATE system to use and how much to spend on it. Because of the rapid fall in price of computers, memories, and peripherals, today's low-cost ATE equals the performance of the high-cost equipment of just two or three years ago. For factory automation, manufacturers must consider many factors, such as production volume, product complexity, and availability of skilled personnel.

One question is whether the ATE system can be used not only for production testing but also for service and repair to reduce the high cost of keeping a substrate inventory in the field. Another is whether assembly and process-induced faults represent a significant percentage of production defects, rather than out-of-tolerance components. These questions need to be answered before deciding on the type of ATE system required.

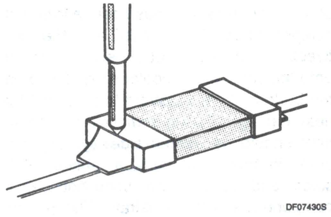
Test and Repair



a. Recommended Location of Test Points Close to SMDs



b. Acceptable, Though Not Recommended, Location of Test Points Close to SMDs



c. Unacceptable Location of Test Points Close to SMDs

Figure 2

Several systems are currently available to the manufacturer, including short-circuit testers, in-circuit testers, in-circuit analyzers, and functional testers. Figure 3 shows a bar-chart giving a comparison of percent fault detection and programming time for various ATE systems.

A loaded-board, short-circuit tester takes from two to six hours to program and its effective fault coverage is between 35% and 65%. It has the advantage of being operationally fast and comparatively inexpensive. On the negative side, however, it is limited to the detection of short-circuits and may require a double-sided, bed-of-nails test fixture (see Figure 4), which for SMD substrates may be expensive and take time to produce. Careful design can, however, often eliminate the need for double-sided test probe fixtures.

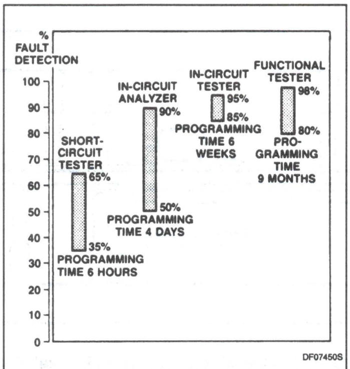


Figure 3. Bar Chart Showing a Comparison of Percent Fault Detection and Programming Time for Various ATE Systems

In-circuit testers power the assembly and check for open or short-circuits, circuit parameters, and can pinpoint defective components. They can provide around 90% fault coverage, but are more expensive than short-circuit testers and programming can take more than six weeks.

In-circuit analyzers are relatively simple to program and can detect manufacturing-induced faults in one third of the time required by an in-circuit tester. Fault coverage is between 50% and 90%. Because they do not power the assembly, they cannot detect digital logic faults, unlike an in-circuit tester or functional tester.

Functional testers, on the other hand, check the assembly's performance and simply make a go or no-go decision. Either the assembly performs its required function or it does not. They are much more expensive, but their fault coverage is between 80% and 98%. Their major disadvantages, apart from cost, are that they cannot locate defective components, and programming for a high-capacity system can take as long as nine months.

ATE Systems

An analysis of defects on a finished substrate will determine which combination of ATE will best meet the test requirements with regard to fault coverage and throughput rate.

If most defects are short-circuits, a loaded-board short-circuit tester, in tandem with an in-circuit tester, will pre-screen the substrate for short-circuits twice as fast as the in-circuit tester. This allows more time for the in-circuit tester to handle the more complex test requirements. This combination of ATE, instead of an in-circuit tester alone, improves the throughput rate.

Combining a short-circuit tester with a functional tester produces even more dramatic results. If most defects are manufacturing-produced shorts, the use of a short-circuit tester to relieve the functional tester of this task can increase throughput five-fold while maintaining a fault coverage of up to 98%.

If manufacturing faults and analog component defects are responsible for the majority of failures, a relatively low-cost, in-circuit analyzer can be used in tandem with an in-circuit tester or functional tester to reduce testing costs and improve throughput. The in-circuit analyzer is three times faster than an in-circuit tester in detecting manufacturing-induced faults, offers test and diagnostics usually within 10 seconds each, and is relatively simple to program. But because it is unpowered, an in-circuit analyzer cannot test digital logic faults; either an in-circuit tester or functional tester following the in-circuit analyzer must be used to locate this type of defect.

POLLUTED POWER SUPPLIES

Today's electronic components and the equipment used to test them are susceptible to electrical noise. Erroneous measurements on pass-or-fail tests could lower test throughput or, even more seriously, allow defective products to pass inspection. Semiconductor chips under test can also be damaged or destroyed as high-energy pulses or line-voltage surges stress the fine-line geometrics separating individual cells.

Noise pulses can be either in the normal (line-to-line) mode or common (line-to-ground) mode. Common-mode electrical noise poses a special threat to modern electronic circuitry since the safety ground line to which common-mode noise is referenced is often used as the system's logic reference point. Since parasitic capacitance exists between safety ground and the reference point, at high frequencies these points are essentially tied together, allowing noise to directly enter the system's logic.

MANUAL REPAIR

The repair of SMD-populated substrates will entail either the resoldering of individual joints and the removal of shorts or the replacement of defective components.

The reworking of defective joints will invariably involve the use of a manual soldering iron. Bits are commercially available in a variety of shapes, including special hollow bits used for desoldering and for the removal of solder bridges. The criteria for the inspec-

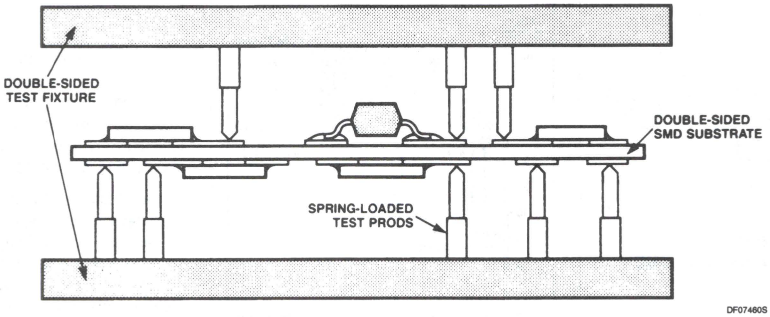


Figure 4. Double-Sided, Bed-of-Nails Test Fixture

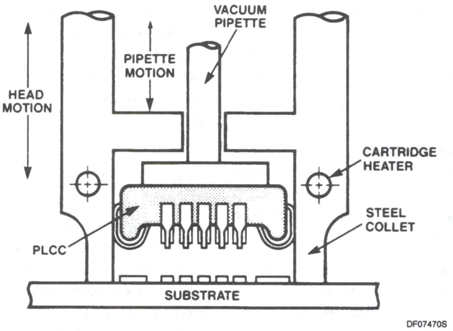


Figure 5. Heated Collet for the Removal and Replacement of Multi-Leaded SMDs (a PLCC is Shown Here)

tion of reworked soldered joints are the same as those for machine soldering.

Special care must be taken when reworking or replacing electrostatic sensitive devices. Soldering irons should be well grounded via a safety resistor of minimum 100kΩ. The ground connection to the soldering iron should be welded rather than clamped. This is because oxidation occurs beneath the clamp, thus isolating the ground connection. Voltage spikes caused by the switching of the iron can be avoided by using either continuously-powered irons, or irons that switch only at zero voltage on the AC sine curve.

To remove defective leadless SMDs, a variety of soldering iron bits are available that will apply the correct amount of heat to both ends of the component simultaneously and allow it to be removed from the substrate. If the substrate has been wave soldered, an adhesive will have been used, and the bond can be broken by twisting the bit. Any adhesive residue must then be removed. The same tool is then used to place and solder the new component, using either solder cream or resin-cored solder.

When a multi-leaded component, such as a plastic leaded chip carrier (PLCC), has to be removed, a heated collet can be used (see Figure 5). The collet is positioned over the PLCC, heat is applied to the leads and solder lands automatically until the solder reflows. The collet, complete with the PLCC, is then raised by vacuum. Solder cream is then reapplied to the solder lands by hand. No adhesive is required in this operation.

The collet is positioned over the replacement PLCC, which is held in place by the slight spring pressure of the PLCC leads against the walls of the collet. The collet, complete with PLCC, is then raised pneumatically and positioned over the solder lands. Using air pressure, the center pin of the collet then pushes the PLCC into contact with the substrate where it is maintained with the correct amount of force. Heat is then applied through the walls of the collet to reflow the solder paste. The center pin maintains pressure on the PLCC until the solder has solidified, then the center pin is raised and the replacement is complete.

Another method, well-suited to densely populated SMD substrates, uses a stream of heated air, directed onto the SMD terminations. Once the solder has been reflowed, the component can be removed with the aid of tweezers. While the hot air is being directed onto the component, cooler air is played onto the bottom of the substrate to protect it from heat damage. During removal, the component should be twisted sideways slightly in order to break the surface tension of the solder and any adhesive bond between the component and the substrate. This prevents damage to the substrate when the component is lifted.

To fit a new component, the solder lands are first retinned and fluxed, the new component accurately placed, and the solder reflowed with hot air. Substituting superheated argon, nitrogen, or a mixture of nitrogen and hydrogen for the hot air stream removes any risk of contaminating or oxidizing the solder.

Focused infrared light has also been used successfully to reflow the solder on densely populated substrates.

In general, the equipment and procedures used for the replacement of PLCCs can be used for leadless ceramic chip carriers (LCCCs) and small-outline packages (SO ICs). SO ICs are somewhat easier to replace, as the leads are more accessible and only on two sides of the component.

Fluxing and Cleaning

INTRODUCTION

The adoption of mass soldering techniques by the electronics industry was prompted not only by economics, and a requirement for high throughput levels, but also by the need for a consistent standard of quality and reliability in the finished product unattainable by using manual methods. With surface-mounted device (SMD) assembly, this need is even greater.

The quality of the end-product depends on the measures taken during the design and manufacturing stages. The foundations of a high-quality electronic circuit are laid with good design, and with correct choice of components and substrate configuration. It is, however, at the manufacturing stage where the greatest number of variables, both with respect to materials and techniques, have to be optimized to produce high-quality soldering, a prerequisite for reliability.

Of the two most commonly-used soldering techniques, wave and reflow, wave soldering is by far the most widely used and understood. Many factors influence the outcome of the soldering operation, some relating to the soldering process itself, and others to the condition of components and substrate to which they are to be attached. These must be collectively assessed to ensure high-quality soldering.

One of the most important, most neglected, and least understood of these processes is the choice and application of flux. This section outlines the fluxing options available, and discusses the various cleaning techniques that may be required, for SMD substrate assembly.

FLUXES

Populating a substrate involves the soldering of a variety of terminations simultaneously. In one operation, a mixture of tinned copper, tin/lead-or gold-plated nickel-iron, palladium-silver, tin/lead-plated nickel-barrier, and even materials like Kovar, each possessing varying degrees of solderability, must be attached to a common substrate using a single solder alloy.

It is for this reason that the choice of the flux is so important. The correct flux will remove surface oxides, prevent reoxidization, help to transfer heat from source to joint area, and leave non-corrosive, or easily removable corrosive residues on the substrate. It will also improve wettability of the solder joint surfaces.

The wettability of a metal surface is its ability to promote the formation of an alloy at its interface with the solder to ensure a strong, low-resistance joint.

However, the use of flux does not eliminate the need for adequate surface preparation. This is very important in the soldering of SMD substrates, where any temptation to use a highly-active flux in order to promote rapid wetting of ill-prepared surfaces should be avoided because it can cause serious problems later when the corrosive flux residues have to be removed. Consequently, optimum solderability is an essential factor for SMD substrate assembly.

Flux is applied before the wave soldering process, and during the reflow soldering process (where flux and solder are combined in a solder cream). By coating both bare metal and solder, flux retards atmospheric oxidization which would otherwise be intensified at soldering temperature. In the areas where the oxide film has been removed, a direct metal-to-metal contact is established with one low-energy interface. It is from this point of contact that the solder will flow.

Types of Flux

There are two main characteristics of flux. The first is efficacy—its ability to promote wetting of surfaces by solder within a specified time. Closely related to this is the activity of the flux, that is, its ability to chemically clean the surfaces.

The second is the corrosivity of the flux, or rather the corrosivity of its residues remaining on the substrate after soldering. This is again linked to the activity; the more active the flux, the more corrosive are its residues.

Although there are many different fluxes available, and many more being developed, they fall into two basic categories; those with residues soluble in organic liquids, and those with residues soluble in water.

Organic Soluble Fluxes

Most of the fluxes soluble in organic liquids are based on colophony or rosin (a natural product obtained from pine sap that has been distilled to remove the turpentine content). Solid colophony is difficult to apply to a substrate during machine soldering, so it is dissolved in a thinning agent, usually an alcohol. It has a very low efficacy, and hence limited cleaning power, so activators are added in varying quantities to increase it. These take the form of either organic acids, or organic salts that are chemically active at soldering temperatures. It is therefore convenient to classify the colophony-based fluxes by their activator content.

Non-Activated Rosin (R) Flux

These fluxes are formed from pure colophony in a suitable solvent, usually isopropanol or ethyl alcohol. Efficacy is low and cleaning action is weak. Their uses in electronic soldering are limited to easily-wettable materials with a high level of solderability. They are used mainly on circuits where no risk of corrosion can be tolerated, even after prolonged use (implanted cardiac pacemakers, for example). Their flux residues are noncorrosive and can remain on the substrate, where they will provide good insulation.

Rosin, Mildly-Activated (RMA) Flux

These fluxes are also composed of colophony in a solvent, but with the addition of activators, either in the form of di-basic organic acids (such as succinc acid), or organic salts (such as dimethylammonium chloride or diethylammonium chloride). It is customary to express the amount of added activator as mass percent of the chlorine ion on the colophony content, as the activator-to-colophony ratio determines the activity, and, hence, the corrosivity. In the case of RMA activated with organic salts, this is only some tenths of one percent.

When organic acids are used, a higher percentage of activator must be added to produce the same efficacy as organic salts, so frequently both salts and acids are added. The cleaning action of RMA fluxes is stronger than that of the R type, although the corrosivity of the residues is usually acceptable. These residues may be left on the substrate as they form a useful insulating layer on the metal surfaces. This layer can, however, impede the penetration of test probes at a later stage.

Rosin, Activated (RA) Flux

The RA fluxes are similar to the RMA fluxes, but contain a higher proportion of activators. They are used mainly when component or substrate solderability is poor and corrosion-risk requirements are less stringent. However, as good solderability is considered essential for SMD assembly, highly-activated rosin fluxes should not be necessary. The removal of flux residues is optional and usually dependent upon the working environment of the finished product and the customer's requirements.

Water-Soluble Fluxes

The water-soluble fluxes are generally used to provide high fluxing activity. Their residues are more corrosive and more conductive than the rosin-based fluxes, and, consequently, must always be removed from the finished substrate. Although termed water soluble, this does not necessarily imply that they contain water; they may also contain alcohols or glycols. It is the flux residues that are water soluble. The usual composition of a water-soluble flux is shown below.

1. A chemically-active component for cleaning the surfaces.
2. A wetting agent to promote the spreading of flux constituents.
3. A solvent to provide even distribution.
4. Substances such as glycols or water-soluble polymers to keep the activator in close contact with the metal surfaces.

Although these substances can be dissolved in water, other solvents are generally used, as water has a tendency to spatter during soldering. Solvents with higher boiling points, such as ethylene glycol or polyethylene glycol are preferred.

Water-Soluble Fluxes With Inorganic Salts

These are based on inorganic salts such as zinc chloride, or ammonium chloride, or inorganic acids such as hydrochloric. Those with zinc or ammonium chloride must be followed by very stringent cleaning procedures as any halide salts remaining on the substrate will cause severe corrosion. These fluxes are generally used for non-electrical soldering. Although the hydrazine halides are among the best active fluxing agents known, they are highly suspect from a health point of view and are therefore no longer used by flux manufacturers.

Water-Soluble Fluxes With Organic Salts

These fluxes are based on organic hydrohalides such as dimethylammonium chloride, cyclo hexalamine hydrochloride, and aniline hydrochloride, and also on the hydrohalides of organic acids. Fluxes with organic halides usually contain vehicles such as glycerol or polyethylene glycol, and non-ionic surface-active agents such as nonylphenol polyoxyethylene. Some of the vehicles, such as the polyethylene glycols, can degrade the insulation resistance of epoxy substrate material and, by rendering the substrate hydrophilic, make it susceptible to electrical leakage in high-humidity environments.

Water-Soluble Fluxes With Organic Acids

Based on acids such as lactic, melonic, or citric, these fluxes are used when the presence of any halide is prohibited. However, their fluxing action is weak, and high acid concentrations have to be used. On the other hand, they have the advantage that the flux residues can be left on the substrate for some time before washing without the risk of severe corrosion.

Solder Creams

For reflow soldering, both the solder and the flux are applied to the substrate before soldering and can be in the form of solder creams (or pastes), preforms, electro-deposit, or a layer of solder applied to the conductors by dipping. For SMD reflow soldering, solder cream is generally used.

Solder cream is a suspension of solder particles in flux to which special compounds have been added to improve the rheological properties. The shape of the particles is important and normally spherical particles are used, although non-spherical particles are now being added, particularly in very fine-line soldering.

In principle, the same fluxes are used in solder creams as for wave soldering. However, due to the relatively large surface area of the solder particles (which can oxidize), more effective fluxing is required and, in general, solder creams contain a higher percentage of activators than the liquid fluxes. The drying of the solder paste during preheating (after component placement) is an important stage as it reduces any tendency for components to become displaced during soldering.

Flux Selection

Choosing an appropriate flux is of prime importance to the soldering system for the production of high-quality, reliable joints. When solderability is good, a mildly-activated flux will be adequate, but when solderability is poorer, a more effective, more active flux will be required. The choice of flux, moreover, will be influenced by the cleaning facilities available, and if, in fact, cleaning is even feasible.

With water-soluble fluxes, aqueous cleaning of the substrate after soldering is mandatory. If thorough cleaning is not carried out, severe problems may arise in the field, due to corrosion or short circuits caused by too low a surface resistance of the conductive residues.

For rosin-based fluxes, the need for cleaning will depend on the activity of the flux. Mildly-activated rosin residues can, in most cases, remain on the substrate where they will afford protection and insulation. In practice, for the great majority of electronic circuits, the choice will be between an RA or an RMA rosin-based flux.

Application of Flux

Three basic factors determine the method of applying flux: the soldering process (wave or reflow), the type of substrate being processed (all-SMD or mixed print), and the type of flux.

For wave soldering, the flux must be applied in liquid form before soldering. While it is possible to apply the flux at a separate fluxing station, with the high throughput rates demanded to maximize the benefits of SMD technology, today's wave-soldering machines incorporate an integral fluxing station prior to the preheat stage. This enables the preheat stage to be used to dry the flux as well as preheat the substrate to minimize thermal shock.

The most commonly-used methods of applying flux for wave soldering are by foam, wave, or spray.

Foam Fluxing

Foam flux is generated by forcing low-pressure clean air through an aerator immersed in liquid flux (see Figure 1). The fine bubbles produced by the aerator are guided to the surface by a chimney-shaped nozzle. The substrates are passed across the top of the nozzle so that the solder side comes in contact with the foam and an even layer of flux is applied. As the bubbles burst, flux penetrates any plated-through holes in the substrate.

Wave Fluxing

A double-sided wave can also be used to apply flux, where the washing action of the wave deposits a layer of flux on the solder side of the substrate (see Figure 2). Wave-height control is essential and a soft, wipe-off brush should be incorporated on the exit side of the fluxing station to remove excess flux from the substrate.

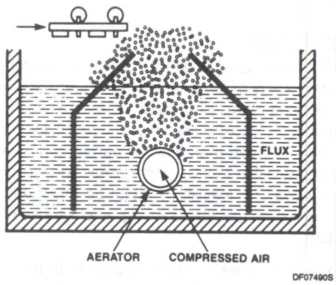


Figure 1. Schematic Diagram of Foam Fluxer

Fluxing and Cleaning

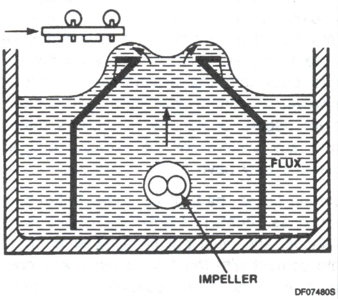


Figure 2. Schematic Diagram of Wave Fluxer

Spray Fluxing

Several methods of spray fluxing exist; the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate (see Figure 3). Four parameters affect the amount of flux deposited: conveyor speed, drum rotation, air pressure, and flux density. The thickness of the flux layer can be controlled using these parameters, and can vary between 1 and 10μm.

The advantages and disadvantages of these three flux application techniques are outlined in Table 1.

Flux Density

One of the main control factors for fluxes used in machine soldering is the flux density. This provides an indication of the solids content of the flux, and is dependent on the nature of the solvents used. Automatic control systems, which monitor flux density and inject more solvent as required, are commercially available, and it is relatively simple to incorporate them into the fluxing system.

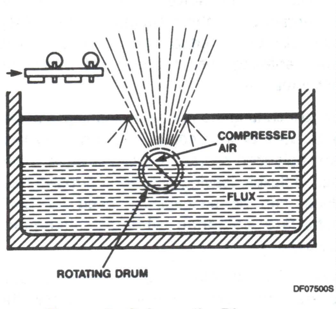


Figure 3. Schematic Diagram of Spray Fluxer

PREHEATING

Preheating the substrate before soldering serves several purposes. It dries the flux to evaporate most of the solvent, thus increasing the viscosity. If the viscosity is too low, the flux may be prematurely expelled from the substrate by the molten solder. This can result in poor wetting of the surfaces, and solder spatter.

Drying the flux also accelerates the chemical action of the flux on the surfaces, and so speeds up the soldering process. During the preheating stage, substrate and components are heated to between 80°C and 90°C (solvent-based fluxes) or to between 100°C and 110°C (water-based systems). This reduces the thermal shock when the substrate makes contact with the molten solder, and minimizes any likelihood of the substrate warping.

The most common methods of preheating are: convection heating with forced air, radiation heating using coils, infrared quartz lamps or heated panels, or a combination of both convection and radiation. The use of forced air has the added advantage of being more effective for the removal of evaporated solvent. Optimum preheat temperature and duration will depend on the nature and design of the substrate and the composition of the flux.

Figure 4 shows a typical method of preheat temperature control. The desired temperature is set on the control panel, and the microprocessor regulates preheater No. 1 to provide approximately 60% of the required heat. The IR detector scans the substrate immediately following No. 1 heater and reads the surface temperature. By taking into account the surface temperature, conveyor speed, and the thermal characteristics of the substrate, the microprocessor then calculates the amount of additional heat required to be provided by heater No. 2 in order to attain the preset temperature. In this way, each substrate will have the same surface temperature on reaching the solder bath.

POSTSOLDERING CLEANING

Now that worldwide efforts in both commercial and industrial electronics are converting old designs from conventional assembly to surface mounting, or a combination of both, it can also be expected that high-volume cleaning systems will convert from in-line aqueous cleaners to in-line solvent cleaners or in-line saponification systems (a technique that uses an alkaline material in water to react with the rosin so that it becomes water soluble). These systems may, however, become subject to environmental objections, and new governmental restrictions on the use of halogenated hydrocarbons.

The major reason for this is that the water-soluble flux residues, containing a higher concentration of activators, or showing hygroscopic behavior, are much more difficult to remove from SMD-populated substrates than rosin-based flux residues. This is primarily because the higher surface tension of water, compared to solvents, makes it difficult for the cleaning agents to penetrate beneath SMDs, especially the larger ones, with their greatly reduced off-contact distance (the distance between component and substrate).

Postsoldering cleaning removes any contamination, such as surface deposits, inclusions, occlusions, or absorbed matter which may degrade to an unacceptable level the chemical, physical, or electrical properties of the assembly. The types of contaminant on substrates that can produce either electrical or mechanical failure over short or prolonged periods are shown in Table 2.

All these contaminants, regardless of their origin, fall into one of two groups: polar and non-polar.

Polar Contaminants

Polar contaminants are compounds that dissociate into free ions which are very good conductors in water, quite capable of causing circuit failures. They are also very reactive with metals and produce corrosive reactions. It is essential that polar contaminants be removed from the substrates.

Non-Polar Contaminants

Non-polar contaminants are compounds that do not dissociate into free ions or carry an electrical current and are generally good insulators. Rosin is a typical example of a non-polar contaminant. In most cases, non-polar contamination does not contribute to corrosion or electrical failure and may be left on the substrate. It may, however, impede functional testing by probes and prevent good conformal coat adhesion.

Solvents

The solvents currently used for the post-soldering cleaning of substrates are normally organic based and are covered by three classifications: hydrophobic, hydrophillic, and azeotropes of hydrophobic/hydrophillic blends.

Azeotropic solvents are mixtures of two or more different solvents which behave like a single liquid insomuch that the vapor produced by evaporation has the same composition as the liquid, which has a constant boiling point between the boiling points of the two solvents that form the azeotrope. The basic ingredients of the azeotropic solvents are combined with alcohols and stabilizers. These stabilizers, such as nitromethane, are included to prevent corrosive reaction be-

Fluxing and Cleaning

Table 1. Advantages and Disadvantages of Flux Application Methods

Method	Advantages	Disadvantages
Foam Fluxing	• Compatible with continuous soldering process • Foam crest height not critical • Suitable for mixed-print substrates	• Not all fluxes have good foaming capabilities • Losses throught evaporation may be appreciable • Prolonged preheating because of high boiling point of solvents
Wave Fluxing	• Can be used with any liquid flux • Compatible with continuous soldering process • Suitable for densely-populated mixed print	• Wave crest height is critical to ensure good contact with bottom of substrate without contaminating the top
Spray fluxing	• Can be used with most liquid fluxes • Short preheat time if appropriate alcohol solvents are used • Layer thickness is controllable	• High flux losses due to non-recoverable spray • System requires frequent cleaning

tween the metallization of the substrate and the basic solvents.

Hydrophobic solvents do not mix with water at concentrations exceeding 0.2%, and consequently have little effect on ionic contamination. They can be used to remove non-polar contaminants such as rosin, oils, and greases.

Hydrophillic solvents do mix with water and can dissolve both polar and non-polar contamination, but at different rates. To overcome these differences, azeotropes of the various solvents are formulated to maximize the dissolving action for all types of contamination.

Solvent Cleaning

Two types of solvent cleaning systems are in use today: batch and conveyorized systems, either of which can be used for high-volume production. In both systems, the contaminated substrates are immersed in the boiling solvents, and ultrasonic baths or brushes may also be used to further improve the cleaning capabilities.

The washing of rosin-based fluxes offers advantages and disadvantages. Washed substrates can usually be inserted into racks easier, as there will be no residues on their edges; test probes can make better contact without a rosin layer on the test points, and the removal of the residues makes it easier to visually examine the soldered joints. On the other hand, washing equipment is expensive, and so are the solvents, and some solvents present a health or environmental hazard if not correctly dealt with.

Aqueous Cleaning

For high-volume production, special machines have been developed in which the substrates are conveyor-fed through the various stages of spraying, washing, rinsing, and drying. The final rinse water is blown from the substrates to prevent any deposits from the water being left on the substrate.

Where water-soluble fluxes have been used in the soldering process, substrate cleaning is mandatory. For the rosin-based fluxes, it is optional, and is often at the discretion of the customer.

Conformal Coatings

A conformal, or protective coating on the substrate, applied at the end of processing, prevents or minimizes the effects of humidity and protects the substrate from contamination by airborne dust particles. Substrates that are to be provided with a conformal coating (dependent on the environmental conditions to which the substrate will be subjected) must first be washed.

Environmental and Ecological Aspects of Fluxes and Solvents

Fumes and vapors produced during soldering processes, or during cleaning, will not, under normal circumstances, present a health hazard, if relevant health and safety regulations are observed.

Fumes originating from colophony can cause respiratory problems, so an efficient fume-extraction system is essential. The extraction system must cover the fluxing, preheating, and soldering stations, remain operational for at least one hour after machine shutdown, and conform to local regulations. Today, the problem of noxious fumes is unlikely to concern the cleaning station, as all commercial systems are equipped to condense the vapors back into the system. In the future, however, it can be expected that a much lower degree of escape of noxious fumes from any system will be allowed, and all systems may have to be reviewed.

Certain fluxes, particularly some water-soluble ones, contain highly aggressive substances, and must not be allowed to come into contact with the skin or eyes. Any contamination should immediately be removed with plenty of clean, fresh water. Deionized water should also be readily available as an eye-wash. Should contamination occur, a qualified medical practitioner should be consulted. Protective clothing should be worn during cleaning or maintenance of the fluxing station.

Conclusion

SMD technology imposes tougher restraints on fluxing and cleaning of substrate assemblies. Traditionally, rosin-based fluxes have been used in electronic soldering where residues were considered "safe" and could be left on the board. However, increased SMD packing density, fine-line tracks, and more rigid specifications have resulted in changes to this basic philosophy.

There is now a demand for surfaces free from residues; test probes are more efficient when they do not have to penetrate rosin flux residues, and conformal coating and board inspection benefit from the absence of such residues.

Cleaning also poses problems for SMD substrates. The close proximity of component and substrate means that solvents cannot effectively clean beneath devices. Components must also be compatible with the cleaning process. They must, for example, be resistant to the solvents used and to the temperatures of the cleaning process. They must also be sealed to prevent cleaning fluids from entering the devices and degrading performance.

So, eliminating the need for cleaning is better than poor or incomplete cleaning. And in a well-balanced system, mildly-activated rosin-based fluxes, leaving only non-corrosive residues, can be successfully used for SMD substrate soldering without subsequent cleaning.

Much research into fluxes and solder creams is presently being done — for example, the production of synthetic resin, with qualities superior to colophony at a lower cost. Another area of research is that of solder creams with non-melting additives, such as lead or ceramic spheres, that increase the distance

Fluxing and Cleaning

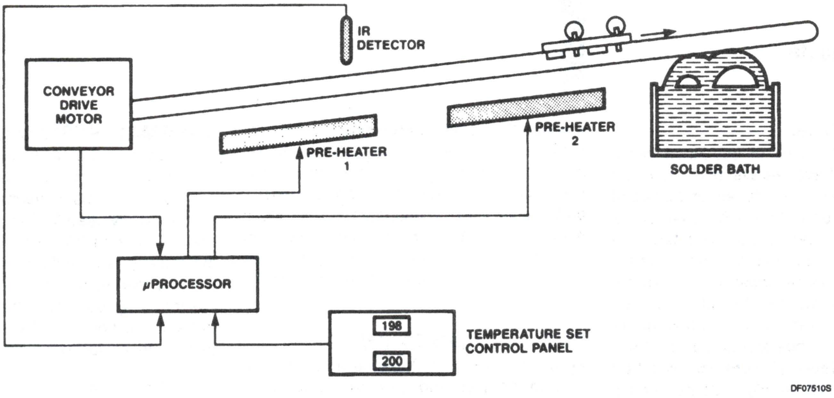

IR DETECTOR
CONVEYOR DRIVE MOTOR
PRE-HEATER 1
PRE-HEATER 2
SOLDER BATH
μPROCESSOR
198
200
TEMPERATURE SET CONTROL PANEL
DF07510S

Figure 4. Schematic Diagram of a Typical Controlled Preheat System

Table 2. Substrate Contaminants

Contaminant	Origin
Organic compounds	Fluxes, solder mask
Inorganic insoluble compounds	Photo-resists, substrate processing
Organo-metallic compounds	Fluxes, substrate processing
Inorganic soluble compounds	Fluxes
Particle matter	Dust, fingerprints

between component and substrate, thus making it easier for cleaning fluids to penetrate beneath the component. It also increases the joint's ability to withstand thermal cycling.

Rosin-free and halide-free fluxes are also being developed with similar activities to conventional rosin-based fluxes. These new types will combine the "safety" of rosin fluxes with easier removal in conventional solvents. Using non-polar materials, ionizable or corrosive residues are eliminated, and the need for cleaning immediately after soldering is avoided.

Signetics

Thermal Considerations for Surface-Mounted Devices

Linear Products

INTRODUCTION

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long-term operating life of an IC. As will be shown in this section, the advantages realized by miniaturization can often have trade-offs in terms of increased junction temperatures. **Some of the VARIABLES affecting T_J are controlled by the PRODUCER of the IC, while others are controlled by the USER and the ENVIRONMENT in which the device is used.**

With the increased use of Surface-Mount Device (SMD) technology, management of thermal characteristics remains a valid concern, not only because the SMD packages are much smaller, but also because the thermal energy is concentrated more densely on the printed wiring board (PWB). For these reasons, the designer and manufacturer of surface-mount assemblies (SMAs) must be more aware of all the variables affecting T_J.

POWER DISSIPATION

Power dissipation (P_D), varies from one device to another and can be obtained by multiplying V_{CC} Max by typical I_{CC}. Since I_{CC} decreases with an increase in temperature, maximum I_{CC} values are not used.

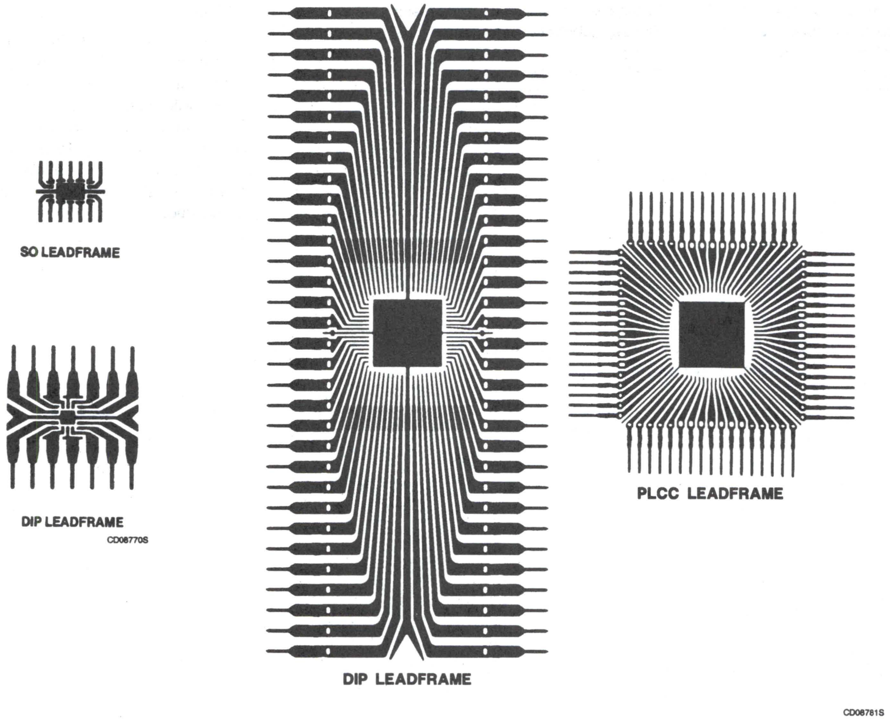
THERMAL RESISTANCE

The ability of the package to conduct this heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC measured by Signetics at the



a. SO-14 Leadframe Compared to a 14-Pin DIP Leadframe

b. PLCC-68 Leadframe Compared to a 64-Pin DIP Leadframe

Figure 1

Thermal Considerations for Surface-Mounted Devices

substrate diode. When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$T_J = (P_D \times \theta_{JA}) + T_A$$

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management demands a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and, to a lesser extent, other variables such as the die size and die attach methods. Other factors that have a significant impact on the θ_{JA} include the substrate upon which the IC is mounted, the density of the layout, the air-gap between the package and the substrate, the number and length of traces on the board, the use of thermally-conductive epoxies, and external cooling methods.

PACKAGE CONSIDERATIONS

Studies with dual in-line plastic (DIP) packages over the years have shown the value of proper leadframe design in achieving minimum thermal resistance. SMD leadframes are smaller than their DIP counterparts (see Figures 1a and 1b). Because the same die is used in each of the packages, the die-pad, or flag, must be at least as large in the SO as in the DIP.

While the size and shape of the leads have a measurable effect on θ_{JA}, the design factors that have the most significant effect are the die-pad size and the tie-bar size. With design constraints caused by both miniaturization and the need to assemble packages in an automated environment, the internal design of an SMD is much different than in a DIP. However, the design is one that strikes a balance between the need to miniaturize, the need to automate the assembly of the package, and the need to obtain optimum thermal characteristics.

LEAD FRAME MATERIAL is one of the more important factors in thermal management. For years, the DIP leadframes were constructed out of Alloy-42. These leadframes met the producers' and users' specifications in quality and reliability. However, three to five years ago the leadframe material of DIPs was changed from Alloy-42 to Copper (CLF) in order to provide reduced θ_{JA} and extend the reliable temperature-operating range. While this change has already taken place for the DIP, it is still taking place for the SO package. Signetics began making 14-pin SO packages with CLF in April 1984 and completed conversion to CLF for all SO packages by 1985. As is shown in Figures 10 through 14, the change to CLF is producing dramatic results in the θ_{JA} of SO packages. All PLCCs are assembled with copper leadframes.

The MOLDING COMPOUND is another factor in thermal management. The compound used by Signetics and Philips is the same high purity epoxy used in DIP packages (at present, HC-10, Type II). This reduces corrosion caused by impurities and moisture.

OTHER FACTORS often considered are the die-size, die-attach methods, and wire bonding. Tests have shown that die size has a minor effect on θ_{JA} (see Figures 10 through 14).

While there is a difference between the thermal resistance of the silver-filled adhesive used for die attach and a gold silicon eutectic die attach, the thickness of this layer (1 – 2 mils) is so small it makes the difference insignificant.

Gold-wire bonding in the range of 1.0 to 1.3 mils does not provide a significant thermal path in any package.

In summary, the SMD leadframe is much smaller than in a DIP and, out of necessity, is designed differently; however, the SMD package offers an adequate θ_{JA} for all moderate power devices. Further, the change to CLF will reduce the θ_{JA} even more, lowering the T_J and providing an even greater margin of reliability.

SIGNETICS' THERMAL RESISTANCE MEASUREMENTS — SMD PACKAGES

The graphs illustrated in this application note show the thermal resistance of Signetics' SMD devices. These graphs give the relationship between θ_{JA} (junction-to-ambient) or θ_{JC} (junction-to-case) and the device die size. Data is also provided showing the difference between still air (natural convection cooling) and air flow (forced cooling) ambients. All θ_{JA} tests were run with the SMD device soldered to test boards. It is important to recognize that the test board is an essential part of the test environment and that boards of different sizes, trace layouts, or compositions may give different results from this data. Each SMD user should compare his system to the Signetics test system and determine if the data is appropriate or needs adjustment for his application.

Test Method

Signetics uses what is commonly called the TSP (temperature-sensitive parameter) method. This method meets MIL-STD 883C, Method 1012.1. The basic idea of this method is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{T_J - T_A}{P_D}$$

Test Procedure

TSP Calibration

The TSP diode is calibrated using a constant-temperature oil bath and constant-current power supply. The calibration temperatures used are typically 25°C and 75°C and are measured to an accuracy of ±0.1°C. The calibration current must be kept low to avoid significant junction heating; data given here used constant currents of either 1.0mA or 3.0mA. The temperature coefficient (K-Factor) is calculated using the following equation:

$$K = \frac{T_2 - T_1}{V_{F2} - V_{F1}} \bigg| \; I_F = \text{Constant}$$

Where: K = Temperature Coefficient (°C/mV)
T_2 = Higher Test Temperature (°C)
T_1 = Lower Test Temperature (°C)
V_{F2} = Forward Voltage at I_F and T_2
V_{F1} = Forward Voltage at I_F and T_1
I_F = Constant Forward Measurement Current
(See Figure 2)

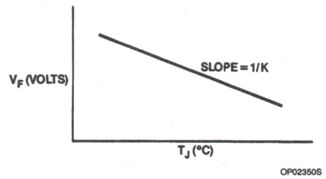


Figure 2. Forward Voltage — Junction Temperature Characteristics of a Semiconductor Junction Operating at a Constant Current. The K Factor is the Reciprocal of the Slope

Thermal Resistance Measurement

The thermal resistance is measured by applying a sequence of constant current and constant voltage pulses to the device under test. The constant current pulse (same current at which the TSP was calibrated) is used to measure the forward voltage of the TSP. The constant voltage pulse is used to heat the part. The measurement pulse is very short

Thermal Considerations for Surface-Mounted Devices

(less than 1% of cycle) compared to the heating pulse (greater than 99% of cycle) to minimize junction cooling during measurement. This cycle starts at ambient temperature and continues until steady-state conditions are reached. The thermal resistance can then be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{K(V_{FA} - V_{FS})}{V_H \times I_H}$$

Where: V_{FA} = Forward Voltage of TSP at Ambient Temperature (mV)

V_{FS} = Forward Voltage of TSP at Steady-State Temperature (mV)

V_H = Heating Voltage (V)

I_H = Heating Current (A)

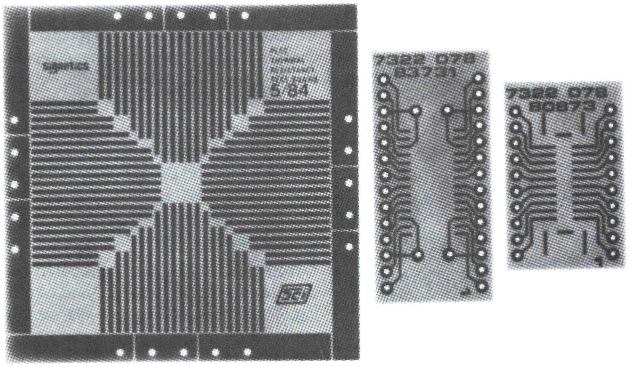


Figure 3. Board Trace Configuration for Thermal Resistance Test Boards

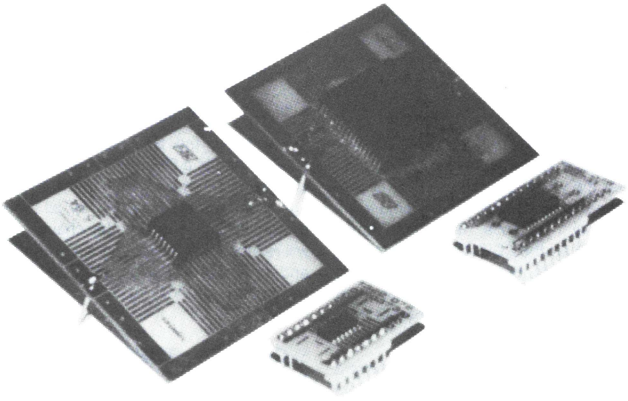


Figure 4. Device/Board Assemblies

Test Ambient

θ_{JA} Tests

All θ_{JA} test data collected in this application note was obtained with the SMD devices soldered to either Philips SO Thermal Resistance Test Boards or Signetics PLCC Thermal Resistance Test Boards with the following parameters:

Board size — SO Small
1.12″ × 0.75″ × 0.059″
— SO Large:
1.58″ × 0.75″ × 0.059″
— PLCC:
2.24″ × 2.24″ × 0.062″

Board Material — Glass epoxy, FR-4 type with 1oz. sq.ft. copper solder coated

Board Trace Configuration — See Figure 3.

SO devices are set at 8 – 9mil stand-off and SO boards use one connection pin per device lead. PLCC boards generally use 2 – 4 connection pins regardless of device lead count. Figure 5 shows a cross-section of an SO part soldered to test board, and Figure 4 shows typical board/device assemblies ready for θ_{JA} Test.

The still-air tests were run in a box having a volume of 1 cubic foot of air at room temperature. The air-flow tests were run in a 4″ × 4″ cross-section by 26″ long wind tunnel with air at room temperature. All devices were soldered on test boards and held in a horizontal test position. The test boards were held in a Textool ZIF socket with 0.16″ stand-off. Figure 6 shows the air-flow test setup.

θ_{JC} Tests

The θ_{JC} test is run by holding the test device against an "infinite" heat sink (water-cooled block approximately 4″ × 7″ × 0.75″) to give a θ_{CA} (case-to-ambient) approaching zero. The copper heat sink is held at a constant temperature (≈20°C) and monitored with a thermocouple (0.040″ diameter sheath, grounded junction type K) mounted flush with heat-sink surface and centered below die in the test device. Figure 7 shows the θ_{JC} test mounting for a PLCC device.

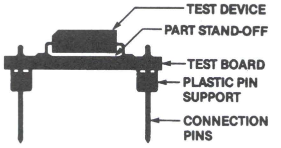
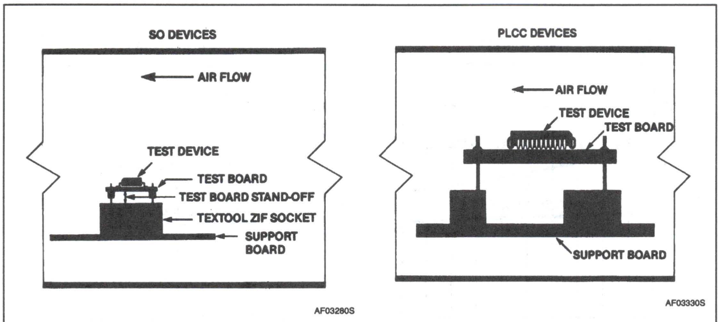


Figure 5. Cross-Section of Test Device Soldered to Test Board

SO devices are mounted with the bottom of the package held against the heat sink. This is achieved by bending the device leads straight out from the package body. Two small wires are soldered to the appropriate leads for tester connection. Thermal grease is used between the test device and heat sink to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heat sink. A small spacer is used between the hold-down mechanism and PLCC bottom pedestal. Small hook-up wires and thermal grease are used as with the SO setup. Figure 7 shows the PLCC mounting.

Thermal Considerations for Surface-Mounted Devices


SO DEVICES
AIR FLOW
TEST DEVICE
TEST BOARD
TEST BOARD STAND-OFF
TEXTOOL ZIF SOCKET
SUPPORT BOARD
AF03280S
PLCC DEVICES
AIR FLOW
TEST DEVICE
TEST BOARD
SUPPORT BOARD
AF03330S

SO Devices **PLCC Devices**

Figure 6. Air-Flow Test Setup

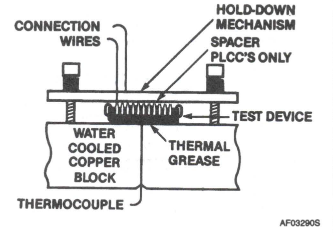

CONNECTION WIRES
HOLD-DOWN MECHANISM
SPACER PLCC'S ONLY
TEST DEVICE
WATER COOLED COPPER BLOCK
THERMAL GREASE
THERMOCOUPLE
AF03290S

Figure 7. θ_{JC} Test Setup With PLCC Device

DATA PRESENTATION

The data presented in this application note was run at constant power dissipation for each package type. The power dissipation used is given under Test Conditions for each graph. Higher or lower power dissipation will have a slight effect on thermal resistance. The general trend of thermal resistance decreasing with increasing power is common to all packages. Figure 8 shows the average effect of power dissipation on SMD θ_{JA}.

Thermal resistance can also be affected by slight variations in internal leadframe design such as pad size. Larger pads give slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. The effect of leadframe design is within the ±15% accuracy of these graphs.

SO devices are currently available in both copper or alloy 42 leadframes; however, Signetics is converting to copper only. PLCC devices are only available using copper leadframes.

The average lowering effect of air flow on SMD θ_{JA} is shown in Figure 9.

Thermal Calculations

The approximate junction temperature can be calculated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

Where: T_J = Junction Temperature (°C)

θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)

P_D = Power Dissipation at a T_J ($V_{CC} \times I_{CC}$) (W)

T_A = Temperature of Ambient (°C)

Example: Determine approximate junction temperature of SOL-20 at 0.5W dissipation using 10,000 sq. mil die and copper leadframe in still air and 200 LFPM air-flow ambients. Given $T_A = 30°C$,

1. Find θ_{JA} for SOL-20 using 10,000 sq. mil die and copper leadframe from typical θ_{JA} data — SOL-20 graph.

   Answer: 88°C/W @ 0.7W

2. Determine θ_{JA} @ 0.5W using Average Effect of Power Dissipation on AMD θ_{JA}, Figure 8.

   Percent change in Power

   $$= \frac{0.5W - 0.7W}{0.7W} \times 100$$

   $$= -28.6\%$$

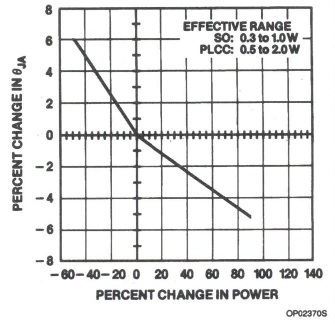


Figure 8. Average Effect of Power Dissipation on SMD θ_{JA}

From Figure 8:
28.6% change in power gives 3.5% increase in θ_{JA}

Answer:
88°C/W + (88 × 0.035)
= 91°C/W @ 0.5W

3. Determine θ_{JA} @ 0.5W in 200 LFPM air flow from Average Effect of Air Flow on SMD θ_{JA}, Figure 9.

From Figure 9: 200 LFPM air flow gives 14% decrease in θ_{JA}

Answer:
91°C/W − (91 × 0.14) = 78°C/W

4. Calculate approximate junction temperature

Answer:
T_J (still-air)
= (91°C/W × 0.5W) + 30
= 76°C
T_J (200 LFPM)
= (78°C/W × 0.5W) + 30
= 69°C

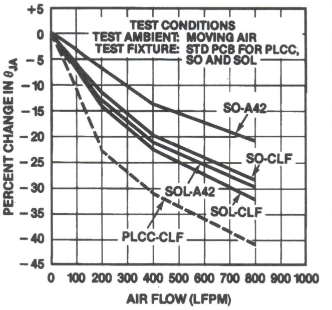
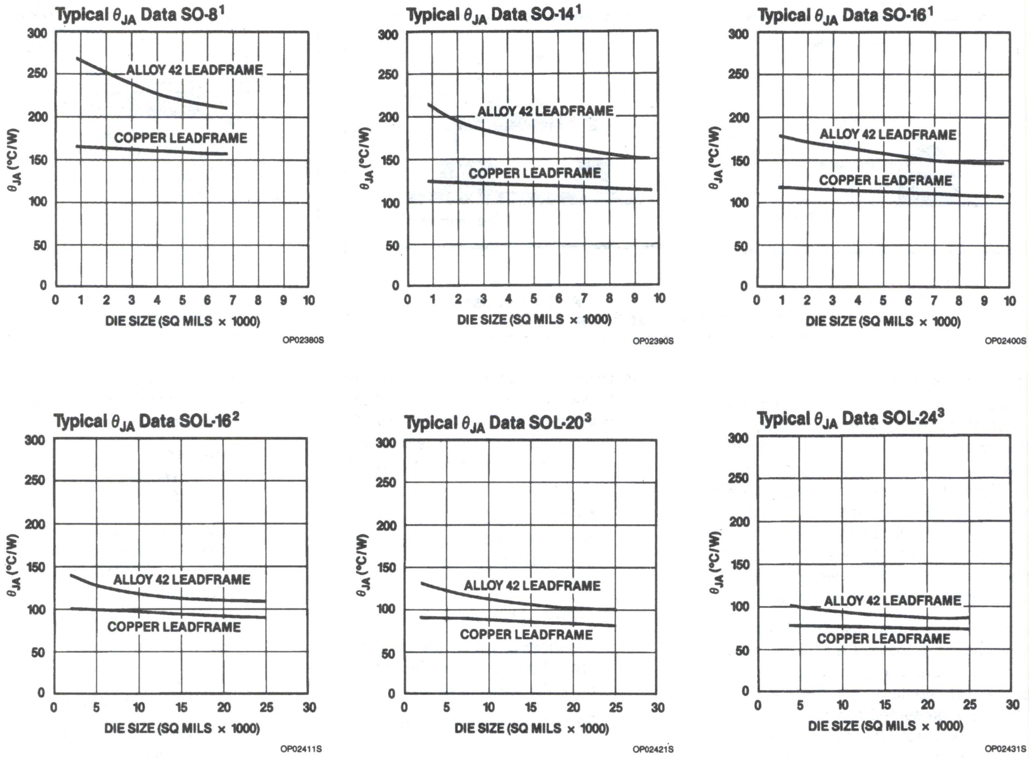
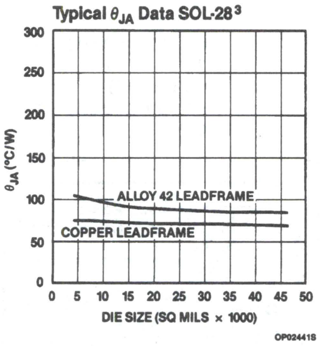


Figure 9. Average Effect of Air Flow on SMD θ_{JA}

Thermal Considerations for Surface-Mounted Devices





NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.12″ × 0.75″ × 0.059″)
Accuracy:	± 15%

2. TEST CONDITIONS:

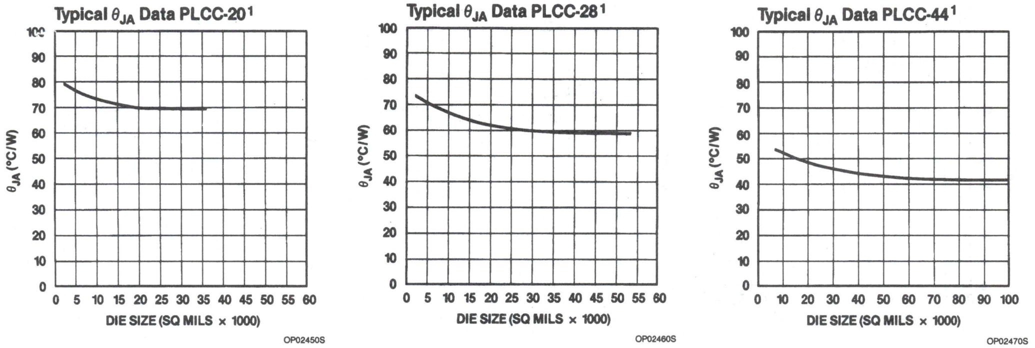
Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0.059″)
Accuracy:	± 15%

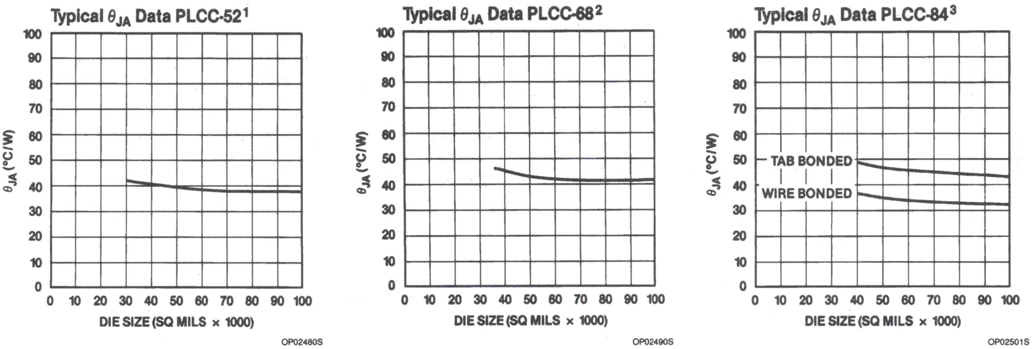
3. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0.059″)
Accuracy:	± 15%

Figure 10. Typical SMD Thermal (θ_{JA}) Characteristics

Thermal Considerations for Surface-Mounted Devices





NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

2. TEST CONDITIONS:

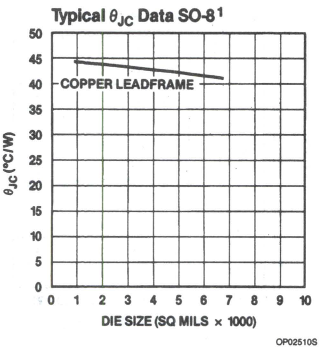
Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

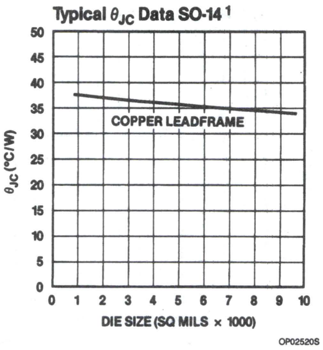
3. TEST CONDITIONS:

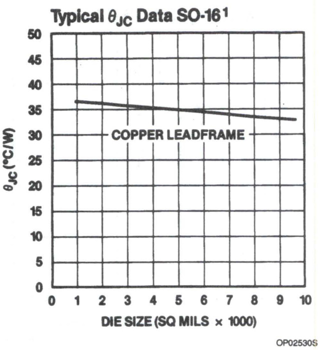
Test ambient	Still air
Power dissipation:	1.5W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

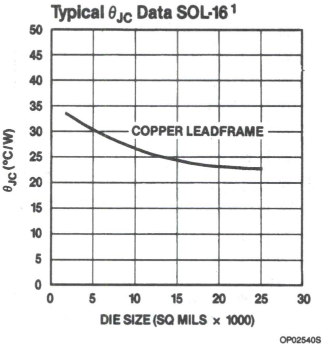
Figure 11. Typical SMD Thermal (θ_{JA}) Characteristics

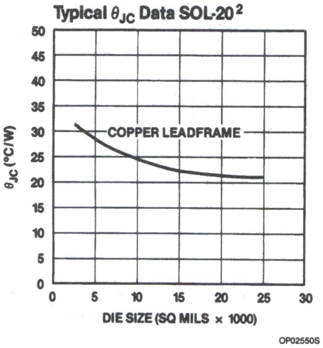
Thermal Considerations for Surface-Mounted Devices

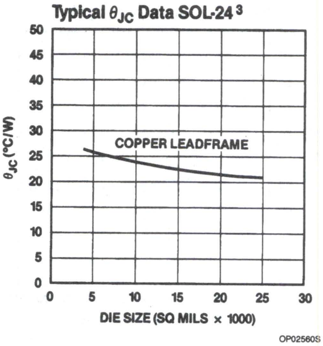

Typical θ_{JC} Data SO-8[1]

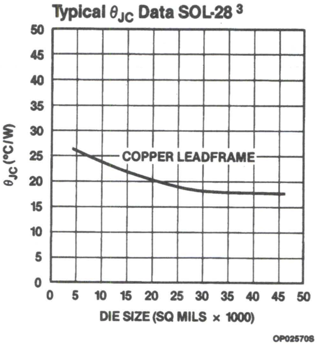

Typical θ_{JC} Data SO-14[1]


Typical θ_{JC} Data SO-16[1]


Typical θ_{JC} Data SOL-16[1]


Typical θ_{JC} Data SOL-20[2]


Typical θ_{JC} Data SOL-24[3]


Typical θ_{JC} Data SOL-28[3]

NOTES:

1. TEST CONDITIONS:

Power dissipation:	0.5W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

2. TEST CONDITIONS:

Power dissipation:	0.7W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

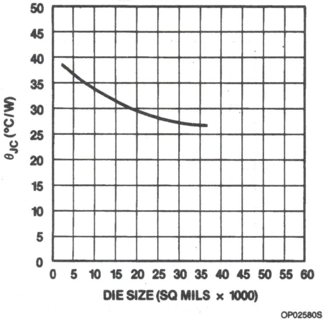
3. TEST CONDITIONS:

Power dissipation:	1.0W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

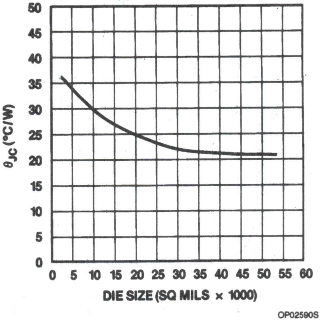
Figure 12. Typical SMD Thermal (θ_{JC}) Characteristics

Thermal Considerations for Surface-Mounted Devices

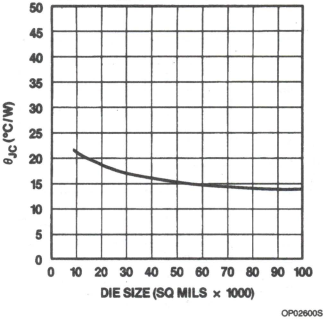
Typical θ_{JC} Data PLCC-20[1]



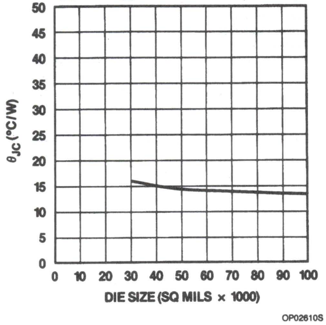
Typical θ_{JC} Data PLCC-28[2]



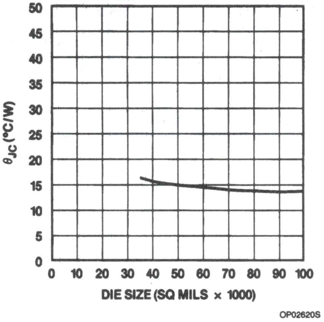
Typical θ_{JC} Data PLCC-44[2]



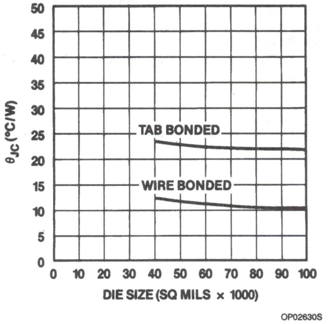
Typical θ_{JC} Data PLCC-52[2]



Typical θ_{JC} Data PLCC-68[3]



Typical θ_{JC} Data PLCC-84[3]



NOTES:

1. TEST CONDITIONS:

Power dissipation:	0.75W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

2. TEST CONDITIONS:

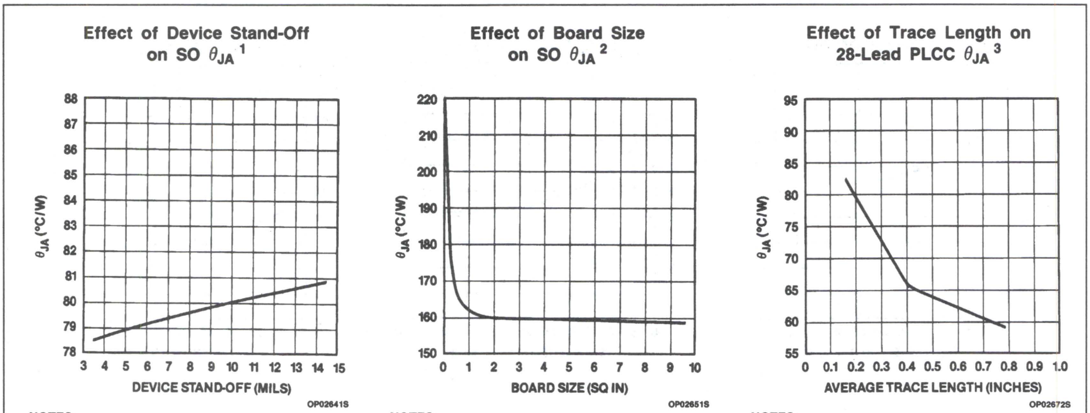
Power dissipation:	1.0W
Test fixture:	"infinite" heat sink
Accuracy:	±15%

3. TEST CONDITIONS:

Power dissipation:	2.0W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

Figure 13. Typical SMD Thermal (θ_{JC}) Characteristics

Thermal Considerations for Surface-Mounted Devices



Effect of Device Stand-Off on SO θ_{JA} [1]

Effect of Board Size on SO θ_{JA} [2]

Effect of Trace Length on 28-Lead PLCC θ_{JA} [3]

NOTES:

1. TEST CONDITIONS

Package type:	SOL-20 CLF
Die size:	11,322sq.mils
Test Ambient:	Still-air
Power dissipation:	0.75W
Test fixture:	Phillips PCB (1.58" × 0.75" × 0.059")

NOTES:

2. TEST CONDITIONS

Package type:	SOL-14 CLF
Die size:	5,040sq.mils
Test Ambient:	Still-air
Power dissipation:	0.6W
Test fixture:	0.062" thick PCB with "no traces" 8 – 9mil stand-off

NOTES:

3. TEST CONDITIONS

Package type:	PLCC-28 CLF
Die size:	10,445sq.mils
Test Ambient:	Still-air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062") trace 27mil-wide 1oz sq.ft copper

Figure 14

Thermal Considerations for Surface-Mounted Devices

SYSTEM CONSIDERATIONS

With the increases in layout density resulting from surface mounting with much smaller packages, other factors become even more important. THE USER IS IN CONTROL OF THESE FACTORS.

One of the most obvious factors is the substrate material on which the parts are mounted. Environmental constraints, cost considerations, and other factors come into play when choosing a substrate. The choice is expanding rapidly, from the standard glass epoxy PWB materials and ceramic substrates to flexible circuits, injection-molded plastics, and coated metals. Each of these has its own thermal characteristics which must be considered when choosing a substrate material.

Studies have shown that the air gap between the bottom of the package and the substrate has an effect on θ_{JA}. The larger the gap, the higher the θ_{JA}. Using thermally conductive epoxies in this gap can slightly reduce the θ_{JA}.

It has long been recognized that external cooling can reduce the junction temperatures of devices by carrying heat away from both the devices and the board itself. Signetics has done several studies on the effects of external cooling on boards with SO packages. The results are shown in Figures 15 through 18.

The designer should avoid close spacing of high power devices so that the heat load is spread over as large an area as possible. Locate components with a higher junction temperature in the cooler locations on the PCBs.

The number and size of traces on a PWB can affect θ_{JA} since these metal lines can act as radiators, carrying heat away from the package and radiating it to the ambient. Although the chips themselves use the same amount of energy in either a DIP or an SO package, the increased density of a surface-mounted assembly concentrates the thermal energy into a smaller area.

It is evident that nothing is free in PWB layout. More heat concentrated into a smaller area makes it incumbent on the system designer to provide for the removal of thermal energy from his system.

Large conductor traces on the PCB conduct heat away from the package faster than small traces. Thermal vias from the mounting surface of the PCB to a large area ground plane in the PCB reduce the heat buildup at the package.

In addition to the package's thermal considerations, thermal management requires one to at least be aware of potential problems caused by mismatch in thermal expansion.

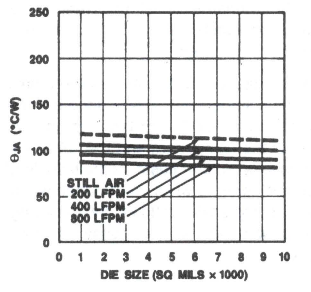


Figure 15. Results of Air Flow on θ_{JA} on SO-14 With Copper Leadframe

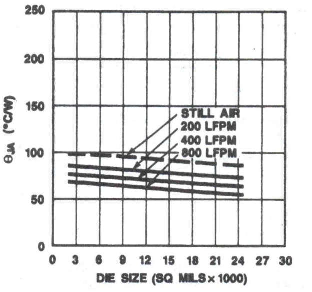


Figure 16. Results of Air Flow on θ_{JA} on SOL-16 With Copper Leadframe

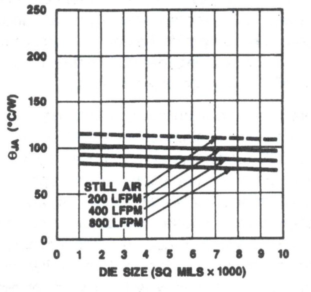


Figure 17. Results of Air Flow on θ_{JA} on SO-16 With Copper Leadframe

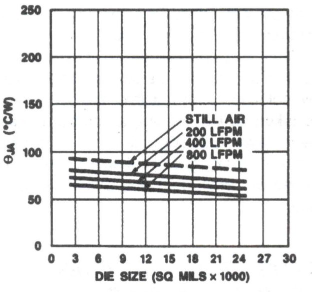


Figure 18. Results of Air Flow on θ_{JA} on SOL-20 With Copper Leadframe

The very nature of the SMD assembly, where the devices are soldered directly onto the surface, not through it, results in a very rigid structure. If the substrate material exhibits a different thermal coefficient of expansion (TCE) than the IC package, stresses can be set up in the solder joints when they are subjected to temperature cycling (and during the soldering process itself) that may ultimately result in failure.

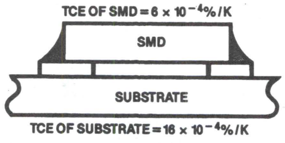
Because some of the boards assembled will require the use of Leadless Ceramic Chip Carriers (LCCCs), TCE must be understood. As will be seen below, TCE is less of a problem with the commercial SMD packages with leads.

Take the example of a leadless ceramic chip carrier with a TCE of about 6×10^{-6}/°C soldered to a conventional glass-epoxy laminate with a TCE in the region of 16×10^{-6}/°C. This thermal expansion mismatch has been shown to fracture the solder joints during thermal cycling. Substrate materials with matched TCEs should be evaluated for these SMD assemblies to avoid problems caused by thermal expansion mismatch.

The stress level associated with thermal expansion and contraction of small SMDs such as capacitors and resistors, where the actual change in length is small, is normally rather low. However, as component sizes increase, stresses can increase substantially.

Thermal expansion mismatch is unlikely to cause too many problems in systems operating in benign environments; but, in harsher conditions, such as thermal cycling in military or avionic applications, the mechanical stresses set up in solder joints due to the different TCEs of the substrate and the component are likely to cause failure.

The basic problem is outlined in Figure 19. The leadless SMD is soldered to the substrate as shown, resulting in a very rigid structure. If the substrate material exhibits a different TCE from that of the SMD material, the amount of expansion for each will differ for any given increase in temperature. The soldered joint will have to accommodate this difference, and failure can ultimately result. The larger the component size, the higher the stress levels so that this phenomenon is at its most critical in applications requiring large LCCCs with high pin counts.


TCE OF SMD = 6 × 10^{-4}%/K
SMD
SUBSTRATE
TCE OF SUBSTRATE = 16 × 10^{-4}%/K
AF03310S

NOTE:
Data provided by N.V. Philips

Figure 19. The Basic Problem of Thermal Expansion Mismatch Is That the Substrate and Component May Each Have Different Thermal Coefficients of Expansion

To address this problem, three basic solutions are emerging. First, the use of leadless ceramic chip carriers can sometimes be avoided by using leaded devices; the leads can flex and absorb the stress. Second, when this solution is not feasible, the stresses can be taken up by inserting a compliant elastomeric layer between the ceramic package and the epoxy glass substrate. Third, TCE values of component and substrate can be matched.

USING LEADED DEVICES (SO, SOL, and PLCC)

The current evolution in commercial electronics includes the adoption of the commercial SMD packages, i.e., SO with gull-wing leads or the PLCC with rolled-under J-leads, rely on the compliance of the leads themselves to avoid any serious problems of thermal expansion mismatch. At elevated temperatures, the leads flex slightly and absorb most of the mechanical stress resulting from the thermal expansion differentials.

Similarly, leaded holders can be used with LCCCs to attach them to the substrate and thus absorb the stress.

Unfortunately, using a lead does not always ensure sufficient compliancy. The material from which the lead is made, and the way it is formed and soldered can adversely affect it. For example, improper soldering techniques, which cause excess solder to over-fill the bend of the gull-wing lead of an SO, can significantly reduce the lead's compliancy.

COMPLIANT LAYER

This approach introduces a compliant layer onto the interface surface of the substrate to absorb some of the stresses. A 50μm thick elastomeric layer is bonded to the laminate. To make contacts, carbon or metallic powders are introduced to form conductive stripes in the nonconductive elastomer material. Unfortunately, substrates using this technique are substantially more expensive than standard uncoated boards.

Another solution is to increase the compliancy of the solder joint. This is done by increasing the stand-off height between the underside of the component and the substrate. To do this, a solder paste containing lead or ceramic spheres which do not melt when the surrounding solder reflows, thus keeping the component above the substrate, can be used.

MATCHING TCE

There are two ways to approach this solution. The TCE of the substrate laminate material can be matched to that of the LCCC either by replacing the glass fibers with fibers exhibiting a lower TCE (composites such as epoxy-Kevlar®or polyimide-Kevlar and polyimide-quartz), or by using low TCE metals (such as Invar®, Kovar, or molybdenum).

This latter approach involves bonding a glass-polyimide or a glass-epoxy multilayer to the low TCE restraining core material. Typical of such materials are copper-Invar-copper, Alloy-42, copper-molybdenum-copper, and copper-graphite. These restraining-core constructions usually require that the laminate be bonded to both sides to form a balanced structure so that they will not warp or twist.

This inevitably means an increase in weight, which has always been a negative factor in this approach. However, the SMD substrate can be smaller and the components more densely packed, in many cases overcoming the weight disadvantages. On the positive side, the material's high thermal conductivity helps to keep the components cool. Moreover, copper-clad Invar lends itself readily to moisture-proof multilayering for the creation of ground and power planes and for providing good inherent EMI/RFI shielding.

Kevlar is lighter and widely used for substrates in military applications; but, it suffers from a serious drawback which, although overcome to a certain extent by careful attention to detail, can cause problems. The material, when laminated, can absorb moisture and chemical processing fluids around the edges. Thermal conductivity, machinability, and cost are not as attractive as for copper-clad Invar.

For the majority of commercial substrates, however, where the use of ceramic chip carriers in any quantity is the exception rather than the rule, and when adequate cooling is available, the mismatch of TCEs poses little or no problem. For these substrates, traditional FR-4 glass-epoxy and phenolic-paper will no doubt remain the most widely-used materials.

Although FR-4 epoxy-glass has been the traditional material for plated-through professional substrates, it is phenolic-paper laminate (FR-2) which finds the widest use in consumer electronics. While it is the cheapest material, it unfortunately has the lowest dimensional stability, rendering it unsuitable for the mounting of LCCCs.

SUBSTRATE TYPES

FR-4 glass-epoxy substrates are the most commonly used for commercial electronic circuits. They have the advantage of being cheap, machinable, and lightweight. Substrate size is not limited. On the negative side, they have poor thermal conductivity and a high TCE, between 13 and 17 × 10^{-6}/°C. This means they are a poor match to ceramic.

Glass polyimide substrates have a similar TCE range to glass-epoxy boards, but better thermal conductivity. They are, however, three to four times more expensive.

Polyimide Kevlar substrates have the advantage of being lightweight and not restricted in size. Conventional substrate processing methods can be used and its TCE (between 4 and 8), matches that of ceramic. Its disadvantages are that it is expensive, difficult to drill, and is prone to resin microcracking and water absorption.

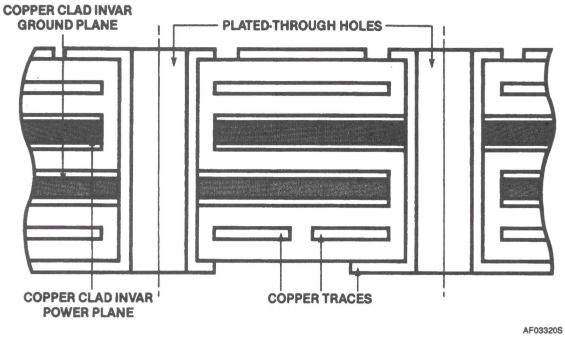
Polyimide quartz substrates have a TCE between 6 and 12, making them a good match for LCCCs. They can be processed using conventional techniques, although drilling vias can be difficult. They have good dielectric properties and compare favorably with FR-4 for substrate size and weight.

Alumina (ceramic) substrates are used extensively for high-reliability military applications and thick-film hybrids. The weight, cost, limited substrate size and inherent brittleness of alumina means that its use as a substrate material is limited to applications where these disadvantages are outweighed by the advantage of good thermal conductivity and a TCE that exactly matches that of LCCCs. A further limitation is that they require thick-film screening processing.

Copper-clad Invar substrates are the leading contenders for TCE control at present. It can be tailored to provide a selected TCE by varying the copper-to-Invar ratio. Figure 20 shows the construction of a typical multilayer substrate employing two cores providing the power and ground planes. Plated-through holes provide an integral board-to-board interconnection. The low TCE of the core dominates the TCE of the overall substrate, making it possible to mount LCCCs with confidence.

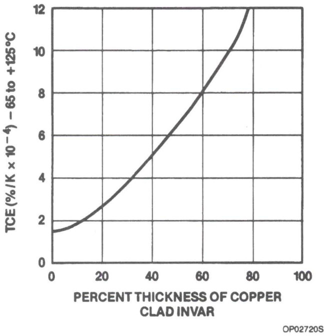
Because the TCE of copper is high, and that of Invar is low, the overall TCE of the substrate can be adjusted by varying the thickness of the copper layers. Figure 21 plots the TCE range of the copper-clad Invar as a function of copper thickness and shows the TCE range of each of several other materials to which the clad material can be matched.

For example, if the TCE of Alumina is to be matched, then the core should have about 46% thickness of copper. When this material is used as a thermal mounting plane, it also acts as a heatsink.



NOTE:
Data provided by N.V. Philips

Figure 20. Section Through a Typical Multilayer Substrate Incorporating Copper-Clad Invar Ground and Power Planes, Interconnected via Plated-Through Holes



NOTE:
Data provided by N.V. Philips

Figure 21. The TCE Range of Copper-Clad Invar as a Function of Copper Thickness

Thermal Considerations for Surface-Mounted Devices

Table 1. Substrate Material Properties

SUBSTRATE MATERIAL	TCE (10^{-6}/°C)	THERMAL CONDUCTIVITY (W/m^3K)
Glass-epoxy (FR-4)	13 – 17	0.15
Glass polyimide	12 – 16	0.35
Polyimide Kevlar	4 – 8	0.12
Polyimide quartz	6 – 12	TBD
Copper-clad Invar	6.4 (typical)	165 (lateral) 16 (transverse)
Alumina	5 – 7	21
Compliant layer Substrate	See Notes	0.15 – 0.3

NOTES:
Compliant layer conforms to TCE of the LCCC and to base substrate material.
Data provided by N.V. Philips
KEVLAR® is a registered trademark of DU PONT.
INVAR® is a registered trademark of TEXAS INSTRUMENTS.

CONCLUSION

Thermal management remains a major concern of producers and users of ICs. The advent of SMD technology has made a thorough understanding of the thermal characteristics of both the devices and the systems they are used in mandatory. The SMD package, being smaller, does have a higher θ_{JA} than its standard DIP counterpart . . . even with copper leadframes. That is the major trade-off one accepts for package miniaturization. However, consideration of all the variables affecting IC junction temperatures will allow the user to take maximum advantage of the benefits derived from use of this technology.

Package Outlines

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

GENERAL

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across / the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120mils square die for plastic packages and a 90mils square die in the smallest available cavity for hermetic packages. All units were solder-mounted to PC boards, with standard stand-off, for measurement.

PLASTIC ONLY

5. Lead material: Alloy 42 (Nickel/Iron Alloy), Olin 194 (Copper Alloy), or equivalents, solder-dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO packages/microminiature packages:
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

HERMETIC ONLY

10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated, tin-plated, or solder-dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent — tin-plated, gold-plated or solder-dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent — gold- or tin-plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel- or tin-plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold-plated, alloy seal.
    d. BeO ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb 0.010 inches.
16. Maximum glass climb or lid skew is 0.010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

PLASTIC PACKAGES

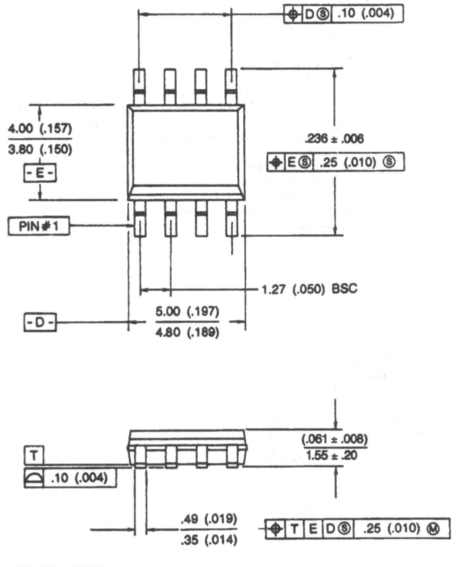
DESCRIPTION	PACKAGE CODE	θ_{JA}/θ_{JC} (°C/W)	PACKAGE TYPE
Standard Dual-In-Line Packages			
8-Pin	N	99/50	
14-Pin	N	86/48	TO-116/MO-001
16-Pin	N	83/42	MO-001
18-Pin	N	63/29	
20-Pin	N	61/24	
22-Pin	N	51/23	
24-Pin	N	52/23	MO-015
28-Pin	N	52/23	MO-015
Metal Headers			
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO-5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Cerdip Family			
8-Pin	FE	110/30	Dual-in-Line Ceramic
14-Pin	F	110/30	Dual-in-Line Ceramic
16-Pin	F	100/30	Dual-in-Line Ceramic
18-Pin	F	93/27	Dual-in-Line Ceramic
20-Pin	F	90/25	Dual-in-Line Ceramic
22-Pin	F	75/27	Dual-in-Line Ceramic
24-Pin	F	60/26	Dual-in-Line Ceramic
28-Pin	F	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side-Brazed Lead			
16-Pin	I	90/25	DIP Laminate

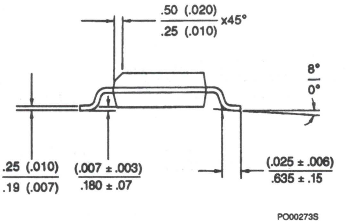
SO Package Thermal Data

PACKAGE TYPE	PACKAGE MOUNTING TECHNIQUE*	MAX. ALLOWABLE POWER DISS. (mW) AT 25°C	MAX. ALLOWABLE POWER DISS. (mW) AT 70°C	THERMAL RESISTANCE (θ_{JA}°C/WATT)	
				Average	Maximum
SO-14	PCB	658	421	190	225
	Ceramic	962	615	130	165
	Ceramic w/H.S.	1471	941	85	110
SO-16	PCB	862	551	145	170
	Ceramic	1250	800	100	125
	Ceramic w/H.S.	1923	1231	65	85
SO-16L	PCB	1250	800	100	140
	Ceramic	1743	1143	70	100
	Ceramic w/H.S.	2500	1600	50	65
SO-20	PCB	1471	941	85	115
	Ceramic	2273	1454	55	85
	Ceramic w/H.S.	3572	2286	35	55
SO-24	PCB	1563	1000	80	110
	Ceramic	2000	1600	50	80
	Ceramic w/H.S.	4167	2667	30	50

PCB = Printed circuit board
Ceramic = Ceramic substrate
Ceramic w/H.S. = Ceramic substrate with heat sink and/or Thermal compound
*Air gap is 0.006 inches unless thermal compound is used

8-PIN PLASTIC SO (D PACKAGE)

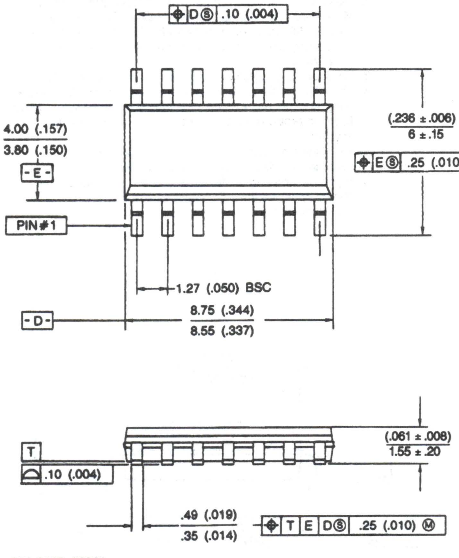

⊕ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
.236 ± .006
⊕ E Ⓢ .25 (.010) Ⓢ
PIN#1
1.27 (.050) BSC
-D-
5.00 (.197)
4.80 (.189)
T
.10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
853-0174 88070

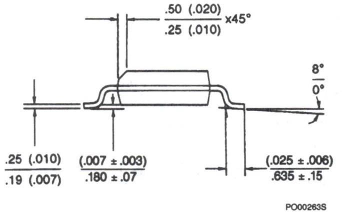

.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15
PO00273S

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

14-PIN PLASTIC SO (D PACKAGE)


⊕ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
(.236 ± .006)
6 ± .15
⊕ E Ⓢ .25 (.010) Ⓢ
PIN#1
1.27 (.050) BSC
-D-
8.75 (.344)
8.55 (.337)
T
.10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
853-0175 88068

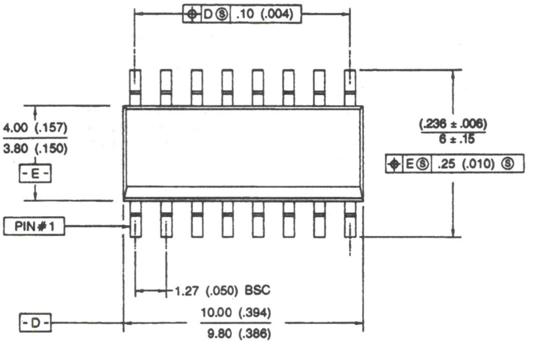

.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15
PO00263S

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

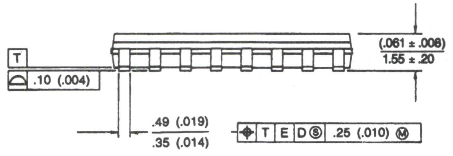
For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

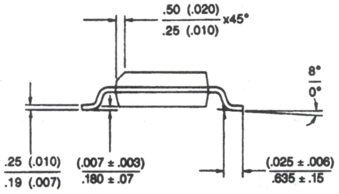
16-PIN PLASTIC SO (D PACKAGE)


D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
PIN#1
(.236 ± .006)
6 ± .15
E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
10.00 (.394)
9.80 (.386)

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

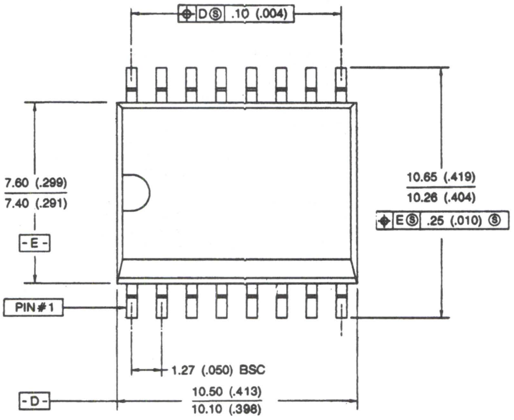

T
.10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
T E D Ⓢ .25 (.010) Ⓜ


.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15

853-0005 88069

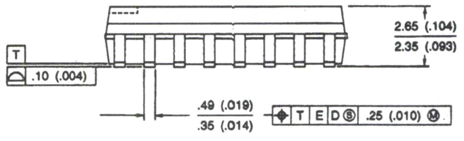
PO00252S

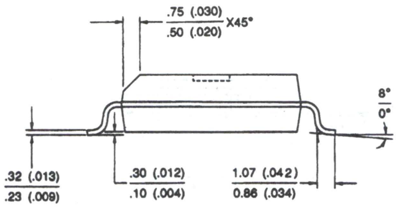
16-PIN PLASTIC SOL (D PACKAGE)


D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN#1
10.65 (.419)
10.26 (.404)
E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
10.50 (.413)
10.10 (.398)

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

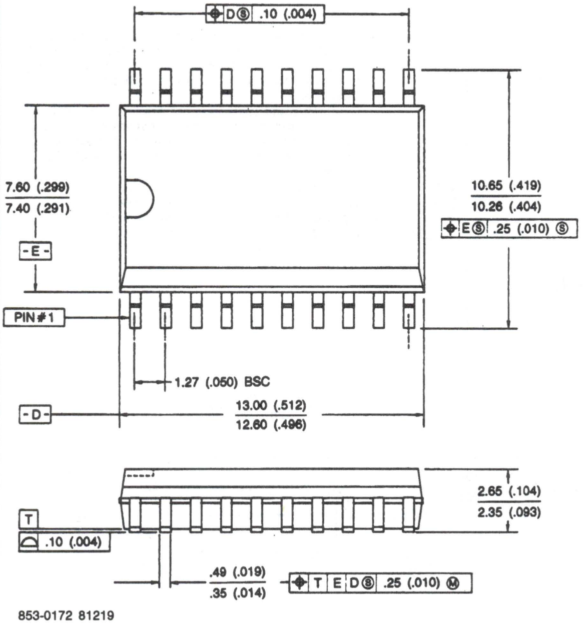

T
.10 (.004)
2.65 (.104)
2.35 (.093)
.49 (.019)
.35 (.014)
T E D Ⓢ .25 (.010) Ⓜ


.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
0.86 (.034)

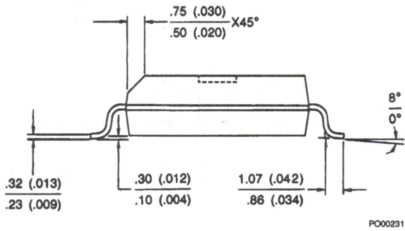
853-0171 81218

PO00241S

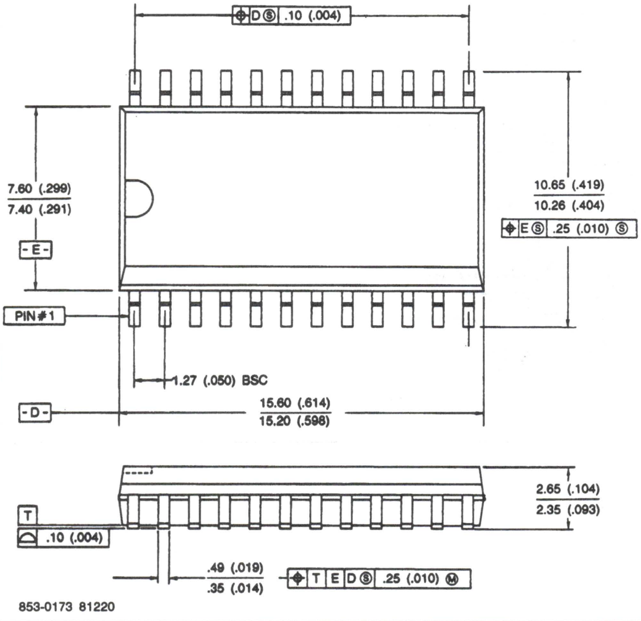
20-PIN PLASTIC SOL (D PACKAGE)


⌖ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN #1
10.65 (.419)
10.26 (.404)
⌖ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
13.00 (.512)
12.60 (.496)
T
.10 (.004)
2.65 (.104)
2.35 (.093)
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ
853-0172 81219

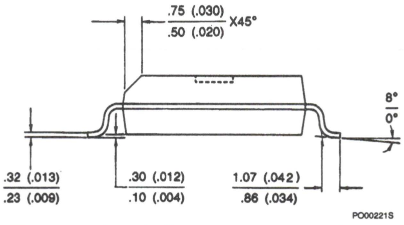
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.


.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
PO00231S

24-PIN PLASTIC SOL (D PACKAGE)


⌖ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN #1
10.65 (.419)
10.26 (.404)
⌖ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
15.60 (.614)
15.20 (.598)
T
.10 (.004)
2.65 (.104)
2.35 (.093)
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ
853-0173 81220

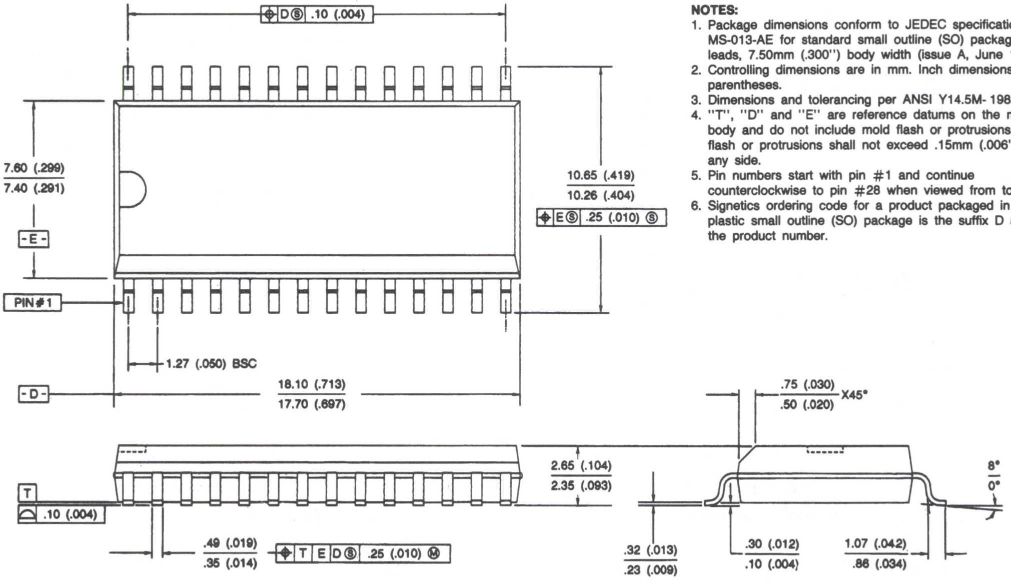
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.


.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
PO00221S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

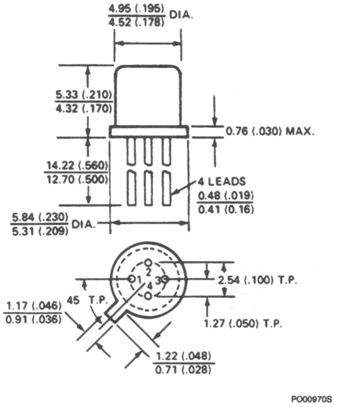
28-PIN PLASTIC SOL (D PACKAGE)


⌖ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
10.65 (.419)
10.26 (.404)
⌖ E Ⓢ .25 (.010) Ⓢ
PIN #1
1.27 (.050) BSC
-D-
18.10 (.713)
17.70 (.697)
.75 (.030)
.50 (.020)
X45°
2.65 (.104)
2.35 (.093)
8°
0°
T
.10 (.004)
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
853-0006 81217
PO00212S

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

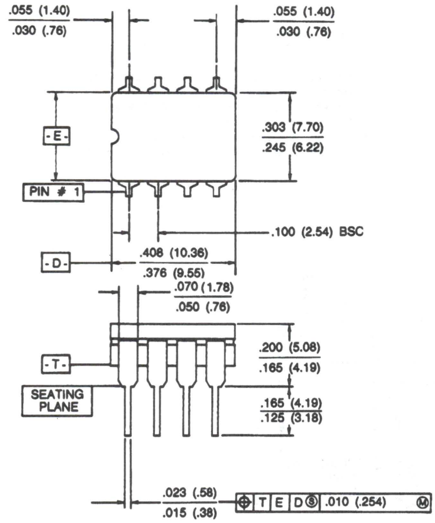
4-PIN HERMETIC TO-72 HEADER (E PACKAGE)

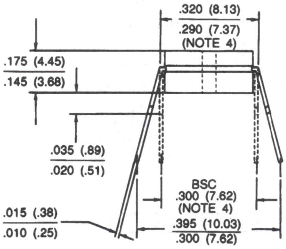

4.95 (.195)
4.52 (.178)
DIA.
5.33 (.210)
4.32 (.170)
0.76 (.030) MAX.
14.22 (.560)
12.70 (.500)
4 LEADS
0.48 (.019)
0.41 (0.16)
5.84 (.230)
5.31 (.209)
DIA.
1
2
3
4
2.54 (.100) T.P.
1.17 (.046)
0.91 (.036)
45 T.P.
1.27 (.050) T.P.
1.22 (.048)
0.71 (.028)
PO00970S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

8-PIN CERDIP (FE PACKAGE)


.055 (1.40)
.030 (.76)
.055 (1.40)
.030 (.76)
-E-
.303 (7.70)
.245 (6.22)
PIN # 1
.100 (2.54) BSC
-D-
.408 (10.36)
.376 (9.55)
.070 (1.78)
.050 (.76)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
T E D S .010 (.254) M


.320 (8.13)
.290 (7.37)
(NOTE 4)
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 4)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

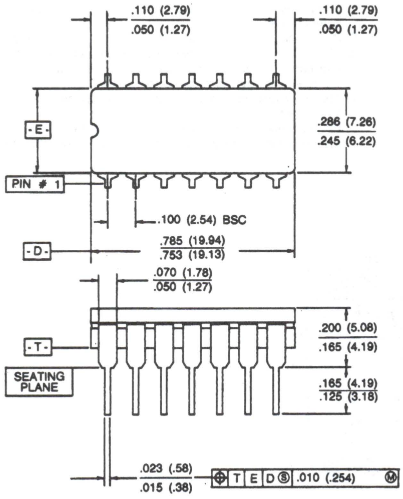
NOTES:

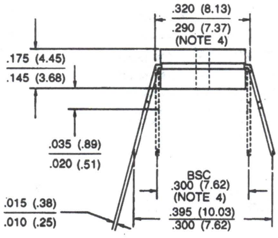
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0580 81594

PO00480S

14-PIN CERDIP (F PACKAGE)


.110 (2.79)
.050 (1.27)
.110 (2.79)
.050 (1.27)
-E-
.286 (7.26)
.245 (6.22)
PIN # 1
.100 (2.54) BSC
-D-
.785 (19.94)
.753 (19.13)
.070 (1.78)
.050 (1.27)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
T E D S .010 (.254) M


.320 (8.13)
.290 (7.37)
(NOTE 4)
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 4)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

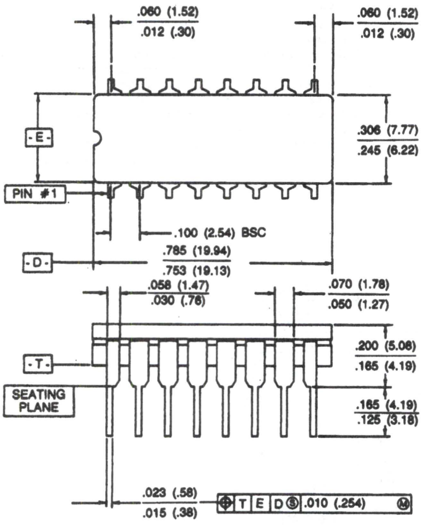
NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

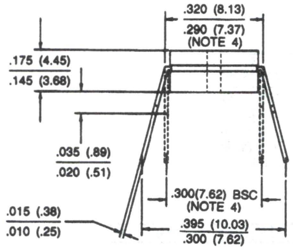
853-0581 81594

PO00440S

16-PIN CERDIP (F PACKAGE)


.060 (1.52)
.012 (.30)
.060 (1.52)
.012 (.30)
-E-
.306 (7.77)
.245 (6.22)
PIN #1
.100 (2.54) BSC
-D-
.785 (19.94)
.753 (19.13)
.058 (1.47)
.030 (.76)
.070 (1.78)
.050 (1.27)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
⊕ T E D Ⓢ .010 (.254) Ⓜ

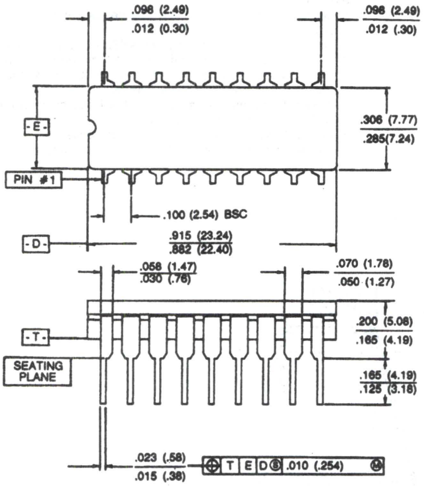
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.


.320 (8.13)
.290 (7.37)
(NOTE 4)
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
.300(7.62) BSC
(NOTE 4)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

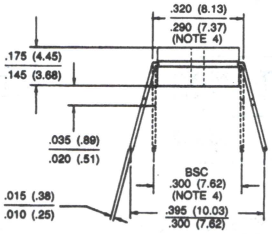
853-0582 81594

PO00490S

18-PIN CERDIP (F PACKAGE)


.098 (2.49)
.012 (0.30)
.098 (2.49)
.012 (.30)
-E-
.306 (7.77)
.285(7.24)
PIN #1
.100 (2.54) BSC
-D-
.915 (23.24)
.882 (22.40)
.058 (1.47)
.030 (.76)
.070 (1.78)
.050 (1.27)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
⊕ T E D Ⓢ .010 (.254) Ⓜ

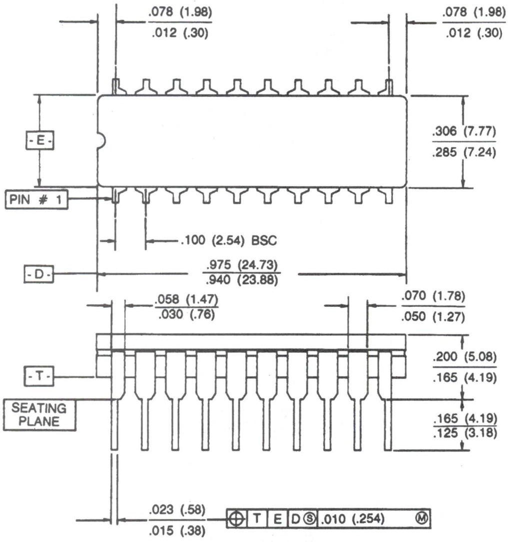
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.


.320 (8.13)
.290 (7.37)
(NOTE 4)
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 4)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

853-0583 81594

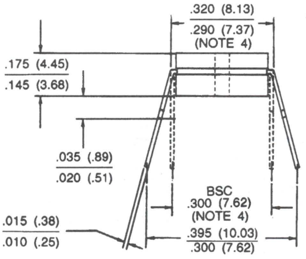
PO00470S

20-PIN CERDIP (F PACKAGE)


.078 (1.98)
.012 (.30)
.078 (1.98)
.012 (.30)
-E-
.306 (7.77)
.285 (7.24)
PIN # 1
.100 (2.54) BSC
-D-
.975 (24.73)
.940 (23.88)
.058 (1.47)
.030 (.76)
.070 (1.78)
.050 (1.27)
-T-
.200 (5.08)
.165 (4.19)
SEATING PLANE
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
T E D Ⓢ .010 (.254) Ⓜ

NOTES:

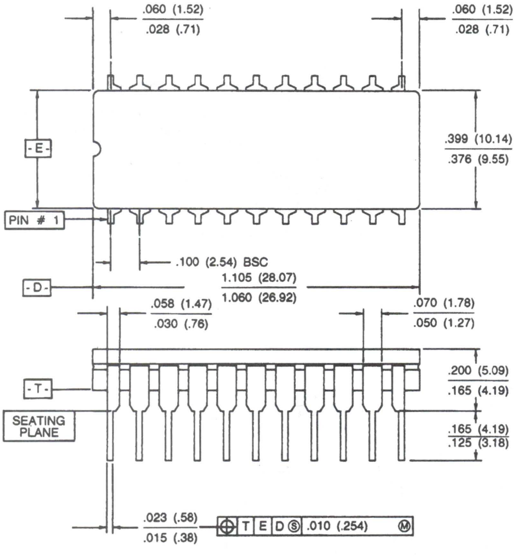
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.


.320 (8.13)
.290 (7.37)
(NOTE 4)
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 4)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

853-0584 81594

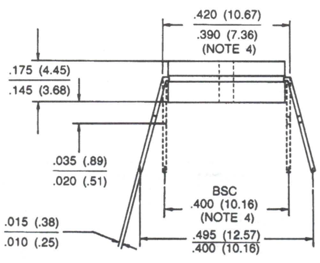
PO00430S

22-PIN CERDIP (F PACKAGE)


.060 (1.52)
.028 (.71)
.060 (1.52)
.028 (.71)
-E-
.399 (10.14)
.376 (9.55)
PIN # 1
.100 (2.54) BSC
-D-
1.105 (28.07)
1.060 (26.92)
.058 (1.47)
.030 (.76)
.070 (1.78)
.050 (1.27)
-T-
.200 (5.09)
.165 (4.19)
SEATING PLANE
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
T E D Ⓢ .010 (.254) Ⓜ

NOTES:

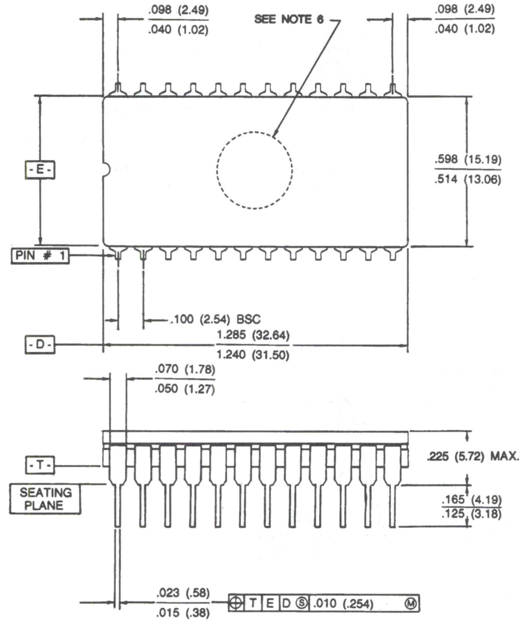
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

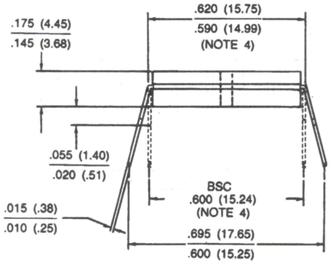

.420 (10.67)
.390 (7.36)
(NOTE 4)
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
BSC
.400 (10.16)
(NOTE 4)
.015 (.38)
.010 (.25)
.495 (12.57)
.400 (10.16)

853-0585 81594

PO00420S

24-PIN CERDIP (F PACKAGE)


.098 (2.49)
.040 (1.02)
SEE NOTE 6
.098 (2.49)
.040 (1.02)
-E-
.598 (15.19)
.514 (13.06)
PIN # 1
.100 (2.54) BSC
-D-
1.285 (32.64)
1.240 (31.50)
.070 (1.78)
.050 (1.27)
-T-
SEATING PLANE
.225 (5.72) MAX.
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
⊕ T E D Ⓢ .010 (.254) Ⓜ

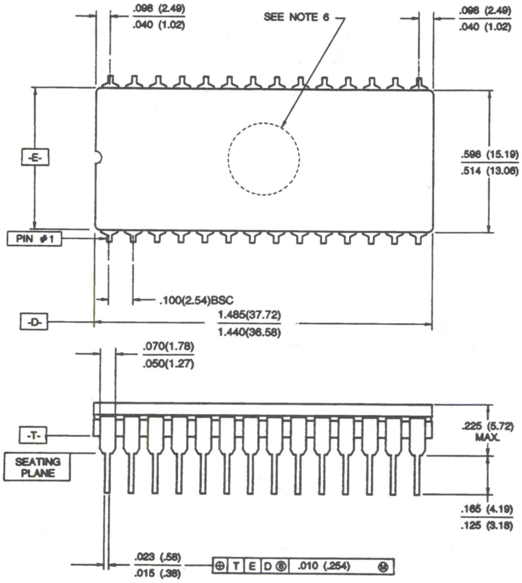

.175 (4.45)
.145 (3.68)
.620 (15.75)
.590 (14.99)
(NOTE 4)
.055 (1.40)
.020 (.51)
BSC
.600 (15.24)
(NOTE 4)
.015 (.38)
.010 (.25)
.695 (17.65)
.600 (15.25)

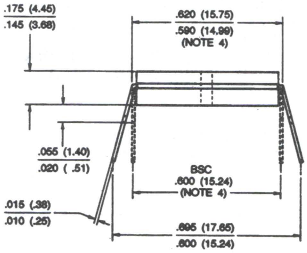
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0588 84221

PO00464S

28-PIN CERDIP (F PACKAGE)


.098 (2.49)
.040 (1.02)
SEE NOTE 6
.098 (2.49)
.040 (1.02)
-E-
.598 (15.19)
.514 (13.06)
PIN #1
.100(2.54)BSC
-D-
1.485(37.72)
1.440(36.58)
.070(1.78)
.050(1.27)
-T-
SEATING PLANE
.225 (5.72) MAX.
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
⊕ T E D Ⓢ .010 (.254) Ⓜ


.175 (4.45)
.145 (3.68)
.620 (15.75)
.590 (14.99)
(NOTE 4)
.055 (1.40)
.020 (.51)
BSC
.600 (15.24)
(NOTE 4)
.015 (.38)
.010 (.25)
.695 (17.65)
.600 (15.24)

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM Products.

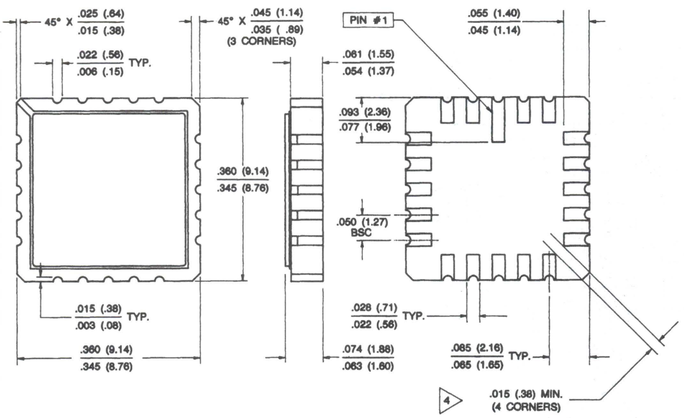
853-0589 84000

PO00660S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

20-PIN PGA (G PACKAGE)

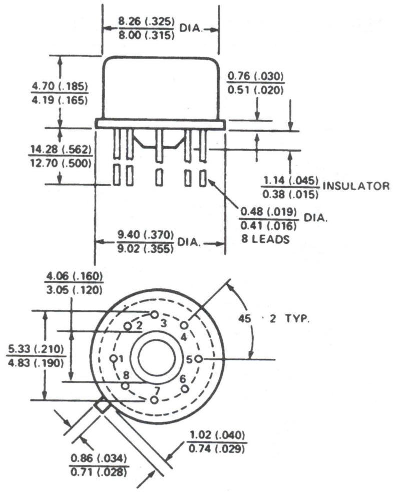

45° X .025 (.64) / .015 (.38)
45° X .045 (1.14) / .035 (.89) (3 CORNERS)
PIN #1
.055 (1.40) / .045 (1.14)
.022 (.56) / .006 (.15) TYP.
.061 (1.55) / .054 (1.37)
.093 (2.36) / .077 (1.96)
.360 (9.14) / .345 (8.76)
.050 (1.27) BSC
.015 (.38) / .003 (.08) TYP.
.028 (.71) / .022 (.56) TYP.
.360 (9.14) / .345 (8.76)
.074 (1.88) / .063 (1.60)
.085 (2.16) / .065 (1.65) TYP.
4
.015 (.38) MIN. (4 CORNERS)

NOTES:
1. Package dimensions conform to Mil-M-38510, outline NO. C – 2, 20 leads, square ceramic leadless chip carrier.
2. Controlling dimension: inches, millimeters are shown in parenthesis.
3. Dimension and tolerancing per ANSI Y14.5M – 1982.
4. This dimension represents the minimum spacing between the corner contact pads. These corner pads may have a .020 inch by 45 degree maximum chamfer to accomplish the .015 minimum spacing.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.
6. Signetics order code for product packaged in a CCCL is the suffix "G" after the product number.

853-0063 82276

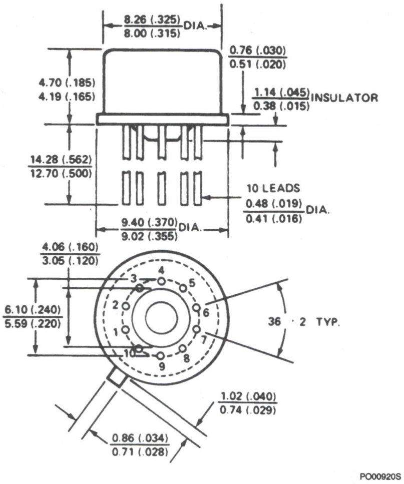
PO00870S

8-PIN HERMETIC TO-5 HEADER (H PACKAGE)

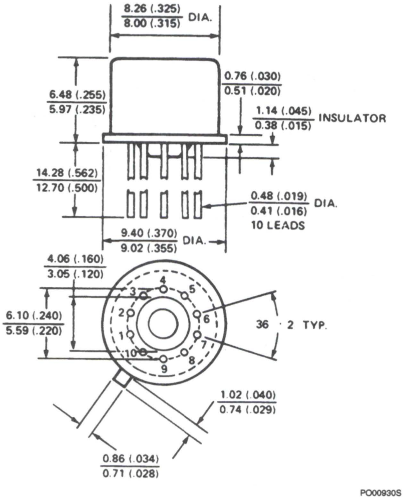

8.26 (.325) / 8.00 (.315) DIA.
4.70 (.185) / 4.19 (.165)
0.76 (.030) / 0.51 (.020)
14.28 (.562) / 12.70 (.500)
1.14 (.045) / 0.38 (.015) INSULATOR
0.48 (.019) / 0.41 (.016) DIA. 8 LEADS
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
45 · 2 TYP.
5.33 (.210) / 4.83 (.190)
1
2
3
4
5
6
7
8
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

PO00910S

10-PIN HERMETIC TO-5/100 HEADER SHORT CAN (H PACKAGE)

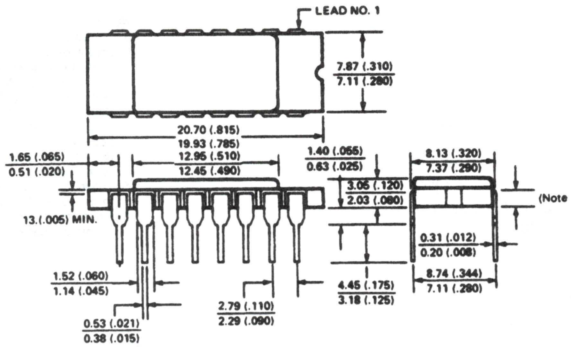

8.26 (.325)
8.00 (.315) DIA.
0.76 (.030)
0.51 (.020)
4.70 (.185)
4.19 (.165)
1.14 (.045)
0.38 (.015) INSULATOR
14.28 (.562)
12.70 (.500)
10 LEADS
0.48 (.019)
0.41 (.016) DIA.
9.40 (.370)
9.02 (.355) DIA.
4.06 (.160)
3.05 (.120)
6.10 (.240)
5.59 (.220)
1
2
3
4
5
6
7
8
9
10
36 · 2 TYP.
1.02 (.040)
0.74 (.029)
0.86 (.034)
0.71 (.028)
PO00920S

10-PIN HERMETIC TO-5/100 HEADER TALL CAN (H PACKAGE)


8.26 (.325)
8.00 (.315) DIA.
0.76 (.030)
0.51 (.020)
6.48 (.255)
5.97 (.235)
1.14 (.045)
0.38 (.015) INSULATOR
14.28 (.562)
12.70 (.500)
0.48 (.019)
0.41 (.016) DIA.
10 LEADS
9.40 (.370)
9.02 (.355) DIA.
4.06 (.160)
3.05 (.120)
6.10 (.240)
5.59 (.220)
1
2
3
4
5
6
7
8
9
10
36 · 2 TYP.
1.02 (.040)
0.74 (.029)
0.86 (.034)
0.71 (.028)
PO00930S

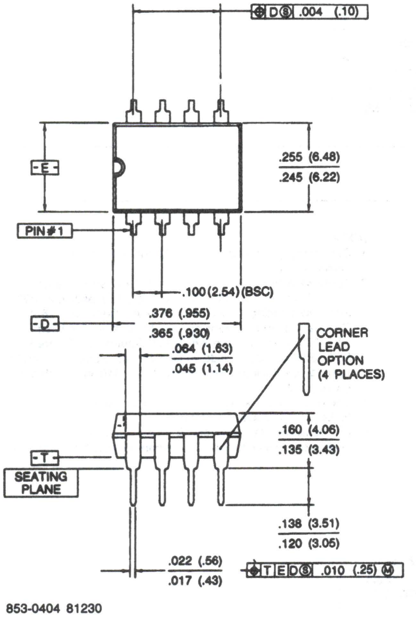
For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

16-PIN HERMETIC SDIP (I PACKAGE)


LEAD NO. 1
7.87 (.310)
7.11 (.280)
20.70 (.815)
19.93 (.785)
1.65 (.065)
0.51 (.020)
12.95 (.510)
12.45 (.490)
1.40 (.055)
0.63 (.025)
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
(Note
13.(.005) MIN.
0.31 (.012)
0.20 (.008)
1.52 (.060)
1.14 (.045)
8.74 (.344)
7.11 (.280)
4.45 (.175)
3.18 (.125)
2.79 (.110)
2.29 (.090)
0.53 (.021)
0.38 (.015)

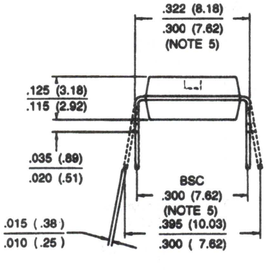
PO00940S

8-PIN PLASTIC PDIP (N PACKAGE)


D S .004 (.10)
-E-
.255 (6.48)
.245 (6.22)
PIN #1
.100 (2.54) (BSC)
-D-
.376 (.955)
.365 (.930)
.064 (1.63)
.045 (1.14)
CORNER
LEAD
OPTION
(4 PLACES)
.160 (4.06)
.135 (3.43)
-T-
SEATING
PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
T E D S .010 (.25) M

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.


.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

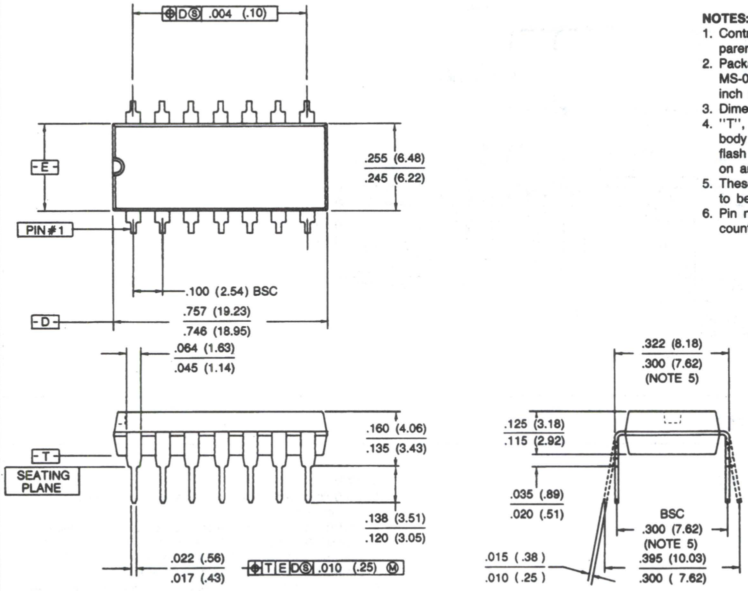
853-0404 81230

PO00312S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

14-PIN PLASTIC DIP (N PACKAGE)

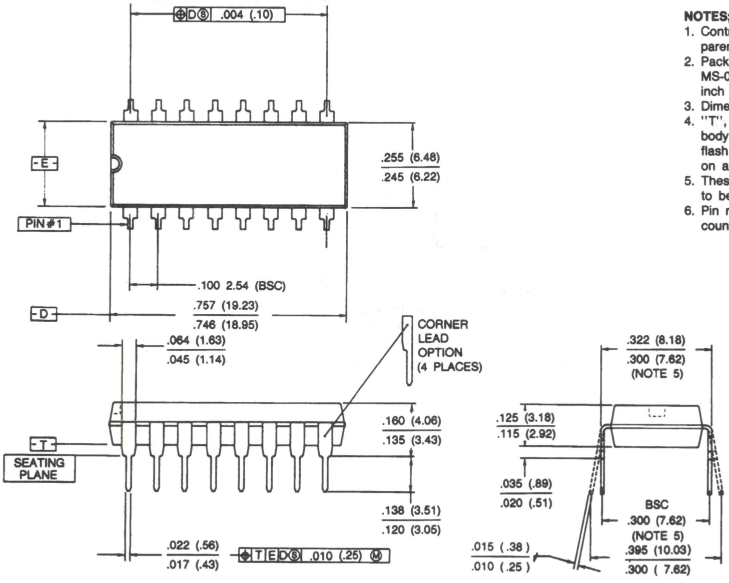


⊕ D Ⓢ .004 (.10)
-E-
PIN #1
.255 (6.48)
.245 (6.22)
.100 (2.54) BSC
-D-
.757 (19.23)
.746 (18.95)
.064 (1.63)
.045 (1.14)
-T-
SEATING PLANE
.160 (4.06)
.135 (3.43)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
853-0405 81231
PO00330S

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

16-PIN PLASTIC DIP (N PACKAGE)



⊕ D Ⓢ .004 (.10)
-E-
PIN #1
.255 (6.48)
.245 (6.22)
.100 2.54 (BSC)
-D-
.757 (19.23)
.746 (18.95)
.064 (1.63)
.045 (1.14)
CORNER LEAD OPTION (4 PLACES)
-T-
SEATING PLANE
.160 (4.06)
.135 (3.43)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
853-0406 81232
PO00280S

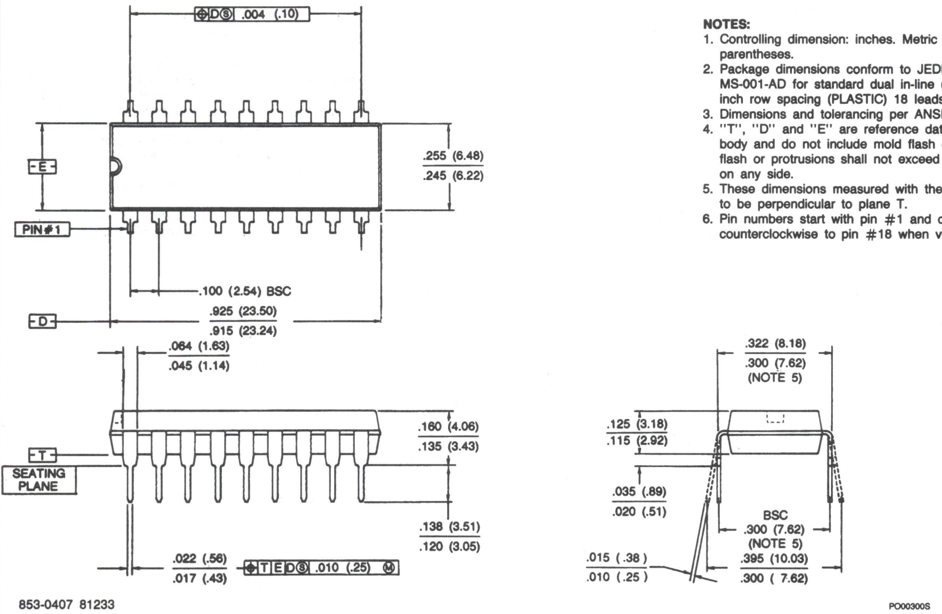
NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

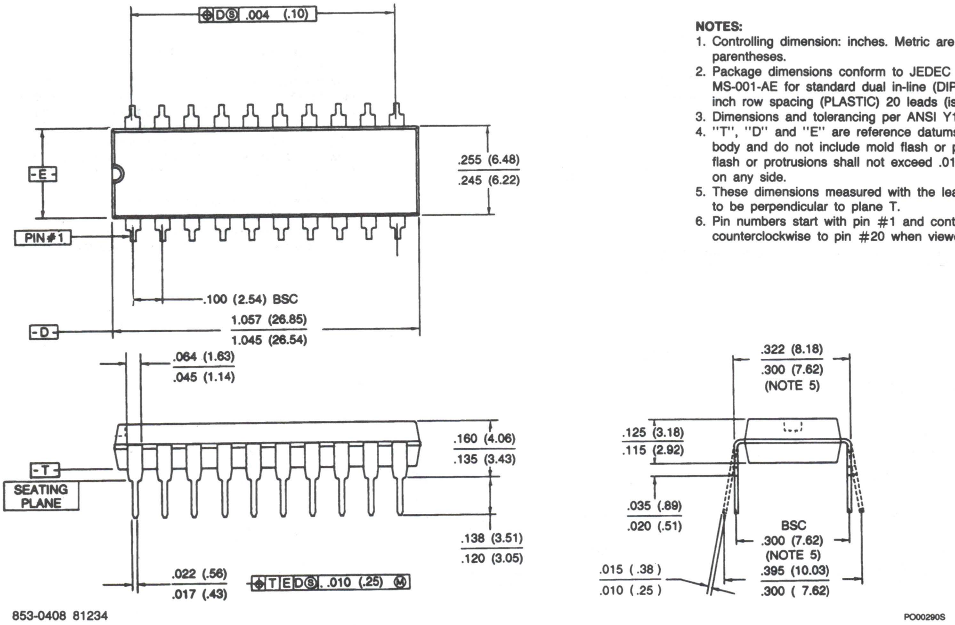
18-PIN PLASTIC DIP (N PACKAGE)


.004 (.10)
-E-
PIN #1
.255 (6.48)
.245 (6.22)
.100 (2.54) BSC
-D-
.925 (23.50)
.915 (23.24)
.064 (1.63)
.045 (1.14)
.160 (4.06)
.135 (3.43)
-T-
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
T E D S .010 (.25) M
853-0407 81233
.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
PO0030OS

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AD for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 18 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

20-PIN PLASTIC DIP (N PACKAGE)


.004 (.10)
-E-
PIN #1
.255 (6.48)
.245 (6.22)
.100 (2.54) BSC
-D-
1.057 (26.85)
1.045 (26.54)
.064 (1.63)
.045 (1.14)
.160 (4.06)
.135 (3.43)
-T-
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
T E D S .010 (.25) M
853-0408 81234
.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)
PO00290S

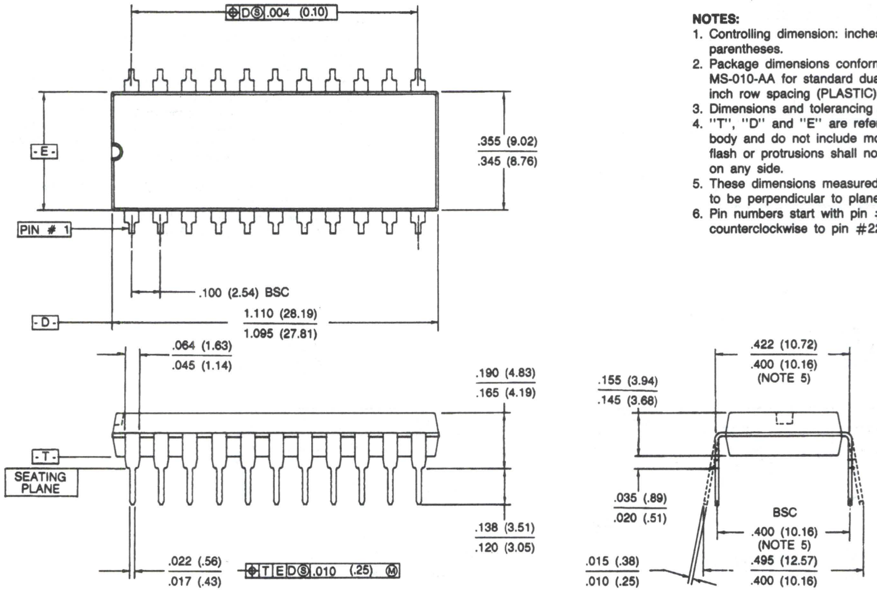
NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

22-PIN PLASTIC DIP (N PACKAGE)

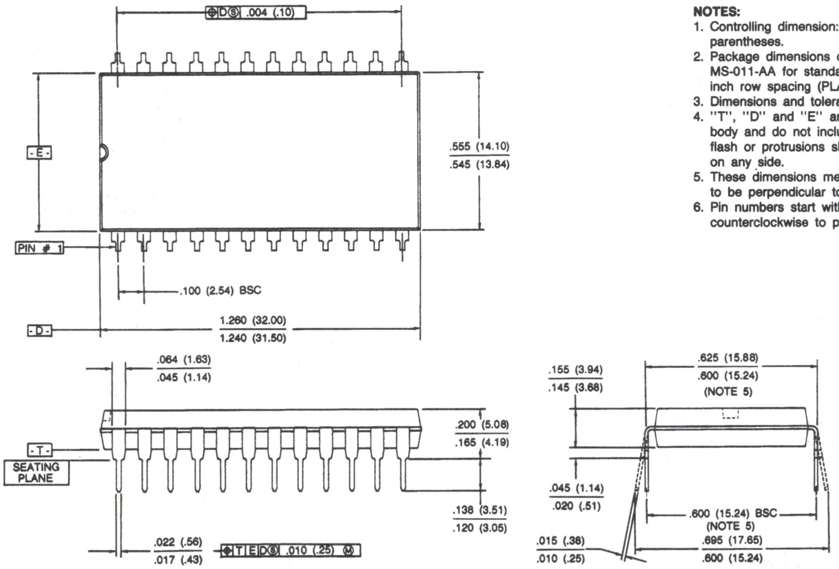

⊕ D Ⓢ .004 (0.10)
-E-
PIN # 1
.355 (9.02)
.345 (8.76)
.100 (2.54) BSC
-D-
1.110 (28.19)
1.095 (27.81)
.064 (1.63)
.045 (1.14)
.190 (4.83)
.165 (4.19)
-T-
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
.155 (3.94)
.145 (3.68)
.422 (10.72)
.400 (10.16)
(NOTE 5)
.035 (.89)
.020 (.51)
BSC
.400 (10.16)
(NOTE 5)
.495 (12.57)
.400 (10.16)
.015 (.38)
.010 (.25)

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-010-AA for standard dual in-line (DIP) package .400 inch row spacing (PLASTIC) 22 leads (issue A. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

853-0409 81235

PO00341S

24-PIN PLASTIC DIP (N PACKAGE)


⊕ D Ⓢ .004 (.10)
-E-
PIN # 1
.555 (14.10)
.545 (13.84)
.100 (2.54) BSC
-D-
1.260 (32.00)
1.240 (31.50)
.064 (1.63)
.045 (1.14)
.200 (5.08)
.165 (4.19)
-T-
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
.155 (3.94)
.145 (3.68)
.625 (15.88)
.600 (15.24)
(NOTE 5)
.045 (1.14)
.020 (.51)
.600 (15.24) BSC
(NOTE 5)
.695 (17.65)
.600 (15.24)
.015 (.38)
.010 (.25)

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

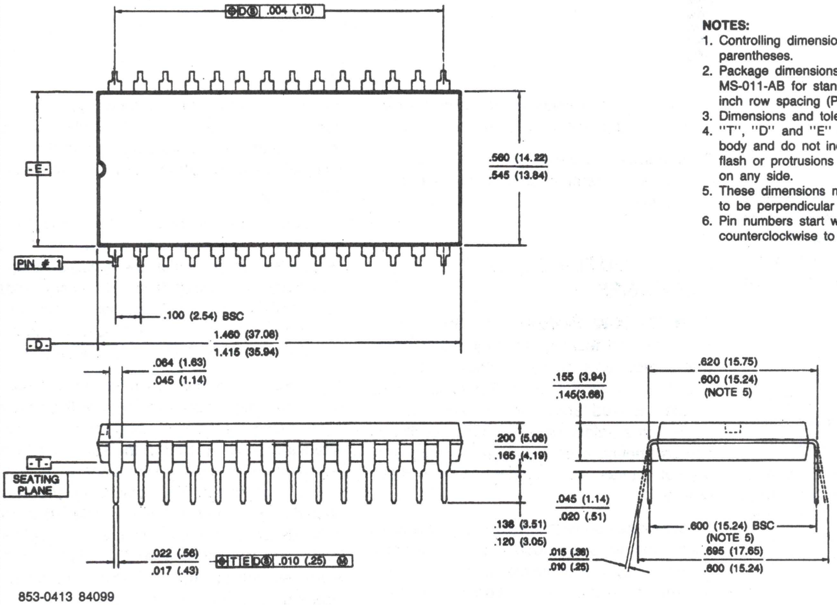
853-0412 81238

PO00361S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

28-PIN PLASTIC DIP (N PACKAGE)


⊕ D Ⓢ .004 (.10)
-E-
PIN # 1
.560 (14.22)
.545 (13.84)
.100 (2.54) BSC
-D-
1.460 (37.08)
1.415 (35.94)
.064 (1.63)
.045 (1.14)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ
.155 (3.94)
.145 (3.68)
.045 (1.14)
.020 (.51)
.015 (.38)
.010 (.25)
.620 (15.75)
.600 (15.24)
(NOTE 5)
.600 (15.24) BSC
(NOTE 5)
.695 (17.65)
.600 (15.24)
853-0413 84099
PO00372S

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

Package Outlines
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

INTRODUCTION

Soldering

1. By hand

Apply the soldering iron below the seating plane (or not more than 2mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300°C and 400°C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260°C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SMALL OUTLINE (SO) PACKAGES

The Reflow Solder Technique

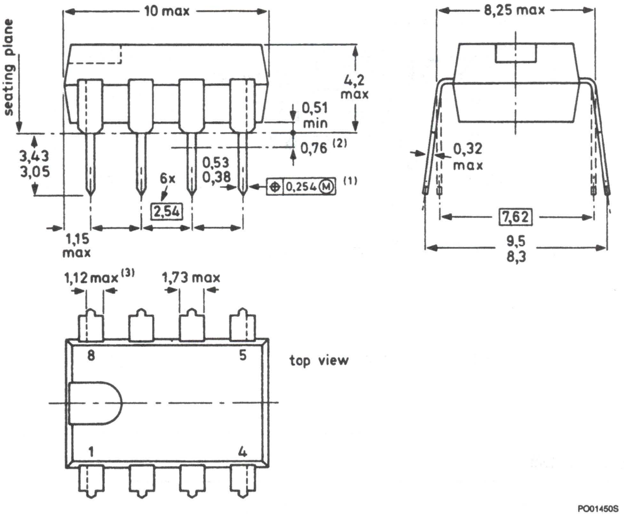
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230°C when a mild flux is used.

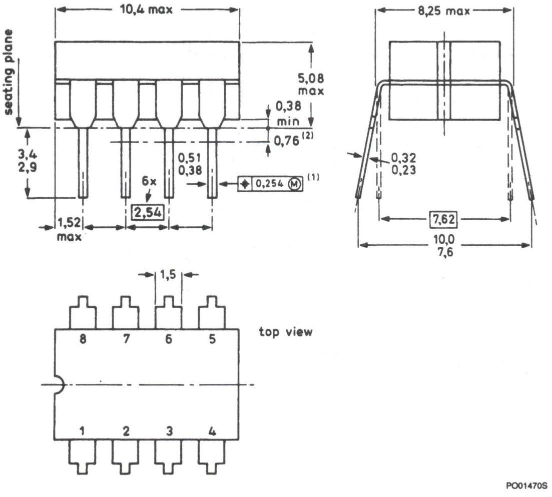
For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105μm is used for which the emulsion thickness should be about 50μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid. After soldering, the substrate must be cleaned of any remaining flux.

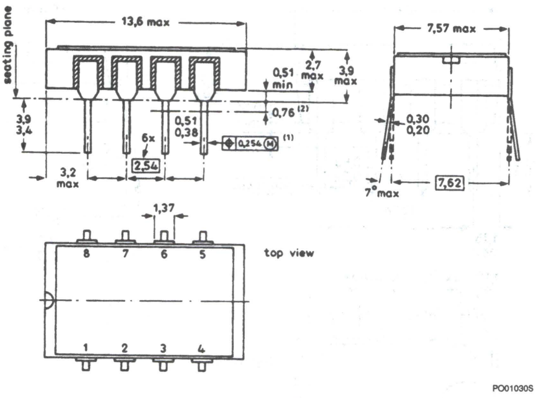
8-PIN PLASTIC SO (SOT-97A)


10 max
seating plane
4,2 max
0,51 min
0,76 (2)
3,43
3,05
6x
0,53
0,38
0,254 M (1)
2,54
1,15 max
8,25 max
0,32 max
7,62
9,5
8,3
1,12 max (3)
1,73 max
8
5
1
4
top view
PO01450S

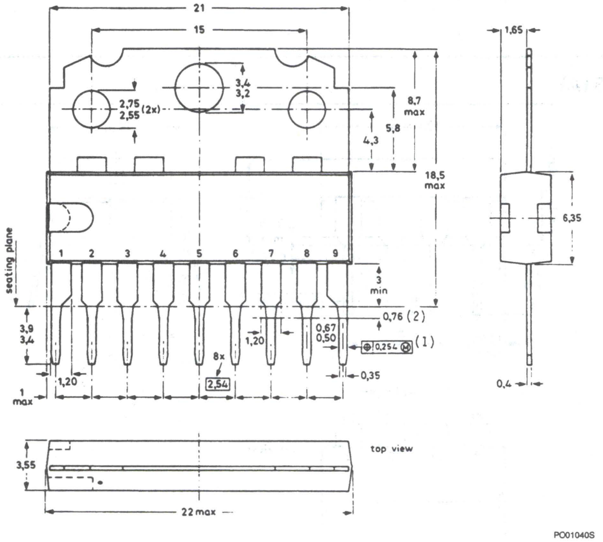
8-PIN CERDIP (SOT-151A)


10,4 max
seating plane
5,08 max
0,38 min
0,76 (2)
3,4
2,9
6x
0,51
0,38
0,254 M (1)
2,54
1,52 max
8,25 max
0,32
0,23
7,62
10,0
7,6
1,5
8
7
6
5
1
2
3
4
top view
PO01470S

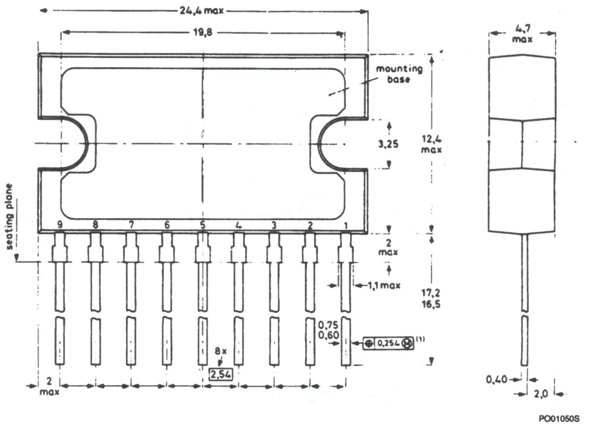
8-PIN METAL CERDIP (SOT-153B)


seating plane
13,6 max
7,57 max
0,51 min
2,7 max
3,9 max
0,76 (2)
3,9
3,4
0,51
0,38
6x
0,254 Ⓜ (1)
2,54
3,2 max
0,30
0,20
7° max
7,62
1,37
8
7
6
5
top view
1
2
3
4
PO01030S

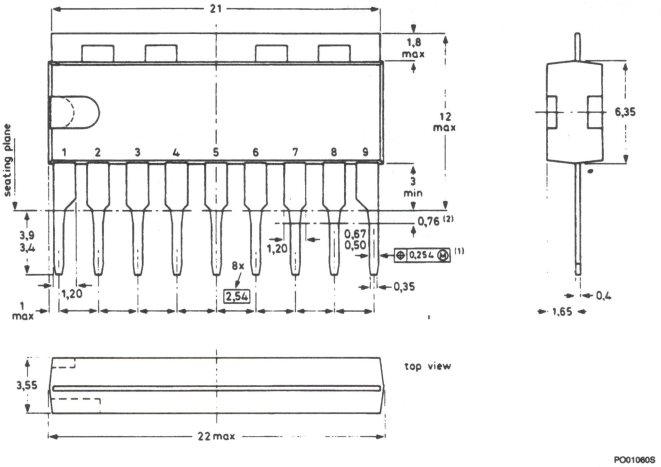
9-PIN PLASTIC SIP (SOT-110B)


21
15
1,65
3,4
3,2
2,75
2,55 (2x)
8,7 max
5,8
4,3
18,5 max
6,35
seating plane
1
2
3
4
5
6
7
8
9
3 min
0,76 (2)
3,9
3,4
0,67
0,50
1,20
0,254 Ⓜ (1)
8x
2,54
0,35
1,20
1 max
0,4
3,55
top view
22 max
PO01040S

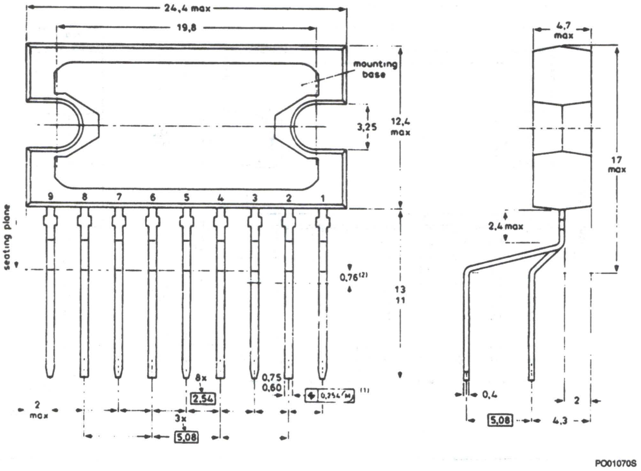
9-PIN PLASTIC POWER SIP (SOT-131A, B)


24,4 max
19,8
mounting base
4,7 max
3,25
12,4 max
seating plane
9
8
7
6
5
4
3
2
1
2 max
1,1 max
17,2
16,5
0,75
0,60
0,254 (1)
8x
2,54
2 max
0,40
2,0
PO01050S

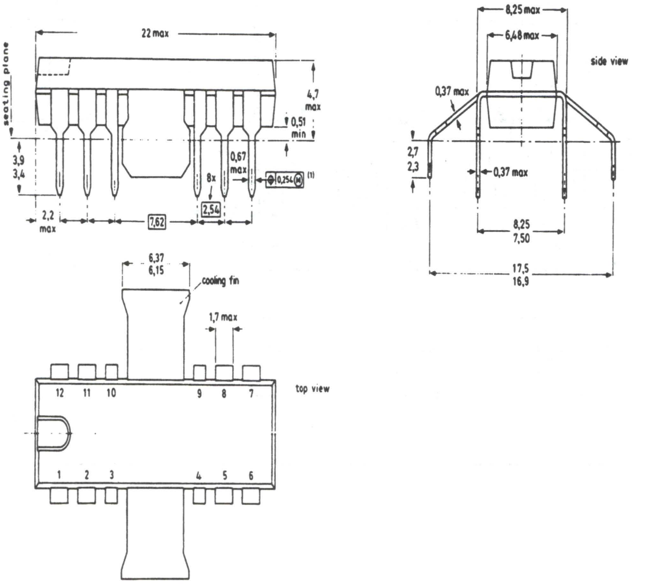
9-PIN PLASTIC SIP (SOT-142)


21
1,8 max
12 max
6,35
seating plane
1
2
3
4
5
6
7
8
9
3 min
0,76 (2)
3,9
3,4
1,20
0,67
0,50
0,254 (1)
8x
2,54
0,35
1,20
1 max
0,4
1,65
top view
3,55
22 max
PO01060S

9-PIN PLASTIC POWER SIP-BENT-TO-DIP (SOT-157B)


24,4 max
19,8
mounting base
3,25
12,4 max
seating plane
9 8 7 6 5 4 3 2 1
0,76(2)
13
11
8x
2,54
0,75
0,60
0,254 (M) (1)
2 max
3x
5,08
4,7 max
17 max
2,4 max
0,4
2
5,08
4,3
PO01070S

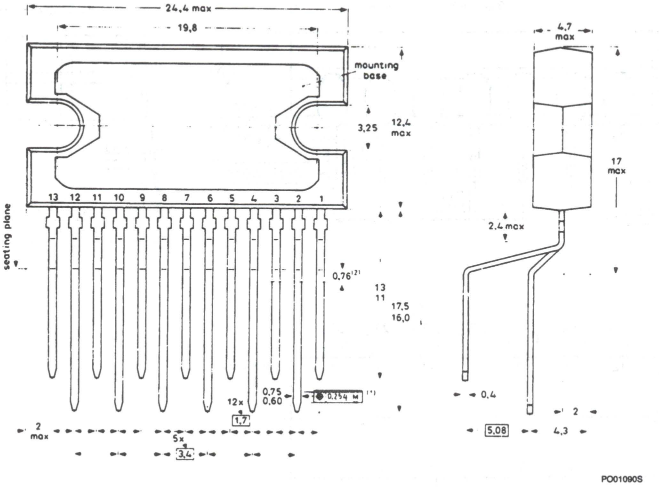
12-PIN PLASTIC DIP WITH METAL COOLING FIN (SOT-150)


22 max
seating plane
4,7 max
0,51 min
3,9
3,4
0,67 max
8x
0,254 (M) (1)
2,54
2,2 max
7,62
8,25 max
6,48 max
side view
0,37 max
2,7
2,3
0,37 max
8,25
7,50
17,5
16,9
6,37
6,15
cooling fin
1,7 max
top view
12 11 10 9 8 7
1 2 3 4 5 6
PO01080S

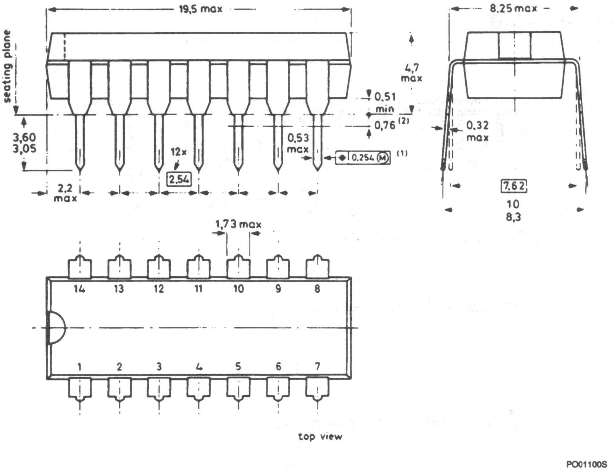
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

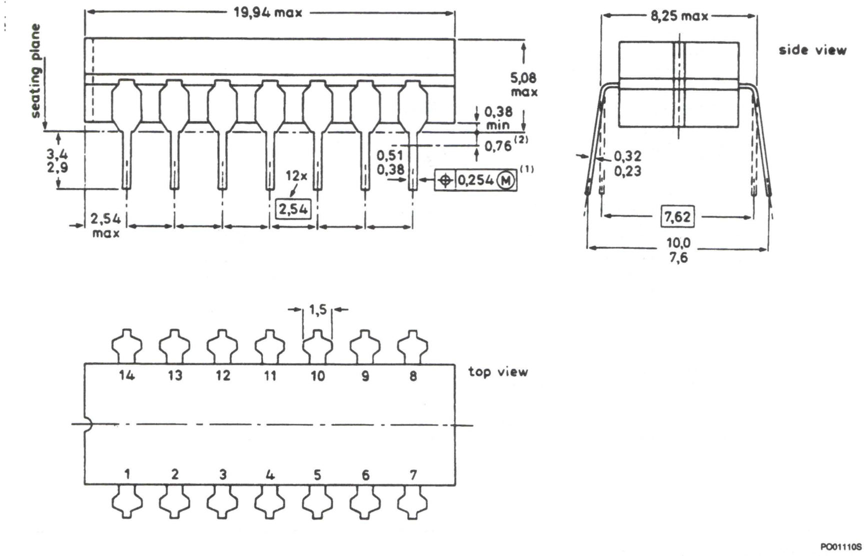
13-PIN PLASTIC POWER SIP-BENT-TO-DIP (SOT-141B)


24,4 max
19,8
mounting base
3,25
12,4 max
13 12 11 10 9 8 7 6 5 4 3 2 1
seating plane
0,76 (2)
13
11
17,5
16,0
0,75
0,60
12x
0,254 M
(1)
1,7
2 max
5x
3,4
4,7 max
17 max
2,4 max
0,4
2
5,08
4,3
PO01090S

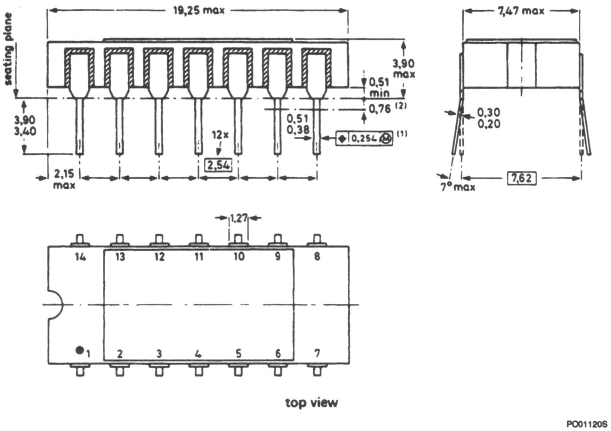
14-PIN PLASTIC DIP (SOT-27K, M, T)


19,5 max
seating plane
4,7 max
0,51 min
0,76 (2)
3,60
3,05
12x
2,54
0,53 max
0,254 (M)
(1)
2,2 max
8,25 max
0,32 max
7,62
10
8,3
1,73 max
14 13 12 11 10 9 8
1 2 3 4 5 6 7
top view
PO01100S

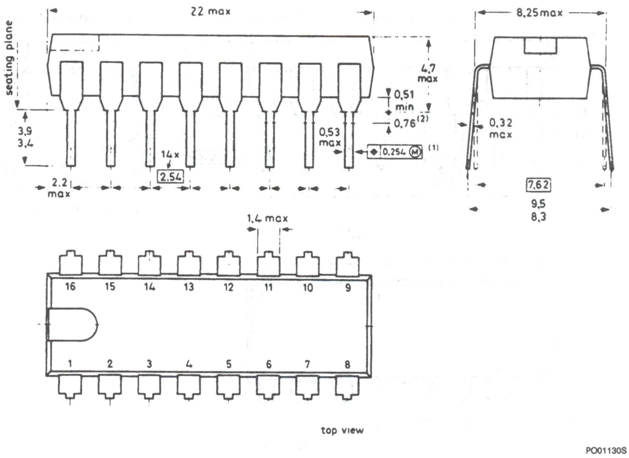
14-PIN CERDIP (SOT-73A, B, C)


19,94 max
seating plane
5,08
max
0,38
min
0,76 (2)
3,4
2,9
0,51
0,38
12x
2,54
0,254 Ⓜ (1)
2,54
max
8,25 max
side view
0,32
0,23
7,62
10,0
7,6
1,5
14
13
12
11
10
9
8
top view
1
2
3
4
5
6
7
PO01110S

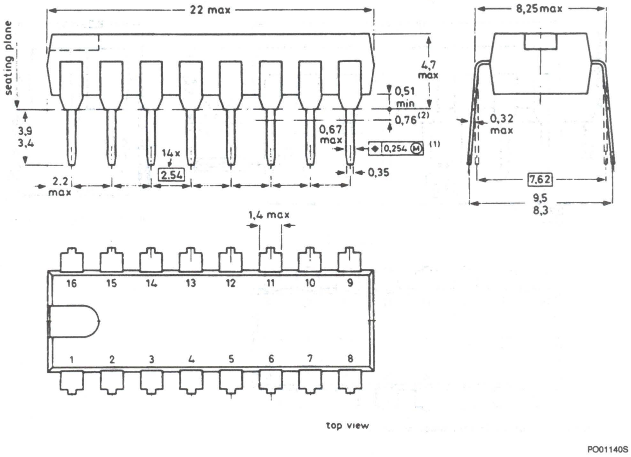
14-PIN METAL CERDIP (SOT-83B)


19,25 max
seating plane
3,90
max
0,51
min
0,76 (2)
3,90
3,40
0,51
0,38
12x
2,54
0,254 Ⓜ (1)
2,15
max
7,47 max
0,30
0,20
7° max
7,62
1,27
14
13
12
11
10
9
8
1
2
3
4
5
6
7
top view
PO01120S

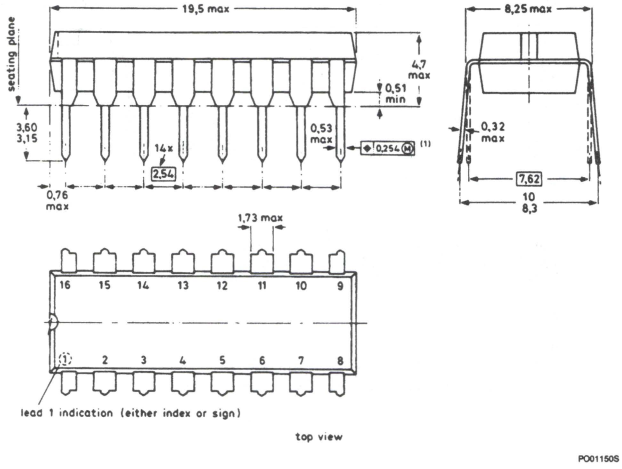
16-PIN PLASTIC DIP (SOT-38)


22 max
seating plane
4,7
max
0,51
min
0,76(2)
3,9
3,4
0,53
max
0,254 M (1)
14x
2.54
2.2
max
8,25max
0,32
max
7,62
9,5
8,3
1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view
PO01130S

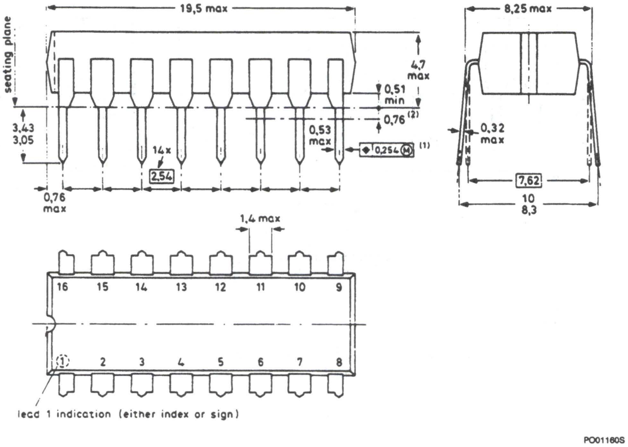
16-PIN PLASTIC DIP (SOT-38A)


22 max
seating plane
4,7
max
0,51
min
0,76(2)
3,9
3,4
0,67
max
0,254 M (1)
14x
2.54
0,35
2.2
max
8,25max
0,32
max
7,62
9,5
8,3
1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view
PO01140S

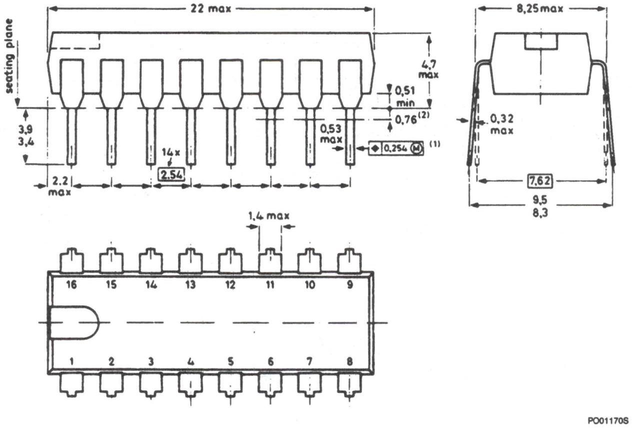
16-PIN PLASTIC DIP (SOT-38D, DE)


19,5 max
seating plane
4,7
max
0,51
min
3,60
3,15
0,53
max
14x
2,54
0,254 (M) (1)
0,76
max
8,25 max
0,32
max
7,62
10
8,3
1,73 max
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
lead 1 indication (either index or sign)
top view
PO01150S

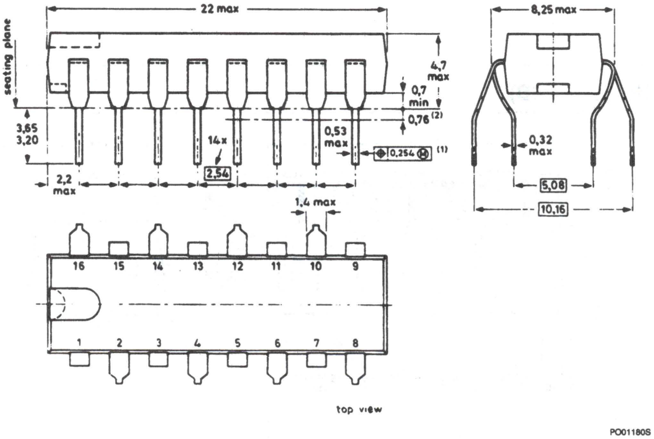
16-PIN PLASTIC DIP (SOT-38Z)


19,5 max
seating plane
4,7
max
0,51
min
0,76 (2)
3,43
3,05
0,53
max
14x
2,54
0,254 (M) (1)
0,76
max
8,25 max
0,32
max
7,62
10
8,3
1,4 max
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
lead 1 indication (either index or sign)
PO01160S

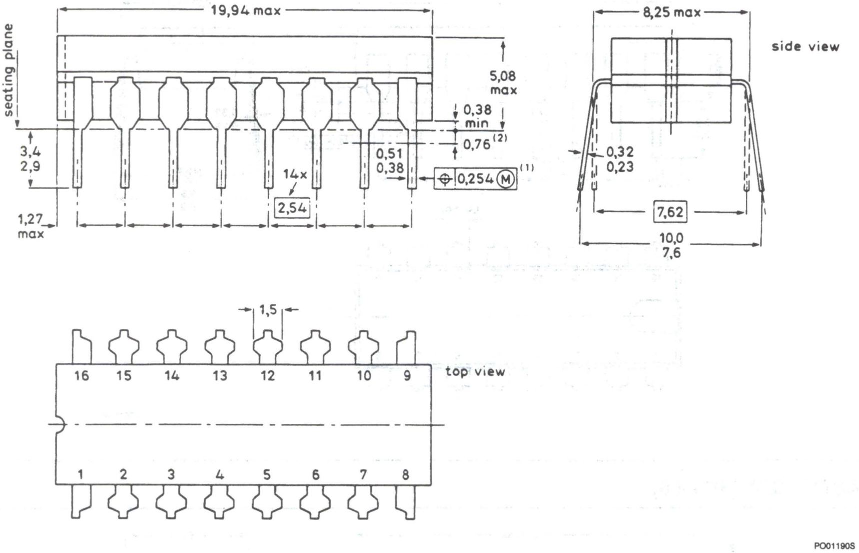
16-PIN PLASTIC DIP WITH INTERNAL HEAT SPREADER (SOT-38WE-2)


22 max
seating plane
4,7
max
0,51
min
0,76(2)
3,9
3,4
0,53
max
14x
2,54
0,254 M (1)
2,2
max
8,25 max
0,32
max
7,62
9,5
8,3
1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
PO01170S

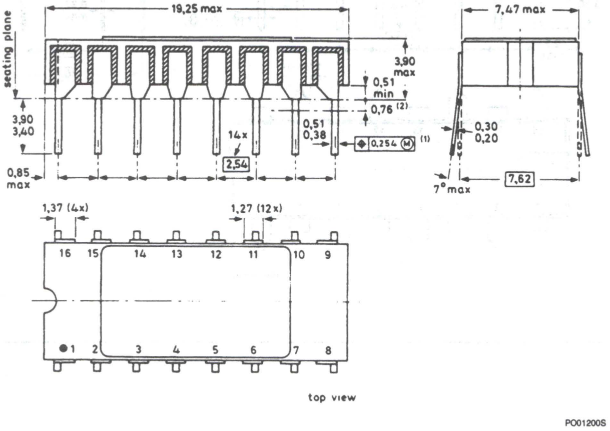
16-PIN PLASTIC QIP (SOT-58)


22 max
seating plane
4,7
max
0,7
min
0,76(2)
3,65
3,20
0,53
max
14x
2,54
0,254 M (1)
2,2
max
8,25 max
0,32
max
5,08
10,16
1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view
PO01180S

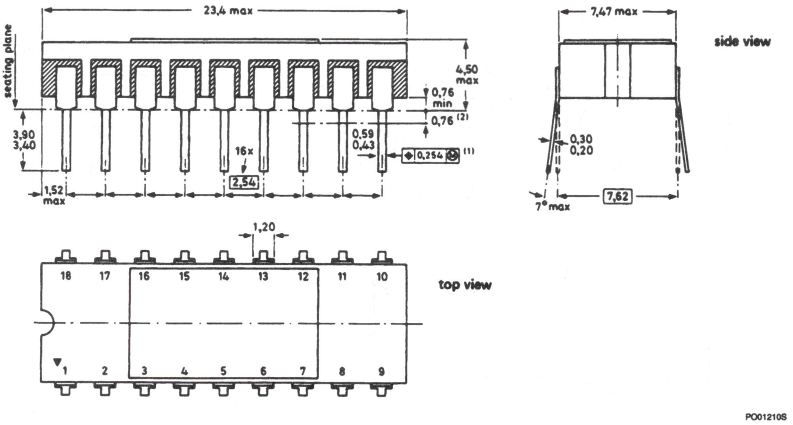
16-PIN CERDIP (SOT-74A, B, C)


19,94 max
seating plane
5,08 max
0,38 min
0,76 (2)
0,51
0,38
14x
2,54
0,254 (M) (1)
3,4
2,9
1,27 max
8,25 max
side view
0,32
0,23
7,62
10,0
7,6
1,5
top view
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
PO01190S

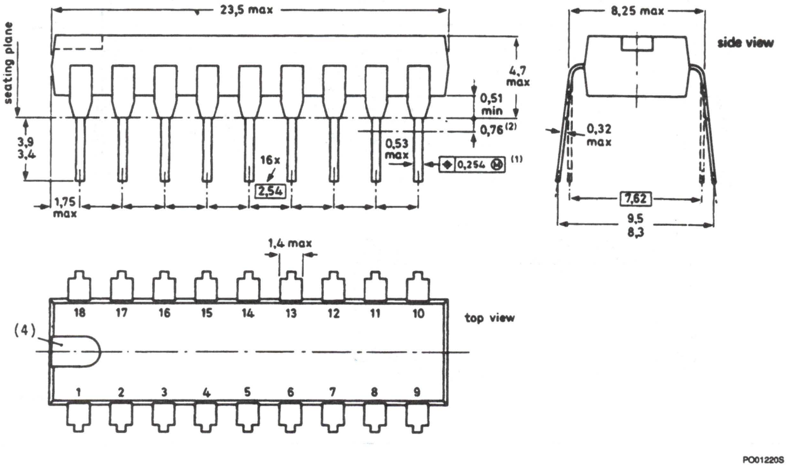
16-PIN METAL CERDIP (SOT-84B)


19,25 max
seating plane
3,90 max
0,51 min
0,76 (2)
0,51
0,38
14x
2,54
0,254 (M) (1)
3,90
3,40
0,85 max
7,47 max
0,30
0,20
7,62
7° max
1,37 (4x)
1,27 (12x)
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
top view
PO01200S

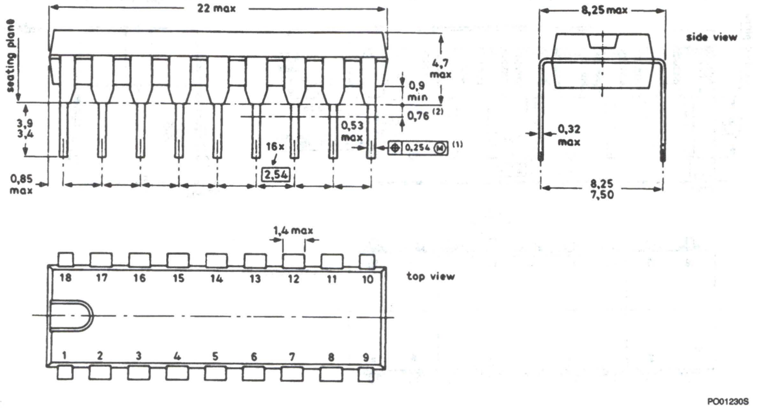
18-PIN METAL CERDIP (SOT-85B)


23,4 max
seating plane
4,50 max
0,76 min
0,76 (2)
3,90
3,40
0,59
0,43
16x
2,54
0,254 (1)
1,52 max
7,47 max
side view
0,30
0,20
7° max
7,62
1,20
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
top view
PO01210S

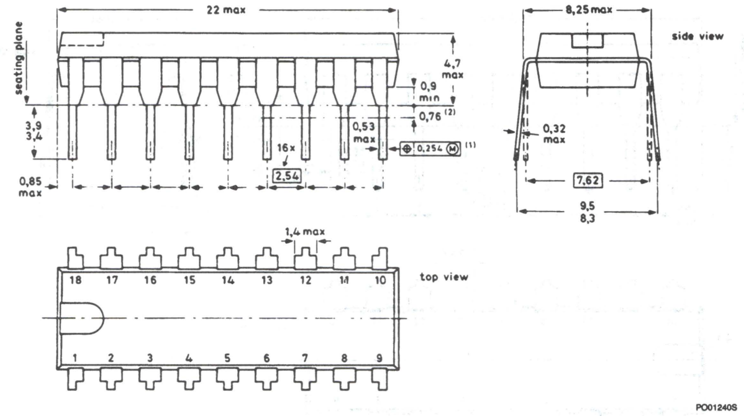
18-PIN PLASTIC DIP (SOT-102A)


23,5 max
seating plane
4,7 max
0,51 min
0,76 (2)
3,9
3,4
0,53 max
16x
2,54
0,254 (1)
1,75 max
8,25 max
side view
0,32 max
7,62
9,5
8,3
1,4 max
(4)
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
top view
PO01220S

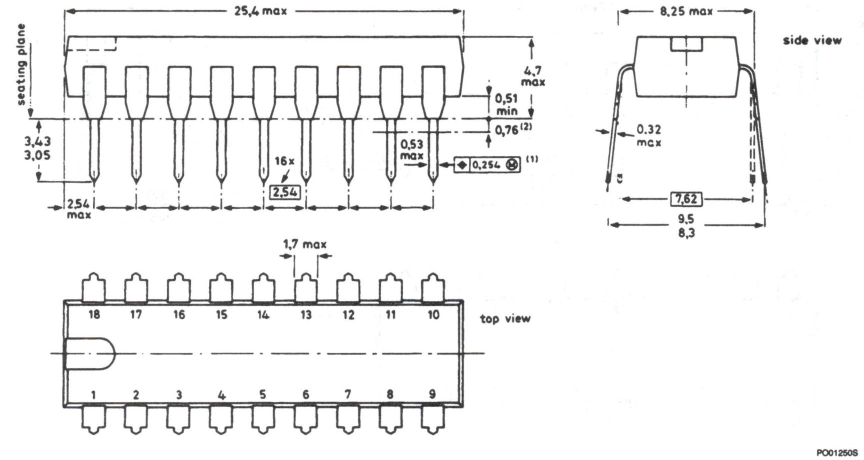
18-PIN PLASTIC DIP (SOT-102C)


22 max
seating plane
4,7 max
0,9 min
0,76 (2)
3,9
3,4
0,53 max
16x
0,254 (M) (1)
2,54
0,85 max
8,25 max
side view
0,32 max
8,25
7,50
1,4 max
18 17 16 15 14 13 12 11 10
top view
1 2 3 4 5 6 7 8 9
PO01230S

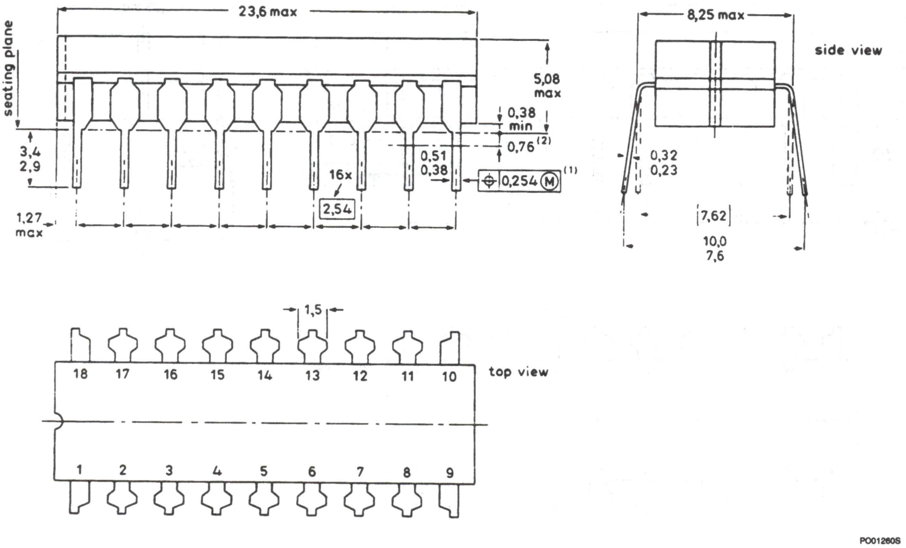
18-PIN PLASTIC DIP (SOT-102CS)


22 max
seating plane
4,7 max
0,9 min
0,76 (2)
3,9
3,4
0,53 max
16x
0,254 (M) (1)
2,54
0,85 max
8,25 max
side view
0,32 max
7,62
9,5
8,3
1,4 max
18 17 16 15 14 13 12 11 10
top view
1 2 3 4 5 6 7 8 9
PO01240S

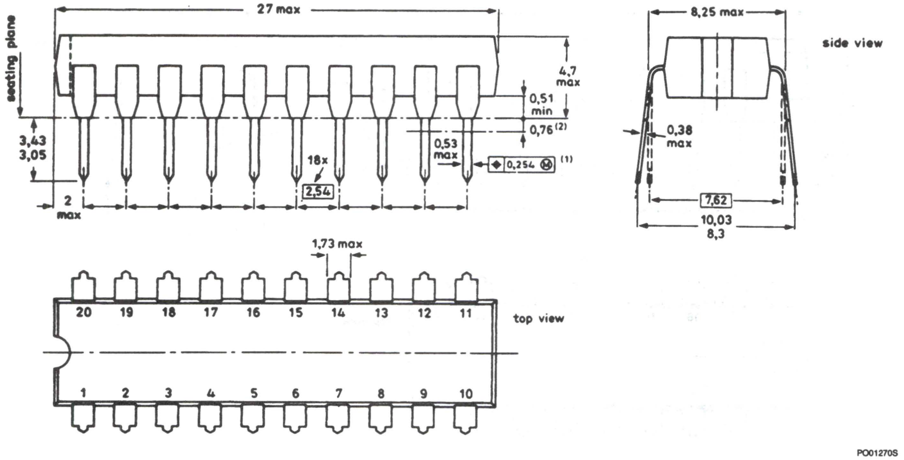
18-PIN PLASTIC DIP (SOT-102G)


25,4 max
seating plane
4,7
max
0,51
min
0,76 (2)
3,43
3,05
0,53
max
16x
2,54
0,254 Ⓜ (1)
2,54
max
8,25 max
side view
0.32
max
7,62
9,5
8,3
1,7 max
18
17
16
15
14
13
12
11
10
top view
1
2
3
4
5
6
7
8
9
PO01250S

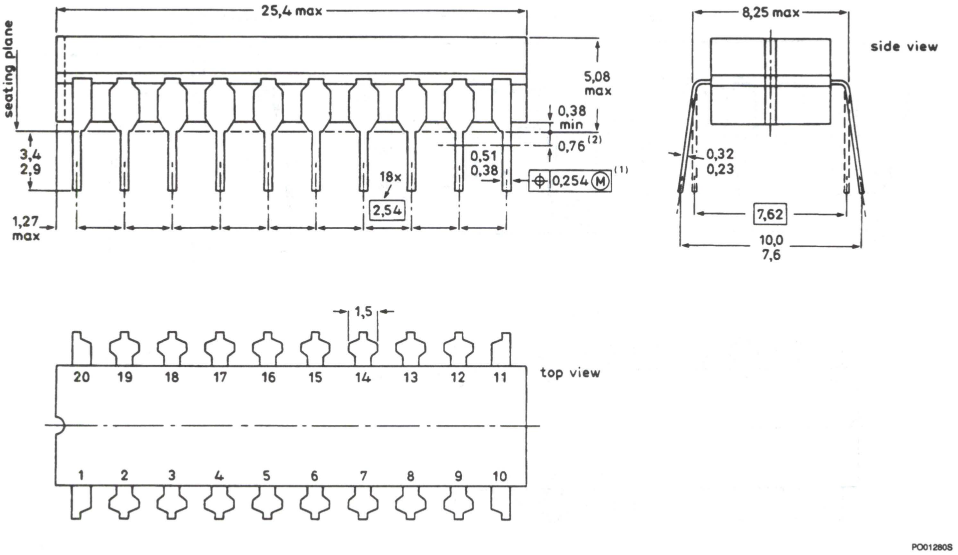
18-PIN CERDIP (SOT-133A, B)


23,6 max
seating plane
5,08
max
0,38
min
0,76 (2)
3,4
2,9
0,51
0,38
16x
2,54
0,254 Ⓜ (1)
1,27
max
8,25 max
side view
0,32
0,23
7,62
10,0
7,6
1,5
18
17
16
15
14
13
12
11
10
top view
1
2
3
4
5
6
7
8
9
PO01260S

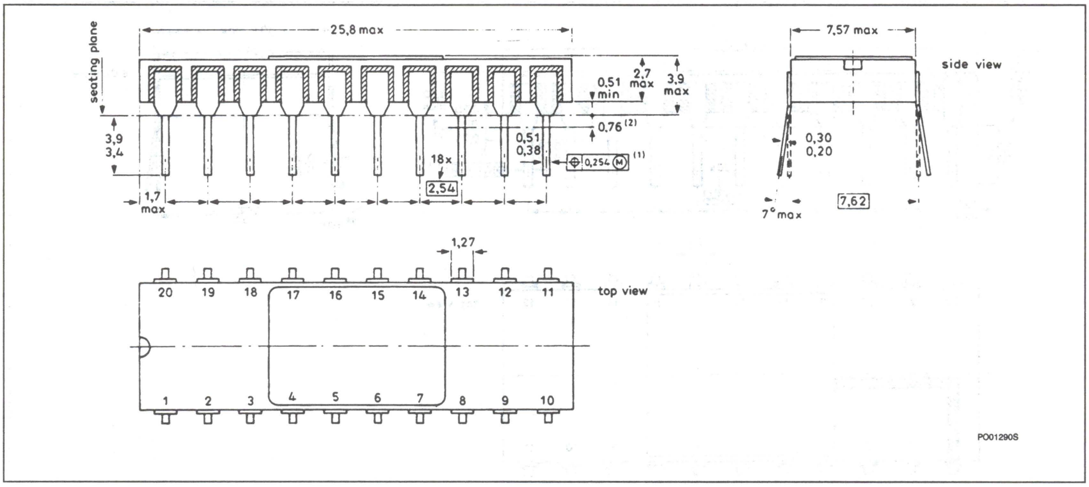
20-PIN PLASTIC DIP (SOT-146)


27 max
seating plane
4,7 max
0,51 min
0,76 (2)
3,43
3,05
0,53 max
18x
2,54
0,254 M (1)
2 max
8,25 max
side view
0,38 max
7,62
10,03
8,3
1,73 max
top view
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
PO01270S

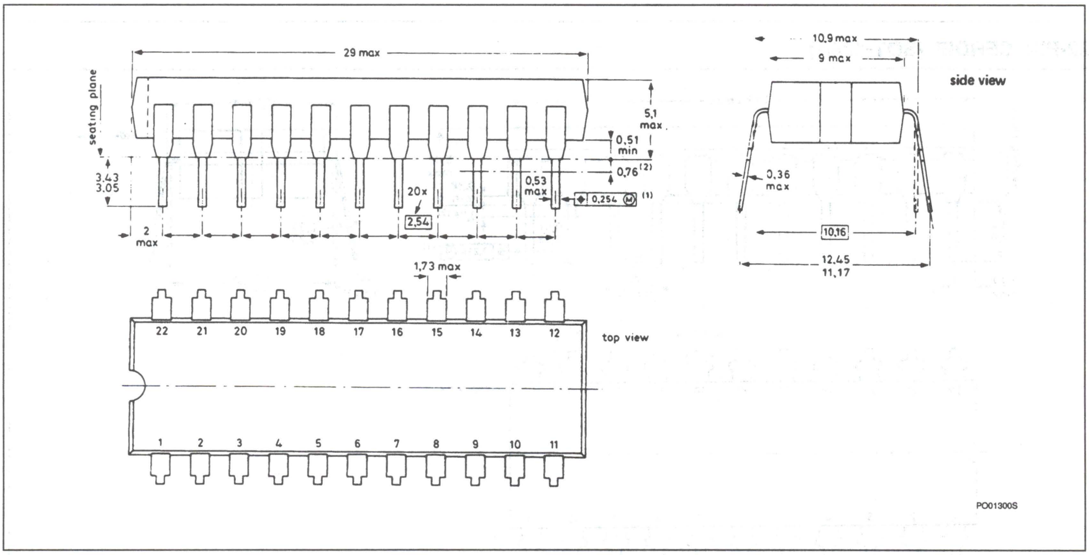
20-PIN CERDIP (SOT-152B, C)


25,4 max
seating plane
5,08 max
0,38 min
0,76 (2)
3,4
2,9
0,51
0,38
18x
2,54
0,254 M (1)
1,27 max
8,25 max
side view
0,32
0,23
7,62
10,0
7,6
1,5
top view
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
PO01280S

20-PIN METAL CERDIP (SOT-154B)


seating plane
25,8 max
0,51 min
2,7 max
3,9 max
0,76 (2)
3,9
3,4
0,51
0,38
18x
2,54
0,254 M (1)
1,7 max
7,57 max
side view
0,30
0,20
7°max
7,62
1,27
20
19
18
17
16
15
14
13
12
11
top view
1
2
3
4
5
6
7
8
9
10
PO01290S

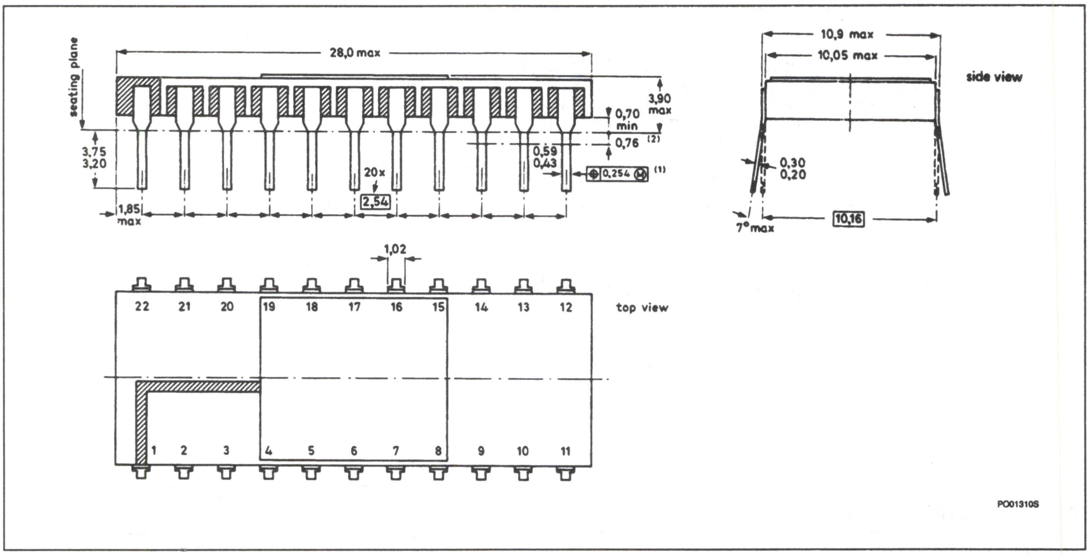
20-PIN PLASTIC DIP (SOT-116)


seating plane
29 max
5,1 max
0,51 min
0,76 (2)
3,43
3,05
0,53 max
20x
2,54
0,254 M (1)
2 max
10,9 max
9 max
side view
0,36 max
10,16
12,45
11,17
1,73 max
22
21
20
19
18
17
16
15
14
13
12
top view
1
2
3
4
5
6
7
8
9
10
11
PO01300S

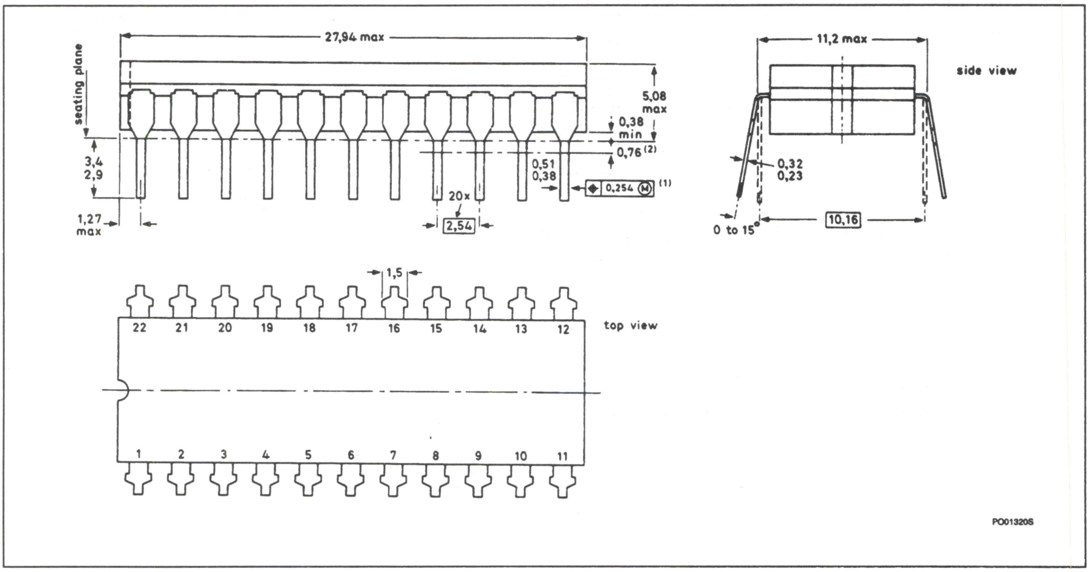
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

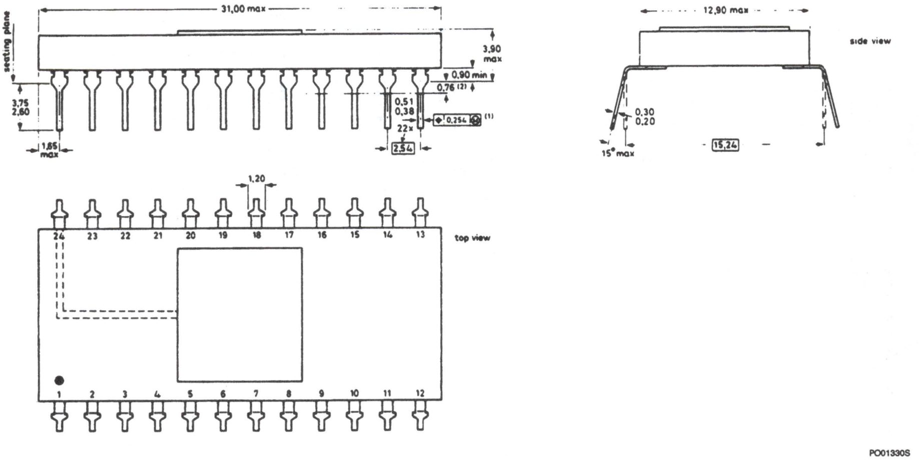
22-PIN METAL CERDIP (SOT-118B)


seating plane
28,0 max
3,90 max
0,70 min
0,76 (2)
0,59
0,43
3,75
3,20
20x
2,54
0,254 M (1)
1,85 max
1,02
22 21 20 19 18 17 16 15 14 13 12
1 2 3 4 5 6 7 8 9 10 11
top view
10,9 max
10,05 max
side view
0,30
0,20
7° max
10,16
PO01310S

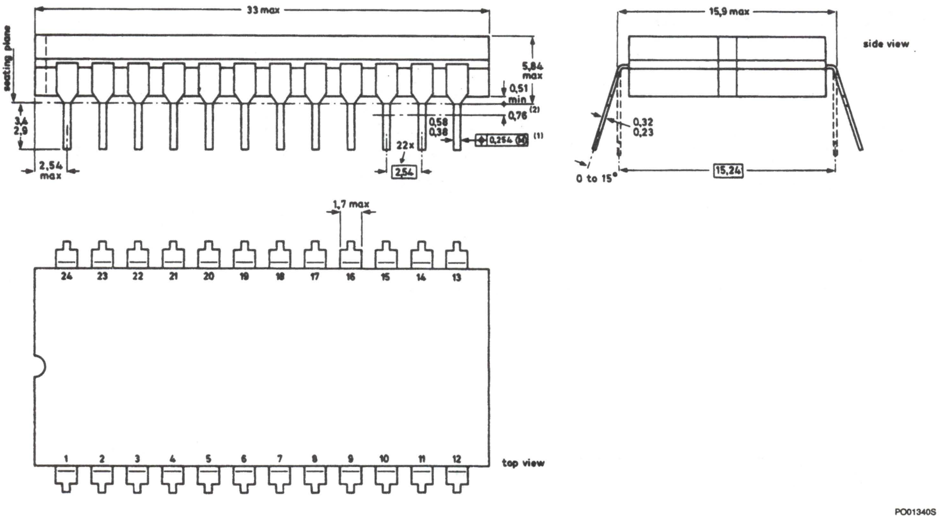
22-PIN CERDIP (SOT-134A)


seating plane
27,94 max
5,08 max
0,38 min
0,76 (2)
0,51
0,38
3,4
2,9
20x
2,54
0,254 M (1)
1,27 max
1,5
22 21 20 19 18 17 16 15 14 13 12
1 2 3 4 5 6 7 8 9 10 11
top view
11,2 max
side view
0,32
0,23
0 to 15°
10,16
PO01320S

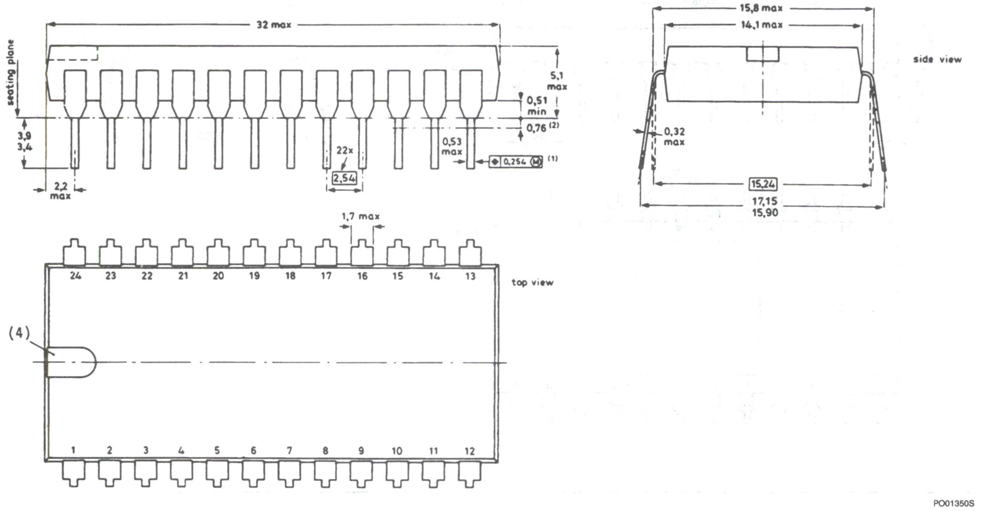
24-PIN METAL CERDIP (SOT-86A)


31,00 max
12,90 max
side view
seating plane
3,90 max
0,90 min
0,76 (2)
3,75
2,60
0,51
0,38
0,254 (1)
22x
2,54
1,65 max
0,30
0,20
15° max
15,24
1,20
24
23
22
21
20
19
18
17
16
15
14
13
top view
1
2
3
4
5
6
7
8
9
10
11
12
PO01330S

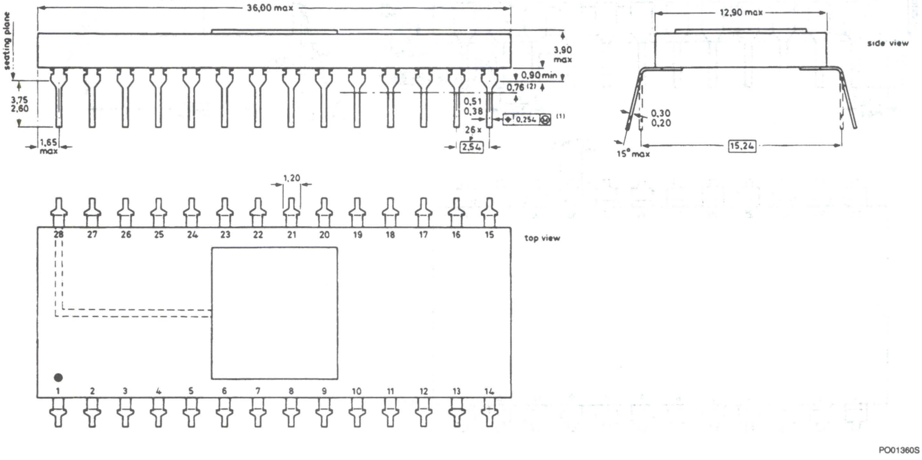
24-PIN CERDIP (SOT-94)


33 max
15,9 max
side view
seating plane
5,84 max
0,51 min
0,76 (2)
3,4
2,9
0,58
0,38
0,254 (1)
22x
2,54
2,54 max
0,32
0,23
0 to 15°
15,24
1,7 max
24
23
22
21
20
19
18
17
16
15
14
13
top view
1
2
3
4
5
6
7
8
9
10
11
12
PO01340S

24-PIN PLASTIC DIP WITH INTERNAL HEAT SPREADER (SOT-101A, B)


32 max
seating plane
5,1 max
0,51 min
0,76 (2)
3,9
3,4
22x
0,53 max
0,254 M (1)
2,54
2,2 max
1,7 max
24 23 22 21 20 19 18 17 16 15 14 13
top view
(4)
1 2 3 4 5 6 7 8 9 10 11 12
15,8 max
14,1 max
side view
0,32 max
15,24
17,15
15,90
PO01350S

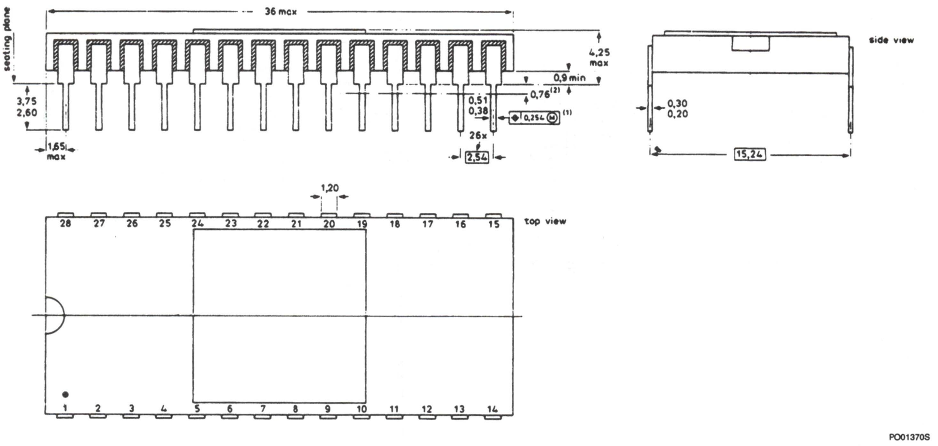
28-PIN METAL CERDIP (SOT-87A)


36,00 max
seating plane
3,90 max
0,90 min
0,76 (2)
3,75
2,60
0,51
0,38
26x
0,254 M (1)
2,54
1,65 max
1,20
28 27 26 25 24 23 22 21 20 19 18 17 16 15
top view
1 2 3 4 5 6 7 8 9 10 11 12 13 14
12,90 max
side view
0,30
0,20
15° max
15,24
PO01360S

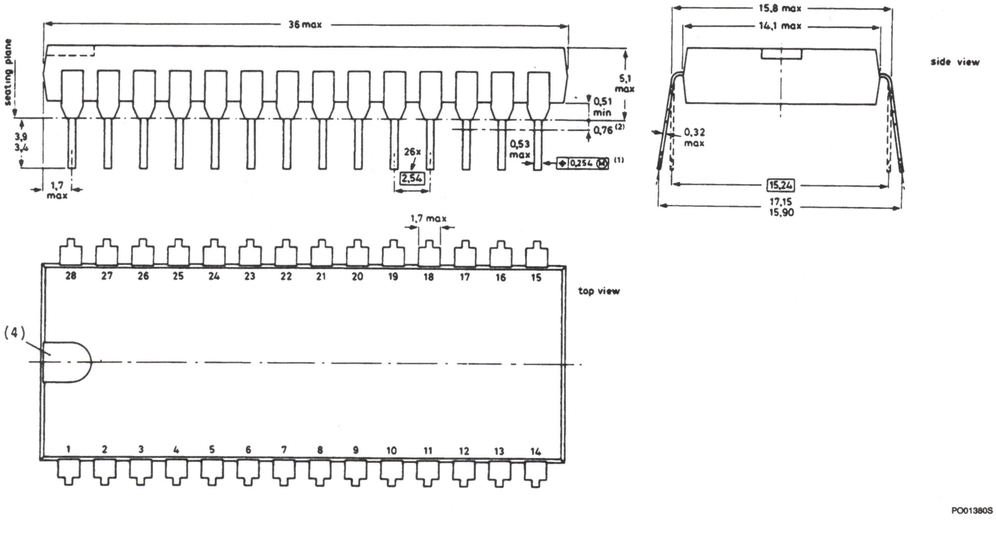
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

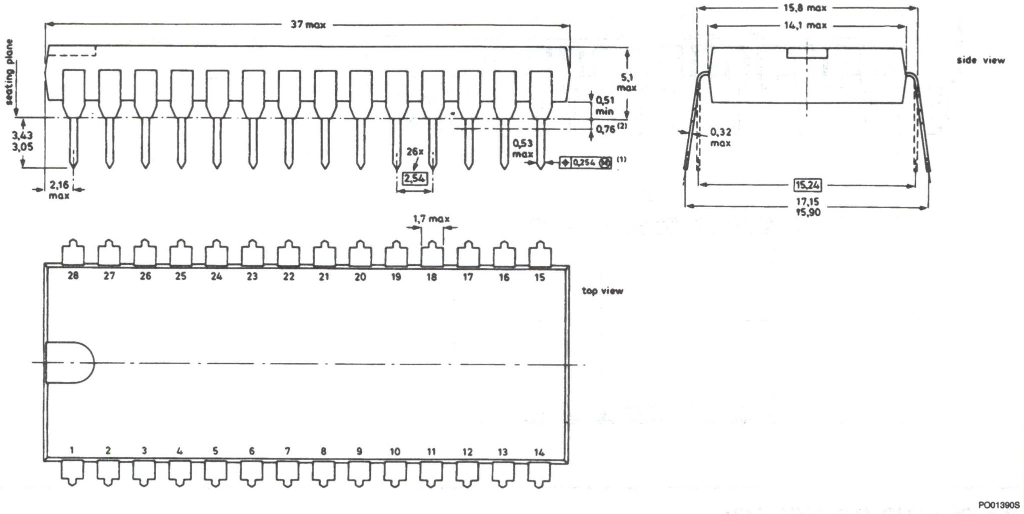
28-PIN METAL CERDIP (SOT-87B)


36 max
seating plane
4,25 max
0,9 min
0,76 (2)
0,51
0,38
0,254 M (1)
26x
2,54
3,75
2,60
1,65 max
side view
0,30
0,20
15,24
1,20
top view
28 27 26 25 24 23 22 21 20 19 18 17 16 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14
PO01370S

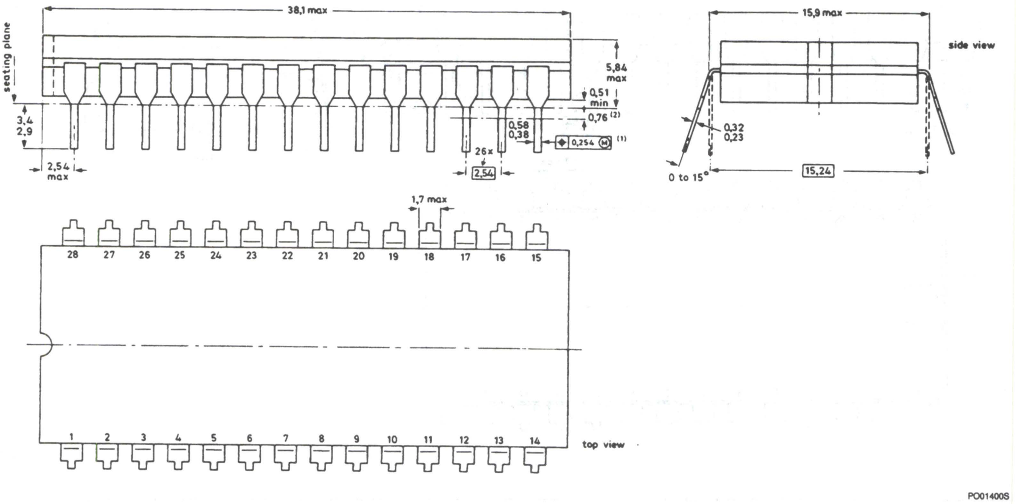
28-PIN PLASTIC DIP (SOT-117)


36 max
seating plane
5,1 max
0,51 min
0,76 (2)
0,53 max
0,254 M (1)
26x
2,54
3,9
3,4
1,7 max
15,8 max
14,1 max
side view
0,32 max
15,24
17,15
15,90
1,7 max
top view
(4)
28 27 26 25 24 23 22 21 20 19 18 17 16 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14
PO01380S

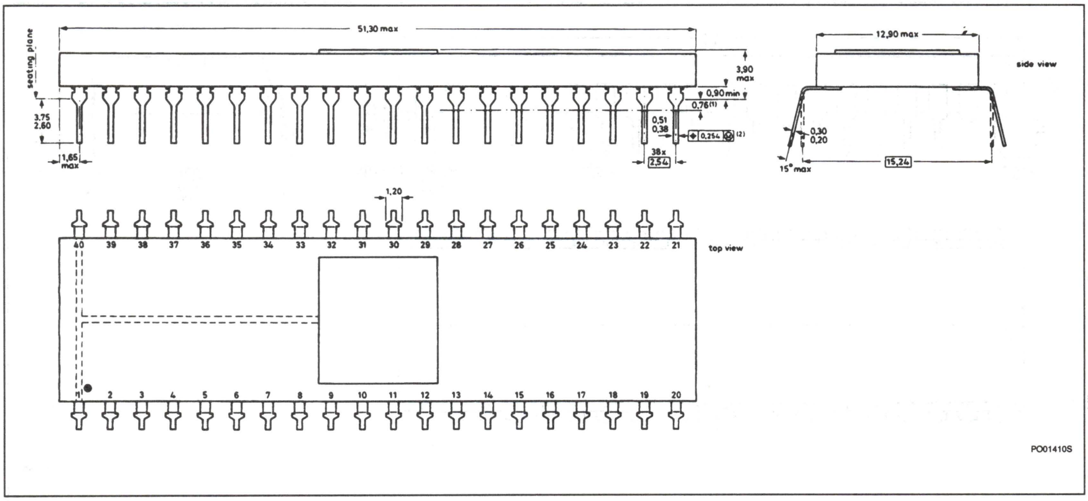
28-PIN PLASTIC DIP (SOT-117D)


37 max
seating plane
5,1 max
0,51 min
0,76 (2)
0,53 max
0,254 M (1)
3,43
3,05
2,16 max
26x
2,54
1,7 max
28 27 26 25 24 23 22 21 20 19 18 17 16 15
top view
1 2 3 4 5 6 7 8 9 10 11 12 13 14
15,8 max
14,1 max
side view
0,32 max
15,24
17,15
15,90
PO01390S

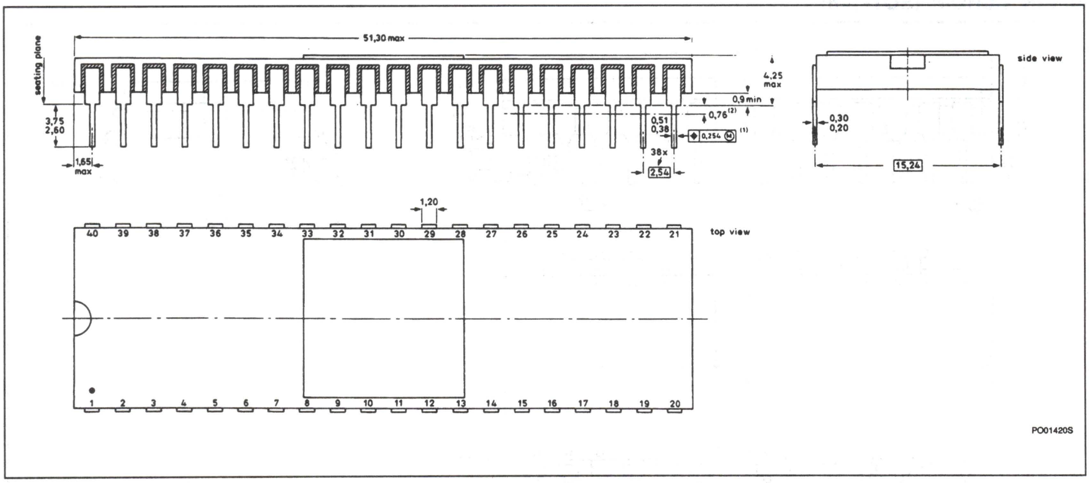
28-PIN CERDIP (SOT-135A)


38,1 max
seating plane
5,84 max
0,51 min
0,76 (2)
0,58
0,38
0,254 M (1)
3,4
2,9
2,54 max
26x
2,54
1,7 max
28 27 26 25 24 23 22 21 20 19 18 17 16 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14
top view
15,9 max
side view
0,32
0,23
0 to 15°
15,24
PO01400S

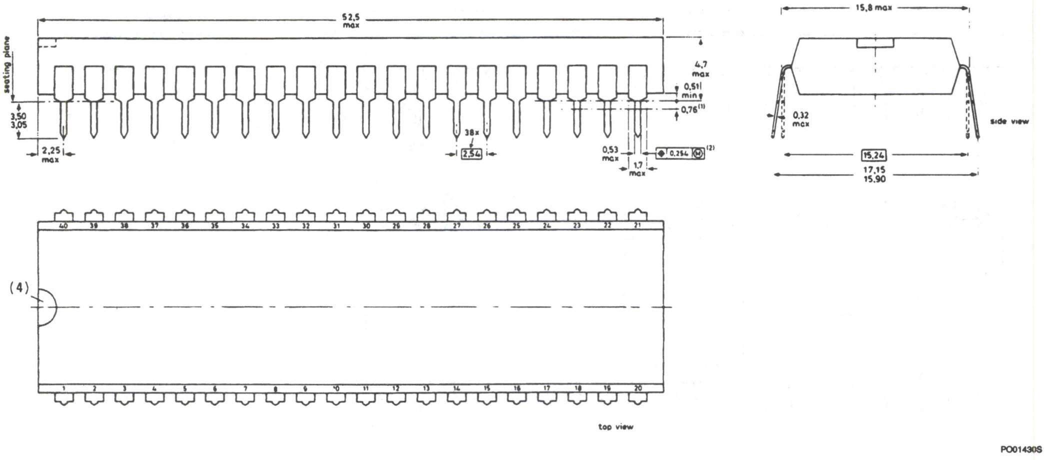
40-PIN METAL CERDIP (SOT-88)


seating plane
51,30 max
3,90 max
0,90 min
0,76(1)
0,51
0,38
0,254 (M) (2)
38x
2,54
3,75
2,60
1,65 max
12,90 max
side view
0,30
0,20
15° max
15,24
1,20
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
top view
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
PO01410S

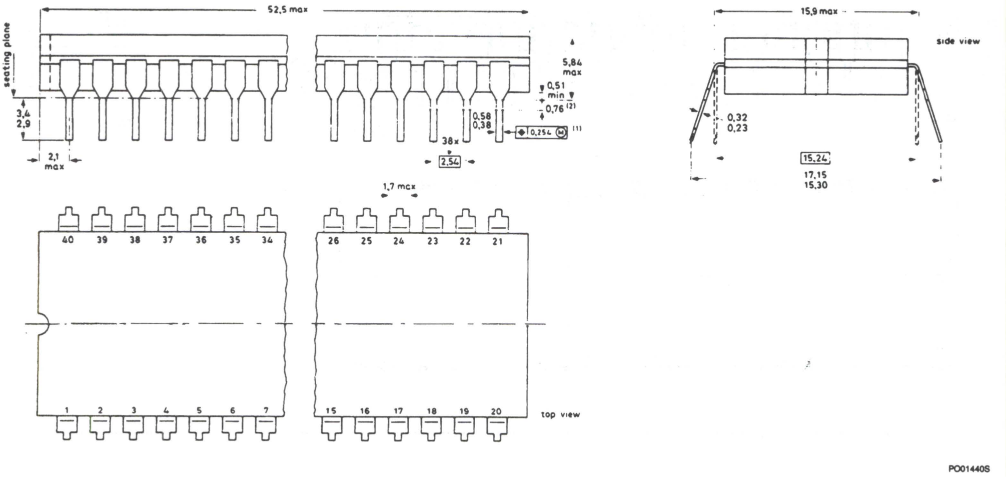
40-PIN METAL CERDIP (SOT-88B)


seating plane
51,30 max
4,25 max
0,9 min
0,76(2)
0,51
0,38
0,254 (M) (1)
38x
2,54
3,75
2,60
1,65 max
side view
0,30
0,20
15,24
1,20
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
top view
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
PO01420S

40-PIN PLASTIC DIP (SOT-129)


52,5 max
seating plane
4,7 max
0,51 min
0,76 (1)
3,50
3,05
2,25 max
38x
2,54
0,53 max
1,7 max
0,254 M (2)
15,8 max
0,32 max
side view
15,24
17,15
15,90
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
(4)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
top view
PO01430S

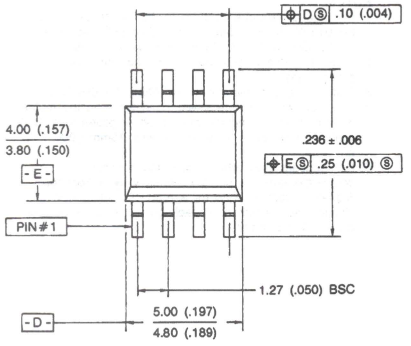
40-PIN CERDIP (SOT-145)


52,5 max
seating plane
5,84 max
0,51 min
0,76 (2)
3,4
2,9
2,1 max
0,58
0,38
0,254 M (1)
38x
2,54
1,7 max
15,9 max
side view
0,32
0,23
15,24
17,15
15,30
40 39 38 37 36 35 34
26 25 24 23 22 21
1 2 3 4 5 6 7
15 16 17 18 19 20
top view
PO01440S

For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

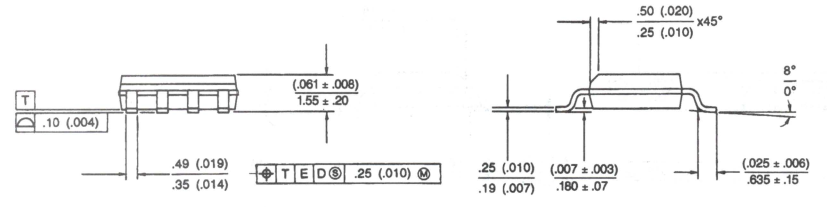
8-PIN PLASTIC SO (D PACKAGE) (SO-8, SOT-96A)



⊕ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
.236 ± .006
⊕ E Ⓢ .25 (.010) Ⓢ
PIN #1
1.27 (.050) BSC
-D-
5.00 (.197)
4.80 (.189)

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

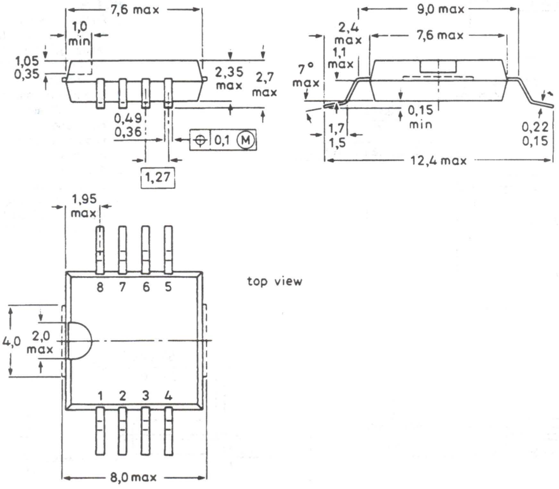


T
.10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15

853-0174 88070

PO00273S

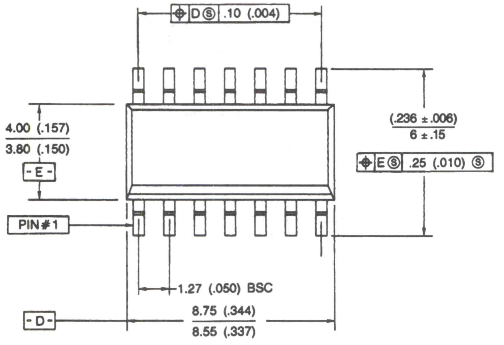
8-PIN PLASTIC SO (VSO-8, SOT-176)

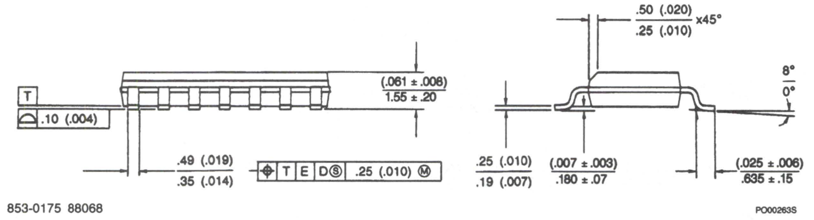


7,6 max
1,0 min
1,05
0,35
2,35 max
2,7 max
0,49
0,36
⊕ 0,1 Ⓜ
1,27
9,0 max
2,4 max
7,6 max
1,1 max
7° max
0,15 min
1,7
1,5
0,22
0,15
12,4 max
1,95 max
8 7 6 5
top view
4,0
2,0 max
1 2 3 4
8,0 max

PO00980S

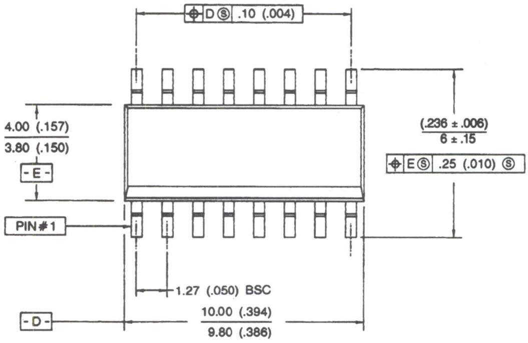
14-PIN PLASTIC SO (D PACKAGE) (SO-14, SOT-108A)

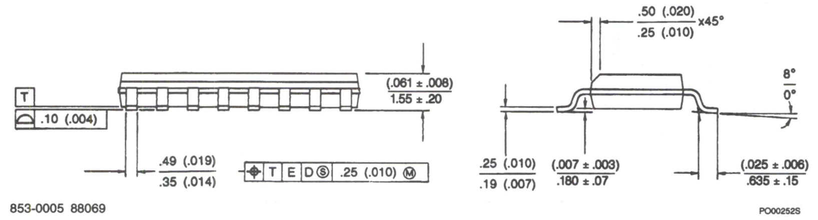

⌖ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
PIN #1
(.236 ± .006)
6 ± .15
⌖ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
8.75 (.344)
8.55 (.337)


T
.10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ
.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15
853-0175 88068
PO00263S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO (D PACKAGE) (SO-16, SOT-109A)


⌖ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
PIN #1
(.236 ± .006)
6 ± .15
⌖ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
10.00 (.394)
9.80 (.386)

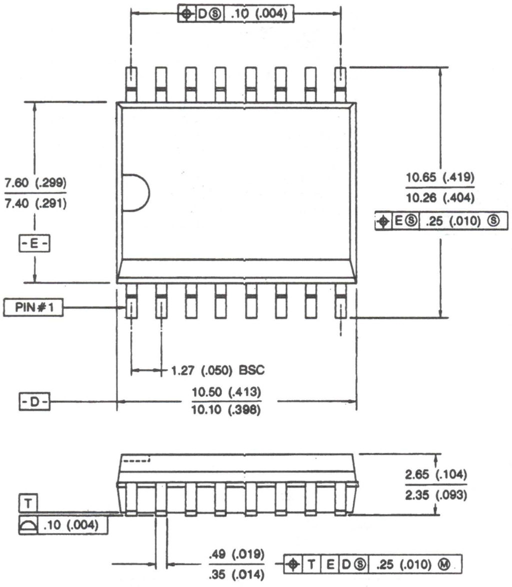

T
.10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ
.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15
853-0005 88069
PO00252S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

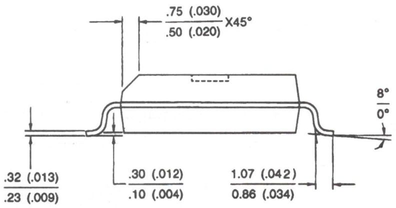
Package Outlines

16-PIN PLASTIC SOL (D PACKAGE) (SOL-16, SOT-162A)


⊕ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN #1
10.65 (.419)
10.26 (.404)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
10.50 (.413)
10.10 (.398)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ

NOTES:

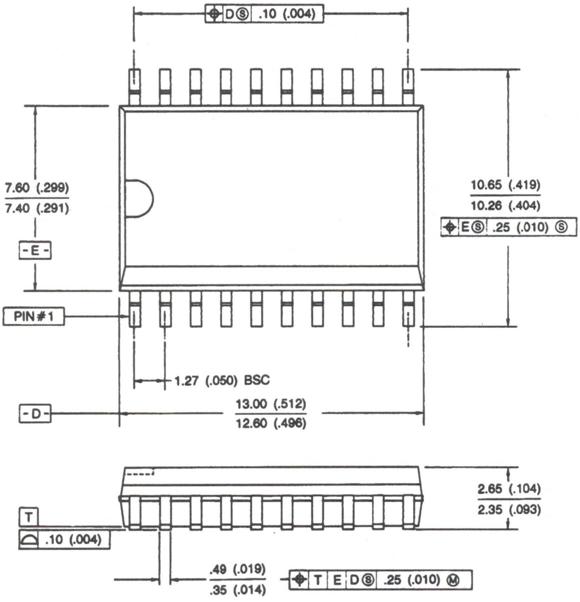
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.


.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
0.86 (.034)

853-0171 81218

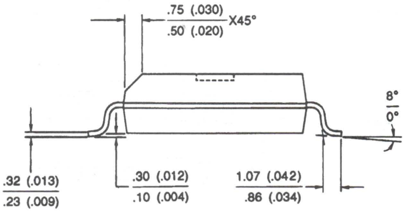
PO00241S

20-PIN PLASTIC SOL (D PACKAGE) (SOL-20, SOT-163A)


⊕ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN #1
10.65 (.419)
10.26 (.404)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
13.00 (.512)
12.60 (.496)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.


.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)

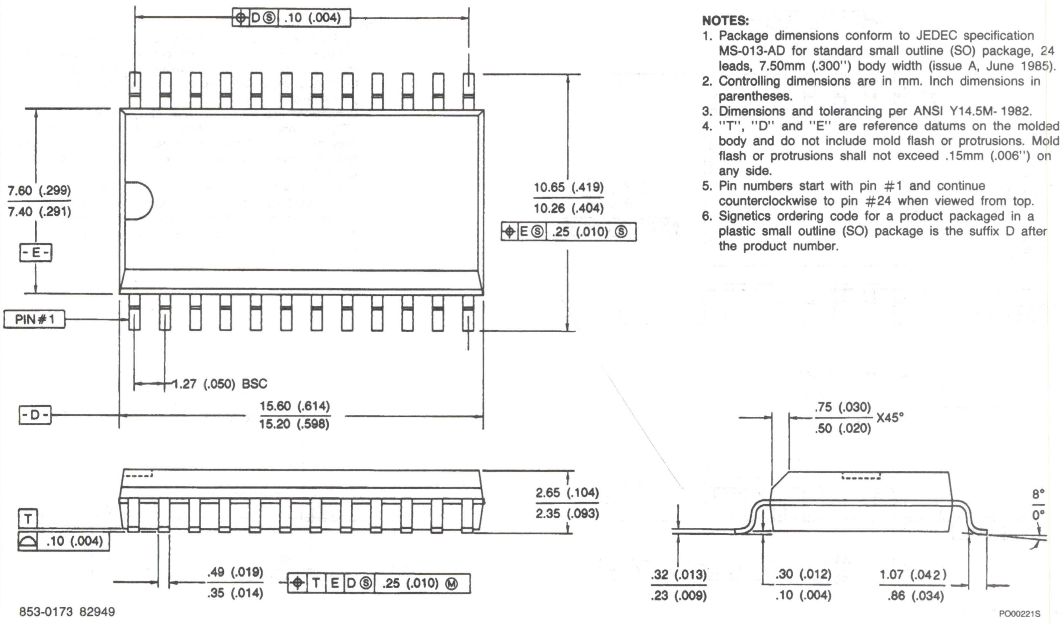
853-0172 82948

PO00231S

For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

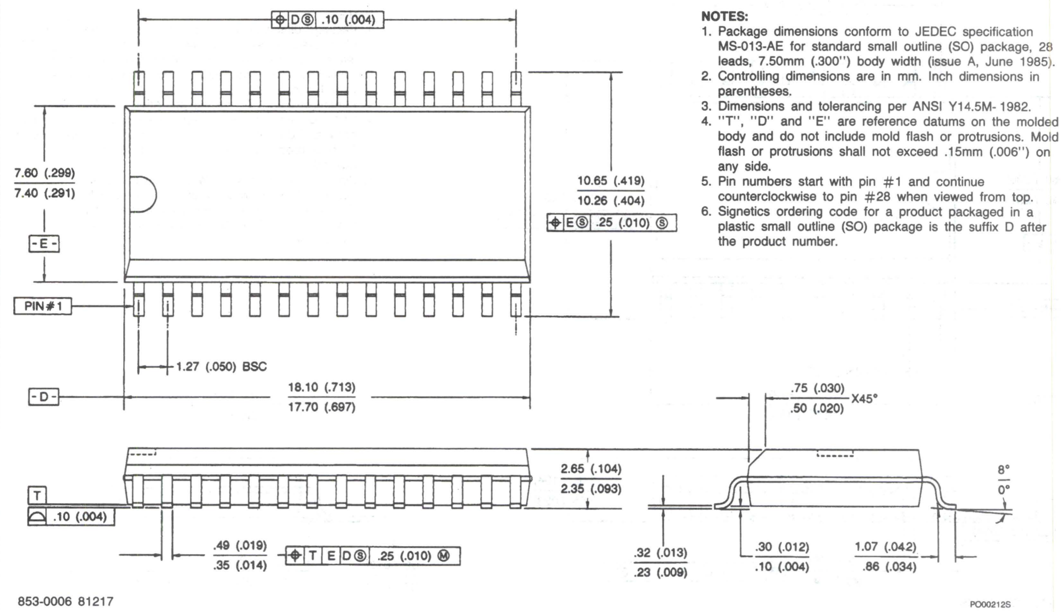
24-PIN PLASTIC SOL (D PACKAGE) (SOL-24, SOT-137A)


⊕ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN #1
10.65 (.419)
10.26 (.404)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
15.60 (.614)
15.20 (.598)
.75 (.030)
.50 (.020)
X45°
2.65 (.104)
2.35 (.093)
T
.10 (.004)
8°
0°
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
853-0173 82949
PO00221S

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

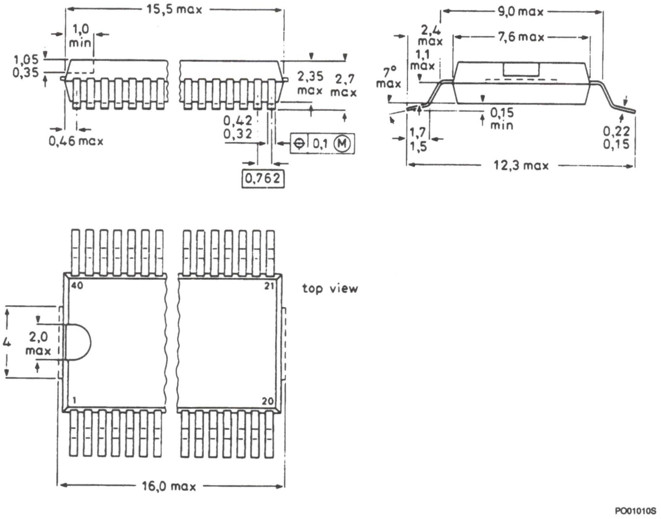
28-PIN PLASTIC SOL (D PACKAGE) (SOL-28, SOT-136A)


⊕ D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
PIN #1
10.65 (.419)
10.26 (.404)
⊕ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
18.10 (.713)
17.70 (.697)
.75 (.030)
.50 (.020)
X45°
2.65 (.104)
2.35 (.093)
T
.10 (.004)
8°
0°
.49 (.019)
.35 (.014)
⊕ T E D Ⓢ .25 (.010) Ⓜ
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)
853-0006 81217
PO00212S

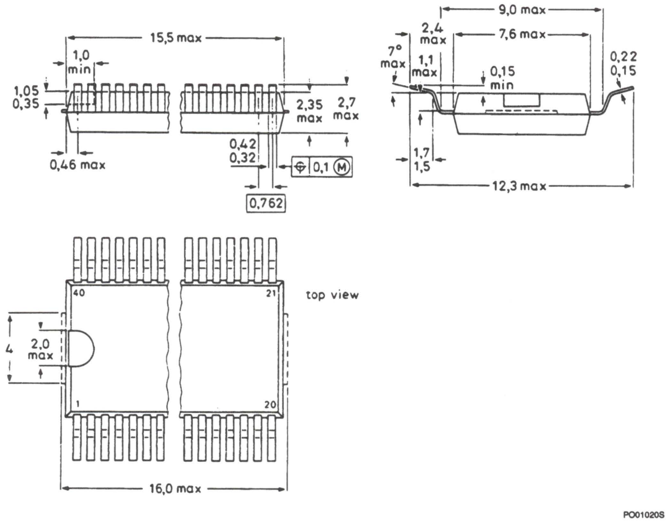
NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

40-PIN PLASTIC SO (VSO-40, SOT-158A)


15,5 max
1,0 min
1,05
0,35
2,35 max
2,7 max
0,42
0,32
0,46 max
⊕ 0,1 Ⓜ
0,762
9,0 max
2,4 max
7,6 max
1,1 max
7° max
0,15 min
1,7
1,5
0,22
0,15
12,3 max
40
21
top view
4
2,0 max
1
20
16,0 max
PO01010S

40-PIN PLASTIC SO (OPPOSITE BENT LEADS) (VSO-40, SOT-158B)


9,0 max
15,5 max
2,4 max
7,6 max
7° max
1,0 min
1,1 max
0,15 min
0,22
0,15
1,05
0,35
2,35 max
2,7 max
0,42
0,32
0,46 max
⊕ 0,1 Ⓜ
0,762
1,7
1,5
12,3 max
40
21
top view
4
2,0 max
1
20
16,0 max
PO01020S

Signetics

Linear Products

Section 10
Sales Offices

INDEX

Sales Office Listing 10-3

Sales Offices

SIGNETICS HEADQUARTERS

811 East Arques Avenue
P.O. Box 3409
Sunnyvale,
California 94088-3409
Phone: (408) 991-2000

ALABAMA
Huntsville
Phone: (205) 830-4001

ARIZONA
Phoenix
Phone: (602) 265-4444

CALIFORNIA
Canoga Park
Phone: (818) 340-1431

Irvine
Phone: (714) 833-8980
(213) 588-3281

Los Angeles
Phone: (213) 670-1101

San Diego
Phone: (619) 560-0242

Sunnyvale
Phone: (408) 991-3737

COLORADO
Aurora
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Clearwater
Phone: (813) 796-7086

Ft. Lauderdale
Phone: (305) 486-6300

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Atlanta
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Overland Park
Phone: (913) 469-4005

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Littleton
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OHIO
Worthington
Phone: (614) 888-7143

OREGON
Portland
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PENNSYLVANIA
Plymouth Meeting
Phone: (215) 825-4404

TENNESSEE
Greeneville
Phone: (615) 639-0251

TEXAS
Austin
Phone: (512) 339-9944

Richardson
Phone: (214) 644-3500

CANADA
SIGNETICS CANADA, LTD.
Etobicoke, Ontario
Phone: (416) 626-6676

Nepean, Ontario
Signetics, Canada, Ltd.
Phone: (613) 726-9576

REPRESENTATIVES

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Thom Luke Sales, Inc.
Phone: (602) 941-1901

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Magna Sales
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Brookfield
M & M Associates
Phone: (203) 775-6888

FLORIDA
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Sigma Technical Associates
Phone: (813) 791-0271

Ft. Lauderdale
Sigma Technical Associates
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Micro-Tex, Inc.
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Mohrfield Marketing Inc.
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Cedar Rapids
J.R. Sales
Phone: (319) 393-2232

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Glen Burnie
Third Wave Solutions, Inc.
Phone: (301) 787-0220

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Needham Heights
Com-Sales, Inc.
Phone: (617) 444-8071
Kanan Associates
Phone: (617) 449-7400

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Enco Marketing
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Raytown
Centech, Inc.
Phone: (816) 358-8100

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East Hanover
Emtec Sales, Inc.
Phone: (201) 428-0600

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Jerry Robinson and
Associates
Phone: (918) 665-3562

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Pittsburgh
Covert & Newman
Phone: (412) 531-2002

Willow Grove
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Phone: (215) 657-7250

UTAH
Salt Lake City
Electrodyne
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WASHINGTON
Bellevue
Western Technical Sales
Phone: (206) 641-3900

Spokane
Western Technical Sales
Phone: (509) 922-7600

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Waukesha
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Phone: (604) 439-1367

Mississauga, Ontario
Tech-Trek, Ltd.
Phone: (416) 238-0366

Nepean, Ontario
Tech-Trek, Ltd.
Phone: (613) 726-9562

Richmond, British Columbia
Tech-Trek, Ltd.
Phone: (604) 271-3149

Ville St. Laurent, Quebec
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Phone: (514) 337-7540

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98-2000-050

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Printed in USA 6132/RRD/60MFP0487
1360 pages